CS6135 PDA HW1 REPORT

(1)

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(2)

Core utilization: 0.95, clock period: 10 ns

```
floorPlan -coreMarginsBy die -site FreePDK45_38x28_10R_NP_162NW_340 -r 1.0 0.95 4.0 4.0 4.0 4.0
```

過程中有額外使用 optDesign -postCTS

	(congestion-driven, timing-driven)					
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
Slack	0.219	0.309	0.467	0.727	0.485	0.433
Total wire length (um)	96696.8300	96876.3900	96783.0000	96438.9000	96866.4350	96775.3500

(L, M, and H stand for Low, Medium, and High congestion effort.)

開啟 timing-driven 可以降低 critical path delay，所以通常可以產生較大的 slack。congestion-driven 會輕微增加 wirelength 進而影響 clock。

(3)

Congestion-driven placement:

當晶片較小時，會出現較多 high cell density 的區域進而可能產生 congestion 導致後面較難進行繞線，congestion-drive placement 透過提升 standard cell 之間的間隔來改善 routability。但同時，其也可能會導致 wirelength 增加，對 clock 產生負面影響。

Timing-driven placement:

Timing-driven placement 會使 critical path 上面的 cell 越靠近越好，來降低 critical path delay，優化 Performance，但可能導致 congestion 的情形變嚴重。

(4)

1. Fill all the gaps between standard cell instances

使得 VDD 、 VSS 與 NWEL 保持連續性，改善電晶體的特性。

2. Provide decoupling capacitances to complete connections in the standard cell rows

如果空隙夠大，可以在 power 的 VDD 與 VSS 之間加上一個 decoupling 的電容，提供穩定電壓的效果，降低 power network 上面的一些抖動的雜訊。

3. 可以提升製造的良率。在積體電路製造過程時，如果 standard cell 密度分布不均勻，這會增加 cell 的 variation，進而對時序的準確性產生負面影響。

(5)

clock period: 3.62

```
[u112062638@ic53 Best_Result]$ cat design.sdc
################################################################

# Created by write_sdc on Fri Jan 14 18:07:42 2022

################################################################
set sdc_version 2.0

set_units -time ns -resistance MOhm -capacitance fF -voltage V -current mA
create_clock [get_ports clk]  -name CLK  -period 3.62  -waveform {0 1.81}
```

total area of chip: 11573.713 um^2

```
============================
Floorplan/Placement Information
============================
Total area of Standard cells: 11191.950 um^2
Total area of Standard cells(Subtracting Physical Cells): 10674.048 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 11191.950 um^2
Total area of Chip: 11573.713 um^2
```

total wire length: 98852.0400 um

```
============================
Wire Length Distribution
============================
Total metal1 wire length: 1009.8650 um
Total metal2 wire length: 23503.8900 um
Total metal3 wire length: 38277.0000 um
Total metal4 wire length: 18264.6700 um
Total metal5 wire length: 9465.7750 um
Total metal6 wire length: 8330.8400 um
Total wire length: 98852.0400 um
```

Slack: 0.000

```
Analysis View: generic_view
Other End Arrival Time          0.000
- Setup                         0.173
+ Phase Shift                   3.620
= Required Time                 3.447
- Arrival Time                  3.447
= Slack Time                    0.000
```

congestion-driven effort: high

timing-driven: on

```
setPlaceMode -congEffort high -timingDriven 1 -clkGateAware 1 -powerDriven 0 -ignoreScan 1
-reorderScan 1 -ignoreSpare 0 -placeIOPins 1 -moduleAwareSpare 0 -preserveRouting 1 -rmAffe
ctedRouting 0 -checkRoute 0 -swapEEQ 0
```

(6)

檔案儲存為 post_route