

CS6135 PDA HW4 REPORT

(1) Your name and student ID

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(2) The wirelength and the runtime of each testcase (makeup)

	public1	public2	public3
wirelength	90241568	13432683	569997702
Runtime	590.29 s	590.65 s	590.84 s

使用 HW4_grading.sh 進行計算

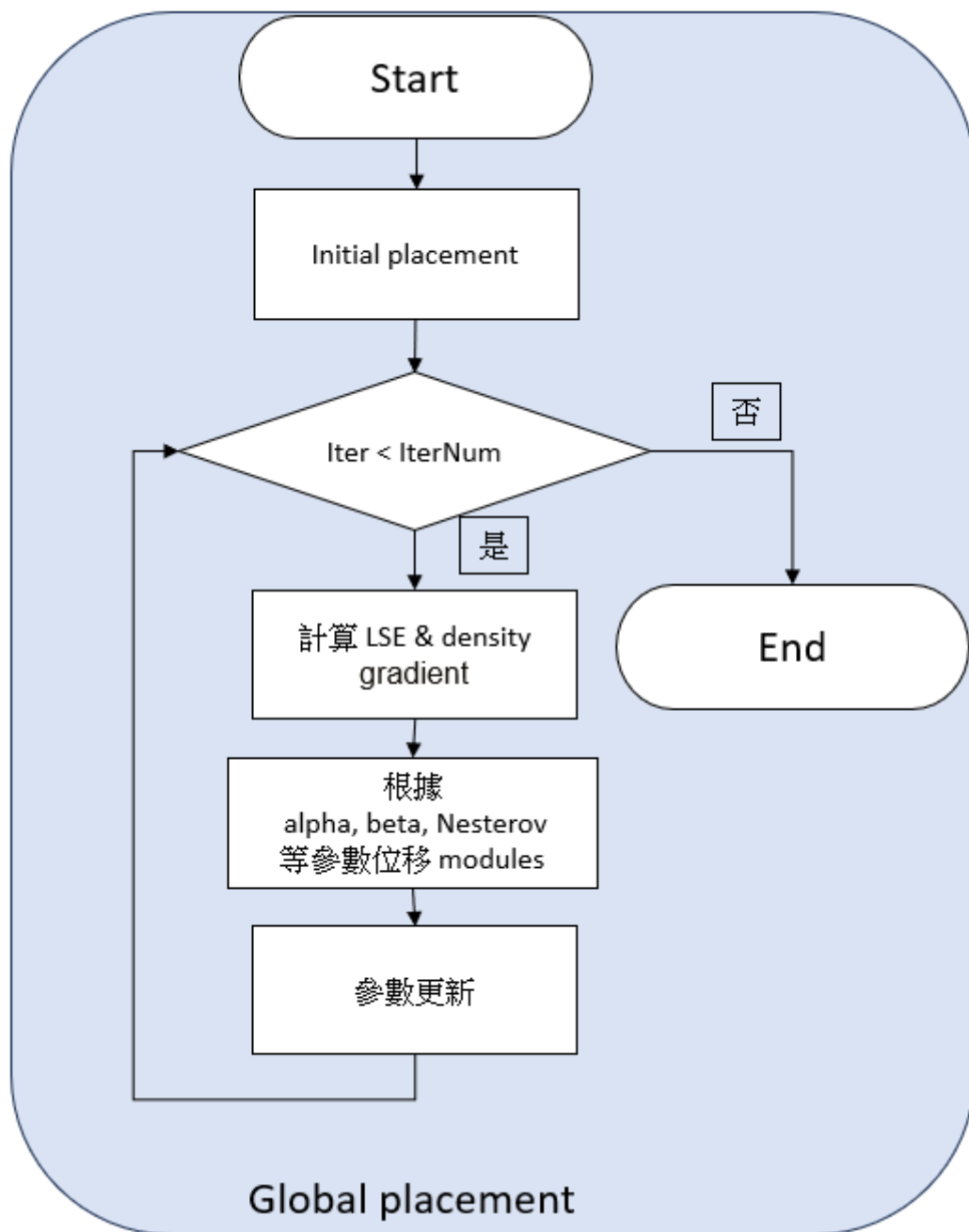
testcase	wirelength	runtime	status
public1	90241568	590.29	success
public2	13432683	590.65	success
public3	569997702	590.84	success

(3) The details of your algorithm. You could use flow chart(s) and/or pseudo code to help elaborate your algorithm. If your method is similar to some previous work/papers, please cite the papers and reveal your difference(s).

Target:

$$\text{Minimize } \sum_{e \in E} c_e \times \text{WL}_e(\mathbf{x}, \mathbf{y}) + \beta \times \sum_b (D_b(\mathbf{x}, \mathbf{y}) - T_b)^2$$

- 使用 LSE 與 Bell Shaped modal
- 將 die 分成 $10 \times 10 = 100$ 個 bins
- 500 iterations
- $\text{Alpha} = 0.3 - 0.00012 \times \text{iter}$
- $\text{Beta} = 0.49 + (0.01 / (1 + \exp(0.03 \times (\text{total_iterNum} / 4 - \text{iter}))))$
- $T_b = 0.97$
- Nesterov = 0.2
- Initial placement 將不是 fixed 的 modules 都擺到 chip 中心附近。



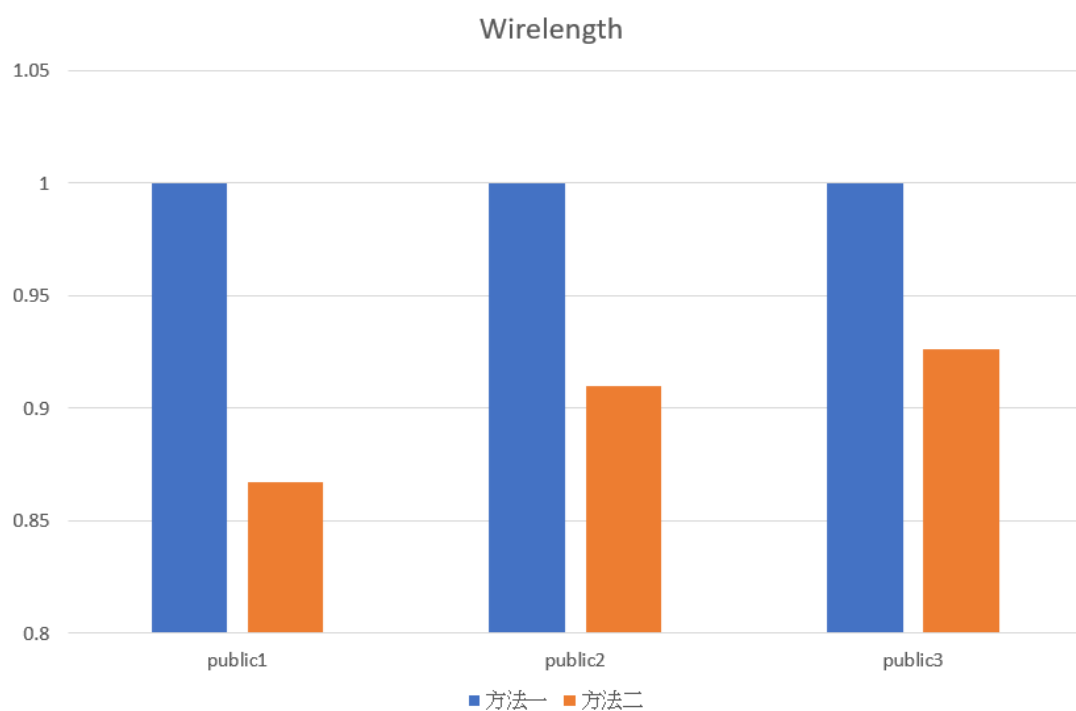
(4) Try your best to enhance your solution quality. What tricks did you do to enhance your solution quality?

使用 Nesterov 進行優化加速收斂。

(1) 法一：沒有使用 Nesterov

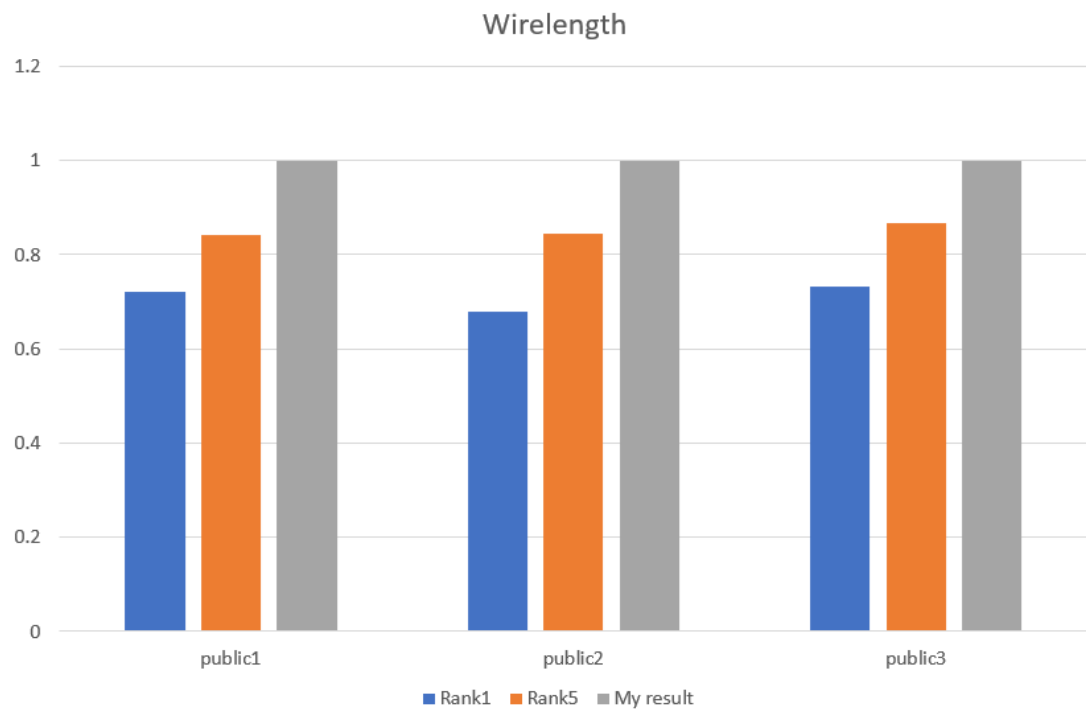
testcase	wirelength	runtime	status
public1	109945974	93.67	success
public2	14225610	243.99	success
public3	671542982	412.53	success

(2) 法二: Nesterov = 0.2 (繳交版本)



採用方法二大約降低 10% 的 wirelength

- (5) Please compare your results with the previous top 5 students' results and show your advantage in solution quality. Are your results better than theirs?
我的設計並沒有任何優點，實驗結果皆比較差。



可能可以優化我程式的方法:

- (1) 將 LSE 改成 WA modal
- (2) 使用較新的 density modal
- (3) 使用 partition 產生多組 modules，每組 modules 之間 cut net 越小越好，分散放置每組 modules 當作 initial case，再對 initial case 微調。