Exercise 6: Single Cycle CPU

Within the scope of this exercise, you will finally piece together your very own CPU. The CPU will be based on the RISC-V instruction set for RV32I Base Instruction Set. Further, within each clock cylce of your CPU one instruction will be executed. Before finishing the CPU, several considerations have to be taken. Are there modifications required for the already designed components? Are there possible hazards? These questions will be answered during the following tasks.

Whiteboard Task 1. List the components you already created for within the previous exercises. Are there modifications necessary for the utilization within the RISC-V CPU? Discuss the execution cycle of the single cycle CPU. Which stages are there? Which components refer to which stage of the execution cycle?

Bonus Task 1. In a previous exercise, you designed an ALU. Review the RV32I instruction set. Adjust your ALU to be feature complete for the RV32I Base Instruction Set.

Whiteboard Task 2. Design the control logic of the CPU. The logic should interconnect all components. Further, the control logic should decompose the RV32I-instruction and set all control ports of components and MUXes accordingly.

The instruction of RISC-V can be categorized by their operation type.

- Arithmetical and logial instructions
  - `op_IMM`: register-immediate instructions
  - `op_OP`: register-register instructions
- (Un)conditional jumps
  - `op_JAL`: jump and link
  - `op_JALR`: jump and link register
  - `op_BRANCH`: conditional branches
- Memory instructions
  - `op_LOAD`: load data from memory
  - `op_STORE`: store data in memory
- Instructions for loading upper immediates
  - `op_LUI`: load upper immediate
  - `op_AUIPC`: add upper immediate to program counter

You can find encodings of (almost) all operation types of RISC-V in the provided package. In fact, the RV32I instruction set holds some more types of opreations for memory reordering and system calls. Though, we will not implement these. In the slides corresponding to this exercise, you can find a full overview over all instructions of RV32I.

Task 1. Implement the control logic as discussed in the previous tasks. Follow the block diagram and discussion created previously. The following files might be useful:

- `isa_riscv.vhd` (Design Source)