

Advanced CPU Design: The Program Counter

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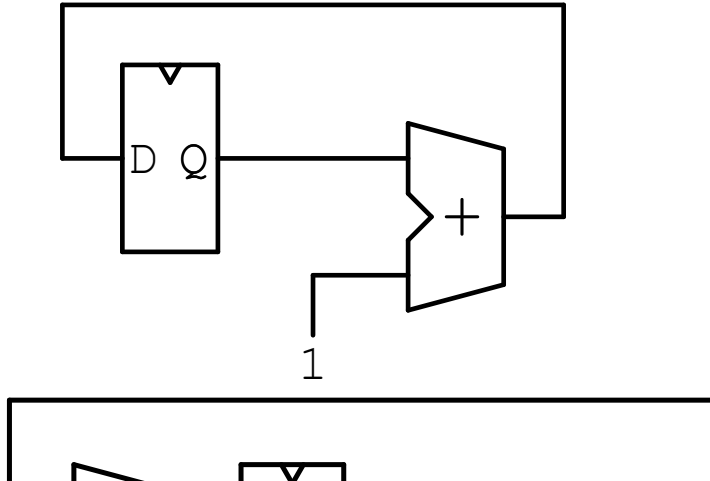
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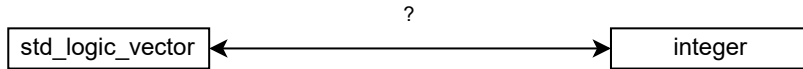
VHDL Recap: What is important

Task Overview

Schematic: The Program Counter



Numerical Operations



Numerical Operations

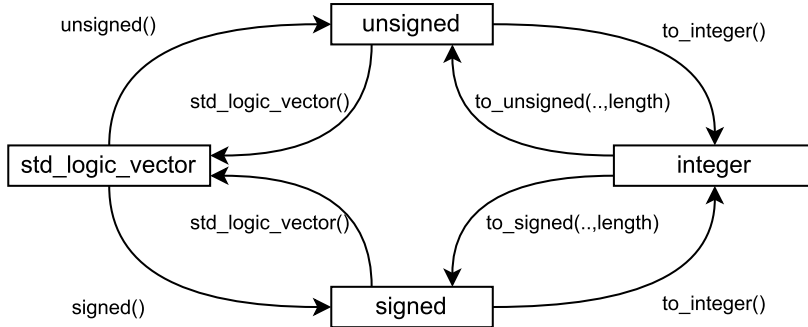
unsigned

std_logic_vector

integer

signed

Numerical Operations



Flip Flop: VHDL Description

Flip Flop

```
process (
begin
    if
    elsif
    then
    then

    end if;
end process;
```

```
process (clk, rst)
begin
    if rst = '1' then
        -- reset ff signal to default
    elsif rising_edge(clk) then
```

Task Overview

1. Adder
2. Register
3. Program Counter
4. (Optimization)