Exercise 05

TASK 3

Run Synthesis and Implementation. Explore the utilized resources. Now, report utilization, power and timing. Utilization and Timing can be explored directly. For Power Analysis, export the saif-file from Post-Implementation-Simulation.

Resource	Utilization	Available	Utilization %
LUT	106	53200	0.20
LUTRAM	88	17400	0.51
FF	32	106400	0.03
IO	81	200	40.50

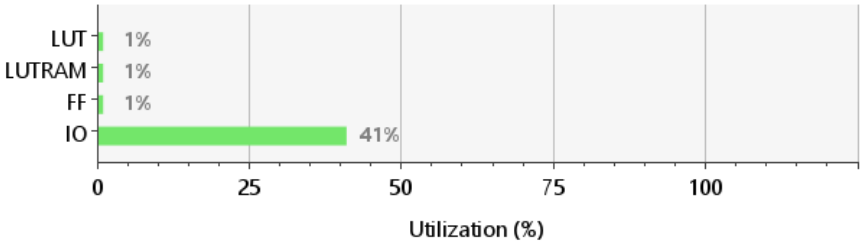

ABBILDUNG 1: UTILIZATION OF THE FPGA RESOURCES

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.112 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26,3°C**
Thermal Margin:	58,7°C (4,9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	11,5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

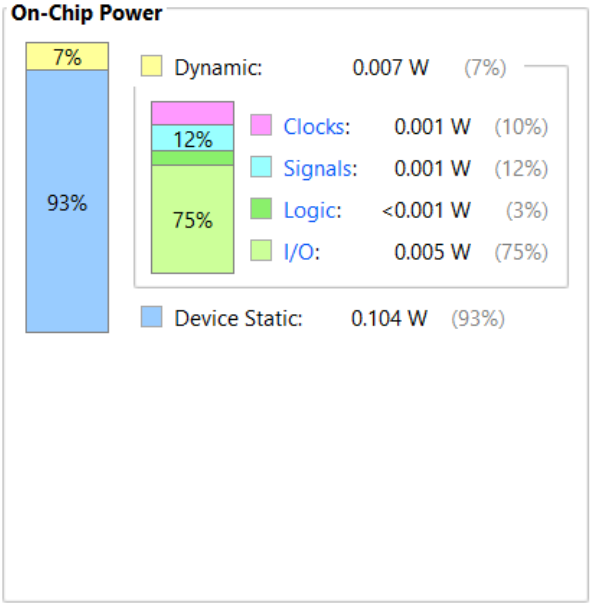

ABBILDUNG 2: POWER OF THE FPGA

TASK 4

In the previous task, you explored a mapping of the entity to the FPGA resources. What other components are available for this mapping? Modify the synthesis settings and rerun synthesis and implementation and the evaluation of your design.

When using unmodified synthesis settings, Vivado will use RAM64M blocks to store the data.

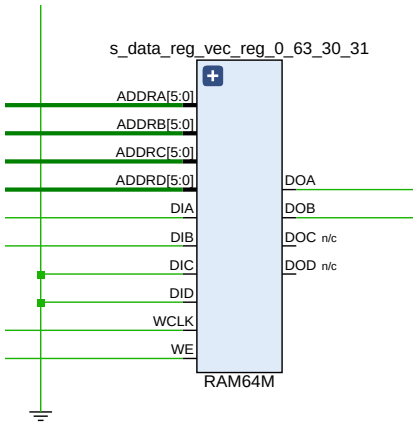

ABBILDUNG 3: RAM64M BLOCK

Modifying the synthesis settings yields no changes.