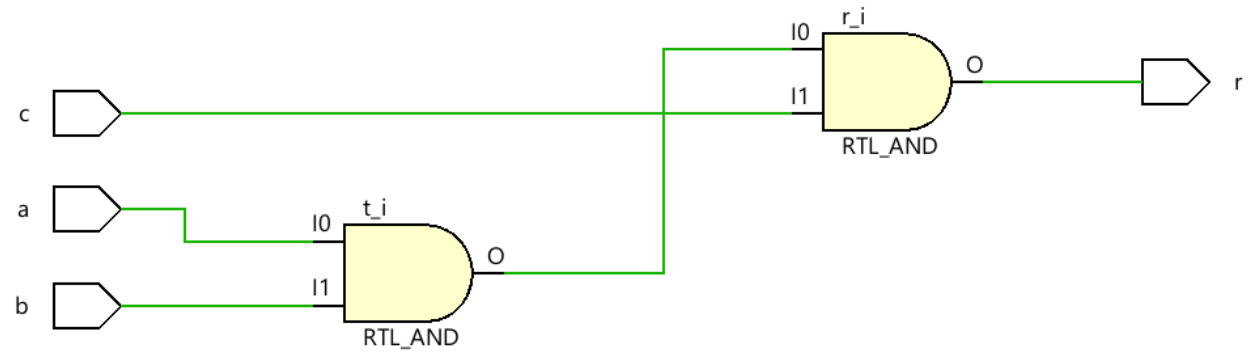
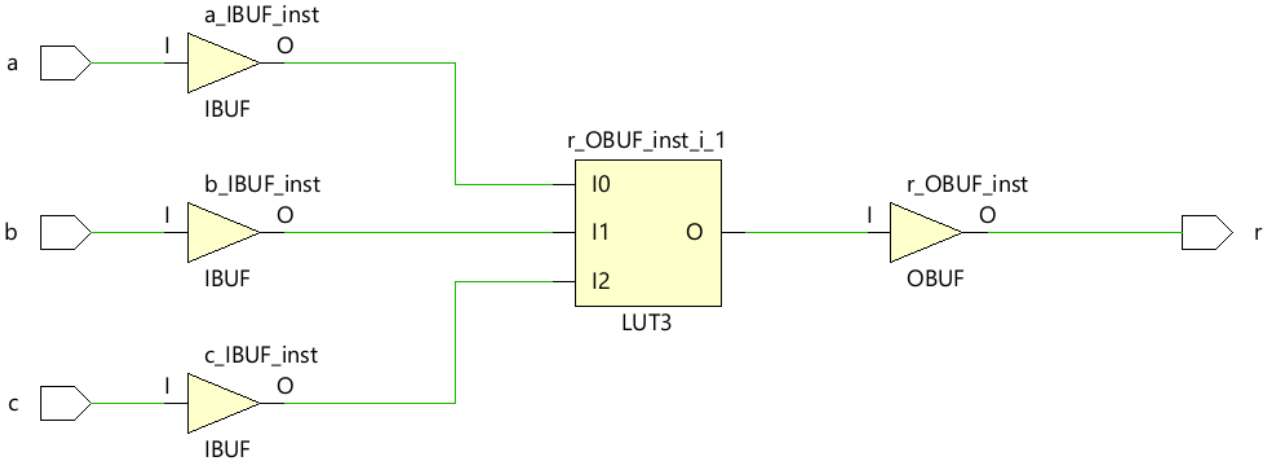
Exercise 01

Task 1 - The AND3 Gate



RTL Analysis - Schematic



Synthesis - Schematic