RV32I Base Integer Instruction Set

imm[31:12]				rd	0110111	LUI rd, imm
imm[31:12]				rd	0010111	AUIPC rd, imm
imm[20|10:1|11|19:12]				rd	1101111	JAL rd, ipc
imm[11:0]		rs1	000	rd	1100111	JALR rd, rs1, imm
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ rs1, rs2, ipc
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE rs1, rs2, ipc
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT rs1, rs2, ipc
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE rs1, rs2, ipc
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU rs1, rs2, ipc
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU rs1, rs2, ipc
imm[11:0]		rs1	000	rd	0000011	LB rd, imm(rs1)
imm[11:0]		rs1	001	rd	0000011	LH rd, imm(rs1)
imm[11:0]		rs1	010	rd	0000011	LW rd, imm(rs1)
imm[11:0]		rs1	100	rd	0000011	LBU rd, imm(rs1)
imm[11:0]		rs1	101	rd	0000011	LHU rd, imm(rs1)
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB rs2, imm(rs1)
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH rs2, imm(rs1)
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW rs2, imm(rs1)
imm[11:0]		rs1	000	rd	0010011	ADDI rd, rs1, imm
imm[11:0]		rs1	010	rd	0010011	SLTI rd, rs1, imm
imm[11:0]		rs1	011	rd	0010011	SLTIU rd, rs1, imm
imm[11:0]		rs1	100	rd	0010011	XORI rd, rs1, imm
imm[11:0]		rs1	110	rd	0010011	ORI rd, rs1, imm
imm[11:0]		rs1	111	rd	0010011	ANDI rd, rs1, imm
000000 | 0	shamt	rs1	001	rd	0010011	SLLI rd, rs1, imm
000000 | 0	shamt	rs1	101	rd	0010011	SRLI rd, rs1, imm
010000 | 0	shamt	rs1	101	rd	0010011	SRAI rd, rs1, imm
0000000	rs2	rs1	000	rd	0110011	ADD rd, rs1, rs2
0100000	rs2	rs1	000	rd	0110011	SUB rd, rs1, rs2
0000000	rs2	rs1	001	rd	0110011	SLL rd, rs1, rs2
0000000	rs2	rs1	010	rd	0110011	SLT rd, rs1, rs2
0000000	rs2	rs1	011	rd	0110011	SLTU rd, rs1, rs2
0000000	rs2	rs1	100	rd	0110011	XOR rd, rs1, rs2
0000000	rs2	rs1	101	rd	0110011	SRL rd, rs1, rs2
0100000	rs2	rs1	101	rd	0110011	SRA rd, rs1, rs2
0000000	rs2	rs1	110	rd	0110011	OR rd, rs1, rs2
0000000	rs2	rs1	111	rd	0110011	AND rd, rs1, rs2
0000 | pred	succ	00000	000	00000	0001111	FENCE
00000000000000000			001	00000	0001111	FENCE.I

RV64I Base Integer Instruction Set (in addition to RV32I)

imm[11:0]		rs1	110	rd	0000011	LWU rd, imm(rs1)
imm[11:0]		rs1	011	rd	0000011	LD rd, imm(rs1)
imm[11:5]	rs2	rs1	011	imm[4:0]	0100011	SD rs2, imm(rs1)
000000 | shamt		rs1	001	rd	0010011	SLLI rd, rs1, imm
000000 | shamt		rs1	101	rd	0010011	SRLI rd, rs1, imm
010000 | shamt		rs1	101	rd	0010011	SRAI rd, rs1, imm
imm[11:0]		rs1	000	rd	0011011	ADDIW rd, rs1, imm
0000000	shamt	rs1	001	rd	0011011	SLLIW rd, rs1, imm
0000000	shamt	rs1	101	rd	0011011	SRLIW rd, rs1, imm
0100000	shamt	rs1	101	rd	0011011	SRAIW rd, rs1, imm
0000000	rs2	rs1	000	rd	0111011	ADDW rd, rs1, rs2
0100000	rs2	rs1	000	rd	0111011	SUBW rd, rs1, rs2
0000000	rs2	rs1	001	rd	0111011	SLLW rd, rs1, rs2
0000000	rs2	rs1	101	rd	0111011	SRLW rd, rs1, rs2
0100000	rs2	rs1	101	rd	0111011	SRAW rd, rs1, rs2

RV32M Standard Extension for Integer Multiply and Divide

0000001	rs2	rs1	000	rd	0110011	MUL rd, rs1, rs2
0000001	rs2	rs1	001	rd	0110011	MULH rd, rs1, rs2
0000001	rs2	rs1	010	rd	0110011	MULHSU rd, rs1, rs2
0000001	rs2	rs1	011	rd	0110011	MULHU rd, rs1, rs2
0000001	rs2	rs1	100	rd	0110011	DIV rd, rs1, rs2

0000001	rs2	rs1	101	rd	0110011	DIVU rd, rs1, rs2
0000001	rs2	rs1	110	rd	0110011	REM rd, rs1, rs2
0000001	rs2	rs1	111	rd	0110011	REMU rd, rs1, rs2

RV64M Standard Extension for Integer Multiply and Divide (in addition to RV32M)

0000001	rs2	rs1	000	rd	0111011	MULW rd, rs1, rs2
0000001	rs2	rs1	100	rd	0111011	DIVW rd, rs1, rs2
0000001	rs2	rs1	101	rd	0111011	DIVUW rd, rs1, rs2
0000001	rs2	rs1	110	rd	0111011	REMW rd, rs1, rs2
0000001	rs2	rs1	111	rd	0111011	REMUW rd, rs1, rs2

RV32A Standard Extension for Atomic Instructions

00010	aqrl	00000	rs1	010	rd	0101111	LR.W rd, (rs1)
00011	aqrl	rs2	rs1	010	rd	0101111	SC.W rd, rs2, (rs1)
00001	aqrl	rs2	rs1	010	rd	0101111	AMOSWAP.W rd, rs2, (rs1)
00000	aqrl	rs2	rs1	010	rd	0101111	AMOADD.W rd, rs2, (rs1)
00100	aqrl	rs2	rs1	010	rd	0101111	AMOXOR.W rd, rs2, (rs1)
01000	aqrl	rs2	rs1	010	rd	0101111	AMOOR.W rd, rs2, (rs1)
01100	aqrl	rs2	rs1	010	rd	0101111	AMOAND.W rd, rs2, (rs1)
10000	aqrl	rs2	rs1	010	rd	0101111	AMOMIN.W rd, rs2, (rs1)
10100	aqrl	rs2	rs1	010	rd	0101111	AMOMAX.W rd, rs2, (rs1)
11000	aqrl	rs2	rs1	010	rd	0101111	AMOMINU.W rd, rs2, (rs1)
11100	aqrl	rs2	rs1	010	rd	0101111	AMOMAXU.W rd, rs2, (rs1)

RV64A Standard Extension for Atomic Instructions (in addition to RV32A)

00010	aqrl	00000	rs1	011	rd	0101111	LR.D rd, (rs1)
00011	aqrl	rs2	rs1	011	rd	0101111	SC.D rd, rs2, (rs1)
00001	aqrl	rs2	rs1	011	rd	0101111	AMOSWAP.D rd, rs2, (rs1)
00000	aqrl	rs2	rs1	011	rd	0101111	AMOADD.D rd, rs2, (rs1)
00100	aqrl	rs2	rs1	011	rd	0101111	AMOXOR.D rd, rs2, (rs1)
01000	aqrl	rs2	rs1	011	rd	0101111	AMOOR.D rd, rs2, (rs1)
01100	aqrl	rs2	rs1	011	rd	0101111	AMOAND.D rd, rs2, (rs1)
10000	aqrl	rs2	rs1	011	rd	0101111	AMOMIN.D rd, rs2, (rs1)
10100	aqrl	rs2	rs1	011	rd	0101111	AMOMAX.D rd, rs2, (rs1)
11000	aqrl	rs2	rs1	011	rd	0101111	AMOMINU.D rd, rs2, (rs1)
11100	aqrl	rs2	rs1	011	rd	0101111	AMOMAXU.D rd, rs2, (rs1)

RV32S Standard Extension for Supervisor-level Instructions

00000000000000000000000001110011					SCALL
00000000000100000000000001110011					SBREAK
00010000000000000000000001110011					SRET
000100000001	rs1	000000001110011			SFENCE.VM
00010000001000000000000001110011					WFI
00110000011000000000000001110011					MRTH
00110000010100000000000001110011					MRTS
00100000010100000000000001110011					HRTS
11000000000000000010			rd	1110011	RDCYCLE rd, csr, rs1
11000000000100000010			rd	1110011	RDTIME rd, csr, rs1
11000000001000000010			rd	1110011	RDINSTRET rd, csr, rs1
11001000000000000010			rd	1110011	RDCYCLEH rd, csr, rs1
11001000000100000010			rd	1110011	RDTIMEH rd, csr, rs1
11001000001000000010			rd	1110011	RDINSTRETH rd, csr, rs1
imm[11:0]	rs1	001	rd	1110011	CSRRW rd, csr, rs1
imm[11:0]	rs1	010	rd	1110011	CSRRS rd, csr, rs1
imm[11:0]	rs1	011	rd	1110011	CSRRC rd, csr, rs1
imm[11:0]	imm[4:0]	101	rd	1110011	CSRRWI rd, csr, irs1
imm[11:0]	imm[4:0]	110	rd	1110011	CSRRSI rd, csr, irs1
imm[11:0]	imm[4:0]	111	rd	1110011	CSRRCI rd, csr, irs1

RV32F Standard Extension for Single-Precision Floating-Point

imm[11:0]		rs1	010	rd	0000111	FLW frd, imm(rs1)
imm[11:5]	rs2	rs1	010	imm[4:0]	0100111	FSW frs2, imm(rs1)
rs3	00	rs2	rs1	rm	rd	1000011	FMADD.S frd, frs1, frs2, frs3
rs3	00	rs2	rs1	rm	rd	1000111	FMSUB.S frd, frs1, frs2, frs3

rs3	00	rs2	rs1	rm	rd	1001011	FNMSUB.S frd, frs1, frs2, frs3
rs3	00	rs2	rs1	rm	rd	1001111	FNMADD.S frd, frs1, frs2, frs3
0000000		rs2	rs1	rm	rd	1010011	FADD.S frd, frs1, frs2
0000100		rs2	rs1	rm	rd	1010011	FSUB.S frd, frs1, frs2
0001000		rs2	rs1	rm	rd	1010011	FMUL.S frd, frs1, frs2
0001100		rs2	rs1	rm	rd	1010011	FDIV.S frd, frs1, frs2
0010000		rs2	rs1	000	rd	1010011	FSGNJ.S frd, frs1, frs2
0010000		rs2	rs1	001	rd	1010011	FSGNJN.S frd, frs1, frs2
0010000		rs2	rs1	010	rd	1010011	FSGNJX.S frd, frs1, frs2
0010100		rs2	rs1	000	rd	1010011	FMIN.S frd, frs1, frs2
0010100		rs2	rs1	001	rd	1010011	FMAX.S frd, frs1, frs2
010110000000			rs1	rm	rd	1010011	FSQRT.S frd, frs1, frs2
1010000		rs2	rs1	000	rd	1010011	FLE.S frd, rs1, frs2
1010000		rs2	rs1	001	rd	1010011	FLT.S frd, rs1, frs2
1010000		rs2	rs1	010	rd	1010011	FEQ.S frd, rs1, frs2
110000000000			rs1	rm	rd	1010011	FCVT.W.S rd, frs1
110000000001			rs1	rm	rd	1010011	FCVT.WU.S rd, frs1
110100000000			rs1	rm	rd	1010011	FCVT.S.W frd, rs1
110100000001			rs1	rm	rd	1010011	FCVT.S.WU frd, rs1
111000000000			rs1	000	rd	1010011	FMV.X.S rd, frs1
111000000000			rs1	001	rd	1010011	FCLASS.S rd, frs1
111100000000			rs1	000	rd	1010011	FMV.S.X frd, rs1
00000000001100000010					rd	1110011	FRCSR rd, csr, rs1
00000000001000000010					rd	1110011	FRRM rd, csr, rs1
00000000000100000010					rd	1110011	FRFLAGS rd, csr, rs1
000000000011			rs1	001	rd	1110011	FSCSR rd, csr, rs1
000000000010			rs1	001	rd	1110011	FSRM rd, csr, rs1
000000000001			rs1	001	rd	1110011	FSFLAGS rd, csr, rs1
000000000010			imm[4:0]	101	rd	1110011	FSRMI rd, csr, irs1
000000000001			imm[4:0]	101	rd	1110011	FSFLAGSI rd, csr, irs1

RV64F Standard Extension for Single-Precision Floating-Point (in addition to RV32F)

110000000010	rs1	rm	rd	1010011	FCVT.L.S rd, frs1
110000000011	rs1	rm	rd	1010011	FCVT.LU.S rd, frs1
110100000010	rs1	rm	rd	1010011	FCVT.S.L frd, rs1
110100000011	rs1	rm	rd	1010011	FCVT.S.LU frd, rs1

RV32D Standard Extension for Double-Precision Floating-Point

imm[11:0]			rs1	011	rd	0000111	FLD frd, imm(rs1)
imm[11:5]		rs2	rs1	011	imm[4:0]	0100111	FSD frs2, imm(rs1)
rs3	01	rs2	rs1	rm	rd	1000011	FMADD.D frd, frs1, frs2, frs3
rs3	01	rs2	rs1	rm	rd	1000111	FMSUB.D frd, frs1, frs2, frs3
rs3	01	rs2	rs1	rm	rd	1001011	FNMSUB.D frd, frs1, frs2, frs3
rs3	01	rs2	rs1	rm	rd	1001111	FNMADD.D frd, frs1, frs2, frs3
0000001		rs2	rs1	rm	rd	1010011	FADD.D frd, frs1, frs2
0000101		rs2	rs1	rm	rd	1010011	FSUB.D frd, frs1, frs2
0001001		rs2	rs1	rm	rd	1010011	FMUL.D frd, frs1, frs2
0001101		rs2	rs1	rm	rd	1010011	FDIV.D frd, frs1, frs2
0010001		rs2	rs1	000	rd	1010011	FSGNJ.D frd, frs1, frs2
0010001		rs2	rs1	001	rd	1010011	FSGNJN.D frd, frs1, frs2
0010001		rs2	rs1	010	rd	1010011	FSGNJX.D frd, frs1, frs2
0010101		rs2	rs1	000	rd	1010011	FMIN.D frd, frs1, frs2
0010101		rs2	rs1	001	rd	1010011	FMAX.D frd, frs1, frs2
010000000001			rs1	rm	rd	1010011	FCVT.S.D frd, frs1
010000100000			rs1	rm	rd	1010011	FCVT.D.S frd, frs1
010110100000			rs1	rm	rd	1010011	FSQRT.D frd, frs1
1010001		rs2	rs1	000	rd	1010011	FLE.D frd, rs1, frs2
1010001		rs2	rs1	001	rd	1010011	FLT.D frd, rs1, frs2
1010001		rs2	rs1	010	rd	1010011	FEQ.D frd, rs1, frs2
110000100000			rs1	rm	rd	1010011	FCVT.W.D rd, frs1
110000100001			rs1	rm	rd	1010011	FCVT.WU.D rd, frs1
110100100000			rs1	rm	rd	1010011	FCVT.D.W frd, rs1
110100100001			rs1	rm	rd	1010011	FCVT.D.WU frd, rs1
111000100000			rs1	000	rd	1010011	FMV.X.D rd, frs1

111000100000	rs1	001	rd	1010011	FCLASS.D rd, frs1
111100100000	rs1	000	rd	1010011	FMV.D.X frd, rs1

RV64D Standard Extension for Double-Precision Floating-Point (in addition to RV32D)

110000100010	rs1	rm	rd	1010011	FCVT.L.D rd, frs1
110000100011	rs1	rm	rd	1010011	FCVT.LU.D rd, frs1
110100100010	rs1	rm	rd	1010011	FCVT.D.L frd, rs1
110100100011	rs1	rm	rd	1010011	FCVT.D.LU frd, rs1

RV32C Standard Extension for Compressed Instructions

000	imm[5:4|9:6|2|3]			rd'	00	C.ADDI4SPN rd, rs1, imm
001	imm[5:3]		rs1'	imm[7:6]	rd'	00	C.FLD frd, imm(rs1)
010	imm[5:3]		rs1'	imm[2|6]	rd'	00	C.LW rd, imm(rs1)
011	imm[5:3]		rs1'	imm[2|6]	rd'	00	C.FLW frd, imm(rs1)
101	imm[5:3]		rs1'	imm[7:6]	rs2'	00	C.FSD frs2, imm(rs1)
110	imm[5:3]		rs1'	imm[2|6]	rs2'	00	C.SW rs2, imm(rs1)
111	imm[5:3]		rs1'	imm[2|6]	rs2'	00	C.FSW frs2, imm(rs1)
0000000000000001							C.NOP
000	imm[5]	rs1/rd		imm[4:0]		01	C.ADDI rd, rs1, imm
001	imm[11|4|9:8|10|6|7|3:1|5]					01	C.JAL rd, ipc
010	imm[5]	rs1/rd		imm[4:0]		01	C.LI rd, rs1, imm
011	imm[17]	rd		imm[16:12]		01	C.LUI rd, imm
011	imm[9]	rs1/rd		imm[4|6|8:7|5]		01	C.ADDI16SP rd, rs1, imm
100	imm	imm	rs1'/rd'	imm	rs2'	01	C.SRLI rd, rs1, imm
100	imm	imm	rs1'/rd'	imm	rs2'	01	C.SRAI rd, rs1, imm
100	imm	imm	rs1'/rd'	imm	rs2'	01	C.ANDI rs1, rs2, ipc
100011			rs1'/rd'	00	rs2'	01	C.SUB rd, rs1, rs2
100011			rs1'/rd'	01	rs2'	01	C.XOR rd, rs1, rs2
100011			rs1'/rd'	10	rs2'	01	C.OR rd, rs1, rs2
100011			rs1'/rd'	11	rs2'	01	C.AND rd, rs1, rs2
100111			rs1'/rd'	00	rs2'	01	C.SUBW rd, rs1, rs2
100111			rs1'/rd'	01	rs2'	01	C.ADDW rd, rs1, rs2
101	imm[11|4|9:8|10|6|7|3:1|5]					01	C.J rd, ipc
110	imm[8|4:3]		rs1'	imm[7:6|2:1|5]		01	C.BEQZ rs1, rs2, ipc
111	imm[8|4:3]		rs1'	imm[7:6|2:1|5]		01	C.BNEZ rs1, rs2, ipc
000	imm[5]	rd		imm[4:0]		10	C.SLLI rd, rs1, imm
001	imm[5]	rd		imm[4:3|8:6]		10	C.FLDSP frd, imm(rs1)
010	imm[5]	rd		imm[4:6|7:6]		10	C.LWSP rd, imm(rs1)
011	imm[5]	rd		imm[4:6|7:6]		10	C.FLWSP frd, imm(rs1)
1000	rs1			0000010			C.JR rd, rs1, imm
1000	rd			rs2		10	C.MV rd, rs1, rs2
1001000000000010							C.EBREAK
1001	rs1			0000010			C.JALR rd, rs1, imm
1001	rd			rs2		10	C.ADD rd, rs1, rs2
101	imm[5:3|8:6]			rs2		10	C.FSDSP frs2, imm(rs1)
110	imm[5:2|7:6]			rs2		10	C.SWSP rs2, imm(rs1)
111	imm[5:2|7:6]			rs2		10	C.FSWSP frs2, imm(rs1)

RV64C Standard Extension for Compressed Instructions (in addition to RV32C)

011	imm[5:3]		rs1'	imm[7:6]	rd'	00	C.LD rd, imm(rs1)
111	imm[5:3]		rs1'	imm[7:6]	rs2'	00	C.SD rs2, imm(rs1)
001	imm[5]	rs1/rd		imm[4:0]		01	C.ADDIW rd, rs1, imm
011	imm[5]	rs1/rd		imm[4:3|8:6]		10	C.LDSP rd, imm(rs1)
111	imm[5:3|8:6]			rs2		10	C.SDSP rs2, imm(rs1)