

JIAQI GU

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EDUCATION

The University of Texas at Austin	Ph.D., Electrical and Computer Engineering Integrated Circuits and System Track. Overall GPA 4.00/4.00	May 2023 (expected)
Fudan University, Shanghai, China	B.E., Microelectronic Science and Engineering (Eminent Engineer Program). Overall GPA: 3.91/4.00	Jul 2018

EXPERIENCE

Graduate Research Assistant, The University of Texas at Austin	Jan 2019 – Present
<ul style="list-style-type: none">Designed novel architecture for area-efficient optical neural network based on Fast Fourier Transformation; achieved 3-4x area reduction than previous ONN architectures; Wrote a research paper that was published at <i>ACM/IEEE ASP-DAC, Jan 2020</i>Developed noise-aware quantization scheme to enable robust optical neural networks with low-precision voltage controls; achieved better accuracy and robustness to limited control resolution and device-level variations than previous methods; Wrote a research paper that will be published at <i>DATE, Mar 2020</i>Developed on-chip learning algorithm to improve training efficiency and robustness for optical neural networks with stochastic zeroth-order optimization; Wrote a research paper that will be published at <i>DAC, Jul 2020</i>Proposed efficient on-chip learning algorithm for optical neural networks with stochastic zeroth-order optimization algorithms; achieved 3-4x higher ONN forward efficiency and better robustness to thermal variation than previous methodsWorked on photonic chip tapeout for novel ONN architectures with AMF PDKs using Synopsys optodesigner and Lumerical toolkits.Collaborated on the design and validation of photonic recurrent neural networksCollaborated on developing accelerated batch-based concurrent VLSI detailed placement with CUDA on GPUsCollaborated on high-performance VLSI analytical global placement acceleration with CUDA on GPUs	
Graduate Research Assistant, The University of Texas at Austin	Sep 2018 – Jan 2019
<ul style="list-style-type: none">Projected RISC-V Rocket Core on Zynq FPGA and achieved communication between themCustomized FIRRTL transformation and built infrastructure for fault injection and system state snapshot	
Research Assistant, Fudan University, Shanghai, China	Aug 2017 – Jul 2018
<ul style="list-style-type: none">Modified infant brain atlas offered by UNC and created complete tissue probability mapsDeveloped two-stage reconstruction framework for infant thin-section MR image reconstruction by using GANs and CNN; research is developing brand new method to improve reconstruction performance by fusing multi-planar MR images, and improving PSNR, SSIM, and NMI by 26.2%, 93.4%, and 25.3% respectively compared to bicubic interpolationWrote a research paper that was published at <i>IEEE Access, May 2019</i>Collaborated on super-resolution reconstruction of ultra-sonic imaging using deep learning techniques	

PUBLICATIONS

- Gu, J., Zhao, Z., Feng, C., Li, W., Chen, R., Pan, Z. "FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization", *ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, Jul. 19-23, 2020*. (accepted)
- Miscuglio, M., Hu, Z., Li, S., Gu, J., Babakhani, A., Gupta, P., Wong, C., Pan, Z., Bank, S., Dalir, H., Sorger, J. "Million-channel parallelism Fourier-optic convolutional filter and neural network processor", *CLEO, San Jose, CA, May 10-15, 2020*.
- Feng, C., Ying, Z., Zhao, Z., Gu, J., Pan, Z., Chen, R. "Integrated WDM-based Optical Comparator for High-speed Computing", *CLEO, San Jose, CA, May 10-15, 2020*.
- Feng, C., Zhao, Z., Ying, Z., Gu, J., Pan, Z., Chen, R. "Compact design of On-chip Elman Optical Recurrent Neural Network", *CLEO, San Jose, CA, May 10-15, 2020*.
- Ying, Z., Feng, C., Zhao, Z., Dhar, S., Dalir, H., Gu, J., Cheng, Y., Soref, R., Pan, Z., Chen, R. "Electronic-photonic Arithmetic Logic Unit for High-speed Computing", *Nature Communications, Apr. 2020*.
- Gu, J., Zhao, Z., Feng, C., Chen, R., Pan, Z. et al. "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, Mar. 09-13, 2020*.
- Liu, M., Zhu, K., Gu, J., Shen, L., Tang, X., Sun, N., Pan, D. "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning", *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, Mar. 09-13, 2020*.
- Feng, C., Ying, Z., Zhao, Z., Gu, J., Pan, D., Chen, R. "Wavelength-division-multiplexing based electronic photonic network for high speed computing", *SPIE Photonics West, San Francisco, CA, United States, Feb. 01-06, 2020*.

- Lin, Y., Li, W., **Gu, J.**, Ren, M., Khailany, B., Pan, D. "ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Feb., 2020.
- **Gu, J.**, Zhao, Z., Feng, C., Liu, M., Chen, R., Pan, D. "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture", *ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020. (**Best Paper Award**)
- Zhao, Z., **Gu, J.**, Ying, Z., Feng, C., Chen, R., Pan, D. "Design Technology for Scalable and Robust Photonic Integrated Circuits", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019. (invited paper)
- **Gu, J.**, Yu, J., Li, Z., Wang, Y., Yang, H., Qiao, Z. "Deep Generative Adversarial Networks for Thin-section Infant MR Image Reconstruction", *IEEE Access*, May, 2019.
- **Gu, J.**, Wang, R., Wang, J., Lai, J., Duan, Q. "Remote Embedded Simulation System for SW/HW Co-design Based On Dynamic Partial Reconfiguration", *IEEE 12th International Conference on ASIC*, 2017.

RELATED GRADUATE COURSES/CERTIFICATE

- Computer Architecture (EE 382N 1)
- High Speed Computer Arithmetic (EE 382N 14)
- Computer Architecture: Parallelism/Locality (EE 382N 20)
- Parallel Algorithm Scientific Computing (CS 395T)
- Reinforcement Learning: Theory & Practice (CS 394R)
- VLSI I (EE 382M.7)
- VLSI Physical Design Automation (EE 382M)
- Cross-layer Machine Learning Algorithm/Hardware Co-design (EE 382V)
- Certificate of NVIDIA workshop on Fundamentals of Accelerated Computing with CUDA Python, NVIDIA DLI, 2019

HONORS

- Best Paper Award, 25th ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC) 2020
- 4th Place, 2019 DAC System Design Contest on Low Power Object Detection 2019
- First Prize Scholarship, Fudan University 2017 – 2018
- Top 5, 2018 HUAWEI & FUTURELAB AI Contest (CV Group) 2018
- Top 11%, 2017 IEEEExtreme Global Programming Competition (out of 3,350 teams worldwide) 2017
- 2nd & 3rd Prize, National Mathematical Contest in Modeling 2016, 2017

ADDITIONAL INFORMATION

Computer Skills: Python (PyTorch/Tensorflow), C/C++, CUDA, Matlab, Verilog

Software: Cadence Virtuoso, Synopsys Hspice, Xilinx Vivado Design Suite, Synopsys Optodesigner