EECE 2322: Fundamentals of Digital Design and Computer Organization

Lecture 12_1: Timing of Digital Systems

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Northeastern University

Timing is IMPORTANT in Digital Systems

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https://en.wikipedia.org › wiki › Apple_M1

Apple M1 - Wikipedia

The **Apple M1** is an ARM-based system on a chip (SoC) designed by Apple Inc. as a central processing unit (CPU) and graphics processing unit (GPU) for its ...

Max. CPU clock rate: 3.2 GHz

Technology node: 5 nm

L1 cache: 192+128 KB per core (perform…

Common manufacturer(s): TSMC

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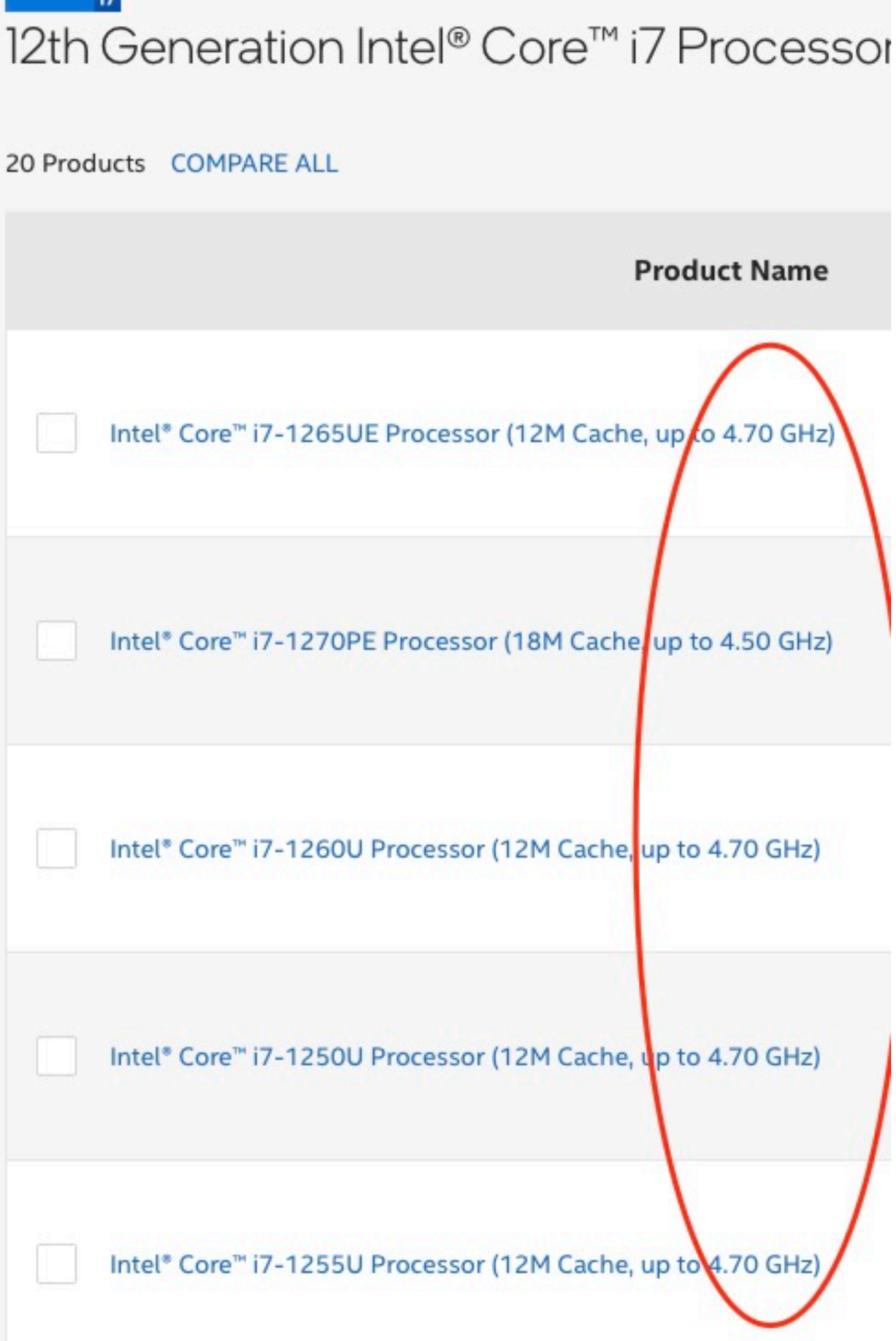

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- One of the most important parameters in designing a digital system
- Determines the highest clock frequency that can be achieved
- Decided by the "slowest" data path, i.e., critical path

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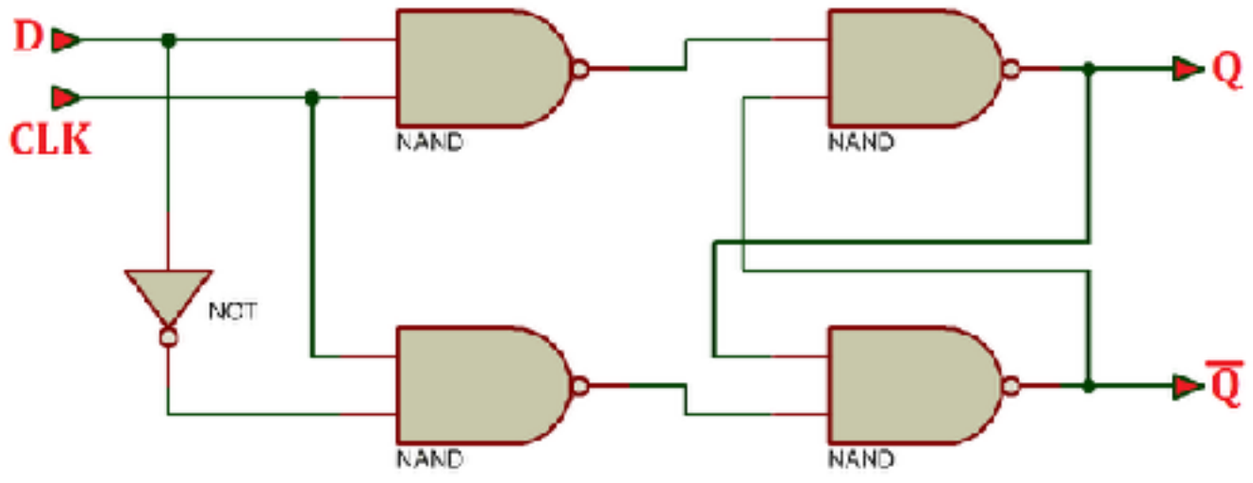
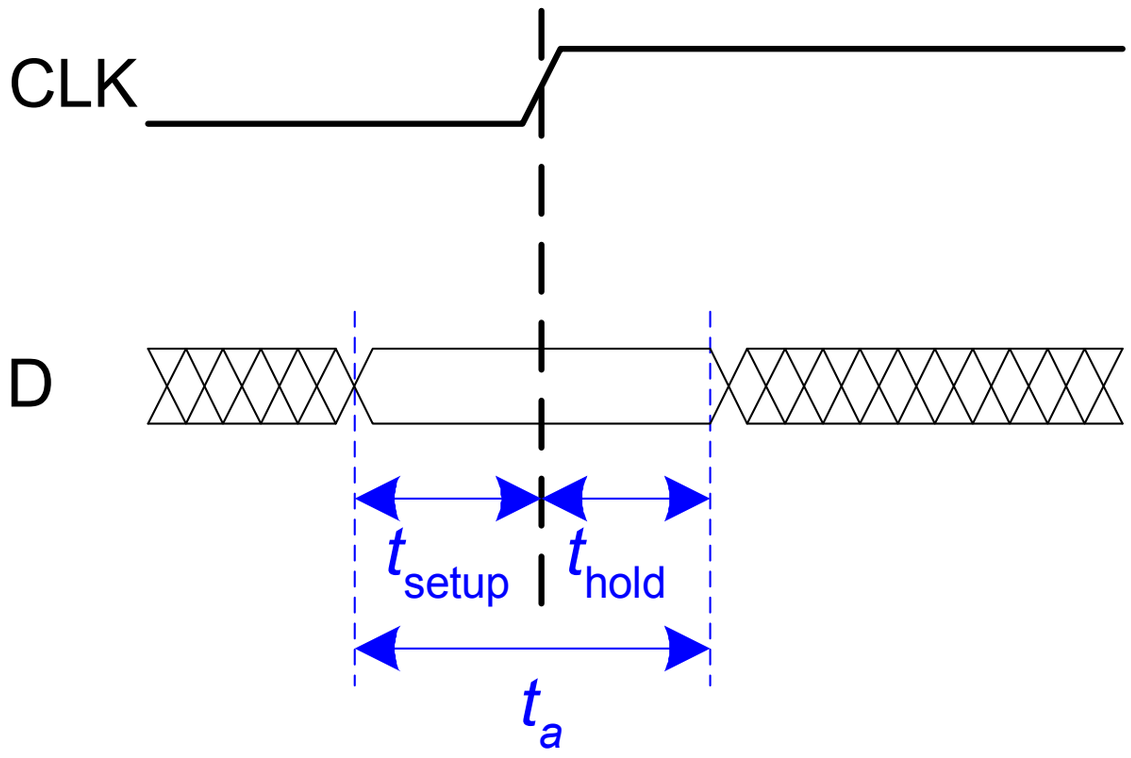
Timing is IMPORTANT in Digital Systems

- Example
  - Flip-flop samples D at clock edge
  - D must be stable when sampled
  - Similar to a photograph, D must be stable around clock edge
  - If not, metastability can occur



Input Timing Constraints

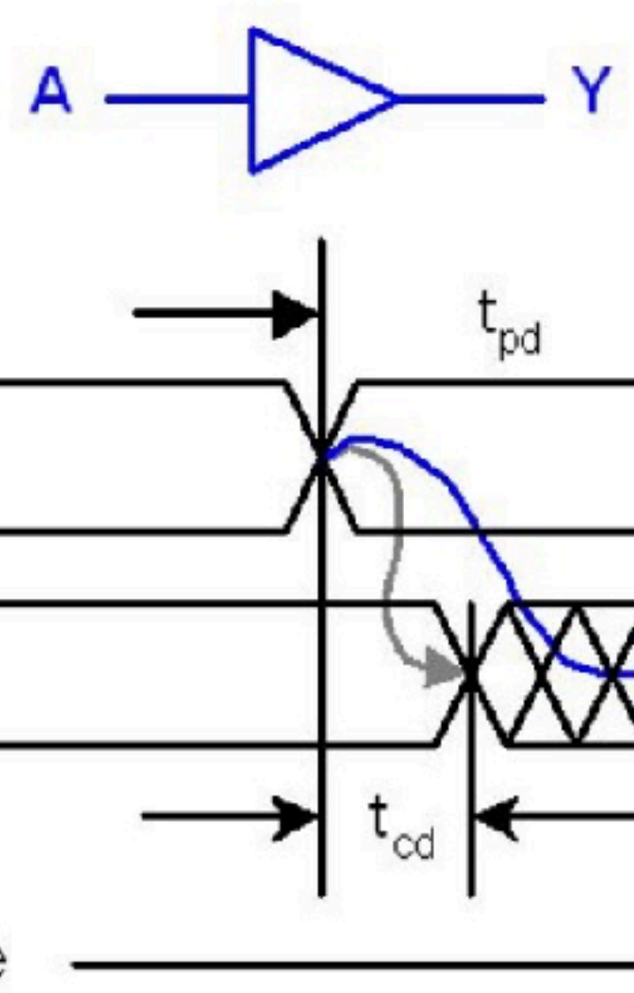
- **Setup time:** t_{setup} = time *before* clock edge data must be stable (i.e. not changing)
- **Hold time:** t_{hold} = time *after* clock edge data must be stable
- **Aperture time:** t_a = time *around* clock edge data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)



Output Timing Constraints

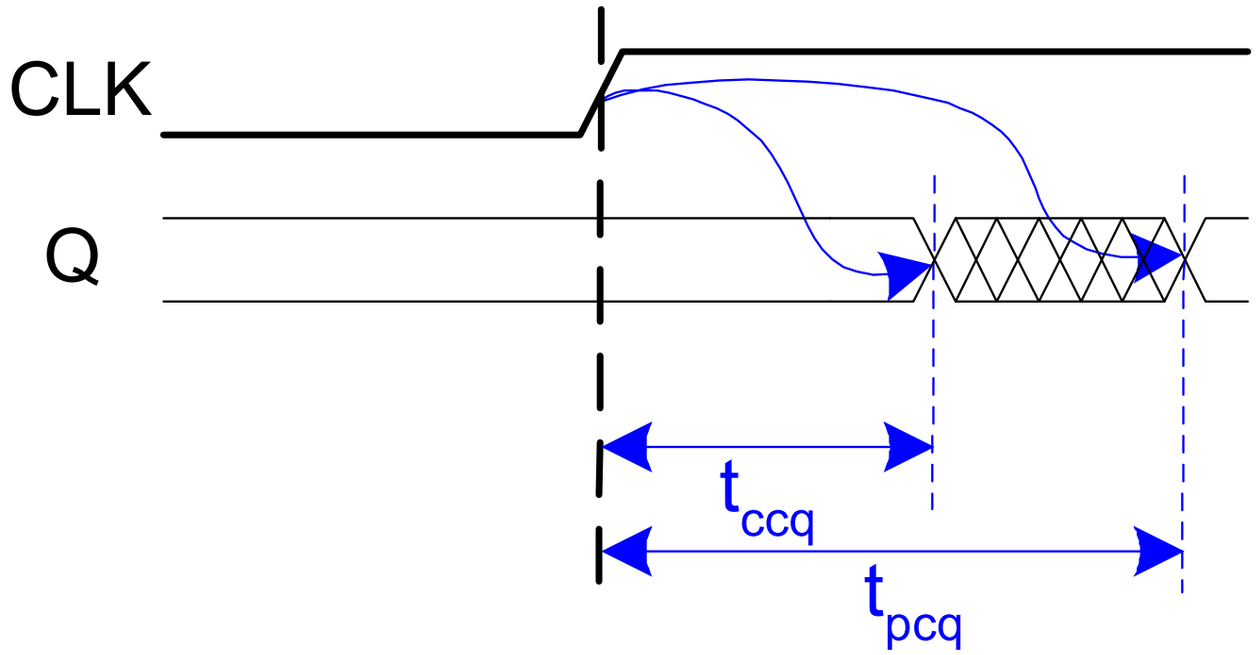
Propagation Delay: t_{pd} = max delay from input to output

Contamination Delay: t_{cd} = min delay from input to output



Output Timing Constraints for **Q-output**

- **Propagation delay:** t_{pcq} = time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)
- **Contamination delay:** t_{ccq} = time after clock edge that Q might be unstable (i.e., start changing)

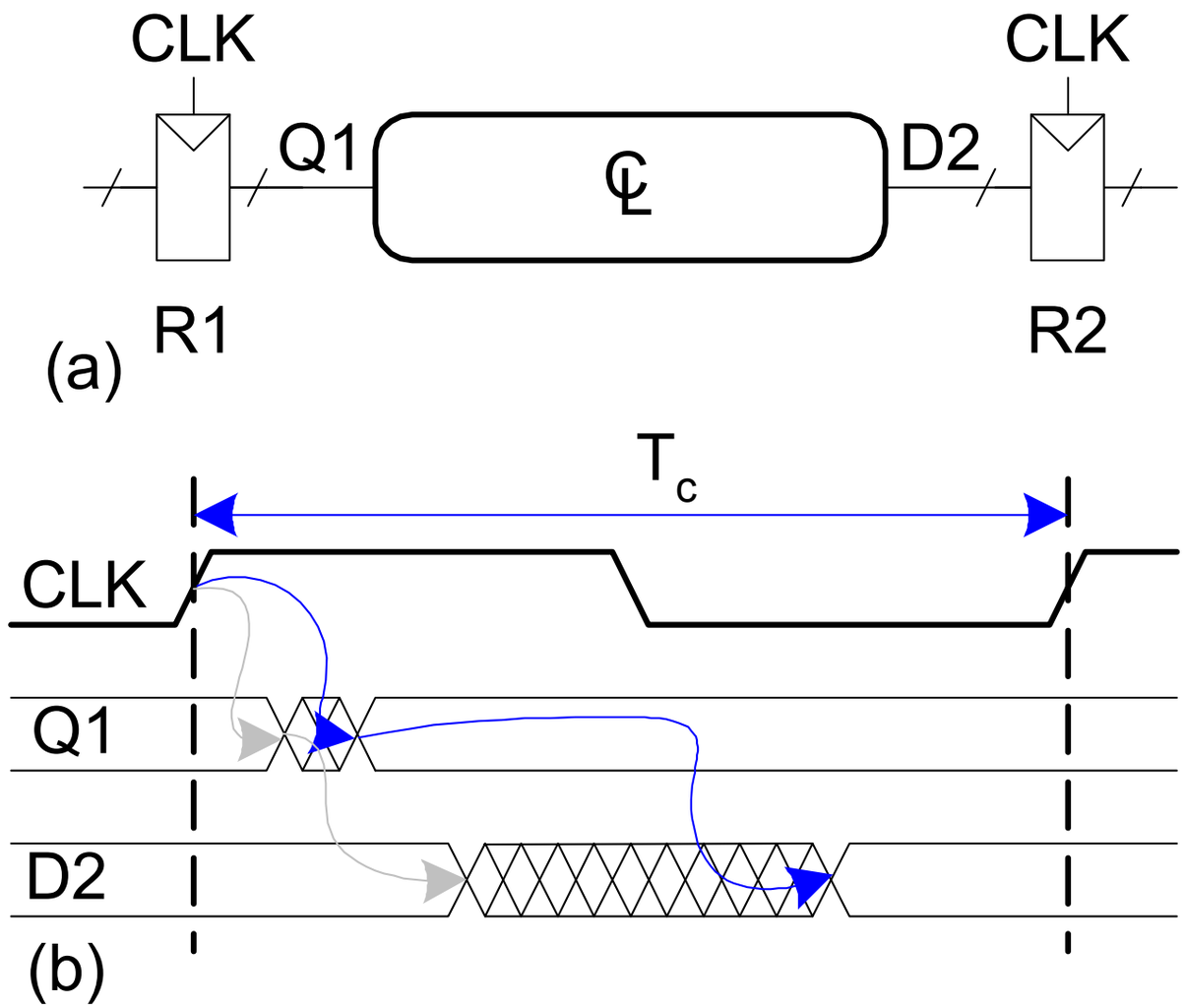


Dynamic Discipline

- Synchronous sequential circuit inputs must be stable during aperture (setup and hold) time around clock edge
- **Specifically, inputs must be stable**
  - **at least t_{setup} before the clock edge**
  - **at least until t_{hold} after the clock edge**

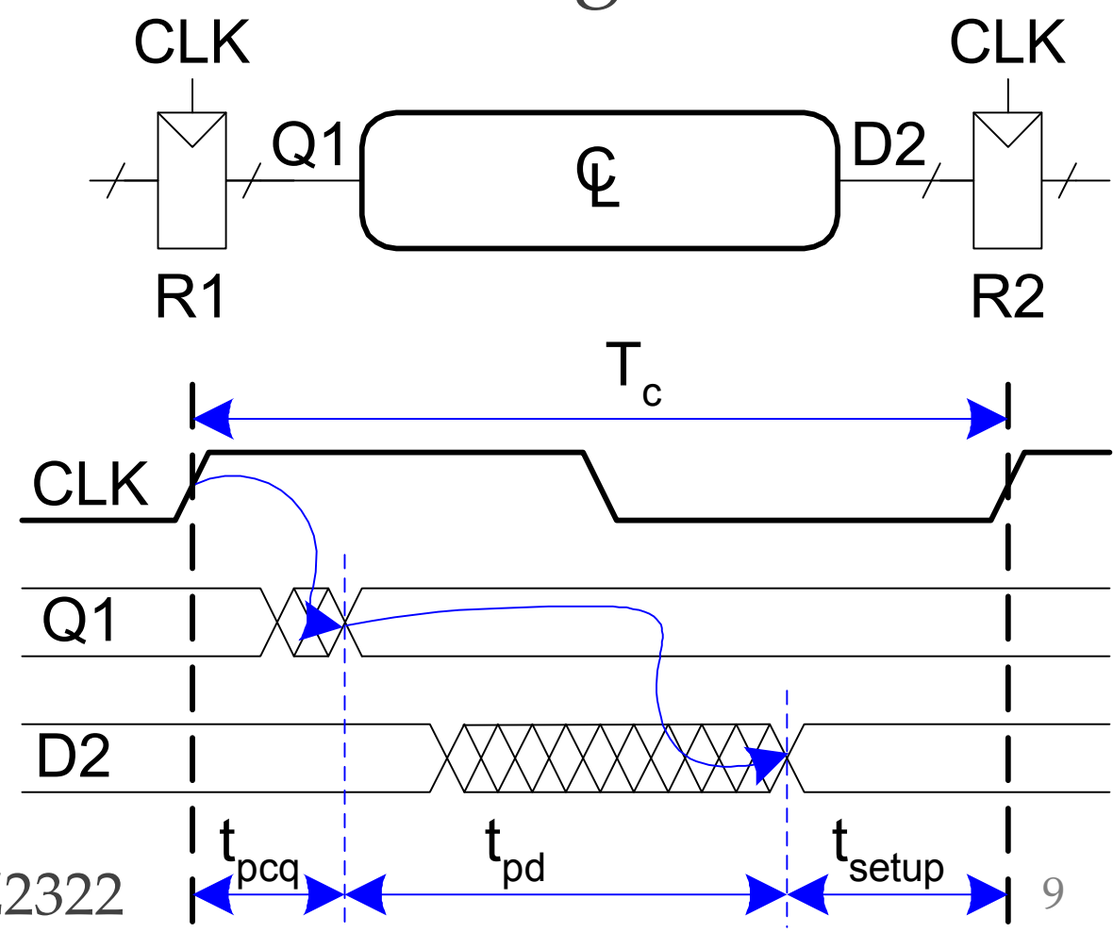
Dynamic Discipline

- The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements



Setup Time Constraint

- Depends on the **maximum** delay from register R1 through combinational logic to R2
- The input to register R2 must be stable at least t_{setup} before clock edge



$$T_c \geq$$

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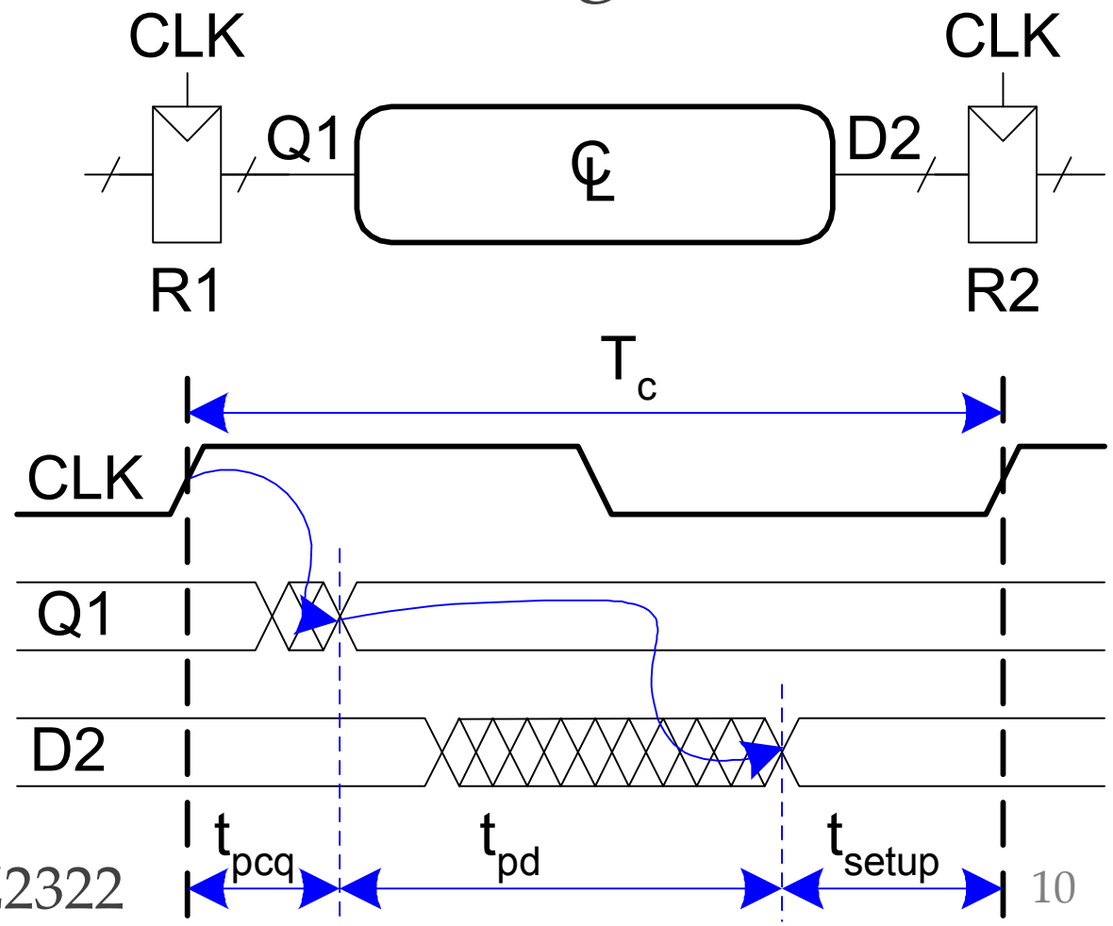

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$$t_{pd} \leq \text{???}$$

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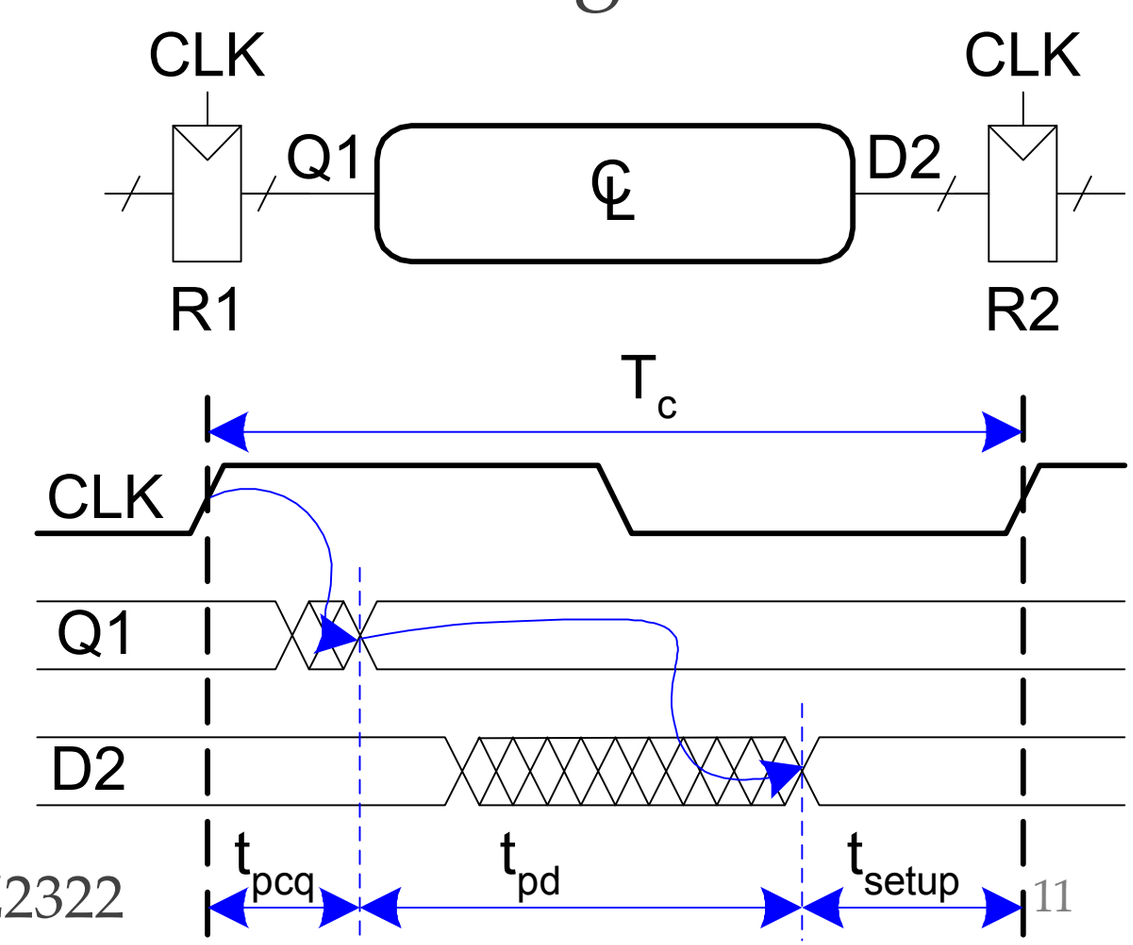
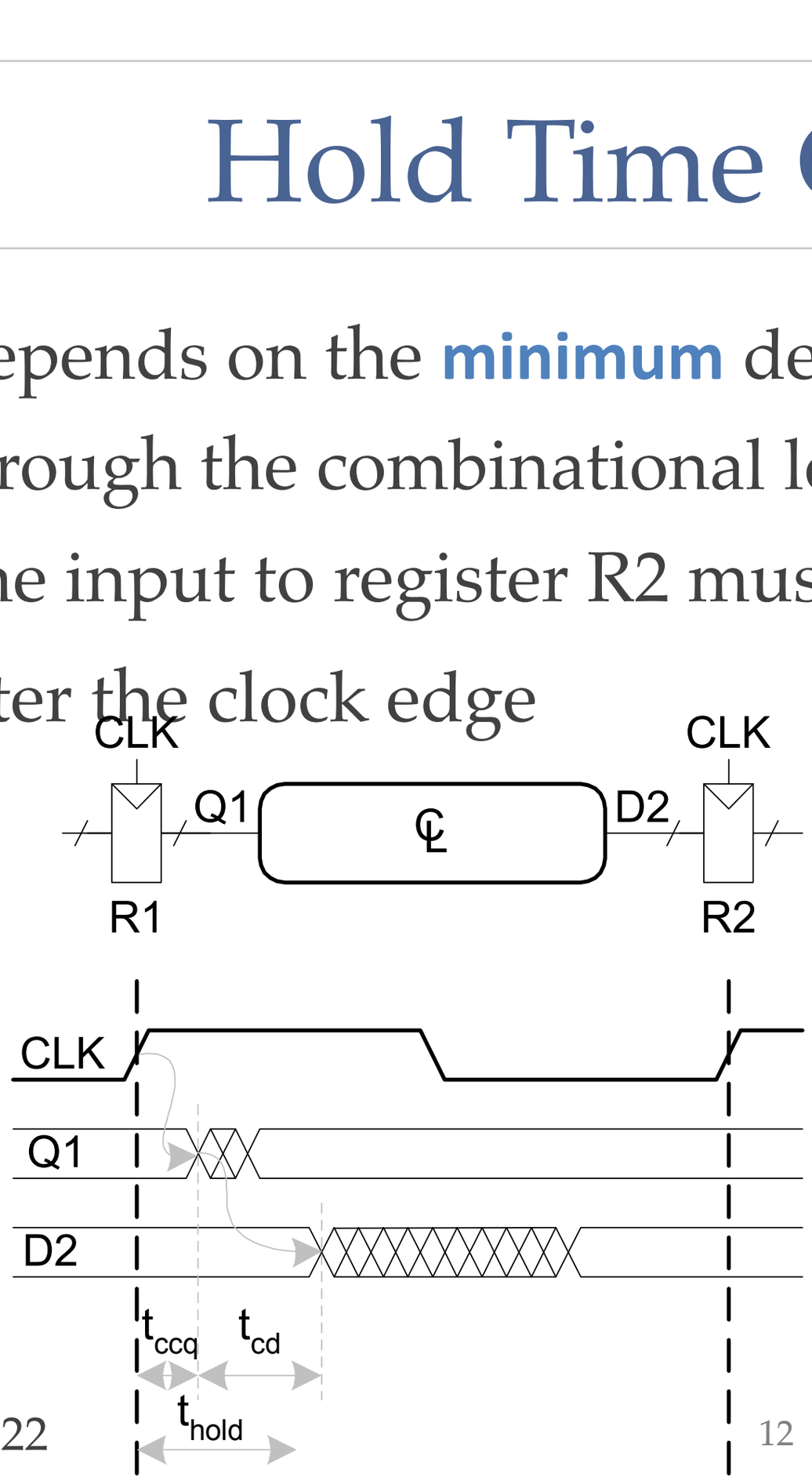


$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$

Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2
- The input to register R2 must be stable for at least t_{hold} after the clock edge



$t_{hold} <$

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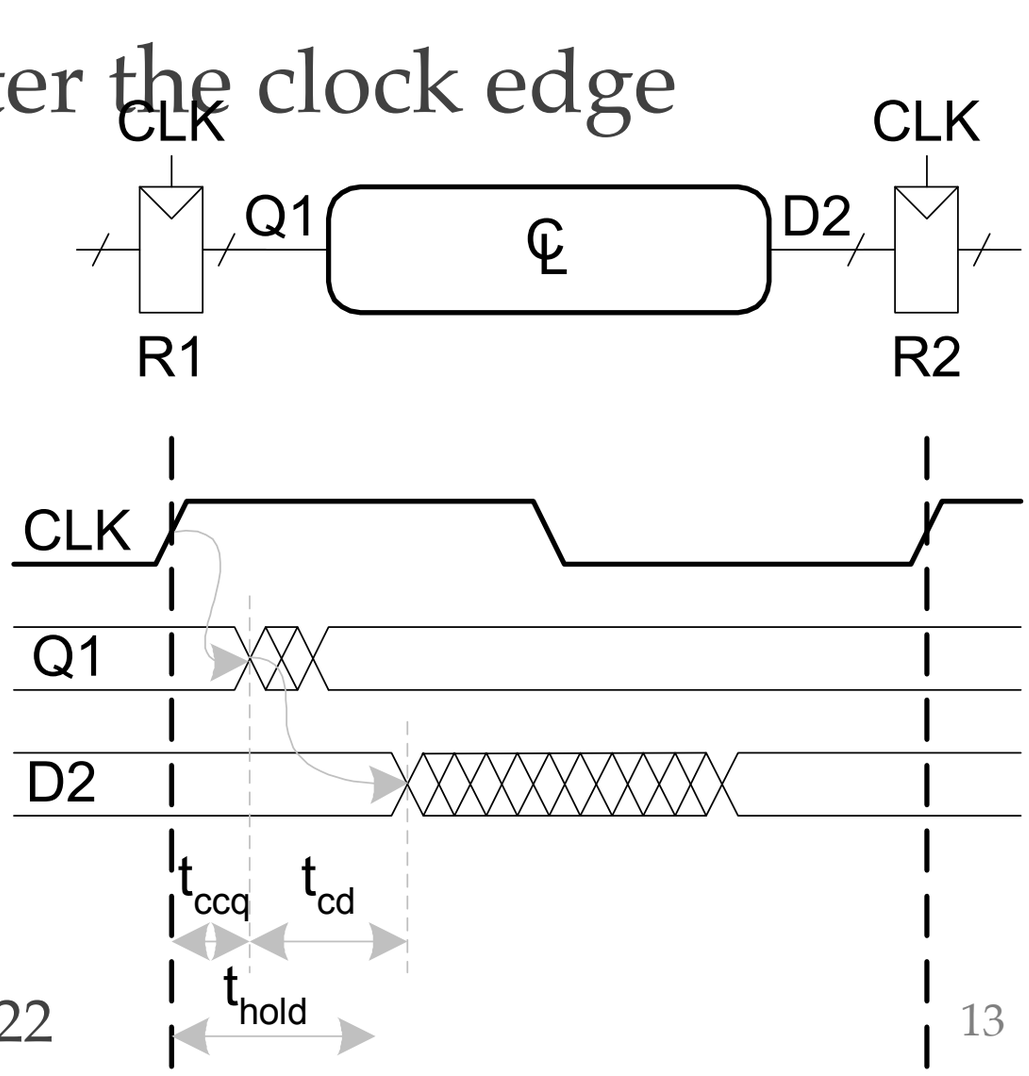
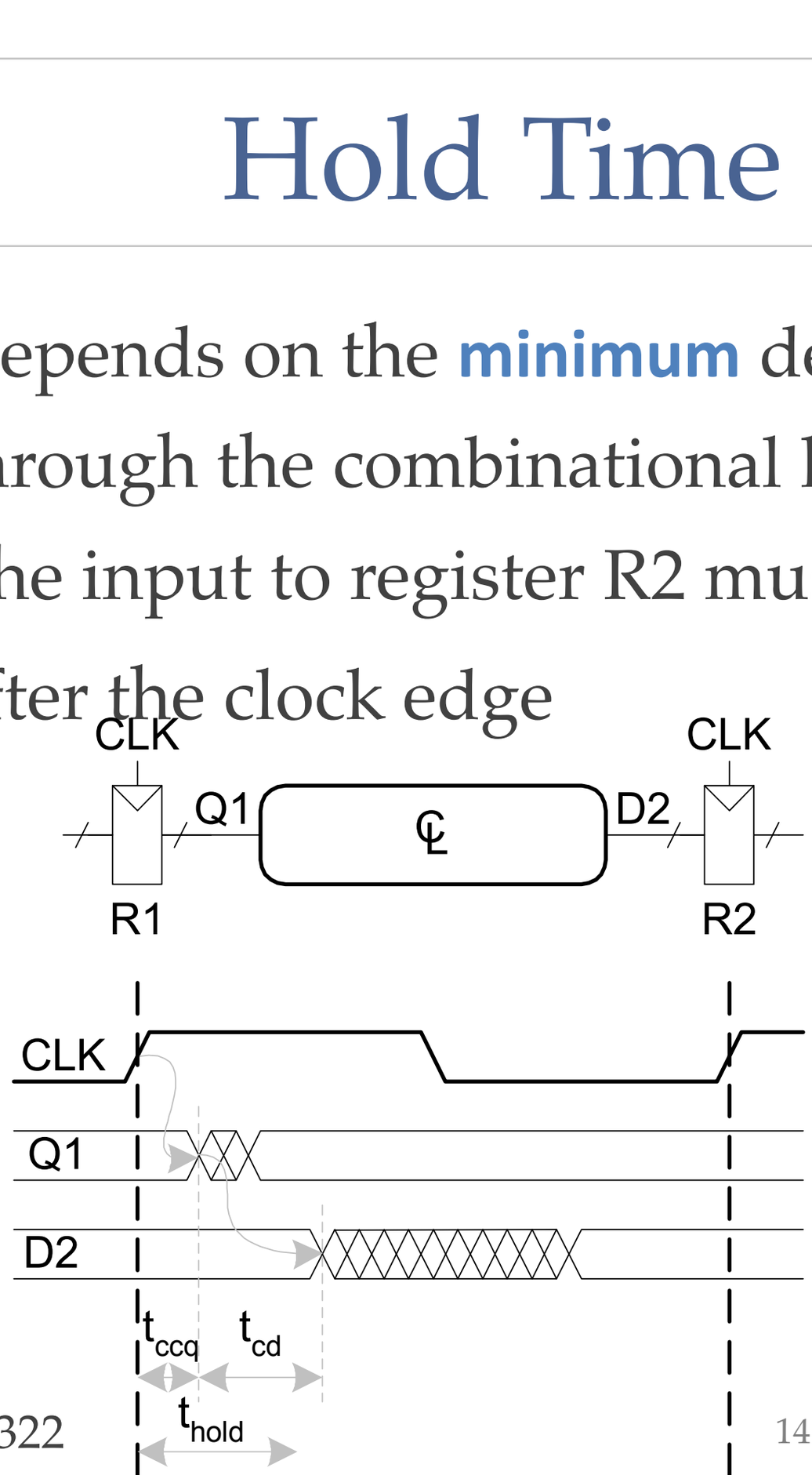


$$t_{\text{hold}} < t_{ccq} + t_{cd}$$

$$t_{cd} >$$

Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2
- The input to register R2 must be stable for at least t_{hold} after the clock edge



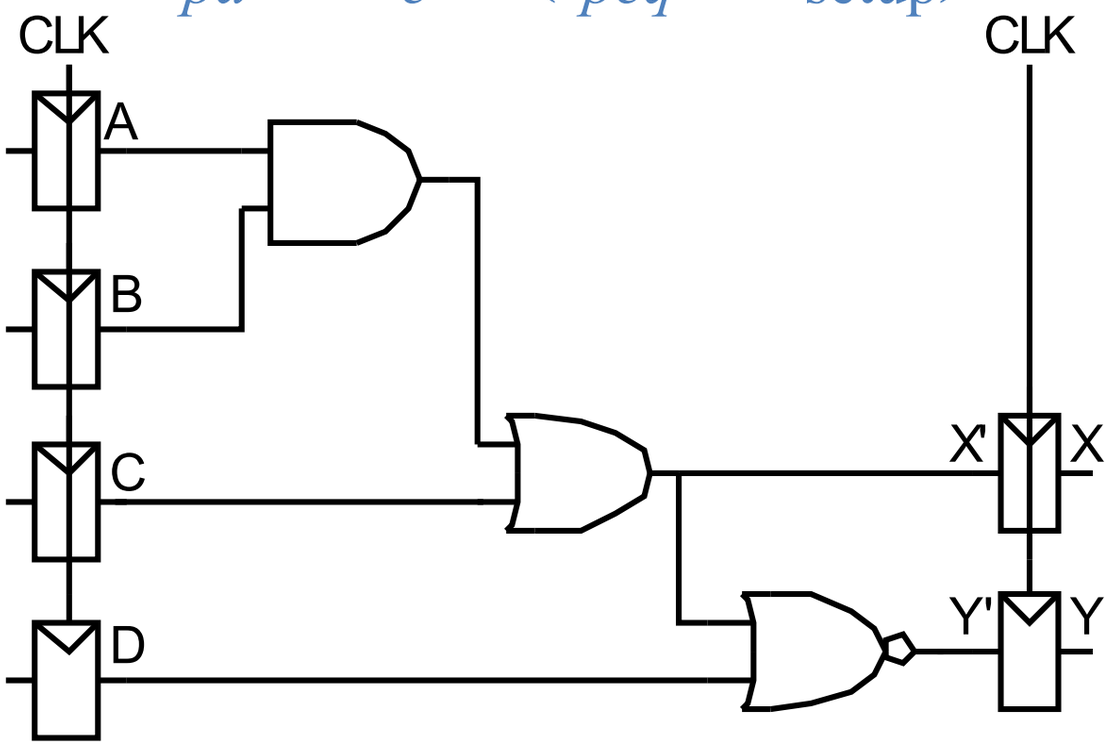
$$t_{hold} < t_{ccq} + t_{cd}$$

$$t_{cd} > t_{hold} - t_{ccq}$$

Timing Analysis

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$



t_{pd} =

t_{cd} =

Setup time constraint:

$T_c \geq$

$f_c =$

Timing Characteristics

t_{ccq} = 30 ps

t_{pcq} = 50 ps

t_{setup} = 60 ps

t_{hold} = 70 ps

per gate

t_{pd} = 35 ps

t_{cd} = 25 ps

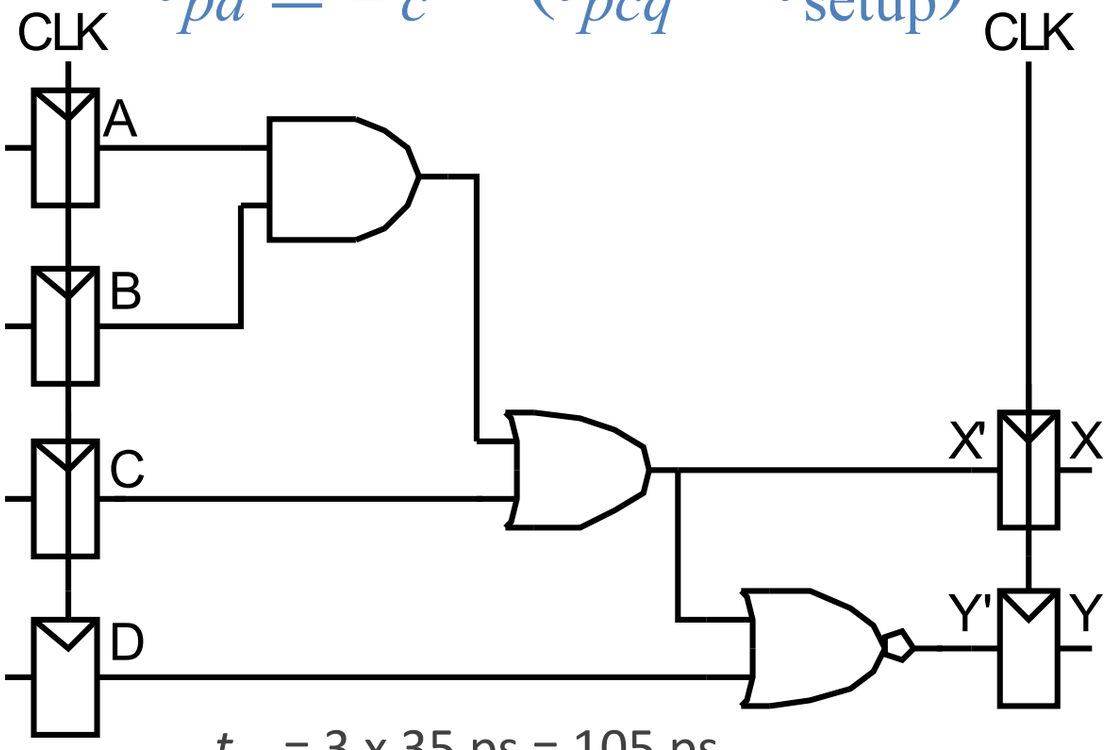
Hold time constraint:

$t_{\text{ccq}} + t_{cd} > t_{\text{hold}}$?

Timing Analysis

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$



t_{pd} = 3 x 35 ps = 105 ps

t_{cd} = 25 ps

Setup time constraint:

$T_c \geq$ (50 + 105 + 60) ps = 215 ps

$f_c = 1/T_c = 4.65$ GHz

Timing Characteristics

t_{ccq} = 30 ps

t_{pcq} = 50 ps

t_{setup} = 60 ps

t_{hold} = 70 ps

per gate

t_{pd} = 35 ps

t_{cd} = 25 ps

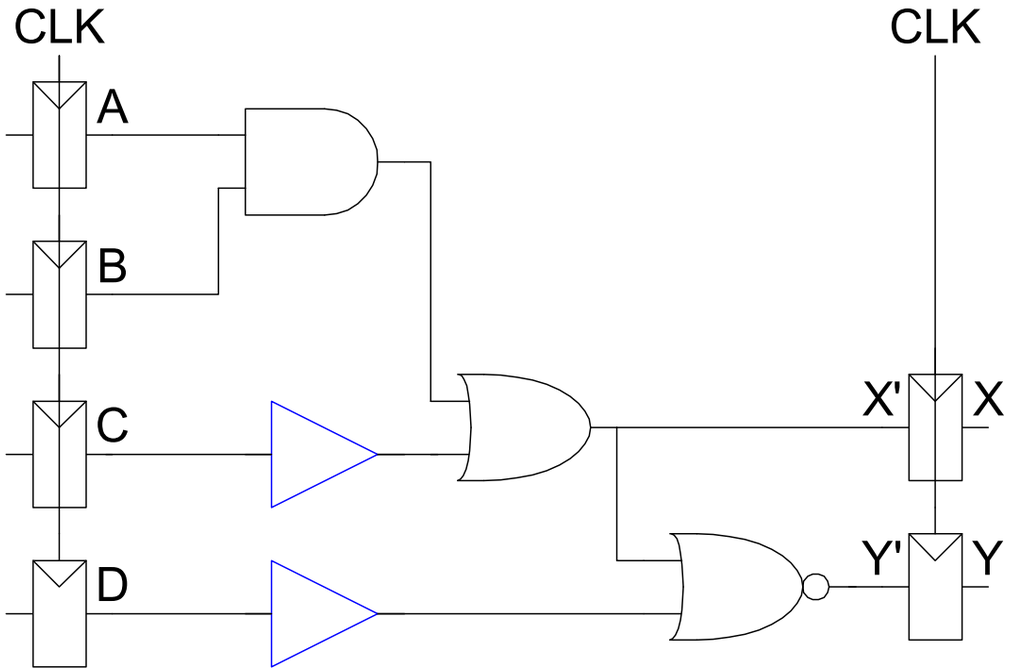
Hold time constraint:

$t_{\text{ccq}} + t_{cd} > t_{\text{hold}}$?

(30 + 25) ps > 70 ps ? **No!**

Timing Analysis

Add buffers to the short paths:



t_{pd} =

t_{cd} =

Setup time constraint:

$T_c \geq$

$f_c =$

Timing Characteristics

t_{ccq} = 30 ps

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Timing Analysis

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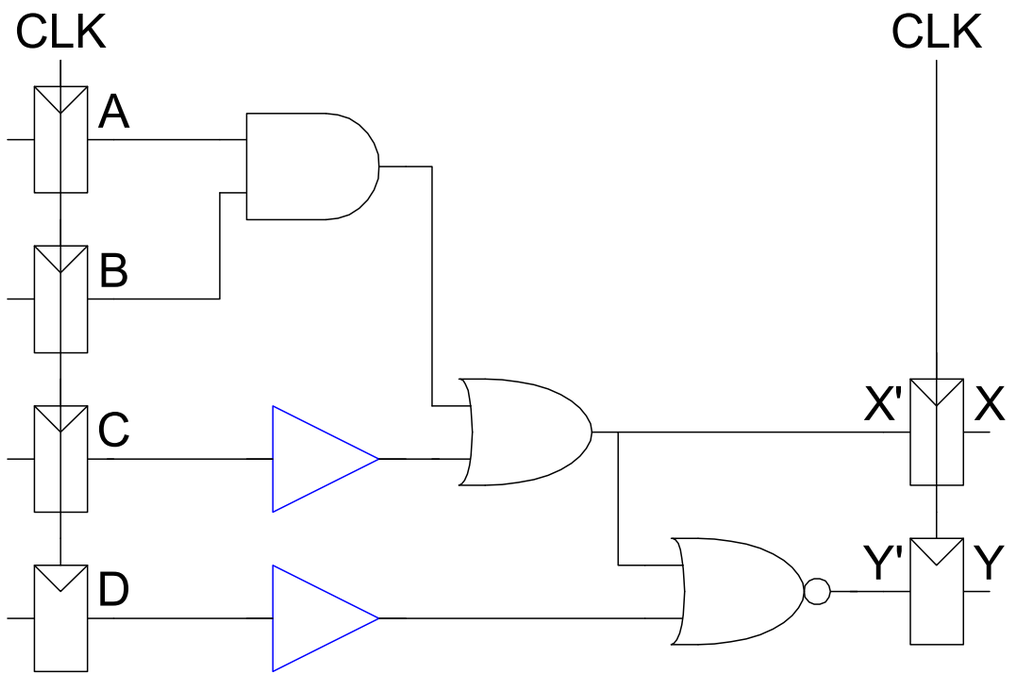

t_{pd} = 3 x 35 ps = 105 ps

t_{cd} = 2 x 25 ps = 50 ps

Setup time constraint:

$T_c \geq (50 + 105 + 60)$ ps = 215 ps

$f_c = 1/T_c = 4.65$ GHz

Timing Characteristics

t_{ccq} = 30 ps

t_{pcq} = 50 ps

t_{setup} = 60 ps

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per gate

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Hold time constraint:

$t_{ccq} + t_{cd} > t_{hold}$?

$(30 + 50)$ ps > 70 ps ? **Yes!**