

EECE 2322: Fundamentals of Digital Design and Computer Organization

Lecture 1_1: Overview

Xiaolin Xu
Department of ECE
Northeastern University

Welcome to the New Semester!

“New” Course!

EECE2322 of Spring 2022

- ❖ Instructor: Xiaolin Xu (x.xu@northeastern.edu)
- ❖ Lecture Time: Mon. / Wed. / Thur. 1:35PM-2:40PM
 - ❖ Zoom will be used for on-line students (if needed by anyone)
 - ❖ Video will be captured and shared (automatically?)
 - ❖ Check Canvas for login and course materials
- ❖ West Village G 106

EECE2322 of Spring 2022

- ❖ Office Hours: Monday / Thursday 3:00PM-4:30PM
 - ❖ Back-to-back with lecture, good for answering real-time confusions
 - ❖ Zoom, weekly link created on Canvas
 - ❖ If you cannot make it? OK!
 - ❖ Or by appointment, Email
- ❖ Teaching Assistants: Bhanu Sai Simha Vanam
 - ❖ Email: vanam.b@northeastern.edu

EECE2323

- ❖ We do have different instructors / sections for these two courses (EECE 2322 and 2323)
 - ❖ Different teaching style, grading policy(?), and syllabus
- ❖ The same materials are covered in the lab course
- ❖ The course and lab are tightly integrated!
- ❖ So, you are strongly encouraged to attend the lab course, though not necessarily my section(s)

EECE2323

- ❖ We do have different instructors / sections for these two courses (EECE 2322 and 2323)
 - ❖ Different teaching style, grading policy(?), and syllabus
- ❖ The same materials are covered in the lab course
- ❖ The course and lab are tightly integrated!
- ❖ So, you are strongly encouraged to attend the lab course, though not necessarily my section(s)

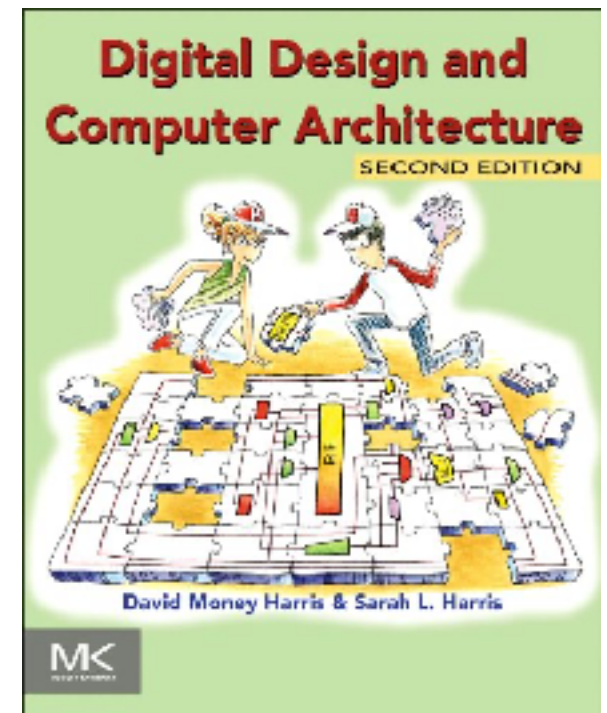
The course lectures are accompanied by lab sessions that guide the student through an incremental design of a fully functional single-cycle processor data path. All design steps are synthesized into the FPGA of a TUL PYNQ-Z2 board. We will only be using the FPGA fabric for this class, and not the ARM processor on-board.

EECE2323

- ❖ Lab 0: Tutorial: Design an XOR logic gate
- ❖ Lab 1: Combinational logic: adder
- ❖ Lab 2: Combinational logic: partial ALU
- ❖ Lab 3: Complete ALU with shift and branch instructions
- ❖ Lab 4: Register file plus ALU
- ❖ Lab 5: Data memory, load and store
- ❖ Lab 6: Machine code for instructions
- ❖ Lab 7: Instruction memory (IM). Straight line code
- ❖ Lab 8: IM plus branching
- ❖ **Result: A working processor!**

Textbook and Tool

- ❖ Harris and Harris (see the cover page), Digital Design and Computer Architecture, Second Edition, Morgan Kaufmann. 2013. **NOT the ARM version!**
- ❖ Software tools for ECE 2322 and ECE 2323
 - ❖ Available from the COE VLAB
 - ❖ Must have a COE account to access the VLAB
 - ❖ Even if you are not in the College of Engineering
 - ❖ You will use the Xilinx Vivado tools for this class and the lab
 - ❖ We are using Vivado version 2020.1
 - ❖ Watch Canvas for handout on using the tools



Syllabus Review

- ❖ Your final grade is calculated as a numeric grade between 0 and 100 based on the percentages below:

Weights

- Homework (~ 8-10 hwks with lowest dropped) 25%
- Midterm 1 20% - on paper with cheat sheet
- Midterm 2 20% - on paper with cheat sheet
- Final exam 35% - on paper with cheat sheet

Your numerical semester grade is converted to a letter grade based on the following scale (your numerical grade is rounded up to the nearest percent):

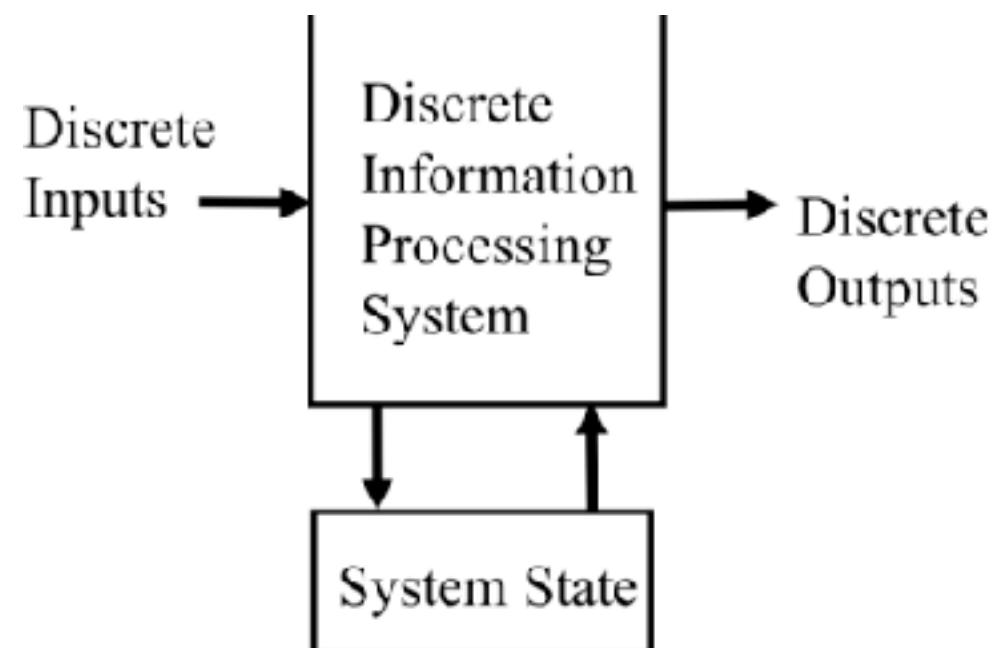
93%-100% = A 90%-92% = A- 87%-89% = B+ 83%-86% = B 80%-82% = B- 77%-79% = C+
73%-76% = C 70%-72% = C- 67%-69% = D+ 63%-66% = D 60%-62% = D- range < 59% = F

Exams and Grading

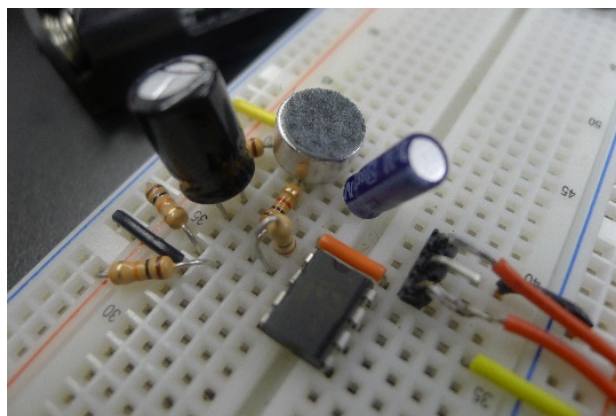
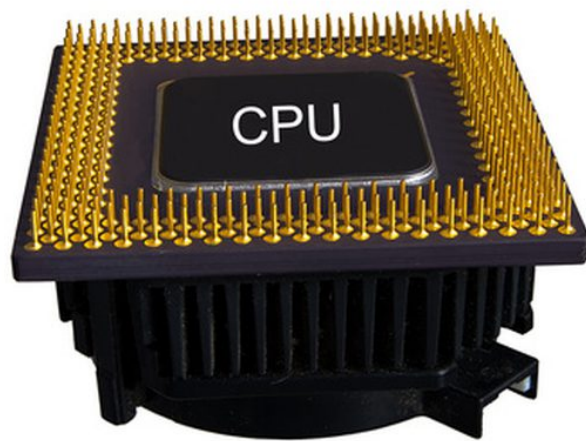
- ❖ HW grading will be by the TA
 - ❖ Submission in PDF format
- ❖ Two midterm exams and a final exam
 - ❖ The exams will be administered in class and will be closed book and closed notes
 - ❖ Exam dates will be announced later. Final exam date: Week of May 2nd, 2022
- ❖ Any Questions?

What is a Digital System

- ❖ Structure: a collection of interconnected digital modules designed to perform a particular service or function
- ❖ Function: takes a set of discrete information inputs and discrete internal information (system state) and generates a set of discrete information outputs.



Digital Systems at a Glance



Application/software
Operating Systems (OS)
Architecture
Micro-architecture
Logic
Digital Circuits
Analog Circuits
Devices
Physics

Programs

Drivers

Instructions

Datapath/controller

Address/memory

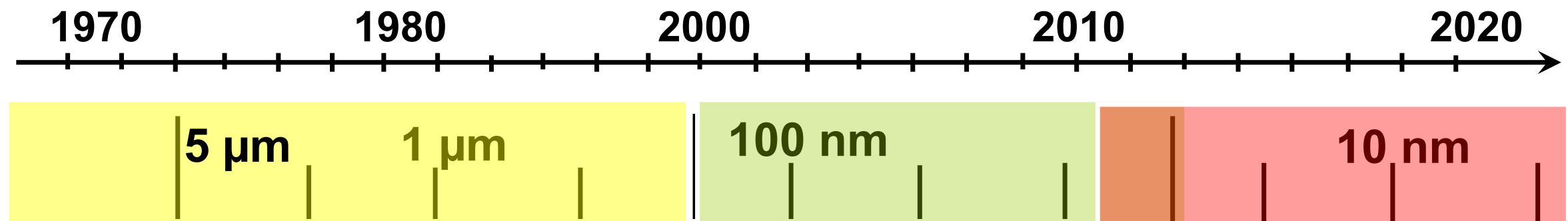
Gates (AND, OR)

Amplifier/filter

Transistor

Electron

Nano-electronics

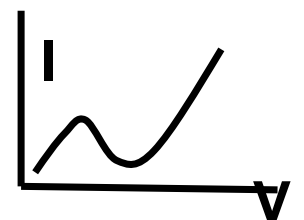
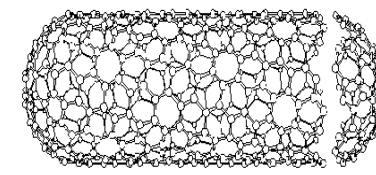


**Silicon Micro
Electronics**

**Silicon Nano
Electronics**

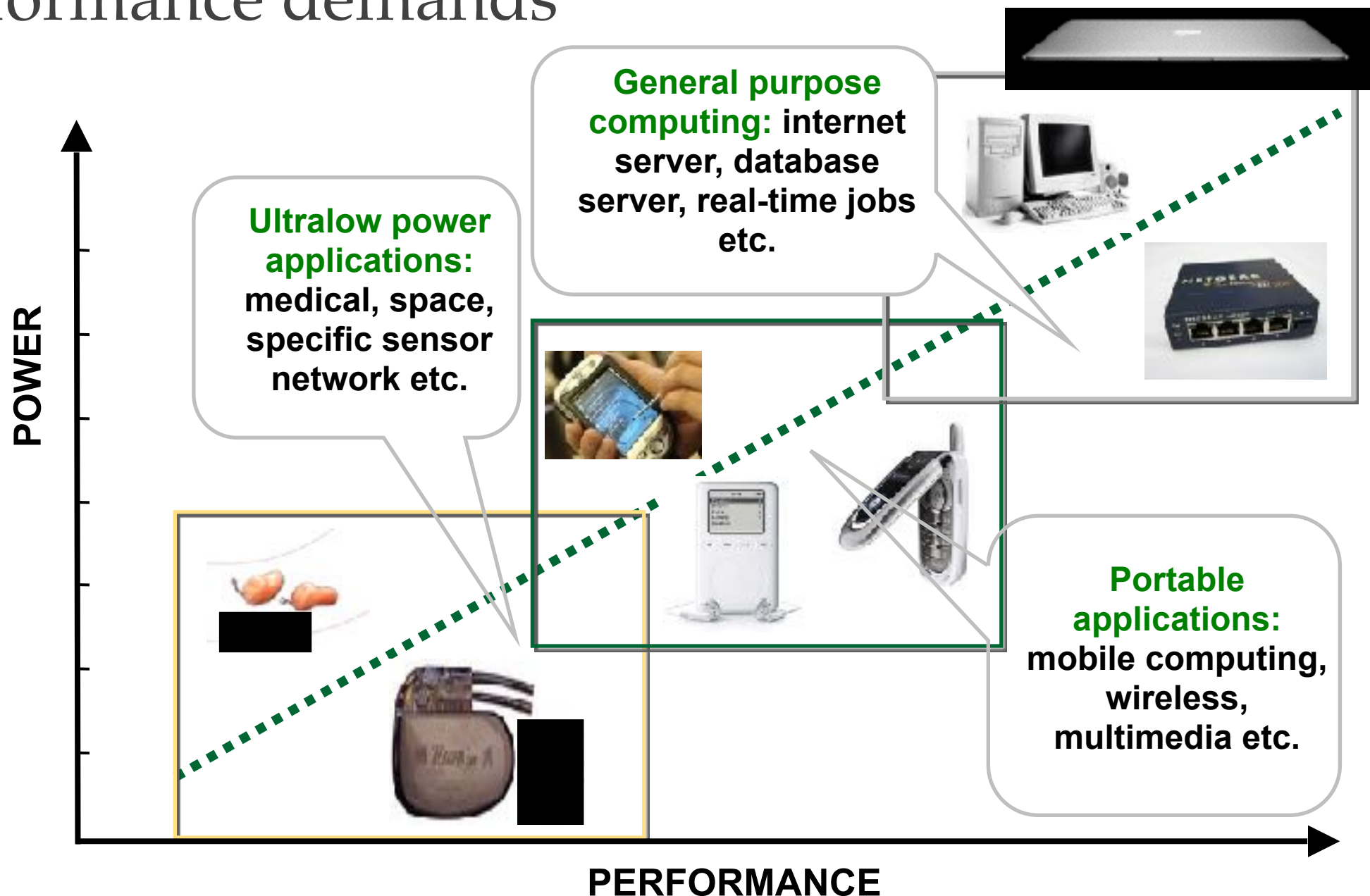
**Non-Silicon
technology**

- ❖ Power will continue to increase
 - ❖ Low-leakage / leakage-tolerance
 - ❖ Dynamic power management
- ❖ Process variation will be a key issue
 - ❖ Design for Manufac. (DFM), Reliability
- ❖ Arch. / design methods for new devices

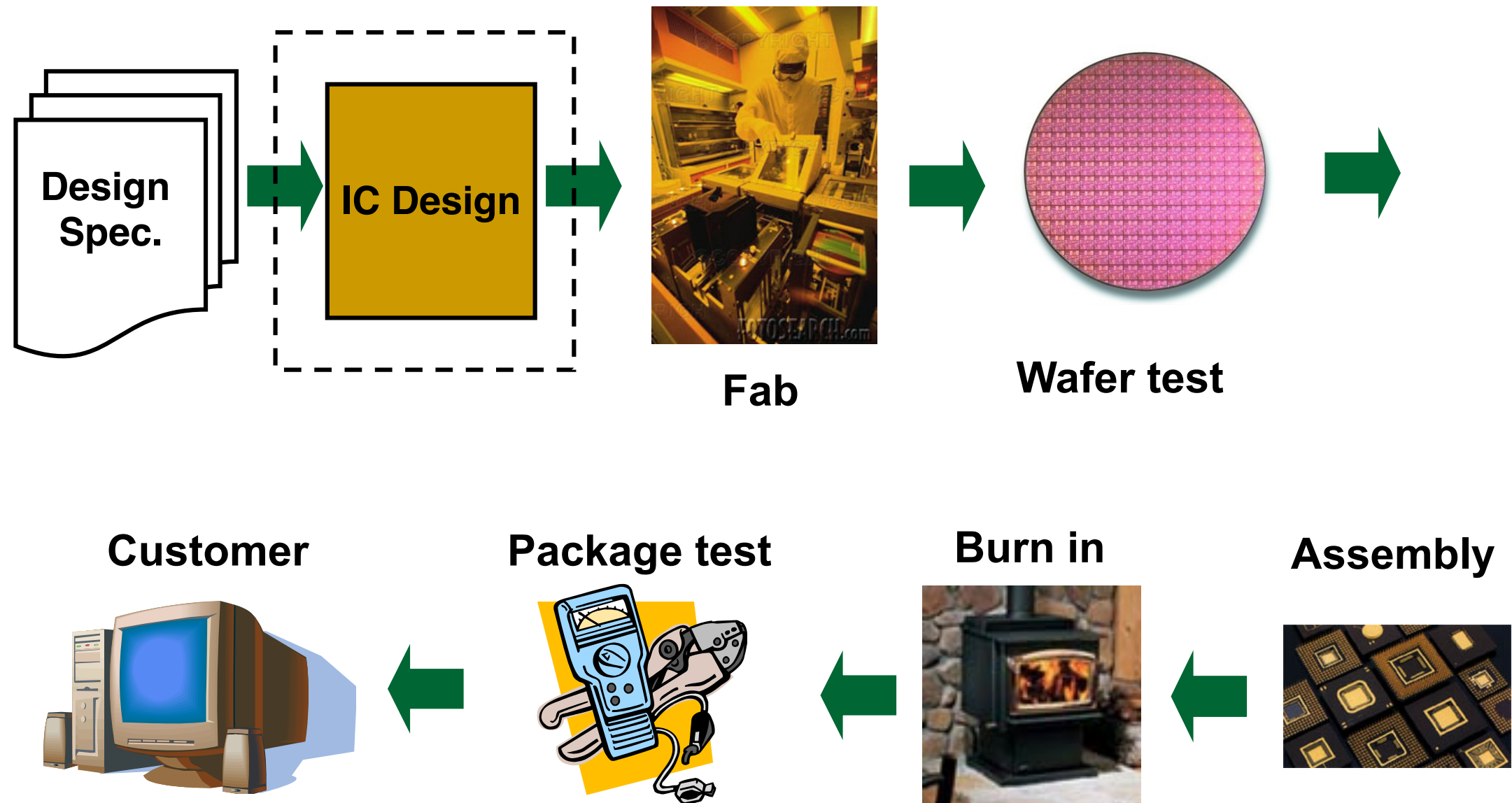


Applications of Digital Systems

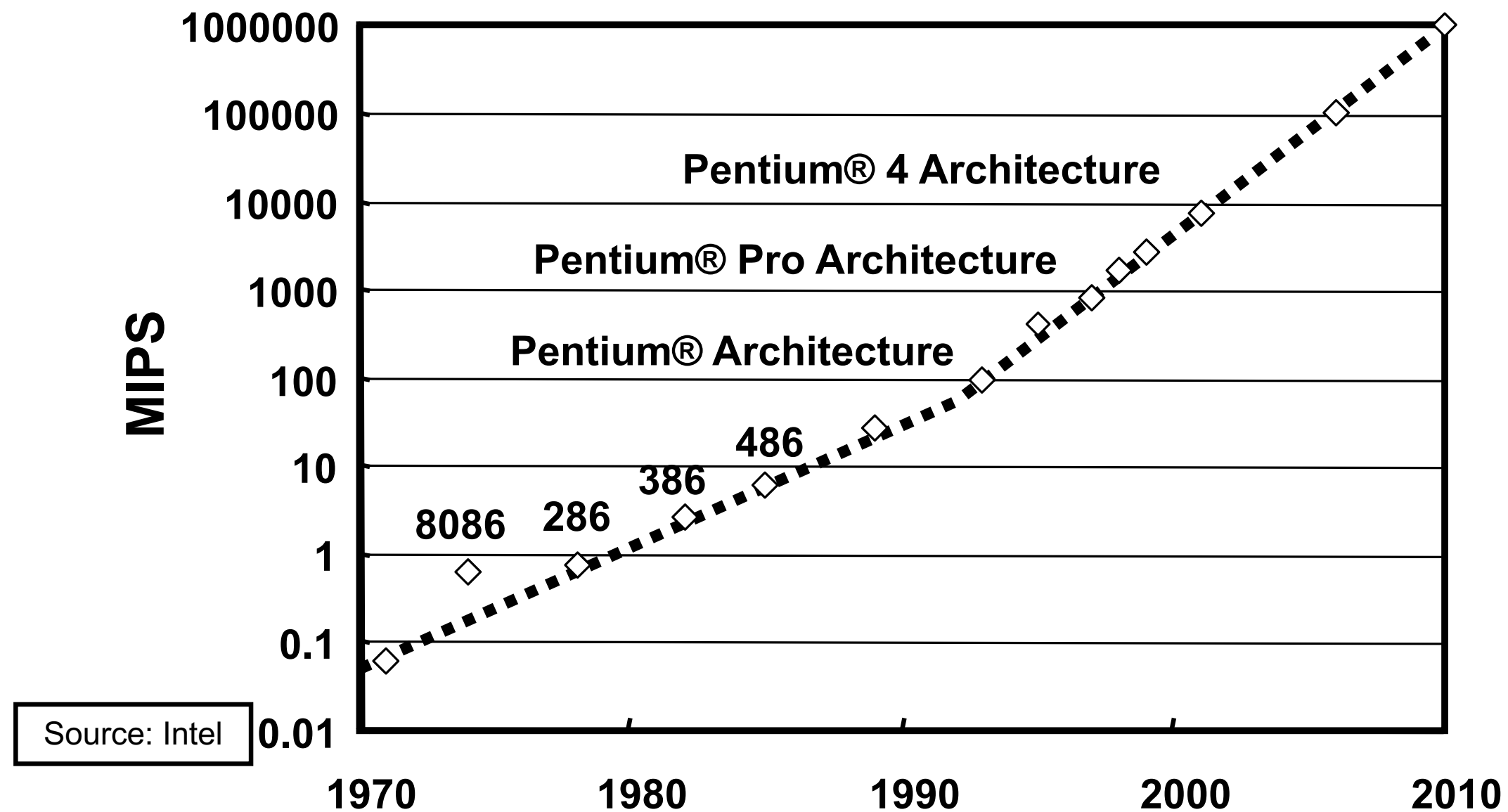
- ❖ Different applications have different power-performance demands



IC Design and Testing Flow

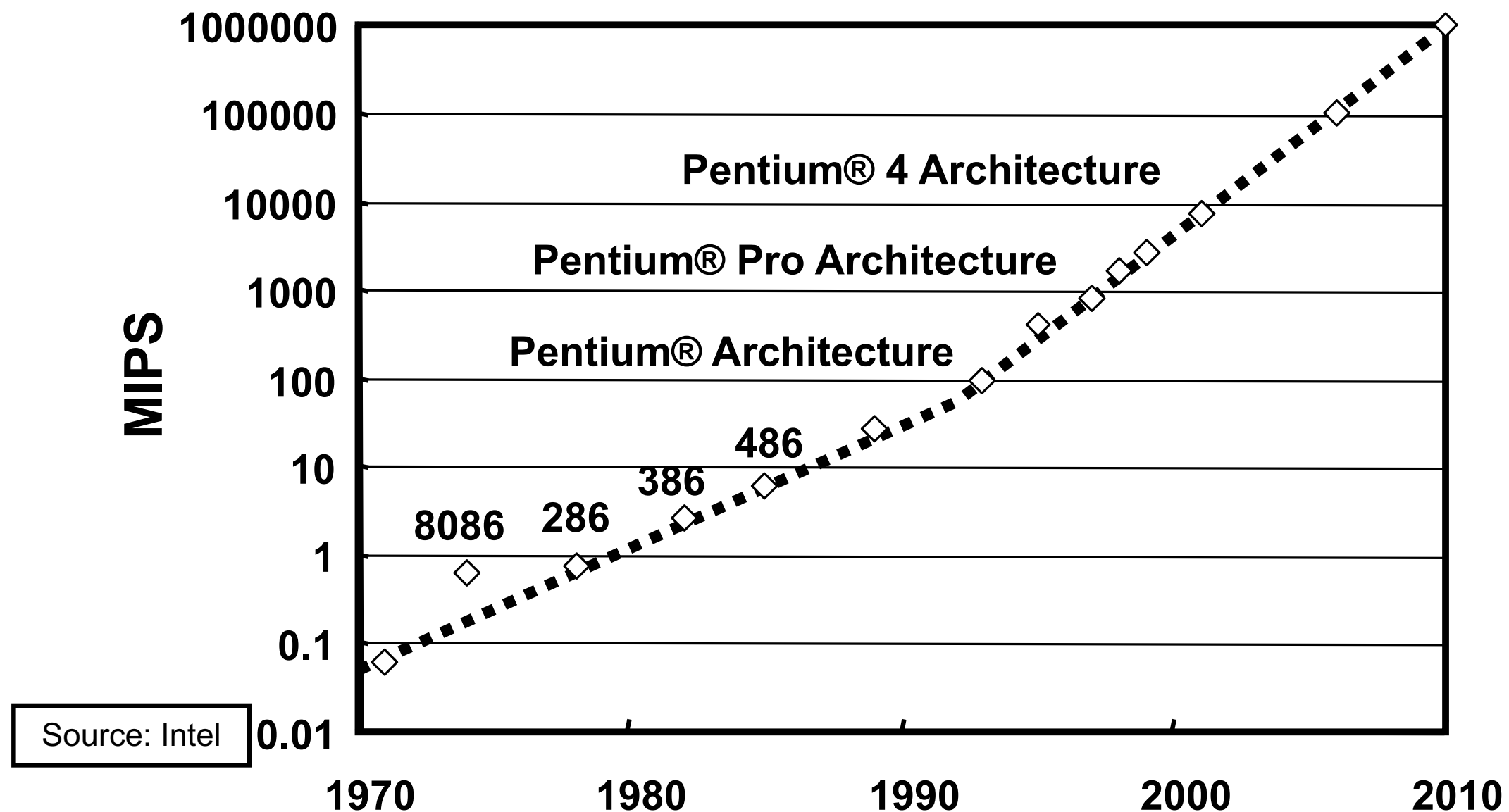


Exponential Growth in Computing Power



Exponential Growth in Computing Power

- ❖ What is the key to the growth in computing power?

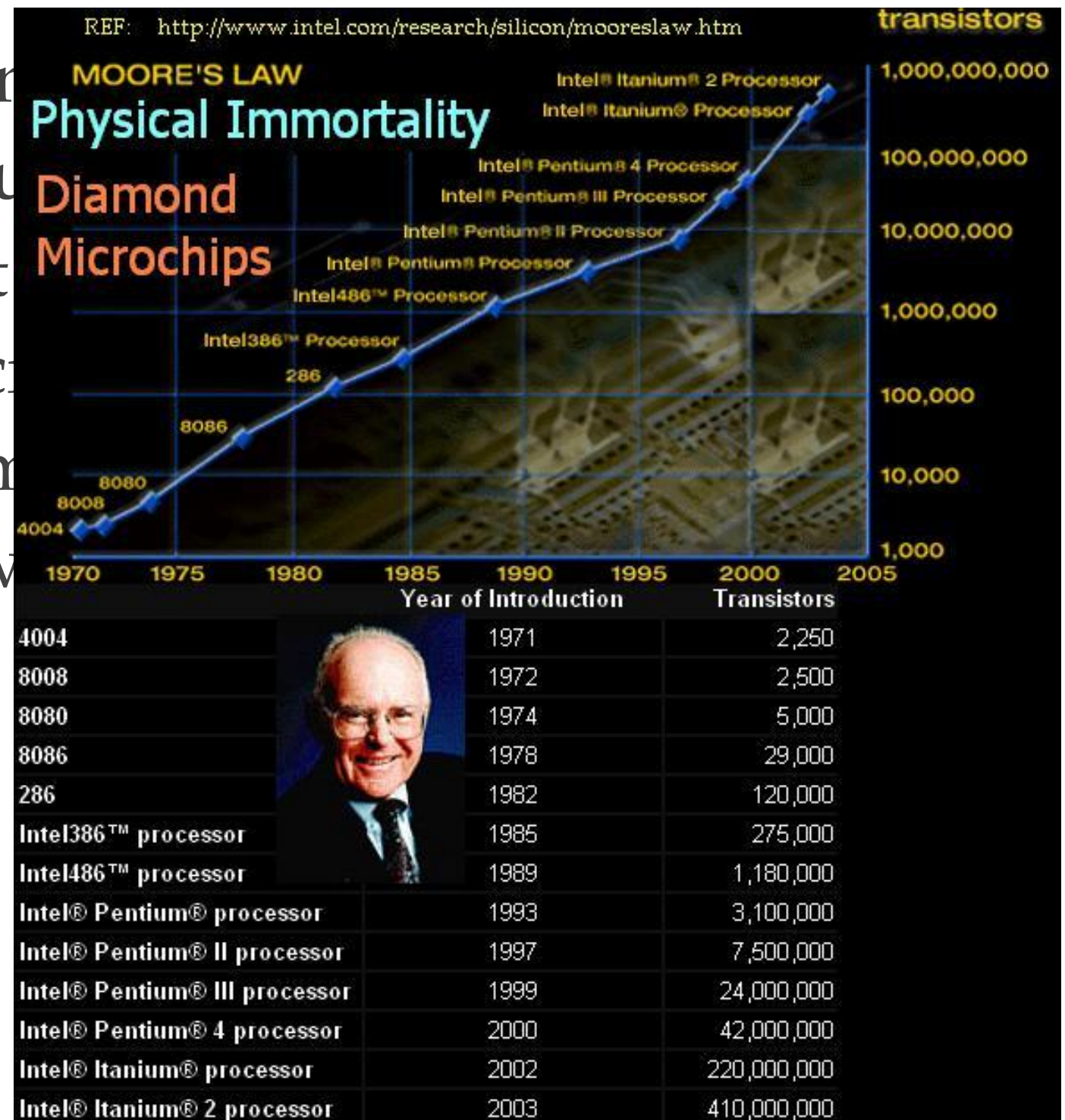


Moore's Law

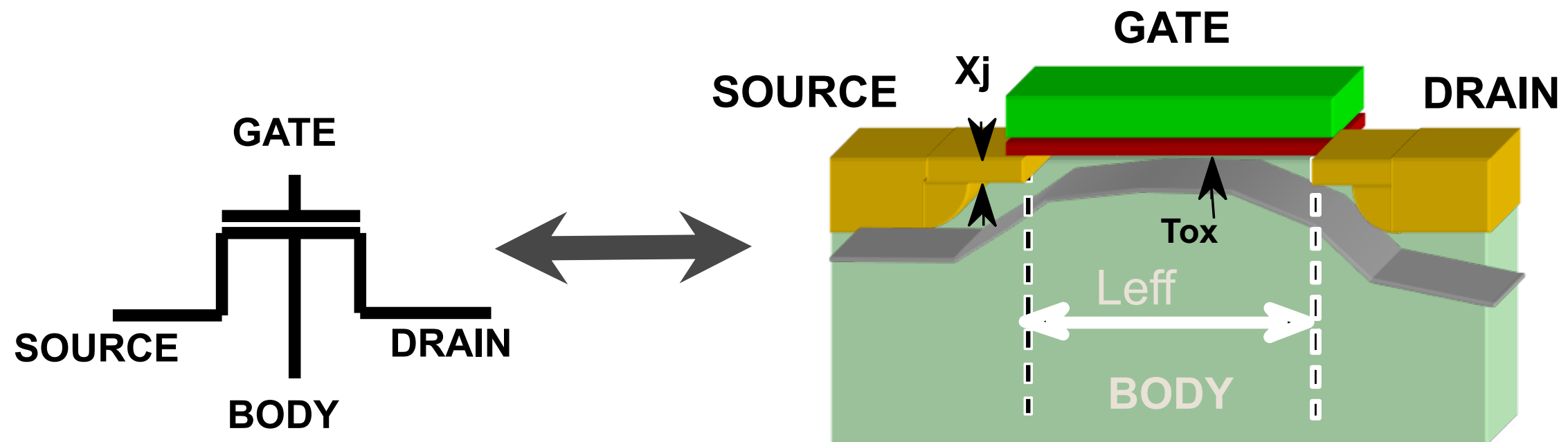
- ❖ “The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. ...”

Moore's Law

- ❖ “The complexity for min increased at a rate of rou Certainly over the short to continue, if not to inc rate of increase is a bit m no reason to believe it w for at least 10 years. ...”



Transistor Technology Scaling



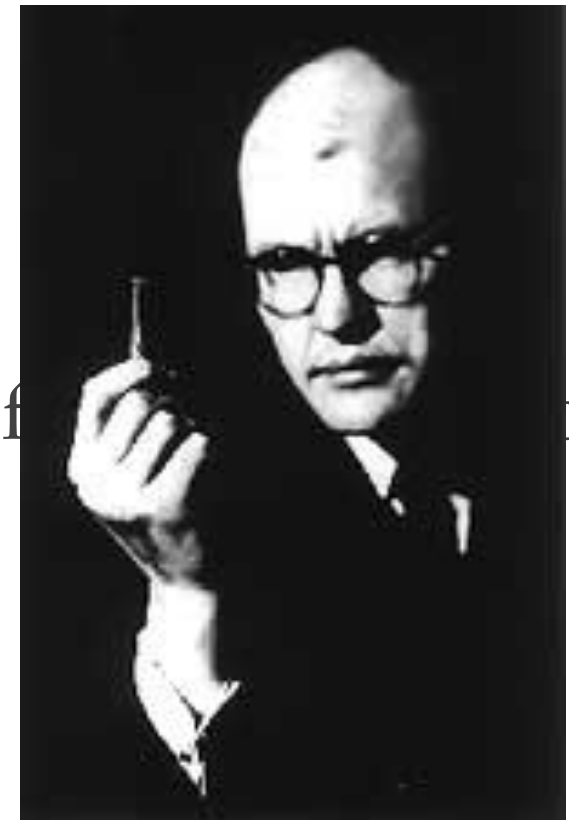
Dimensions scale down by 30%	Doubles transistor density
Oxide thickness scales down	Faster transistor, higher performance
V_{dd} & V_t scaling	Lower active power

VLSI Design

- ❖ What is VLSI Design
 - ❖ Very Large Scale Integrated Circuit
 - ❖ The process of creating an integrated circuit from specifications to fabrication
- ❖ Then, what is an integrated circuit?
 - ❖ A single integrated component that contains all the primary elements of an electrical circuit: transistors, wiring, resistors, capacitors, etc

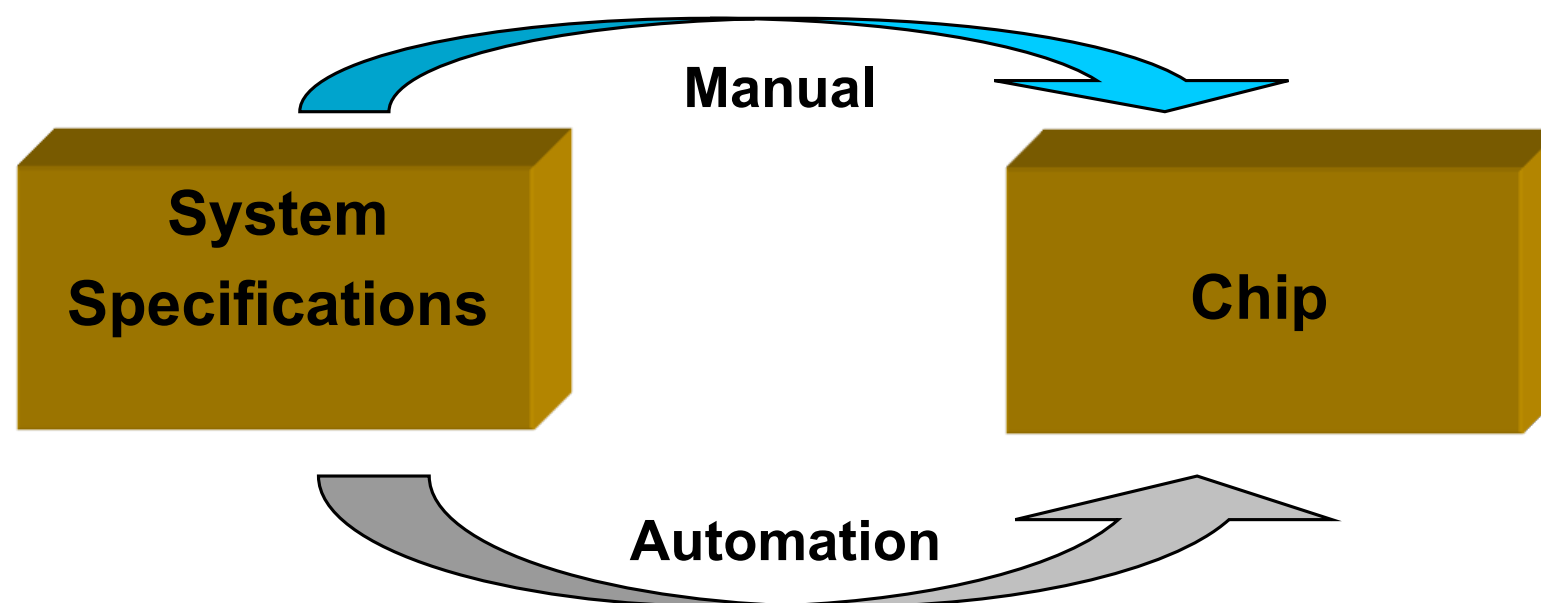
VLSI Design

- ❖ What is VLSI Design
 - ❖ Very Large Scale Integrated Circuit
 - ❖ The process of creating an integrated circuit from design to fabrication
- ❖ Then, what is an integrated circuit?
 - ❖ A single integrated component that contains all the primary elements of an electrical circuit: transistors, wiring, resistors, capacitors, etc

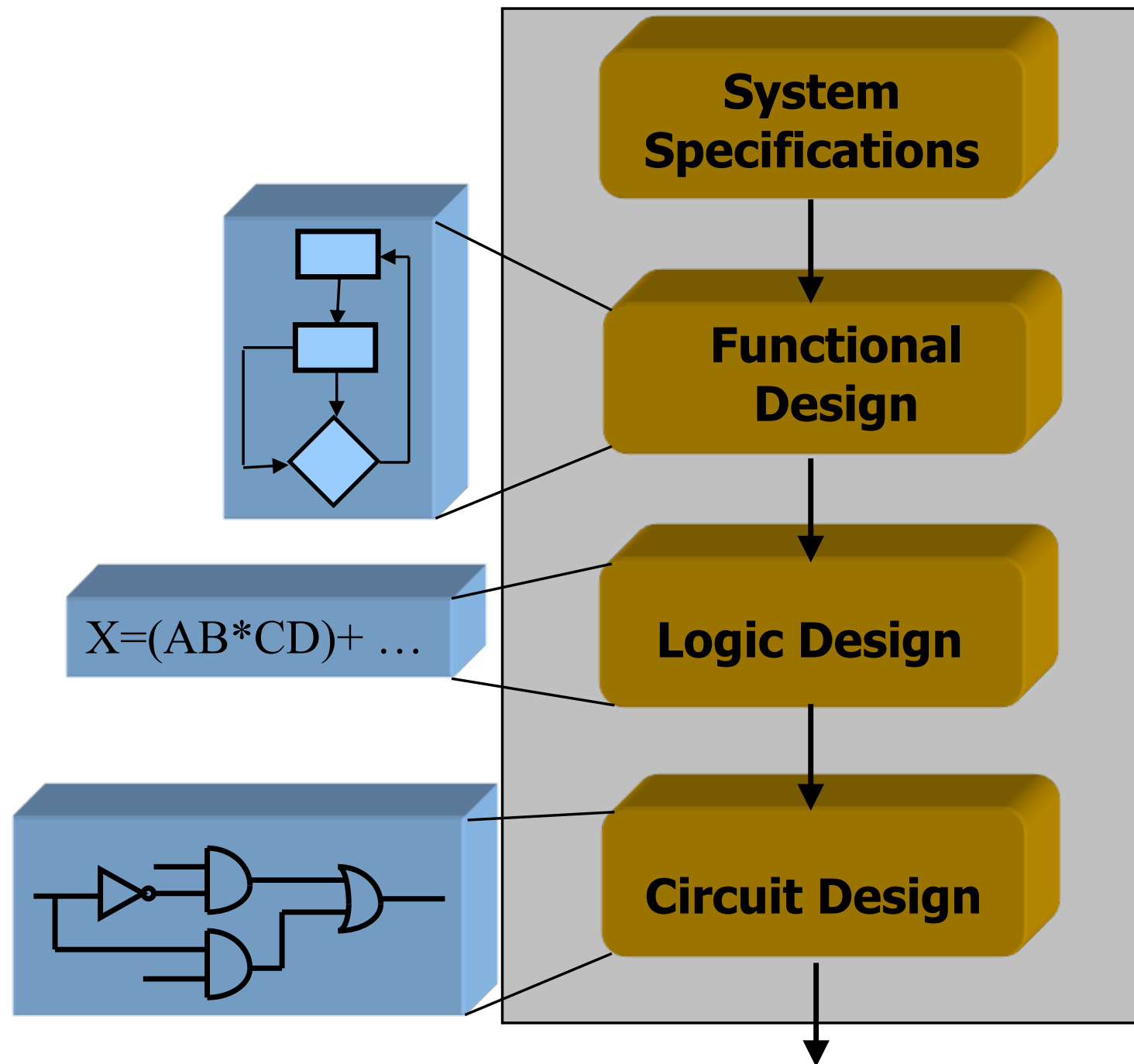


VLSI Design Automation

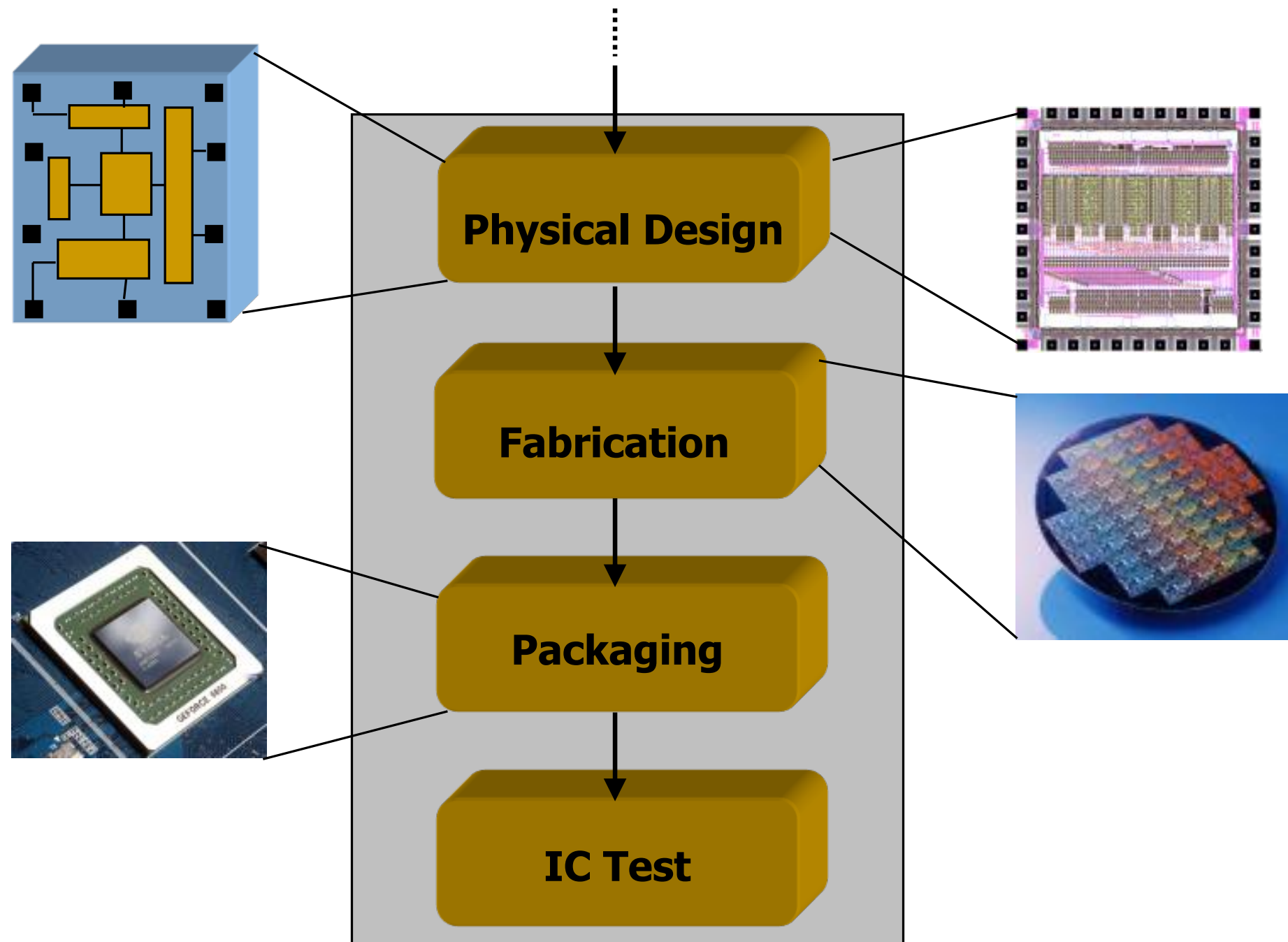
- ❖ Large number of components
- ❖ Optimize requirements for higher performance
 - ❖ Performance relates to speed, power and size.
- ❖ Time to market competition, Cost
 - ❖ Using computer makes it cheaper by reducing time-to-market



VLSI Design Cycle

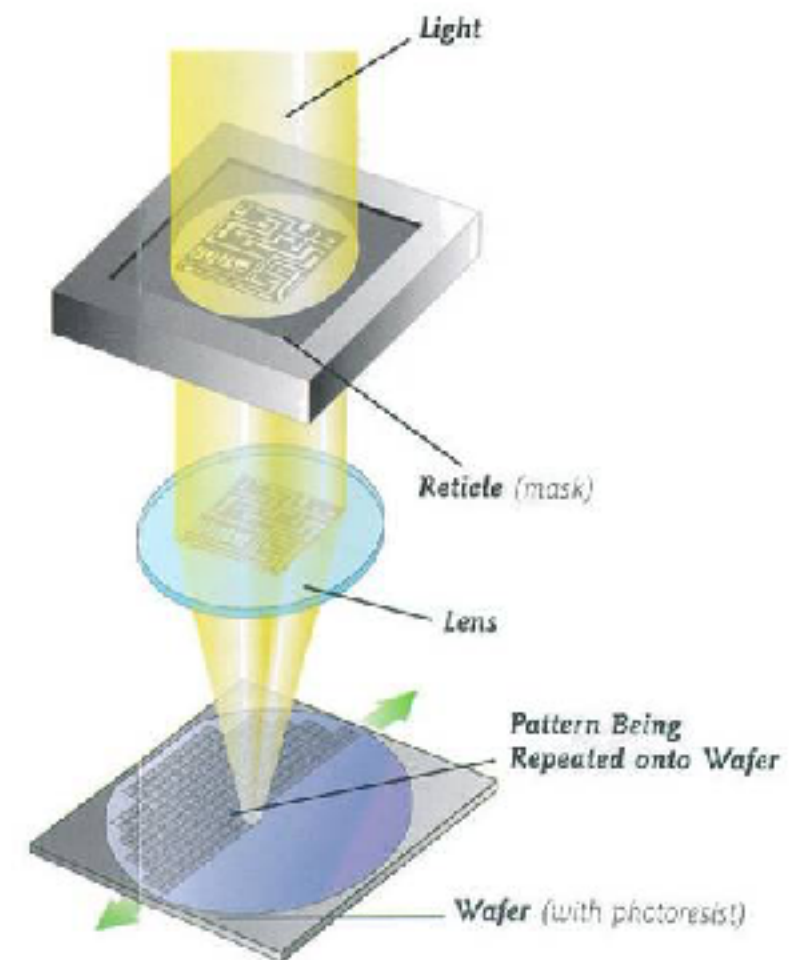
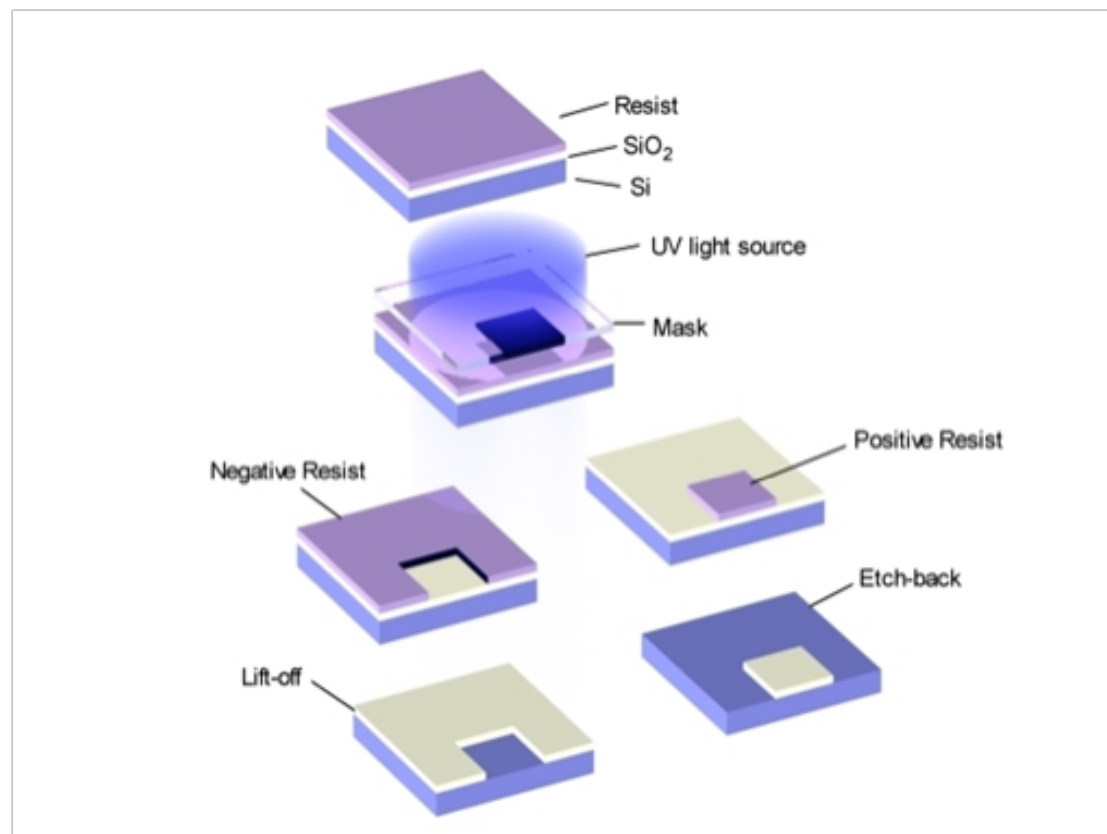


VLSI Design Cycle



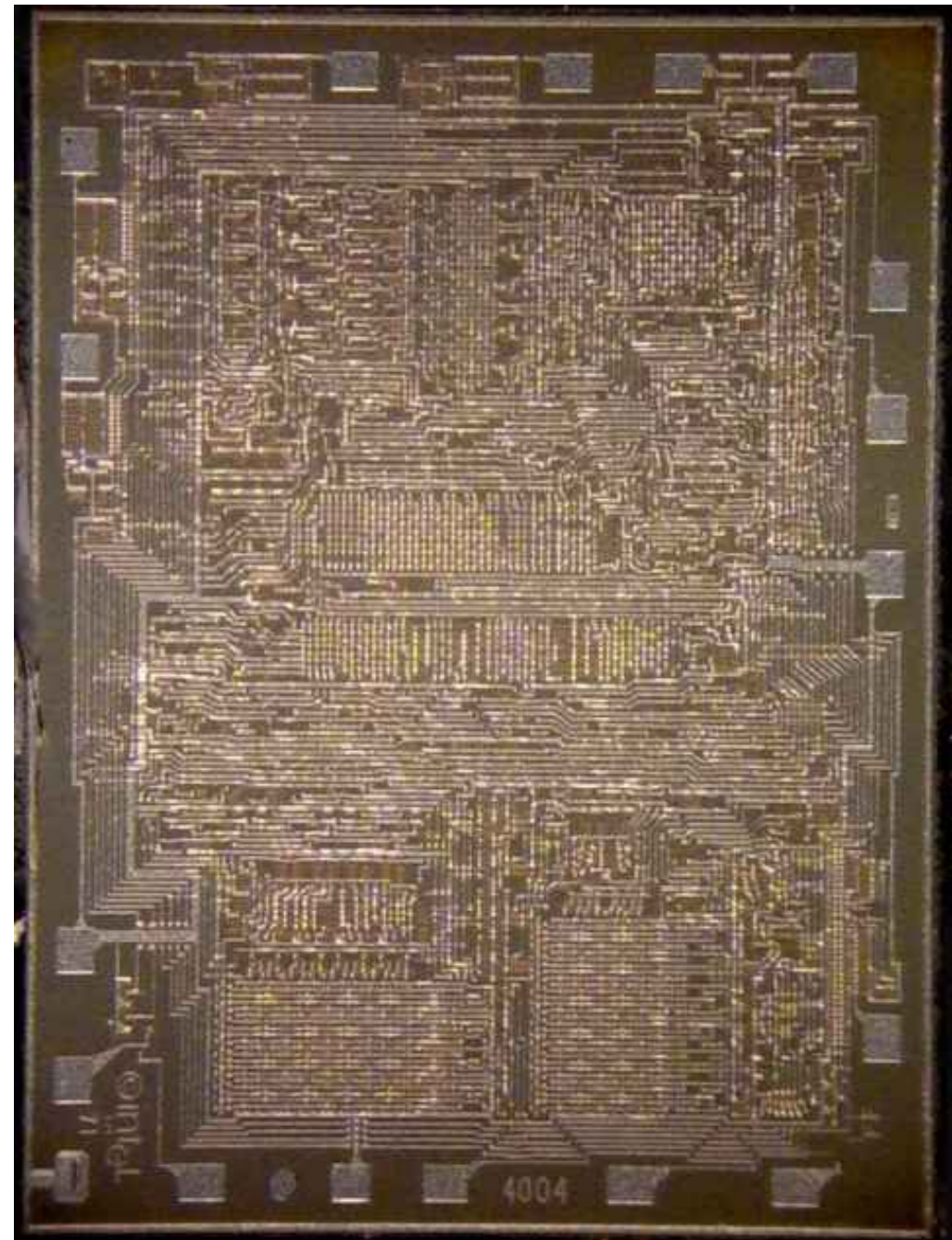
Semiconductor Processing

- ❖ How do we make a transistor?
- ❖ How to control where the features get placed?
 - ❖ Photo lithography masks



Intel 4004

- ❖ First microprocessor
 - ❖ Designed in 1971
 - ❖ 2300 transistors
 - ❖ 10-um process
 - ❖ ~100 KHz



Intel Itanium Processor

- ❖ Released in 2005
- ❖ 1.72 Billion transistors
- ❖ 90-nm process
- ❖ 2 GHz

