EECE 2322: Fundamentals of Digital Design and Computer Organization

Lecture 2_1: Gates and Numbers

Xiaolin Xu
Department of ECE
Northeastern University

A few updates

- 1, Turn to Zoom/online will be communicated ASAP
- 2, Slides before class
  - However, not the finalized version due to **Uncertainty + Hybrid**
  - So, only use them for reference
  - I will update the final version after each lecture

Truth Table

- One line for each possible combination of input values
- Shows the output value of the function for all possible input values
- There are four possible combinations of 2 input variables

Truth Table:

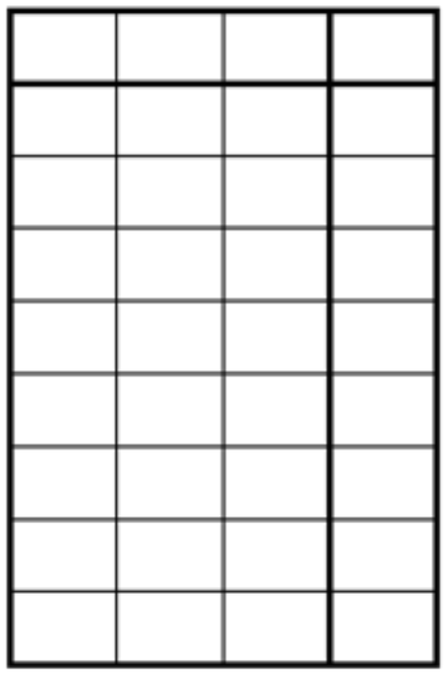
X	Y	Z=XY

Truth Table

Truth table for F = X + YZ:

___ variables

Number of rows in a truth table is _____.



- There is only one way that a Boolean function can be represented in a truth table

From Truth Table to Digital Circuit

- General Truth Table Structure for a 3-Variable Logic Function, F(X,Y, Z)

Row	X	Y	Z	F
0	0	0	0	F(0,0,0)
1	0	0	1	F(0,0,1)
2	0	1	0	F(0,1,0)
3	0	1	1	F(0,1,1)
4	1	0	0	F(1,0,0)
5	1	0	1	F(1,0,1)
6	1	1	0	F(1,1,0)
7	1	1	1	F(1,1,1)

From Truth Table to Digital Circuit

- General Truth Table Structure for a 3-Variable Logic Function, F(X,Y, Z)

Row	X	Y	Z	F
0	0	0	0	F(0,0,0)
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5	1	0	1	F(1,0,1)
6	1	1	0	F(1,1,0)
7	1	1	1	F(1,1,1)

Row	X	Y	Z	F
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

Minterms and Maxterms for a 3-Variable Logic Function, F(X,Y, Z)

Row	X	Y	Z	F	*Minterm*	*Maxterm*
0	0	0	0	F(0,0,0)	$X' \cdot Y' \cdot Z'$	$X + Y + Z$
1	0	0	1	F(0,0,1)	$X' \cdot Y' \cdot Z$	$X + Y + Z'$
2	0	1	0	F(0,1,0)	$X' \cdot Y \cdot Z'$	$X + Y' + Z$
3	0	1	1	F(0,1,1)	$X' \cdot Y \cdot Z$	$X + Y' + Z'$
4	1	0	0	F(1,0,0)	$X \cdot Y' \cdot Z'$	$X' + Y + Z$
5	1	0	1	F(1,0,1)	$X \cdot Y' \cdot Z$	$X' + Y + Z'$
6	1	1	0	F(1,1,0)	$X \cdot Y \cdot Z'$	$X' + Y' + Z$
7	1	1	1	F(1,1,1)	$X \cdot Y \cdot Z$	$X' + Y' + Z'$

Minterms and Maxterms for a 3-Variable Logic Function, F(X,Y, Z)

Row	X	Y	Z	F
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

$$F = \Sigma_{X,Y,Z}(0,3,4,6,7)$$

$$= X' \cdot Y' \cdot Z' + X' \cdot Y \cdot Z + X \cdot Y' \cdot Z' + X \cdot Y \cdot Z' + X \cdot Y \cdot Z$$

Minterms and Maxterms for a 3-Variable Logic Function, F(X,Y, Z)

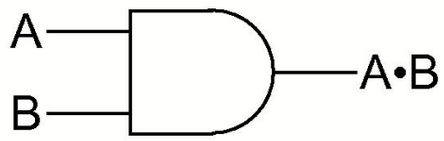
Row	X	Y	Z	F
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

$$F = \prod_{X,Y,Z}(1,2,5)$$
$$= (X + Y + Z') \cdot (X + Y' + Z) \cdot (X' + Y + Z')$$

Boolean Algebra

- Basic operator
  - AND

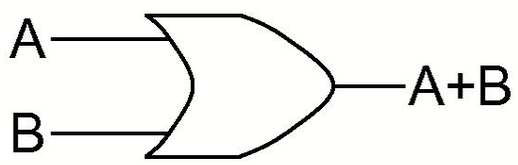
$$f(A,B) = A \cdot B = A \cap B$$



A	B	A•B
0	0	0
0	1	0
1	0	0
1	1	1

  - OR

$$f(A,B) = A + B = A \cup B$$



A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

One Input Logic Gate

- Inverter
  - F = X'

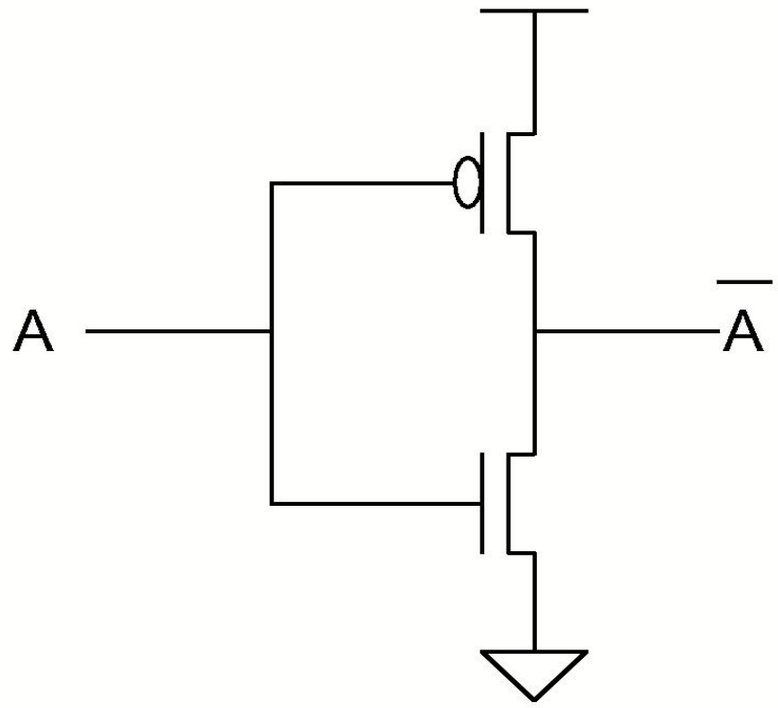
One Input Logic Gate

- Inverter
  - F = X'

- Buffer
  - F=X
  - Primarily used to amplify an electrical signal
  - To drive gates
  - How to design it?

CMOS Circuit Implementation Examples

- Inverter
  - Smallest digital circuit: 2 transistors



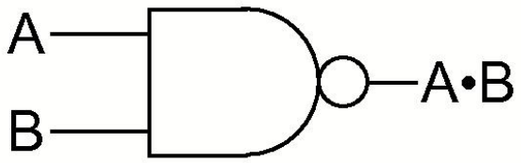
Truth Table

- One line for each possible combination of input values
- Shows the output value of the function for all possible input values
- There are four possible combinations of 2 input variables

Boolean Algebra

- Basic operator
  - NAND

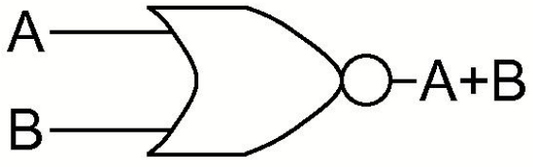
$$f(A,B) = \overline{A \cdot B} = \overline{A \cap B}$$



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

  - NOR

$$f(A,B) = \overline{A + B} = \overline{A \cup B}$$

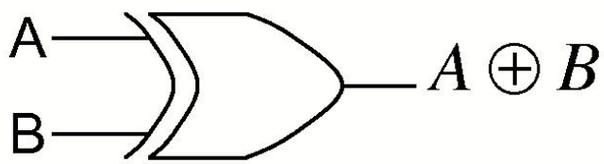


A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Boolean Algebra

- Basic operator
  - XOR
    - The most common operator in security and crypto
    - Equal 1 and 0: obfuscation

$$f(A,B) = A \oplus B$$



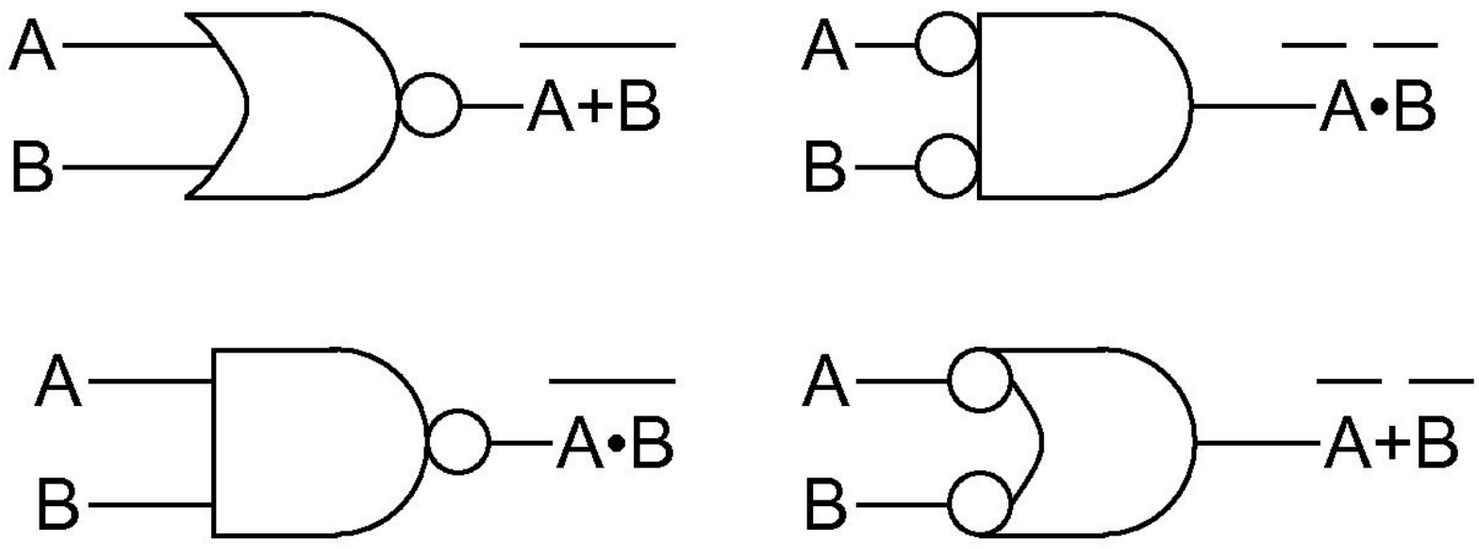
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Boolean Algebra

- DeMorgan's theorem

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$



Boolean Algebra

- Representation of the function to be realized
- Sum of Products representation
  - Sum of minterms

$$F = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + A\overline{B}C + AB\overline{C}$$

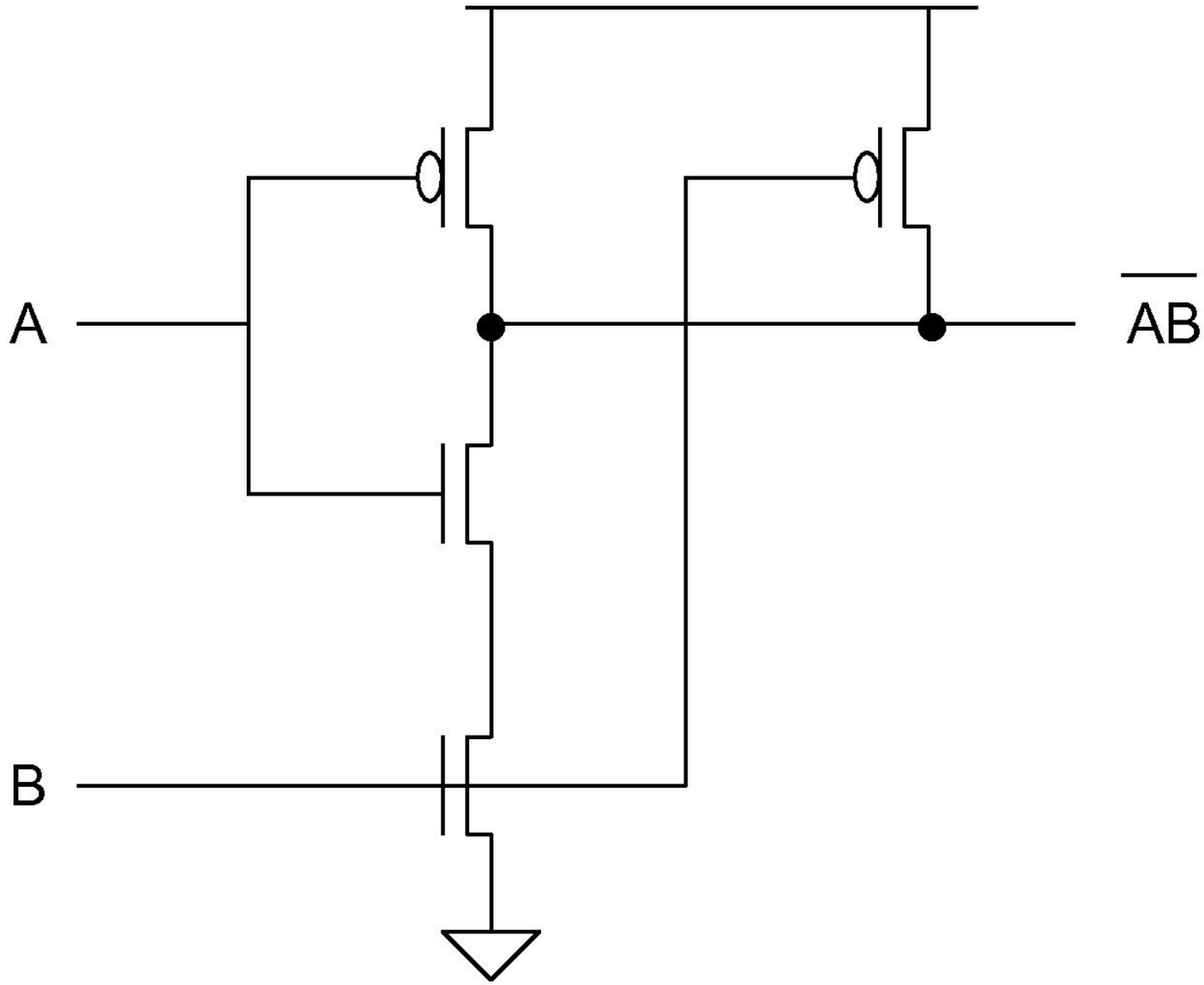
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

- Product of Sums representation
  - Product of maxterms

$$F = (A + B + C) \cdot (A + \overline{B} + \overline{C}) \cdot (\overline{A} + \overline{B} + \overline{C})$$

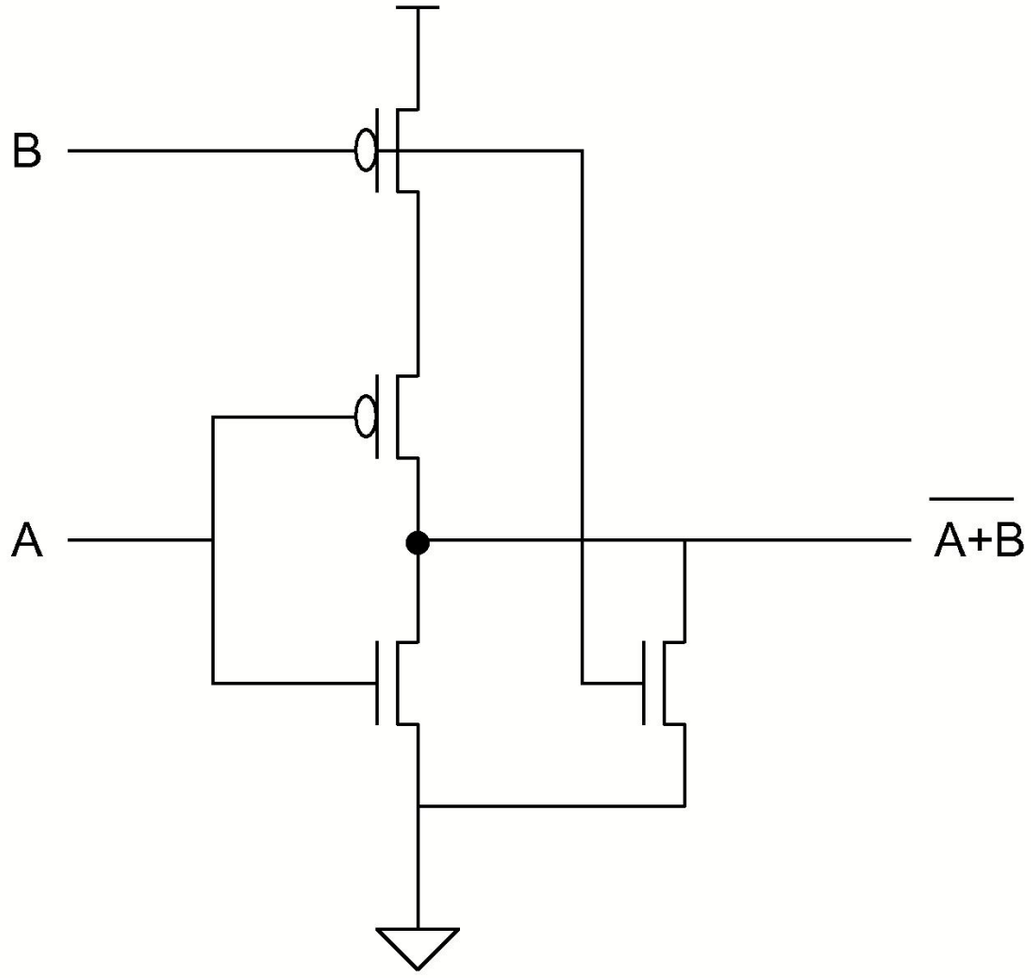
CMOS Circuit Implementation Examples

- NAND



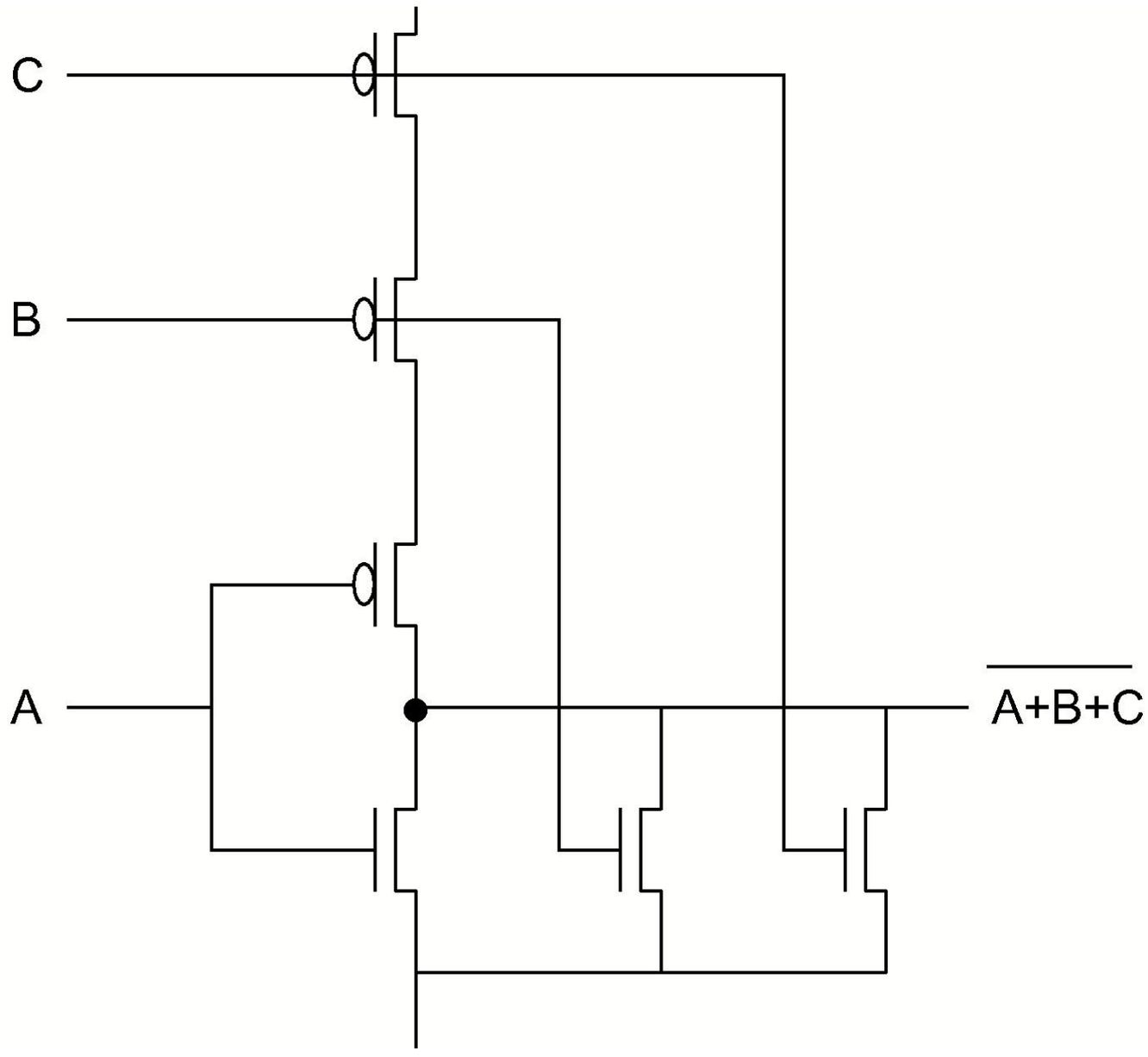
CMOS Circuit Implementation Examples

- NOR



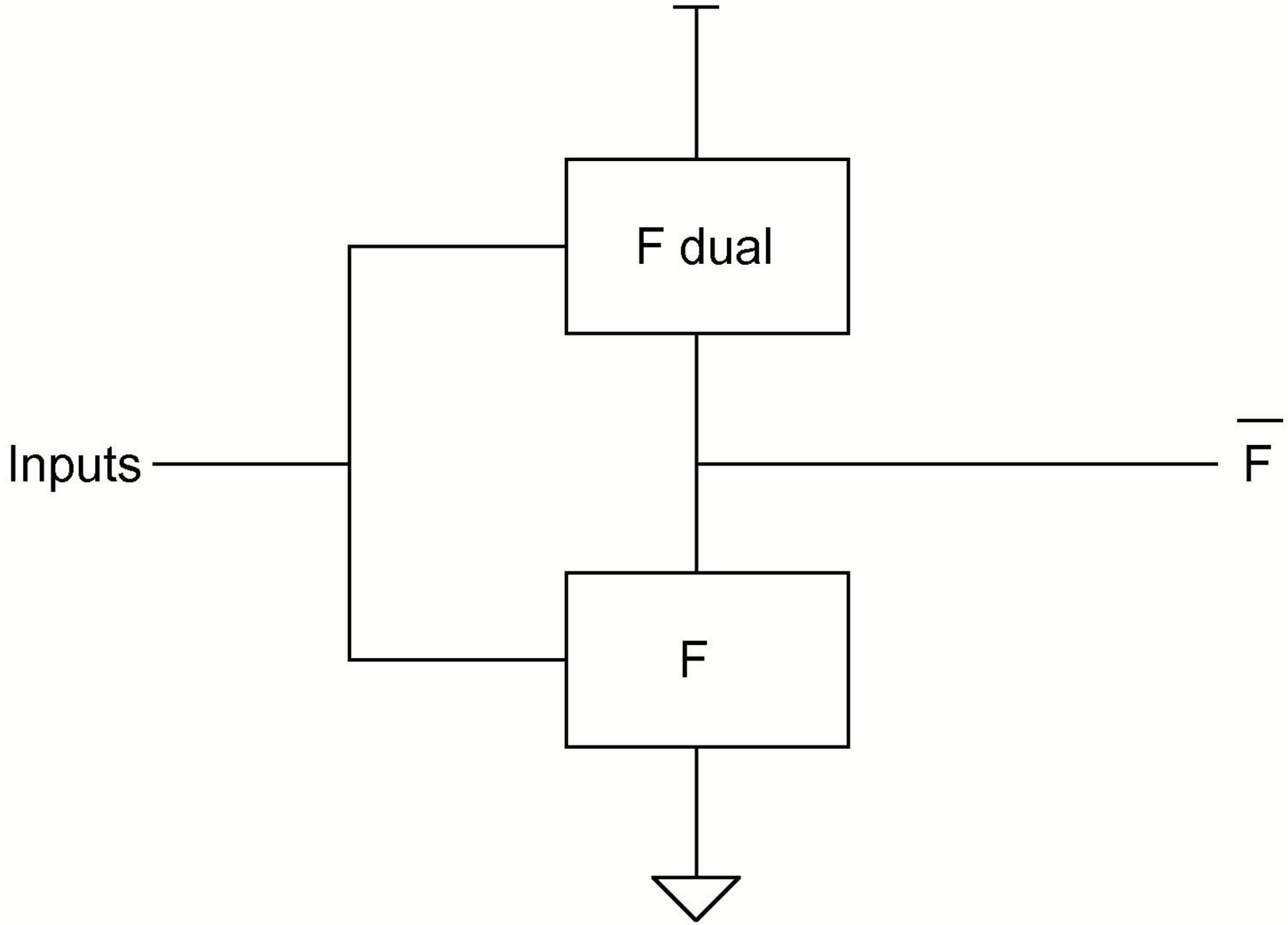
CMOS Circuit Implementation Examples

- Multi-input NOR



CMOS Circuit Implementation Examples

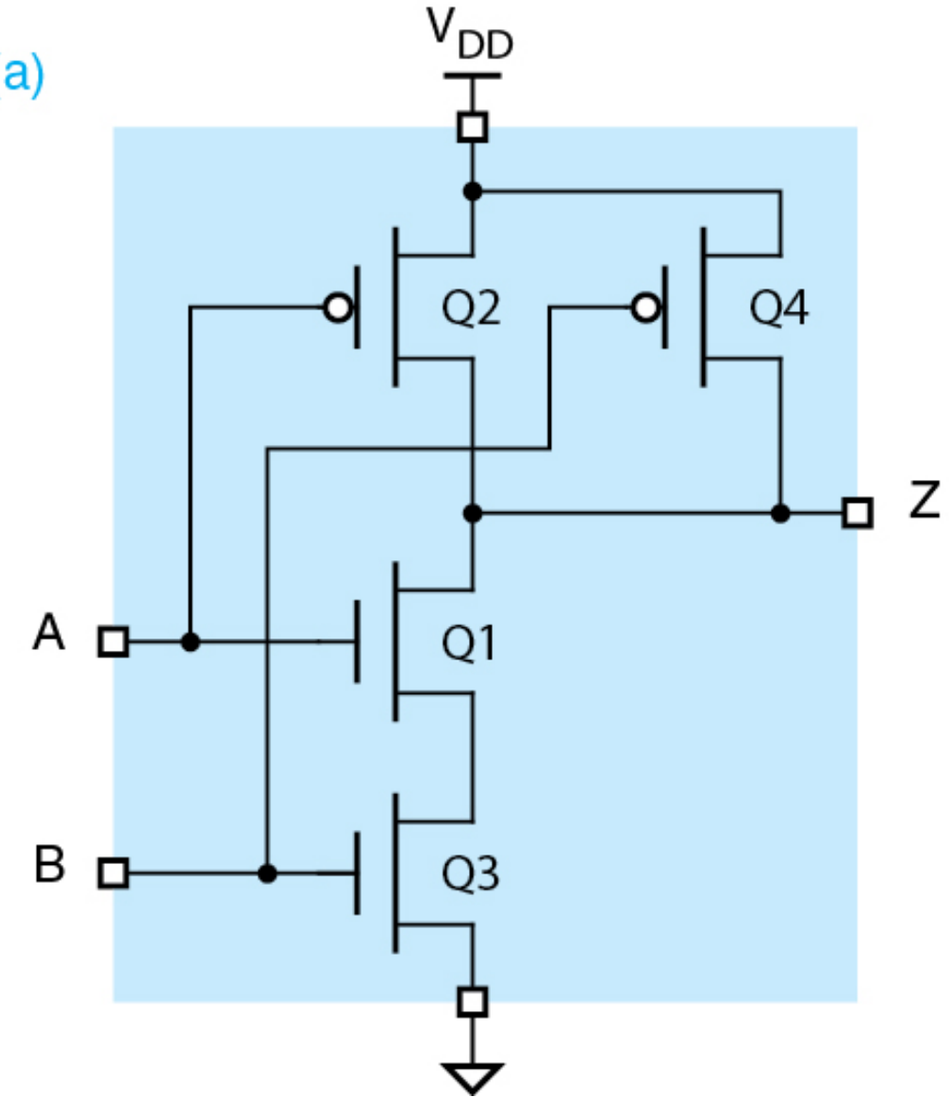
- The general design scheme



CMOS 2-Input NAND Gate

- (A) Circuit Diagram; (B) Function Table; (C) Logic Symbol

(a)



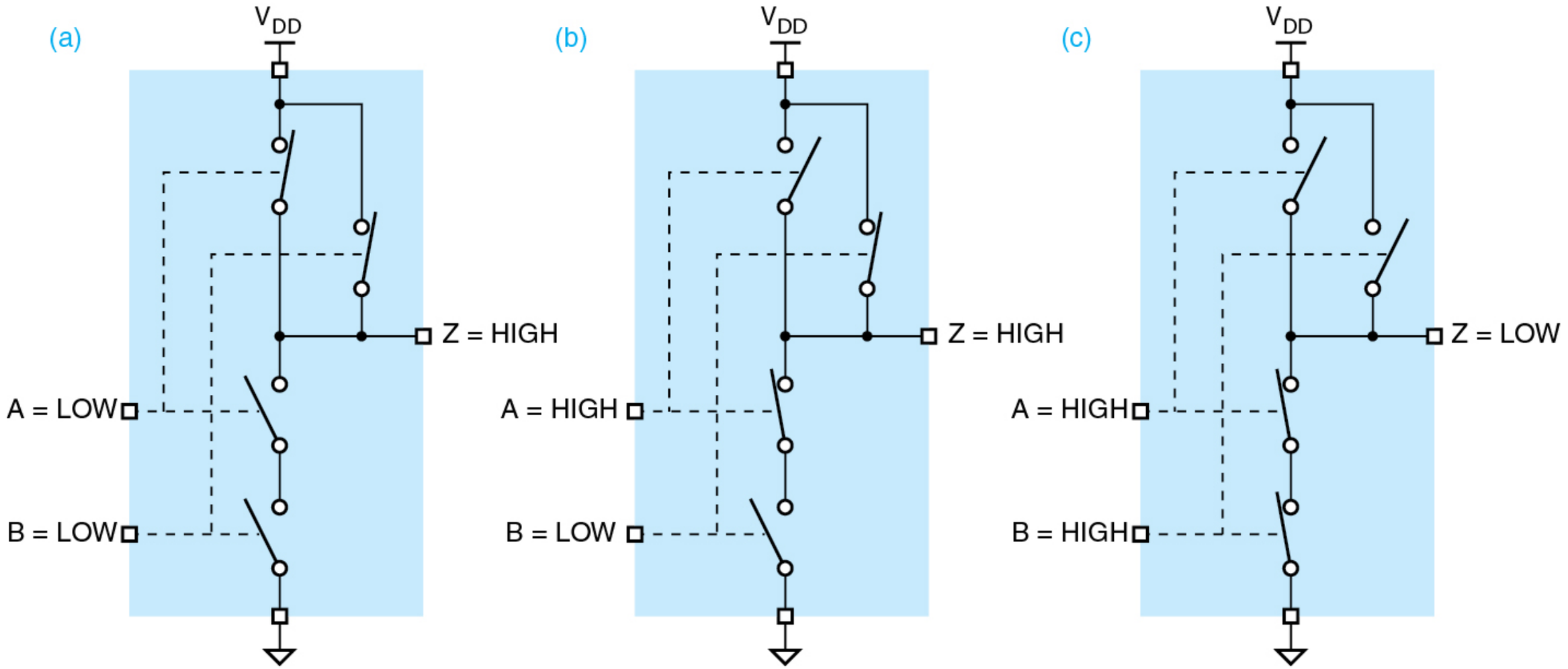
(b)

A	B	Q1	Q2	Q3	Q4	Z
LOW	LOW	off	on	off	on	HIGH
LOW	HIGH	off	on	on	off	HIGH
HIGH	LOW	on	off	off	on	HIGH
HIGH	HIGH	on	off	on	off	LOW

(c)

Switch Model for CMOS 2-Input NAND Gate

- (A) Both Inputs LOW; (B) One Input HIGH; (C) Both Inputs HIGH



Switching-Algebra Theorems with One Variable

(T1)	$X + 0 = X$	(T1D)	$X \cdot 1 = X$	(Identities)
(T2)	$X + 1 = 1$	(T2D)	$X \cdot 0 = 0$	(Null elements)
(T3)	$X + X = X$	(T3D	$X \cdot X = X$	(Idempotency)
(T4)	$(X')' = X$			(Involution)
(T5)	$X + X' = 1$	(T5'D)	$X \cdot X' = 0$	(Complements)

Switching-Algebra Theorems with Two or Three Variables

(T6)	$X + Y = Y + X$	(T6D)	$X \cdot Y = Y \cdot X$	(Commutativity)
(T7)	$(X + Y) + Z = X + (Y + Z)$	(T7D)	$(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$	(Associativity)
(T8)	$X \cdot Y + X \cdot Z = X \cdot (Y + Z)$	(T8D)	$(X + Y) \cdot (X + Z) = X + Y \cdot Z$	(Distributivity)
(T9)	$X + X \cdot Y = X$	(T9D)	$X \cdot (X + Y) = X$	(Covering)
(T10)	$X \cdot Y + X \cdot Y' = X$	(T10D)	$(X + Y) \cdot (X + Y') = X$	(Combining)
(T11)	$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$			(Consensus)
(T11′)	$(X + Y) \cdot (X' + Z) \cdot (Y + Z) = (X + Y) \cdot (X' + Z)$			

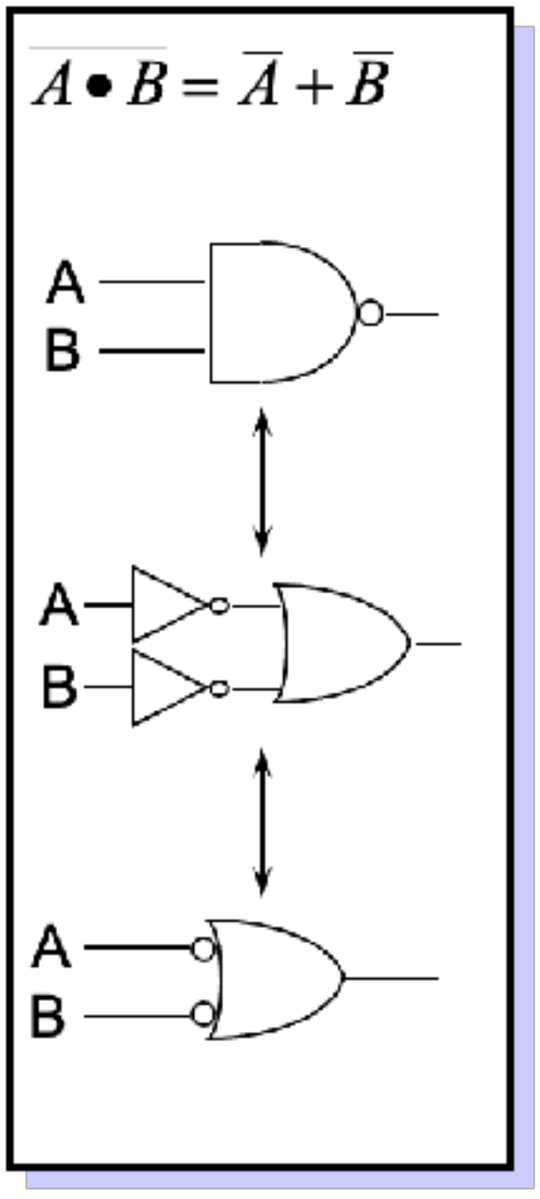
DeMorgan's Laws

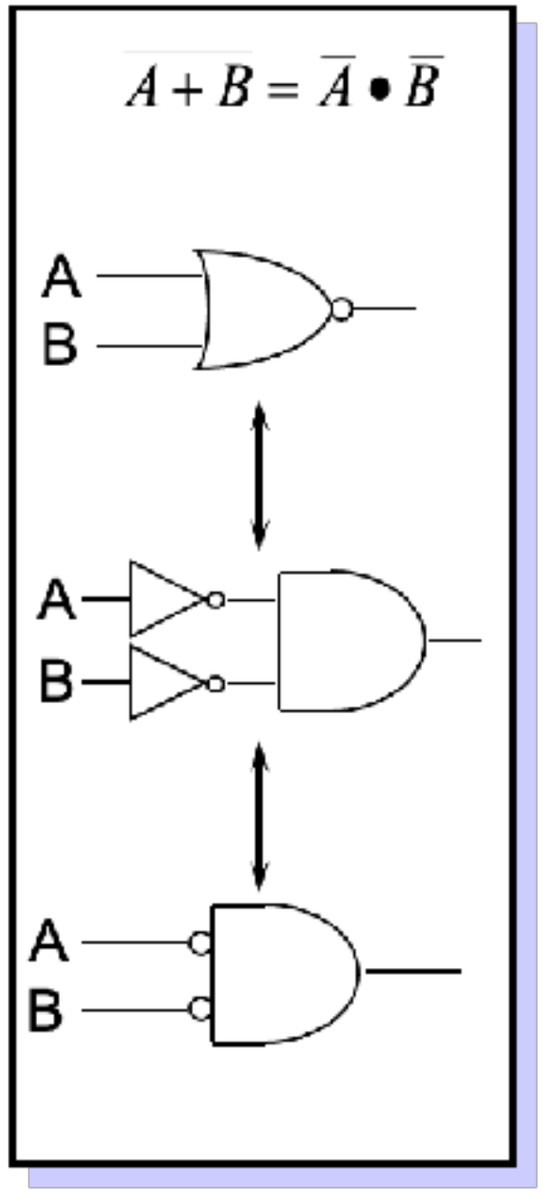
$$\overline{(a \bullet b)} = \overline{a} + \overline{b}$$

$$\overline{(a + b)} = \overline{a} \bullet \overline{b}$$

- Replace AND with OR and OR with AND
- Remove complement from the entire expression and place over each variable instead
- These laws are duals of one another

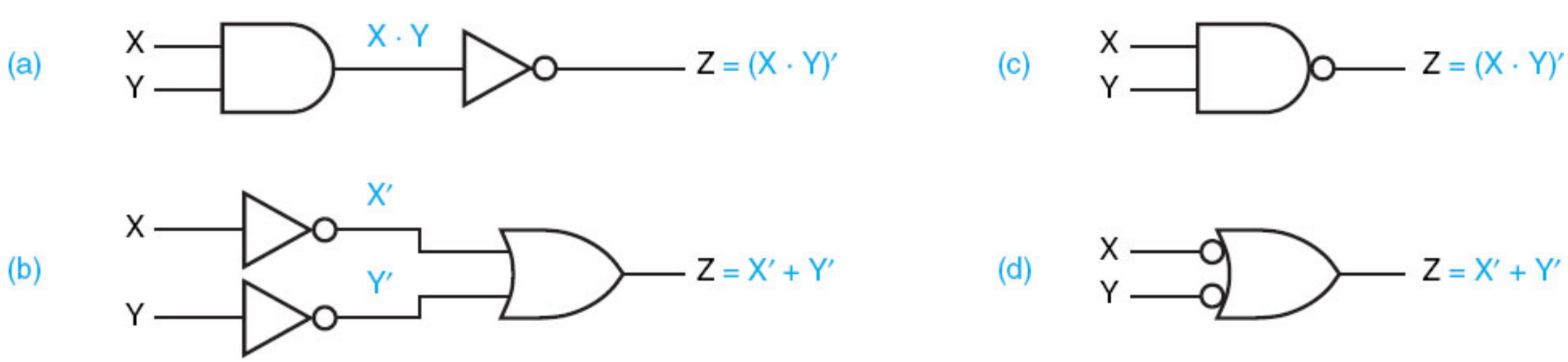
DeMorgan's Laws in Pictures





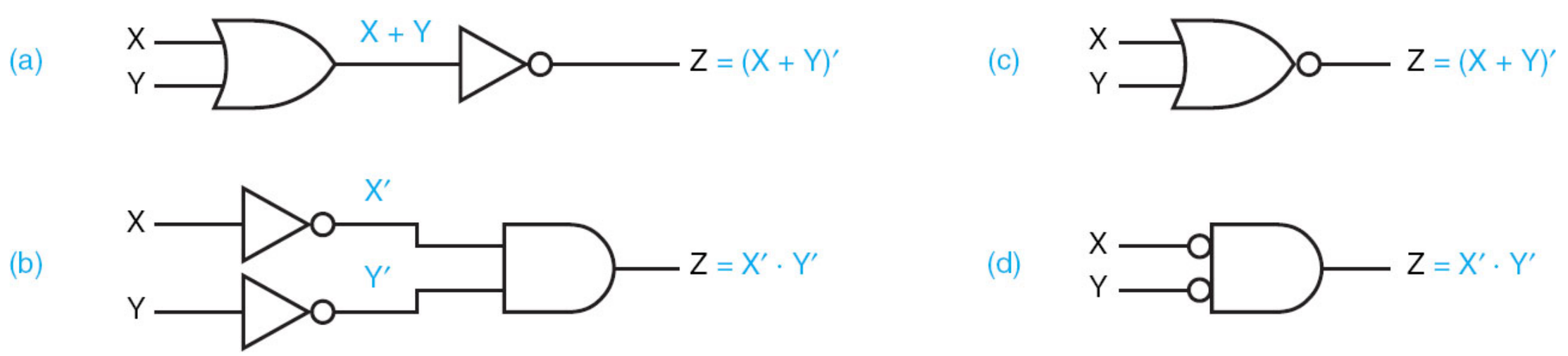
Equivalent Circuits According to DeMorgan's Theorem

- (A) AND-NOT; (B) NOT-OR; (C) Logic Symbol for a NAND Gate; (D) Equivalent Symbol for a NAND Gate



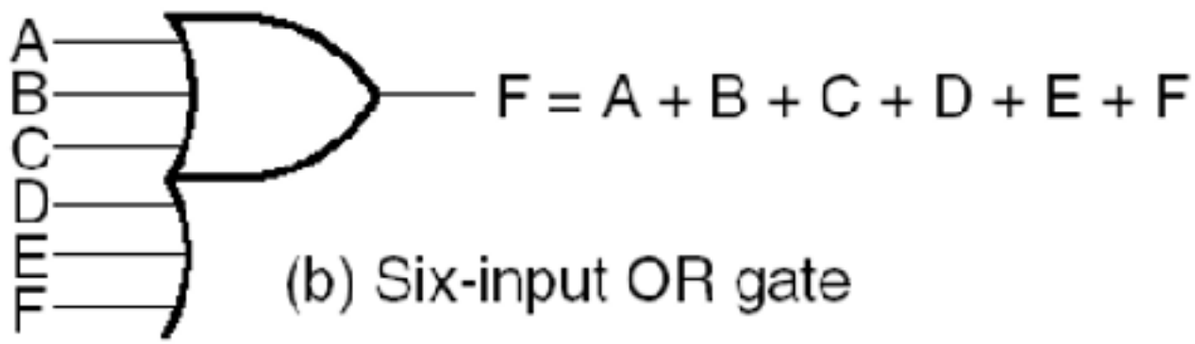
Equivalent Circuits According to DeMorgan's Theorem

- (A) OR-NOT; (B) NOT-AND; (C) Logic Symbol for a NOR Gate; (D) Equivalent Symbol for a NOR Gate



Gates can Have More than Two Inputs

(a) Three-input AND gate



(b) Six-input OR gate

Some Quick Rules

- An n-input AND gate has
  - output 1 when ALL inputs are 1
  - output 0 when ANY input is 0
- An n-input OR gate has
  - output 1 when ANY input is 1
  - output 0 when ALL inputs are 0

A 3-Input,1-Output Logic Circuit