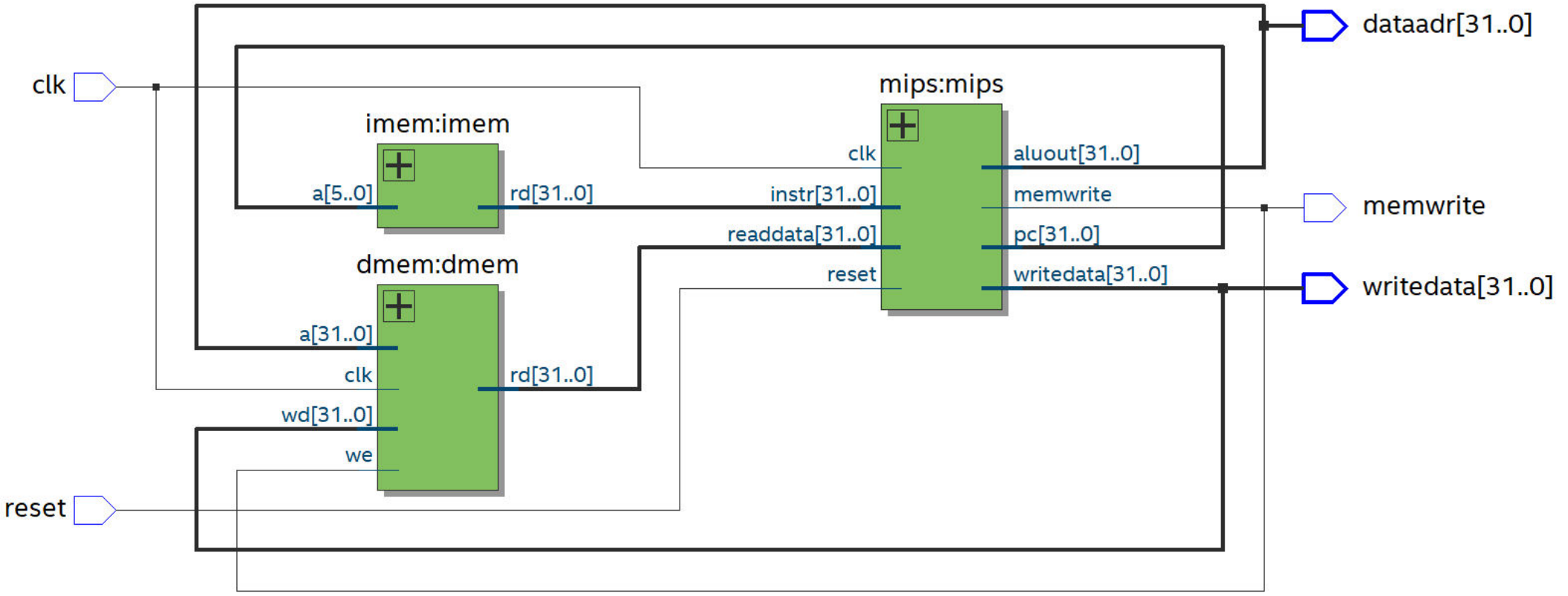
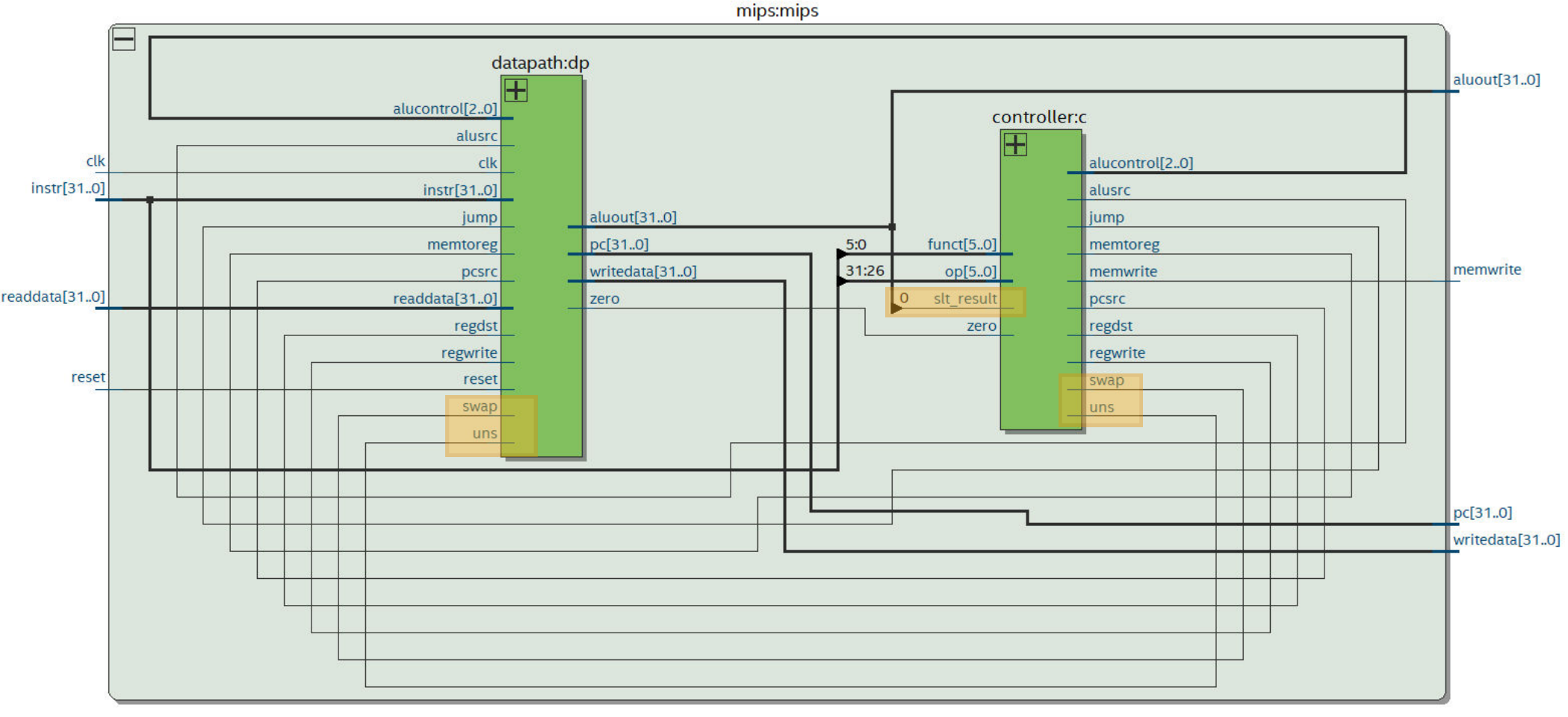
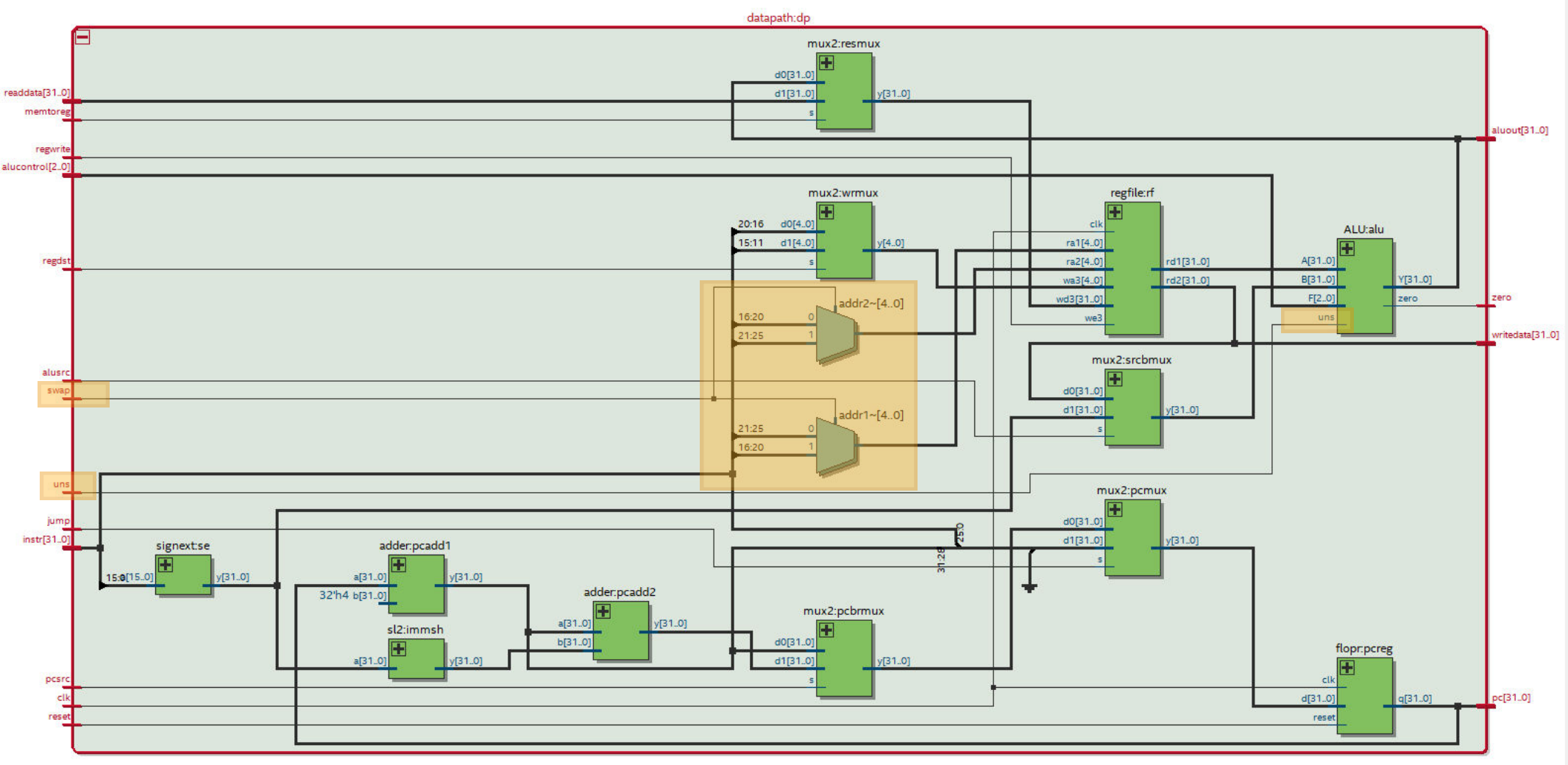
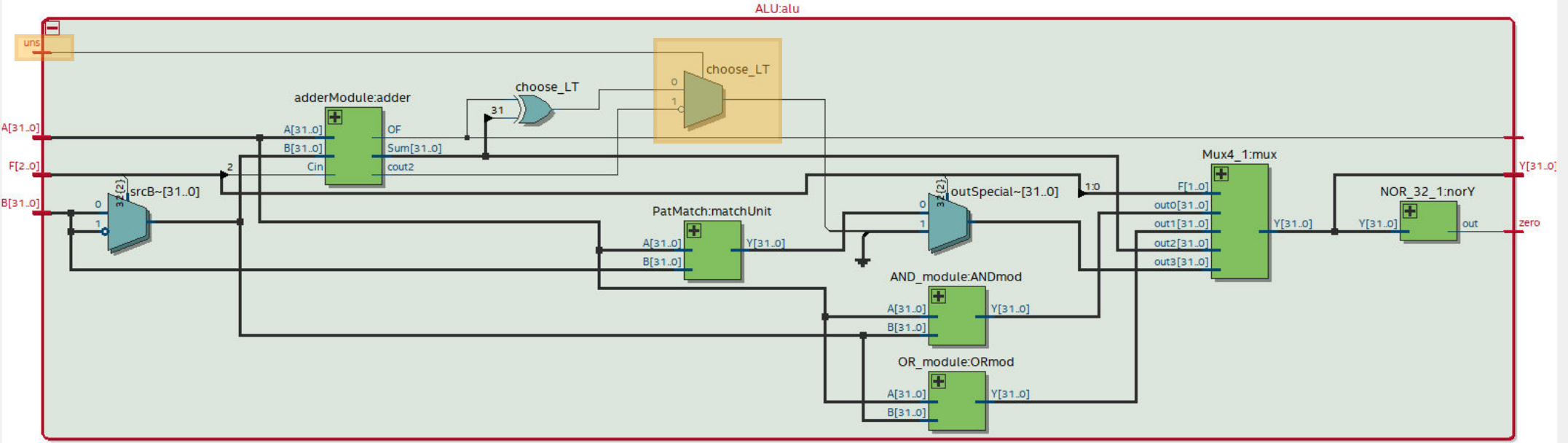
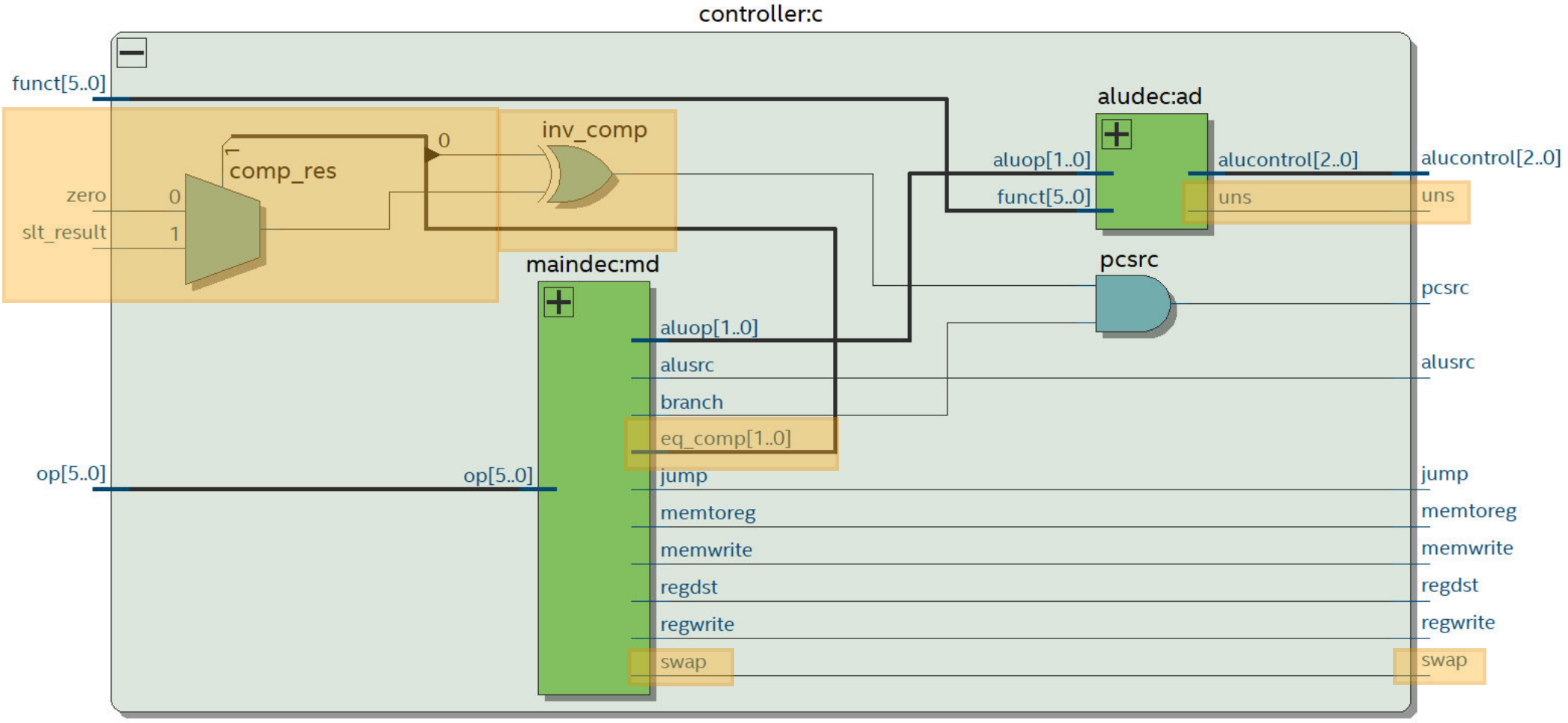
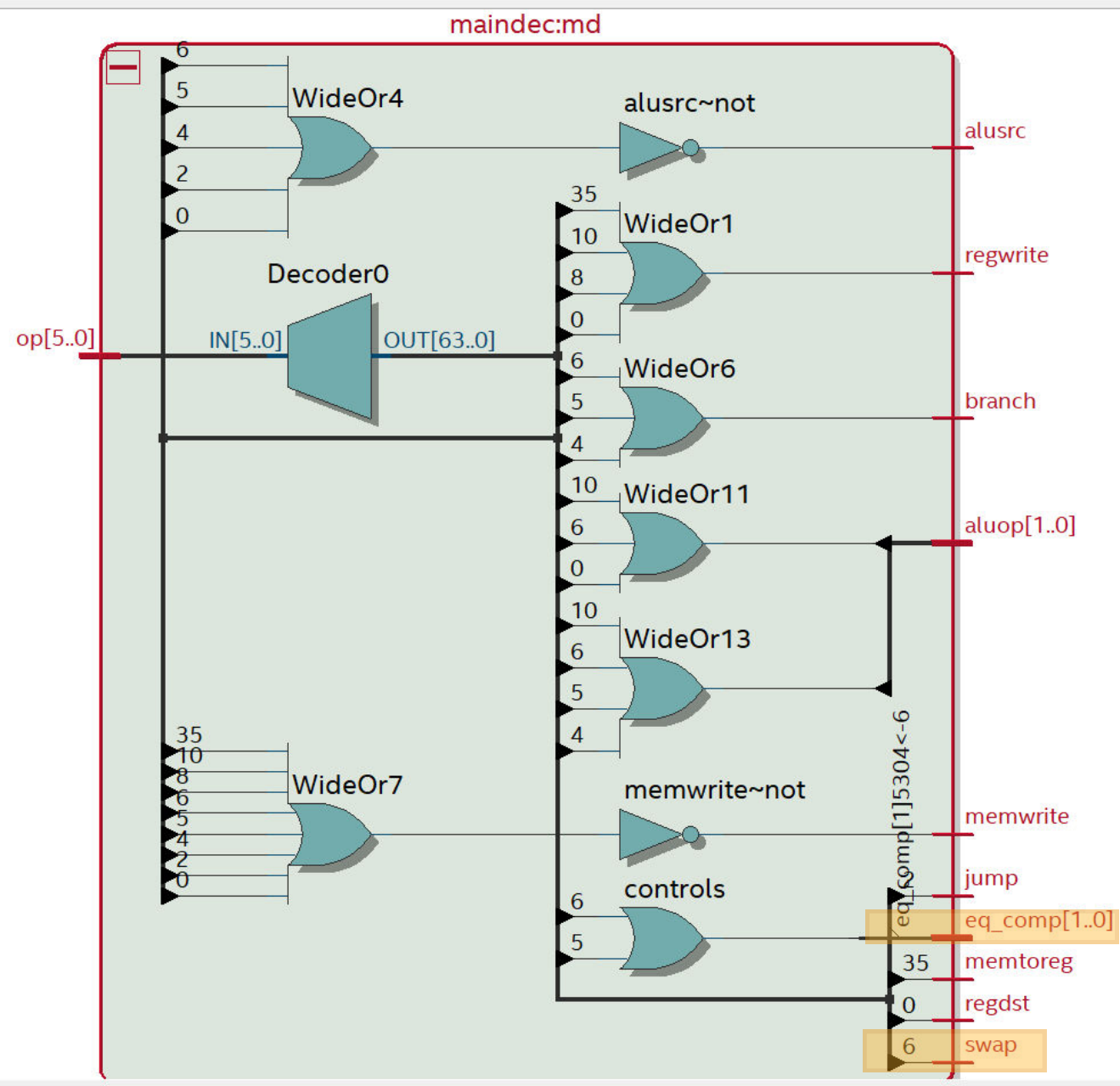

clk
reset
imem:imem
a[5..0]
rd[31..0]
dmem:dmem
a[31..0]
clk
wd[31..0]
we
rd[31..0]
mips:mips
clk
instr[31..0]
readdata[31..0]
reset
aluout[31..0]
memwrite
pc[31..0]
writedata[31..0]
dataadr[31..0]
memwrite
writedata[31..0]

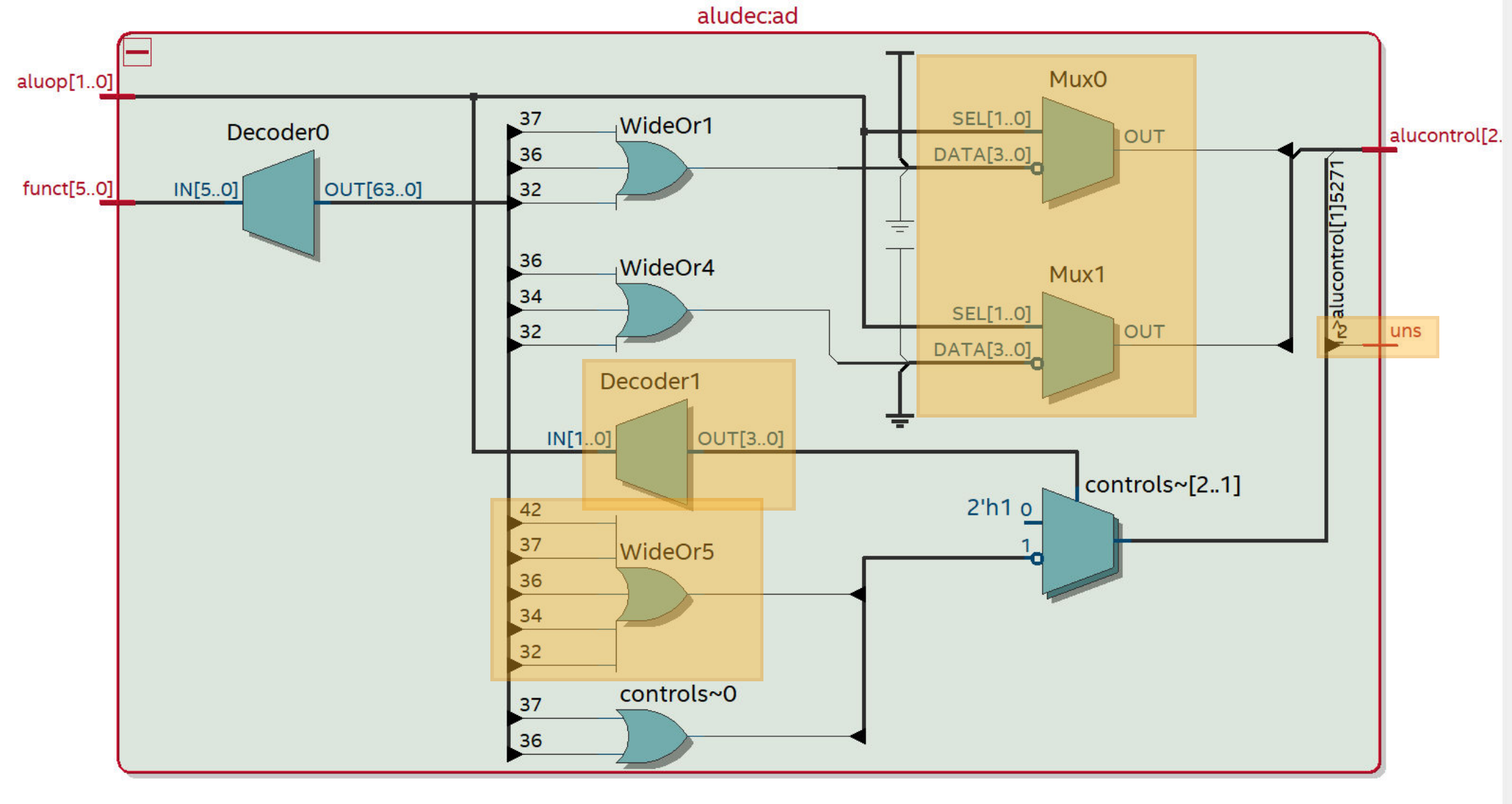

mips:mips
datapath:dp
alucontrol[2..0]
alusrc
clk
instr[31..0]
jump
memtoreg
pcsrc
readdata[31..0]
regdst
regwrite
reset
swap
uns
aluout[31..0]
pc[31..0]
writedata[31..0]
zero
controller:c
5:0
31:26
funct[5..0]
op[5..0]
0
slt_result
zero
alucontrol[2..0]
alusrc
jump
memtoreg
memwrite
pcsrc
regdst
regwrite
swap
uns
clk
instr[31..0]
readdata[31..0]
reset
aluout[31..0]
memwrite
pc[31..0]
writedata[31..0]


datapath:dp
mux2:resmux
d0[31..0]
d1[31..0]
s
y[31..0]
readdata[31..0]
memtoreg
regwrite
alucontrol[2..0]
aluout[31..0]
mux2:wrmux
20:16
15:11
d0[4..0]
d1[4..0]
y[4..0]
regdst
regfile:rf
clk
ra1[4..0]
ra2[4..0]
wa3[4..0]
wd3[31..0]
we3
rd1[31..0]
rd2[31..0]
ALU:alu
A[31..0]
B[31..0]
F[2..0]
uns
Y[31..0]
zero
writedata[31..0]
addr2~[4..0]
16:20
21:25
0
1
addr1~[4..0]
21:25
16:20
alusrc
swap
mux2:srcbmux
uns
mux2:pcmux
jump
instr[31..0]
31:28
2'b0
signext:se
15:0
y[31..0]
adder:pcadd1
a[31..0]
32'h4
b[31..0]
sl2:immsh
adder:pcadd2
mux2:pcbrmux
flopr:pcreg
d[31..0]
q[31..0]
pcsrc
clk
reset
pc[31..0]


ALU:alu
uns
A[31..0]
F[2..0]
B[31..0]
srcB~[31..0]
adderModule:adder
A[31..0]
B[31..0]
Cin
OF
Sum[31..0]
cout2
choose_LT
choose_LT
PatMatch:matchUnit
A[31..0]
B[31..0]
Y[31..0]
outSpecial~[31..0]
AND_module:ANDmod
OR_module:ORmod
Mux4_1:mux
F[1..0]
out0[31..0]
out1[31..0]
out2[31..0]
out3[31..0]
NOR_32_1:norY
out
zero
Y[31..0]


controller:c
funct[5..0]
comp_res
1
0
zero
0
slt_result
1
inv_comp
aludec:ad
aluop[1..0]
funct[5..0]
alucontrol[2..0]
uns
alucontrol[2..0]
uns
pcsrc
pcsrc
maindec:md
aluop[1..0]
alusrc
branch
eq_comp[1..0]
op[5..0]
op[5..0]
jump
memtoreg
memwrite
regdst
regwrite
swap
alusrc
jump
memtoreg
memwrite
regdst
regwrite
swap


maindec:md
WideOr4
alusrc~not
alusrc
WideOr1
regwrite
Decoder0
op[5..0]
IN[5..0]
OUT[63..0]
WideOr6
branch
WideOr11
aluop[1..0]
WideOr13
WideOr7
memwrite~not
memwrite
jump
controls
eq_comp[1..0]
memtoreg
regdst
swap
eq_comp[1]5304<-6


aludec:ad
aluop[1..0]
funct[5..0]
Decoder0
IN[5..0]
OUT[63..0]
37
36
32
WideOr1
36
34
32
WideOr4
Decoder1
IN[1..0]
OUT[3..0]
42
37
36
34
32
WideOr5
37
36
controls~0
Mux0
SEL[1..0]
DATA[3..0]
OUT
Mux1
SEL[1..0]
DATA[3..0]
OUT
alucontrol[2.
alucontrol[1]5271
uns
controls~[2..1]
2'h1
0
1