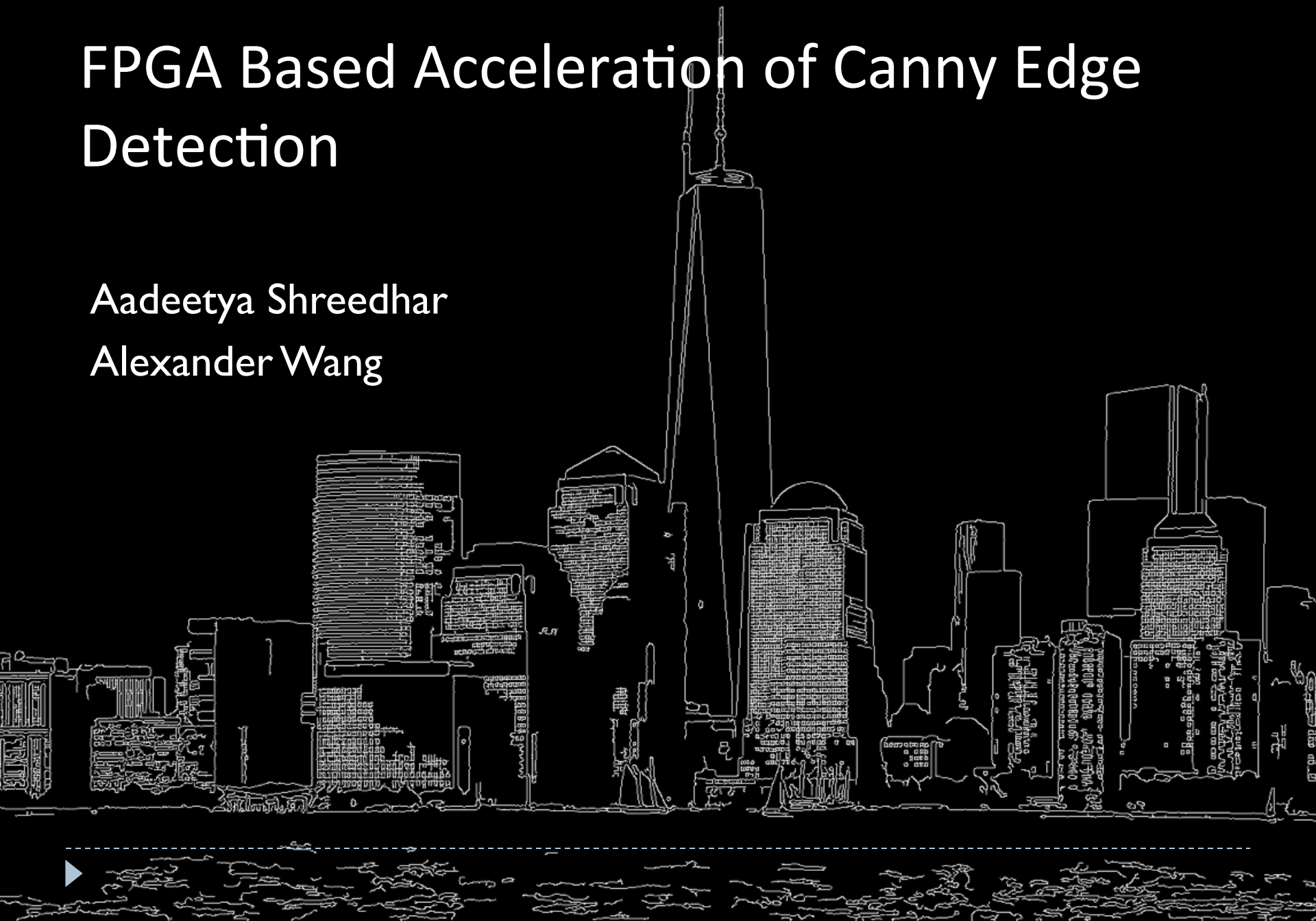
FPGA Based Acceleration of Canny Edge Detection

Aadeetya Shreedhar
Alexander Wang



Overview

- Edge detection identifies discontinuities in an image
- Picks out important information
- Reduces the amount of information in the image
- Critical step in image processing
  - Feature detection
  - Feature extraction
  - Computer vision

Motivation for HW Acceleration

- Flexibility – edge detection is an important part of a large family of computational problems
- Performance – edge detection is often used in systems that have real-time constraints, and HW acceleration can:
  - help solve bigger problems
  - help set more aggressive performance targets
- Energy efficiency – dedicated hardware reduces the energy consumption of compute intensive tasks

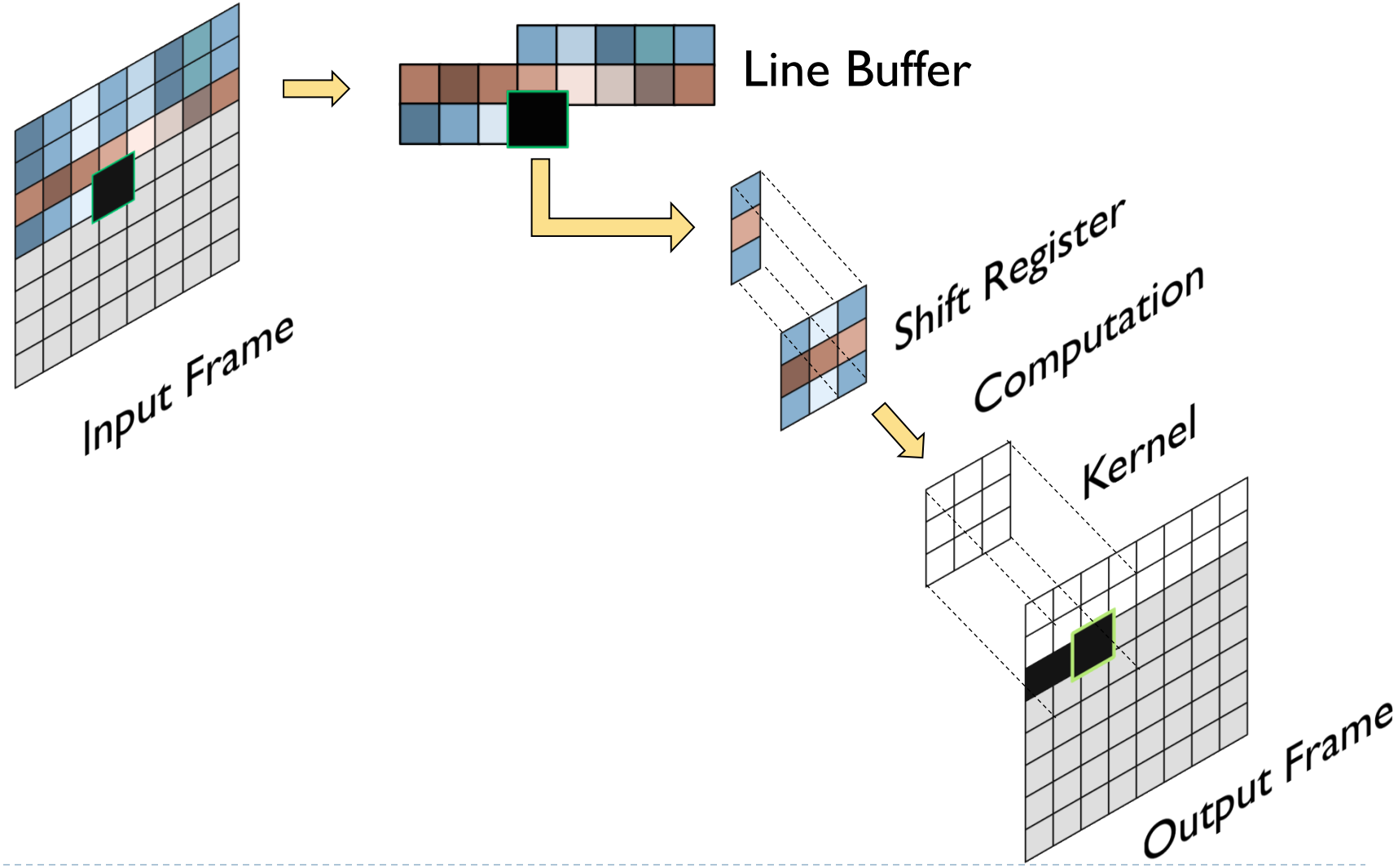
Algorithm Description

Input Frame → Grayscaling → Noise Reduction

Algorithm Description

Gradient → Non-maximum Suppression → Hysteresis

HLS Implementation

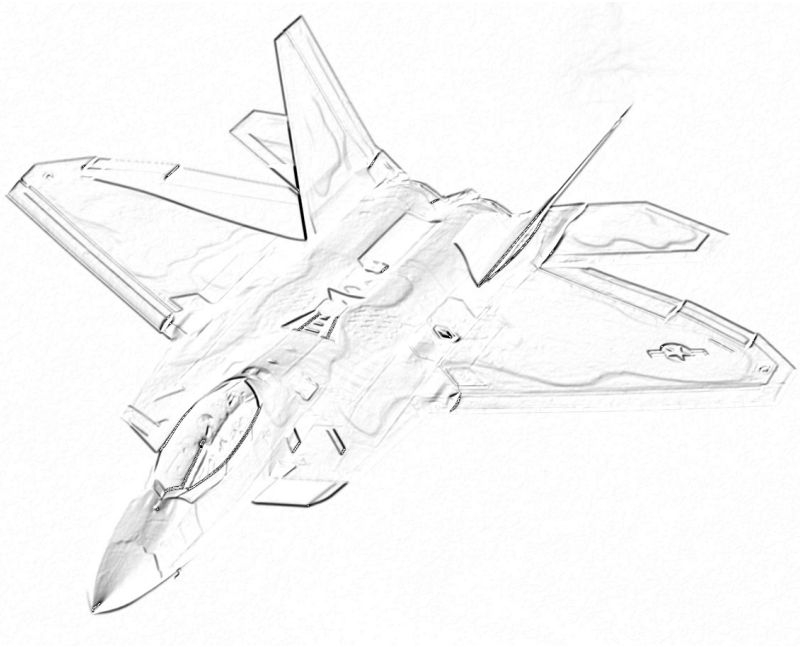


Results

- Device clock frequency – **83.738 MHz**
- Can process a 1920x1080 stream at **40.38 FPS**

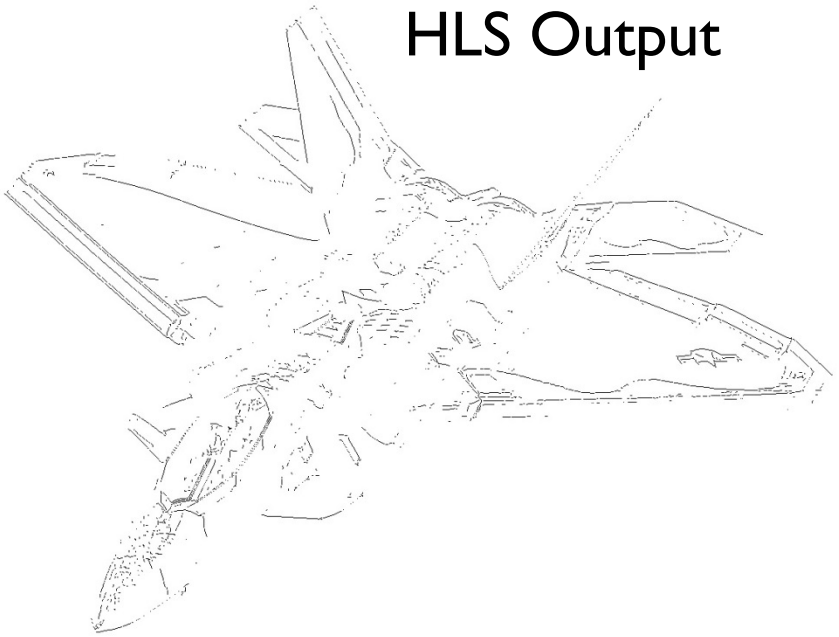
Resource	Utilization Count	Utilization %
BRAM_18K	25	8%
DSP48E	62	28%
FF	27391	25%
LUT	23948	45%

Quality of Result



Sobel Output

HLS Output



Conclusion

- Productivity – Designing coprocessors and algorithm accelerators using high-level synthesis is quicker than using RTL
- HLS Image processing constructs – converting video streams to matrices, line buffers, shift registers, and matrix operations
- Express HW design characteristics – express HW features with HLS directives and gain intuition of what the translated hardware will look like

Acknowledgements

- Professor Zhiru Zhang
- Image and Video Processing Platform for FPGAs Using High-Level Synthesis by C. Desmouliers, E. Oruklu, S. Aslan, and J. Saniie and F. Martinez Vallina
- Accelerating OpenCV Applications with Zynq-7000 All Programmable SoC using Vivado HLS Video Libraries by Stephen Neuendorffer, Thomas Li, and Devin Wang

Questions