The 9's complement of 167_{10} equals to ___

Select one:

- a. 832
- b. 233
- c. 232
- d. 732

Clear my choice

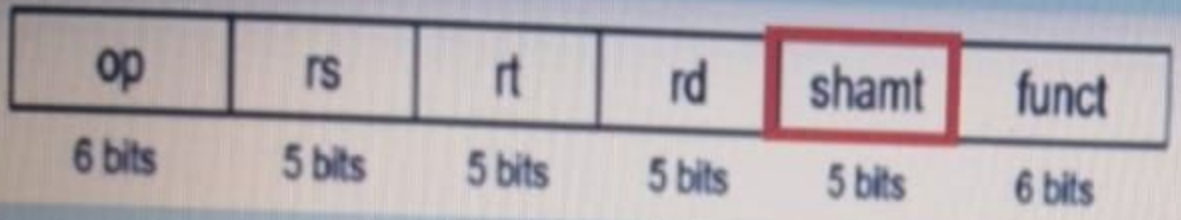
The fastest data access is provided using _____

Select one:

- a. Registers
- b. DRAM's
- c. SRAM's
- d. Caches

Clear my choice

Bits 6-10 of an R-format instruction are only used for particular instructions. Which of the following R-format instructions uses those bits?



- a. xor
- b. sub
- c. add
- d. sll

Which method of representation has **one** representation for '0'?

Select one:

- a. Sign Magnitude
- b. 2's complement
- c. 1's complement
- d. None of the mentioned

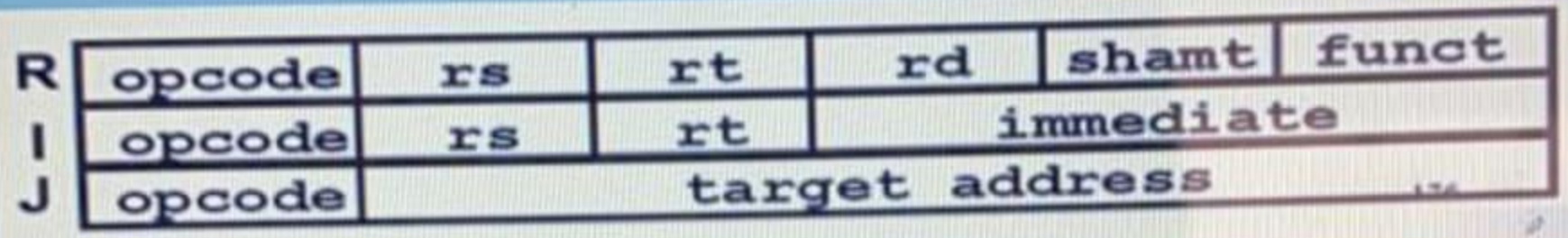
Clear my choice

Which of the following instruction-format pairings is **incorrect?**

- a. lw- R-format
- b. j - J-format
- c. slt- R-format
- d. addi- I-format

Clear my choice

There are 3 basic instruction formats in the MIPS instruction set architecture. They are:



R	opcode	rs	rt	rd	shamt	funct
I	opcode	rs	rt	immediate		
J	opcode	target address				

What aspect of the instruction's machine language encoding distinguishes between these different formats?

- a. The presence or absence of the constant field in the instruction
- b. The number of register fields in the instruction
- c. Either appending an "i" to the end of a normal instruction or beginning the instruction with a "j"
- d. None of the above

How many bytes does the (MIPS -32) word take up?

- a. 8 bytes
- b. 4 bytes
- c. 16 bytes
- d. 1 byte

Clear my choice

Which of the following instructions performs the instruction move $t1, $t2?

- a. add $t1, $t2, $t1
- b. add $t2, $zero, $t1
- c. add $t1, $zero, $t2
- d. lui $t1, 0

Clear my choice

The complement of any number can be given by a general term

- a. $B^n + 1 - N$
- b. $B^n - 1 + N$
- c. $B^n + 1 + N$
- d. $B^n - 1 - N$

Clear my choice

Specify the destination register in the instruction:

beq $t6, $t7, 24

- a. no destination
- b. $t8
- c. $t7
- d. $t6

Excess Biased

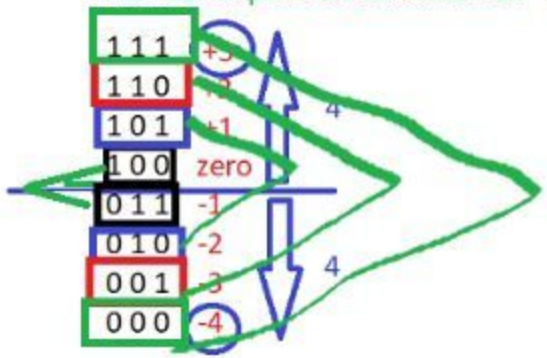
- 3 bits excess notation
- 4 bits excess notation
- 5 bits excess notation
- 6 bits excess notation
- 8 bits excess notation

1: positive
0: negative

How to represent Zero?

- 3 bits excess:
  0 = 100
- 4 bits excess:
  0 = 1000
- 5 bits excess:
  0 = 10000
- 6 bits excess:
  0 = 100000

3 bits excess,
number of possible combination = 8



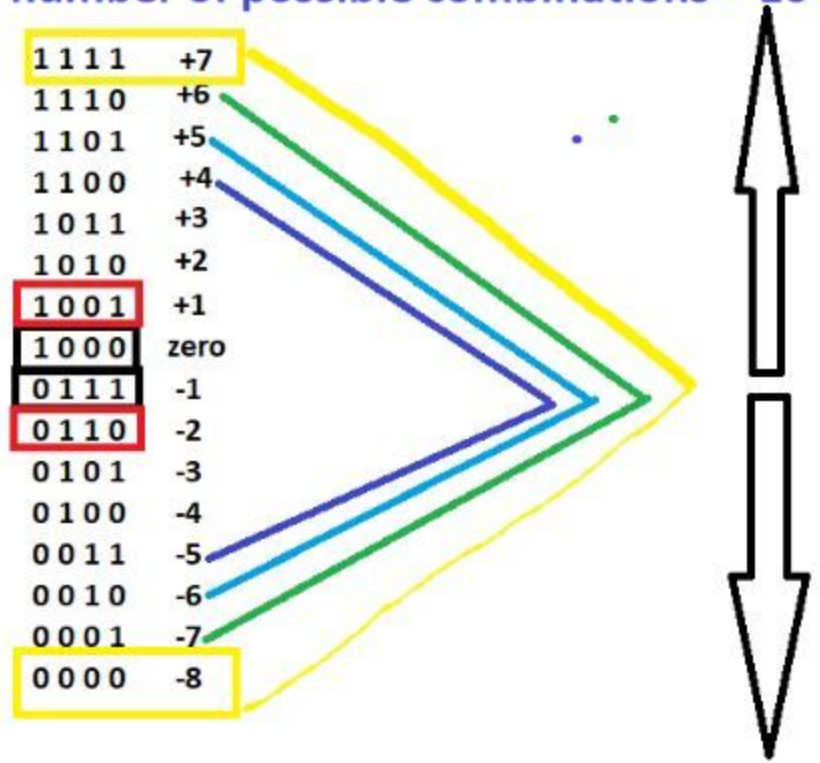
The negation of zero is -1
The negation of +1 is -2
The negation of +2 is -3
The negation of +3 is -4

+3: 111
-4: 000

0: 100
0: 1000

4 bits excess

number of possible combinations = 16



The complement of any number can be given by a general term

- a. $B^n + 1 - N$
- b. $B^n - 1 + N$
- c. $B^n + 1 + N$
- d. $B^n - 1 - N$

Clear my choice

Back

Question 3

Answer saved

Marked out of 1

Flag question

In which mode the operand is stored in the register and this register is present in CPU?

- Variable Mode
- Register mode
- Register indirect mode
- Immediate mode

Clear my choice

Previous page

Previous activity

Text Book

Jump to...

Which of the following is **not** an I-type instruction?

Select one:

- a. sll $t1, $t2, 3
- b. slti $t1, $t2, 5
- c. bne $t1, $t0, Label
- d. addi $t1, $t2, 3

Clear my choice

In IEEE754 format, the size of the mantissa (fractional part) is _____

Select one:

a. 23 bit

b. 8 bit

c. 64 bit

d. 32 bit

Clear my choice

When we want to load a register with 32 bits value, the assembler actually needs to perform two MIPS instructions. The first of these two instructions is **lui** (load upper immediate), which takes the upper 16 bits provided and stores them as the upper 16 bits of the register. What is the other command?

- a. add
- b. addi
- c. and
- d. ori

Assume the values stored in registers $s0 is zero and the value stored in $s1 is 19, what execution of the following instruction?

addi $s0, $s1, 11

- 11110 in $s0 and 11110 in $s1
- 0 in $s0 and 10011 in $s1
- 10011 in $s0 and 10011 in $s1
- **11110 in $s0 and 10011 in $s1**

Clear my choice

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Which of the following statements is not correct about Assembly language?

- Explicit manipulation of memory management
- Readable
- Machine-dependent
- Mnemonic names for machine operation

Clear my choice

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Previous activity

Text Book

Jump to...

لمادة تصميم وتنظيم الحاسوب

Back

Question 1

Answer saved

Marked out of 1

Flag question

The performance of a program depends on all of the following except:

- Software system
- Computer
- Programmer
- Algorithm

Clear my choice

Previous activity

Text Book

Jump to...

I-format and J-format instructions both accomodate an immediate value to be specified. What is the maximum number of bits that can be specified for each instruction format?

- a. 28 for I, 28 for J
- b. 16 for I, 28 for J
- c. 20 for I, 26 for J
- d. 16 for I, 26 for J

Which of the following instructions performs the instruction move $t1, $t2?

- a. add $t1, $t2, $t1
- b. add $t2, $zero, $t1
- c. add $t1, $zero, $t2
- d. lui $t1, 0

Clear my choice

A 32 bit address generates an address space of _____ locations.

Select one:

- 1024
- 16,777,216
- 4 gibibytes
- 2048
- 2^{48}

Clear my choice

Which representation is most efficient to perform arithmetic operations on signed numbers in MIPS architecture?

Select one:

- a. Sign-magnitude
- b. 1's complement
- c. None of the mentioned
- d. 2's complement

Clear my choice

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A 32 bit address generates an address space of _____ locations.

Select one:

- 1024
- 16,777,216
- 4 gibibytes
- 2048
- 2^{48}

Clear my choice

Question 17

Answer saved

Marked out of 2

Flag question

When we want to load a register with 32 bits value, the assembler actually needs to perform two MIPS instructions. The first of these two instructions is **lui** (load upper immediate), which takes the upper 16 bits provided and stores them as the upper 16 bits of the register. What is the other command?

- a. ori
- b. and
- c. addi
- d. add

Clear my choice

The fastest data access is provided using _____

Select one:

- a. DRAM's
- b. SRAM's
- c. Registers
- d. Caches

Clear my choice

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The product of 1101 & 1011 is _____

Select one:

a. 10001001

b. 11101110

c. 10001111

d. 10101111

Clear my choice

The equivalent hexadecimal nota

- a. ACABE
- b. AD0BE
- c. FADED
- d. AEOBE

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If a system is 64 bit machine, then the length of each word will be _____

Select one:

- a. 8 bytes
- b. 4 bytes
- c. 16 bytes
- d. 2 bytes

Clear my choice

The instruction that reads data from a register and transfers data into memory is:

a. load

b. store

In IEEE754 format, the sign bit is followed by string of digits called as _____

Select one:

- a. Exponent
- b. Significant
- c. Determinant
- d. Mantissa

Clear my choice

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ut of 1

Which of the following is correct about computer architecture?

- Expresses the realization of architecture.
- It acts as the interface between hardware and software.
- Deals with low-level design issues
- Involves Physical Components (Circuit design, Adders, Signals, Peripherals)

Clear my choice

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ext Book

Jump to...

Which of the following instruction-format pairings is **incorrect?**

- a. lw- R-format
- b. j - J-format
- c. slt- R-format
- d. addi- I-format

Clear my choice

The 3-bits Excess representation of zero is _____

a. 100

b. 000

c. 101

d. 111

Which of the following instructions is a J-format instruction?

- a. jal
- b. bne
- c. slt
- d. addi

Clear my choice

If a system is 64 bit machine, then the length of each word will be

Select one:

- a. 2 bytes
- b. 4 bytes
- c. 16 bytes
- d. 8 bytes

Which of the following instructions is a J-format instruction?

- a. jal
- b. bne
- c. slt
- d. addi

Clear my choice

If a system is 64 bit machine, then the length of each word will be

Select one:

- a. 2 bytes
- b. 4 bytes
- c. 16 bytes
- d. 8 bytes

Which method of representation has **one** representation for '0'?

Select one:

- a. Sign Magnitude
- b. 2's complement
- c. 1's complement
- d. None of the mentioned

Clear my choice

Let's say we have an Array with 64 integer elements. The address of t
following moves the data from Array[60] into the register $t1?

- lw $t1, 60($t0)
- lw 60($t0), $t1
- sw $t1, 60($t0)
- sw 60($t0), $t1

Clear my choice

Which of the following instructions is a J-format instruction?

- a. jal
- b. bne
- c. slt
- d. addi

Clear my choice

Assuming the content of $s5 0000000000001010, what would be the de

sll $t2,$s5, 1

- a. 40
- b. 10
- c. 20
- d. 80

Clear my choice

In IEEE754 format, the sign bit is followed by string of digits called as

Which of the following is **not true** about Endianness?

- a. MIPS is little Endian
- b. Most significant byte starts at the smallest address
- c. Little Endian vs Big Endian
- d. Endianness specifies the order of accessing the data

Assume the values stored in registers $s0 is zero and the value stored in $s1 is 19, what execution of the following instruction?

addi $s0, $s1, 11

- 11110 in $s0 and 11110 in $s1
- 0 in $s0 and 10011 in $s1
- 10011 in $s0 and 10011 in $s1
- **11110 in $s0 and 10011 in $s1**

Clear my choice

Which of the following instructions performs the instruction move $t1, $t2?

- a. add $t1, $t2, $t1
- b. add $t2, $zero, $t1
- c. add $t1, $zero, $t2
- d. lui $t1, 0

Clear my choice

A 32 bit address generates an address space of _____ locations.

Select one:

- 1024
- 16,777,216
- 4 gibibytes
- 2048
- 2^{48}

Clear my choice

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Which of the following is **not** an I-type instruction?

Select one:

- a. sll $t1, $t2, 3
- b. slti $t1, $t2, 5
- c. addi $t1, $t2, 3
- d. bne $t1, $t0, Label

Clear my choice

The two's complement of 101110100 is represent

a. 101110100

b. 010001100

c. 010001100

d. 101110101

Which method of representation has **one** representation for '0'?

Select one:

- a. Sign Magnitude
- b. 2's complement
- c. 1's complement
- d. None of the mentioned

Clear my choice

Which representation is most efficient to perform arithmetic operations architecture?

Select one:

- a. 2's complement
- b. 1's complement
- c. None of the mentioned