○ d. 233

Clear my choice

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Flag
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Which of the following is an R-type instruction?

Select one:

○ andi $t0,$t1, 7

● add $t0, $t0, $t1

○ jr $ra

○ addi $t1, $t2, 3

Clear my choice

Question 18

Not yet
answered

How many bits does the single space in the MEMORY o

○ a. 16 bits

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Which of the following is an R-type instruction?

Select one:

- add $t0, $t0, $t1
- jr $ra
- andi $t0,$t1, 7
- addi $t1, $t2, 3

I-format and J-format instructions both accomodate an immediate value.
What is the maximum number of bits that can be specified for each value?

- a. 20 for I, 25 for J
- b. 28 for I, 28 for J
- c. 16 for I, 26 for J
- d. 26 for I, 26 for J

addi $t1, $t2, 3

Clear my choice

I-format and J-format instructions both accomodate an immediate value to be specified. What is the maximum number of bits that can be specified for each instruction format?

a. 20 for I, 26 for J

b. 28 for I, 28 for J

c. 16 for I, 28 for J

d. 16 for I, 26 for J

The MIPS instruction for j 15 is:

Name	Format	
		6 bits

7 8 9

13 14 15

19 20 21

25

Finish attempt

Time left 0:29

There are 3 basic instruction formats in the MIPS instruction set architecture. They are:

R	opcode	rs	rt	rd	shamt	funct
I	opcode	rs	rt	immediate		
J	opcode	target address				

What aspect of the instruction's machine language encoding distinguishes between these different formats?

- a. The presence or absence of the constant field in the instruction
- b. The number of register fields in the instruction
- c. Either appending an "i" to the end of a normal instruction or beginning the instruction with a "j"
- d. None of the above

24 Let's say we have an Array with 64 integer elements. The address of the first

on 13

The MIPS instruction for j 15 is:

Name	Format	
		6 bits
		op
j	J	2
jal	J	3

a. 000010 00000000000000000000001111

b. 000011 00000000000000000000001111

c. 000011 00000000000000000000001110

d. 000010 00000000000000000000001110

uestion 14

A 32 bit address generates an address space of _____ locations.

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Question 25

Not yet answered

Marked out of 2

Flag question

The fastest data access is provided using _____

Select one:

- a. Caches
- b. DRAM's
- c. SRAM's
- d. Registers

Previous page

Previous activity

◀ Assignment2 (Deadline for submission 28/4/2021)

Jump to...

8086 assembly

Type here to search

Assuming the content of $s5 0000000000001010, what woul
executing this instruction?

sll $t2,$s5, 1

- a. 20
- b. 80
- c. 10
- d. 40

Clear my choice

5

The instruction used to cause unconditional jump is _____

Select one:

- a. j address
- b. move address
- c. beq
- d. bne

search

b. 80

c. 10

d. 40

Clear my choice

The instruction used to cause unconditional jump is _____

Select one:

a. j address

b. move address

c. beq

d. bne

Clear my choice

- 2048
- 2^{48}

Clear my choice

The complement of 5_8 equals to 2

Select one:

- True
- False

Assuming the content of $s5 0000000000001010, what wo
executing this instruction?

sll $t2,$s5, 1

- a. 20
- b. 80

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The fastest data access is provided using _____

Select one:

- a. Registers
- b. SRAM's
- c. DRAM's
- d. Caches

Clear my choice

22

A 32 bit address generates an address space of _____ locations.

earch

b. SRAM's

c. DRAM's

d. Caches

Clear my choice

A 32 bit address generates an address space of _____ locations.

Select one:

- 4 gibibytes
- 16,777,216
- 1024
- 2048
- 2^{48}

Clear my choice

23 The complement of 5_8 equals to 2

- addi $t1, $t2, 3
- andi $t0,$t1, 7
- jr $ra

Clear my choice

Which of the following instruction-format pairings is **incorrect**?

- a. j - J-format
- b. slt- R-format
- c. lw- R-format
- d. addi- I-format

Clear my choice

Select one:

- a. Mantissa
- b. Significant
- c. Determinant
- d. Exponent

Clear my choice

Which of the following is an R-type instruction?

Select one:

- add $t0, $t0, $t1
- addi $t1, $t2, 3
- andi $t0,$t1, 7
- jr $ra

Clear my choice

Which of the following instruction-format codings is incorrect?

d. 000011 00000000000000000000001110

Clear my choice

In IEEE754 format, the sign bit is followed by string of digits called

Select one:

a. Mantissa

b. Significant

c. Determinant

d. Exponent

Clear my choice

Which of the following is an R - type instruction?

Select one:

add $t0, $t0, $t1

addi $t1, $t2, 3

The MIPS instruction for j 15 is:

Name	Format	
		6 bits
		op
j	J	2
jal	J	3

- a. 000010 00000000000000000000001110
- b. 000010 00000000000000000000001111
- c. 000011 00000000000000000000001111
- d. 000011 00000000000000000000001110

Clear my choice

In IEEE754 format, the sign bit is followed by string of digits called as _ _

Select one:

a. Mantissa

d. 2 bytes

Clear my choice

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Flag
uestion

When we want to load a register with 32 bits value, the assembler actually needs to perform two MIPS instructions. The first of these two instructions is **lui** (load upper immediate), which takes the upper 16 bits provided and stores them as the upper 16 bits of the register. What is the other command?

a. ori

b. and

c. addi

d. add

Clear my choice

Question 18
Not yet answered
Marked out of 2
Flag question

The instruction used to cause unconditional jump is _____

Select one:

a. bne

b. j address

c. move address

b. 2's complement

c. 1's complement

d. None of the mentioned

Clear my choice

Which representation is most efficient to perform arithmetic operations on signe architecture?

Select one:

a. 2's complement

b. 1's complement

c. None of the mentioned

d. Sign-magnitude

Clear my choice

In IEEE754 format, the size of the mantissa (fractional part) is

Select one:

Question 21

Not yet answered

Marked out of 2

Flag question

Which method of representation has **one** representation for '0'?

Select one:

- a. Sign Magnitude
- b. 2's complement
- c. 1's complement
- d. None of the mentioned

Clear my choice

Question 22

Not yet answered

Marked out of

Let's say we have an Array with 64 integer elements. The address of the first element in the array is stored
following moves the data from Array[60] into the register $t1?

- lw $t1, 60($t0)

d. beq

Clear my choice

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lag
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Assume the values stored in registers $s0 is zero and the value stored in $s1 is 19, what would be stored in $s0 and $s1 after the execution of the following instruction?

addi $s0, $s1, 11

- 11110 in $s0 and 11110 in $s1
- 0 in $s0 and 10011 in $s1
- 10011 in $s0 and 10011 in $s1
- 11110 in $s0 and 10011 in $s1

Clear my choice

Question 20
Not yet answered
Marked out of 2
Flag

The fastest data access is provided using _____

Select one:

a. Registers

b. DRAM's

c. None of the mentioned

d. Sign-magnitude

Clear my choice

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Flag

uestion

In IEEE754 format, the size of the mantissa (fractional part) is _____

Select one:

a. 23 bit

b. 8 bit

c. 64 bit

d. 32 bit

Clear my choice

0 0 0 0 in 4 bits excess biased representation

Clear my choice

9's complement of 23456 is _____

- a. 54321
- b. 12345
- c. 87654
- d. 76543

Clear my choice

The instruction that reads data from a register and transfers data into memory is:

- a. store




Clear my choice

14

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0 0 0 0 in 4 bits Excess Biased represents _____

- a. -8
- b. -7
- c. zero
- d. +7

Clear my choice

n 15

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The 3-bits Excess representation of zero is _____

- a. 100
- b. 000
- c. 101
- d. 111

to search

sw 60($t0), $t1

Clear my choice

Question 23

Not yet answered

Marked out of 2

Flag question

Which of the following instructions performs the instruction move $t1, $t2?

a. add $t1, $t2, $t1

b. add $t2, $zero, $t1

c. add $t1, $zero, $t2

d. lui $t1, 0

Clear my choice

Question 24

Not yet answered

A 32 bit address generates an address space of _____ locations.

Select one:

d. or

Clear my choice

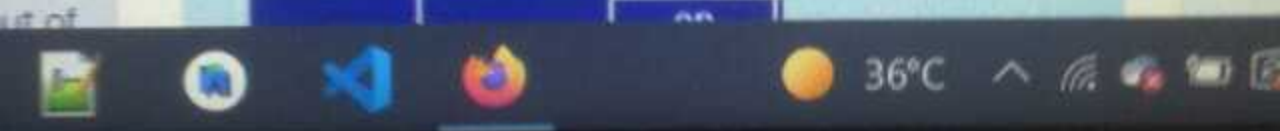
Which of the following instructions is a J-format instruction?

- a. bne
- b. slt
- c. jal
- d. addi

Clear my choice

The MIPS instruction for j 15 is:

Name	Format	
		6 bits



c. add $t1, $zero, $t2

d. lui $t1, 0

Clear my choice

Question 24

Not yet answered

Marked out of 2

Flag question

A 32 bit address generates an address space of _____ locations.

Select one:

- 1024
- 16,777,216
- 4 gibibytes
- 2048
- 2^{48}

Clear my choice

Question 25

How many bytes does the (MIPS -32) word take up?

Question 1

Answer saved

Marked out of 2

Flag question

Which representation is most efficient to perform arithmetic operations on signed numbers in MIPS architecture?

Select one:

- a. Sign-magnitude
- b. 1's complement
- c. None of the mentioned
- d. 2's complement

Clear my choice

Question 2

Answer saved

Marked out of 2

Remove flag

The product of 1101 & 1011 is _____

Select one:

- a. 10001001
- b. 11101110
- c. 10001111
- d. 10101111

Clear my choice

Question 6
Answer saved
Marked out of 2
Remove flag

How many bits does the single space in the MEMORY of 32-MIPS take up?

- a. 64 bits
- b. 8 bits
- c. 32 bits
- d. 16 bits

Clear my choice

Question 7
Answer saved
Marked out of 2
Flag question

The 9's complement of 167_{10} equals to _____

Select one:

- a. 732
- b. 233
- c. 232
- d. 832

Clear my choice

Question 8

Which of the following instructions is a J-format instruction?

d. 80

Clear my choice

Question 10

Answer saved

Marked out of 2

Remove flag

In IEEE754 format, the sign bit is followed by string of digits called as _____

Select one:

a. Exponent

b. Significant

c. Determinant

d. Mantissa

Clear my choice

Previous page

Previous activity

◄ Assignment2 (Deadline for submission 28/4/2021)

Jump to...

Ne

8086 assembly languag

Question 8

Answer saved

Marked out of 2

Flag question

Which of the following instructions is a J-format instruction?

- a. jal
- b. bne
- c. slt
- d. addi

Clear my choice

Question 9

Answer saved

Marked out of 2

Flag question

Assuming the content of $s5 0000000000001010, what would be the decimal value stored in $t2 after executing this instruction?

sll $t2,$s5, 1

- a. 40
- b. 10
- c. 20
- d. 80

Clear my choice

Question 10

In IEEE754 format, the sign bit is followed by string of digits called as _____

Question 16
Answer saved
Marked out of 2
Flag question

If a system is 64 bit machine, then the length of each word will be _____

Select one:

- a. 8 bytes
- b. 4 bytes
- c. 16 bytes
- d. 2 bytes

Clear my choice

Question 17
Answer saved
Marked out of 2
Flag question

When we want to load a register with 32 bits value, the assembler actually needs to perform two MIPS instructions. T
these two instructions is **lui** (load upper immediate), which takes the upper 16 bits provided and stores them as the
bits of the register. What is the other command?

- a. ori

Question 13

Answer saved

Marked out of 2

Flag question

In IEEE754 format, the size of the mantissa (fractional part) is _____

Select one:

- a. 23 bit
- b. 8 bit
- c. 32 bit
- d. 64 bit

Clear my choice

Question 14

Answer saved

Marked out of 2

Flag question

Which of the following instruction-format pairings is **incorrect?**

- a. addi- I-format
- b. j - J-format
- c. lw- R-format
- d. slt- R-format

Clear my choice

Question 15

Which of the following is **not** an I-type instruction?

c. lw- R-format

d. slt- R-format

Clear my choice

Question 15

Answer saved

Marked out of 2

Remove flag

Which of the following is **not** an I-type instruction?

Select one:

a. sll $t1, $t2, 3

b. slti $t1, $t2, 5

c. addi $t1, $t2, 3

d. bne $t1, $t0, Label

Clear my choice

Previous page

Previous activity

Question 19

Answer saved

Marked out of 2

Flag question

Assume the values stored in registers $s0 is zero and the value stored in $s1 is 19, what would be stored in $s0 and $s1 after the execution of the following instruction?

addi $s0, $s1, 11

- 11110 in $s0 and 11110 in $s1
- 0 in $s0 and 10011 in $s1
- 10011 in $s0 and 10011 in $s1
- 11110 in $s0 and 10011 in $s1

Clear my choice

Question 20

Answer saved

Marked out of 2

Flag question

The fastest data access is provided using _____

Select one:

- a. Registers
- b. DRAM's
- c. SRAM's
- d. Caches

Clear my choice

Question 23

Answer saved

Marked out of 2

Flag question

Which of the following instructions performs the instruction move $t1, $t2?

- a. add $t1, $t2, $t1
- b. add $t2, $zero, $t1
- c. add $t1, $zero, $t2
- d. lui $t1, 0

Clear my choice

Question 24

Answer saved

Marked out of 2

Flag question

A 32 bit address generates an address space of _____ locations.

Select one:

- 1024
- 16,777,216
- 4 gibibytes
- 2048
- 2^{48}

Clear my choice

Question 17
Answer saved
Marked out of 2
Flag question

When we want to load a register with 32 bits value, the assembler actually needs to perform two MIPS instructions. The first of these two instructions is **lui** (load upper immediate), which takes the upper 16 bits provided and stores them as the upper 16 bits of the register. What is the other command?

- a. ori
- b. and
- c. addi
- d. add

Clear my choice

Question 18
Answer saved
Marked out of 2
Flag question

The instruction used to cause unconditional jump is _____

Select one:

- a. bne
- b. j address
- c. move address
- d. beq

Question 21

Answer saved

Marked out of 2

Flag question

Which method of representation has **one** representation for '0'?

Select one:

- a. Sign Magnitude
- b. 2's complement
- c. 1's complement
- d. None of the mentioned

Clear my choice

Question 22

Answer saved

Marked out of 2

Flag question

Let's say we have an Array with 64 integer elements. The address of the first element in the array is stored in $t0. Which of the following moves the data from Array[60] into the register $t1?

- lw $t1, 60($t0)
- lw 60($t0), $t1
- sw $t1, 60($t0)
- sw 60($t0), $t1

Clear my choice

Question 23

Which of the following instructions performs the instruction move $t1, $t2?

○ 2^{48}

Clear my choice

Question 25

Answer saved

Marked out of 2

Remove flag

How many bytes does the (MIPS -32) word take up?

○ a. 8 bytes

● b. 4 bytes

○ c. 16 bytes

○ d. 1 byte

Clear my choice

Previous page

Previous activity

◀ Assignment2 (Deadline for submission

Jump to...

8086 assembly

Question 2

Not yet answered

Marked out of 1

Flag question

Using **5 bits excess** notation, how many possible combinations can you get?

- a. 16 possible combinations
- b. 32 possible combinations
- c. 5 possible combinations
- d. 25 possible combinations

Previous page

Next page

Previous activity

◀ Assignment1 (Deadline for submission 4/4/2021)

What is the purpose of address bus?

Select one:

- a. to select a specified chip
- b. to select a location within the memory
- c. to provide data to and from the chip
- d. to select a read/write cycle

Clear my choice

As soon as the first activity of an instruction is done you move it to the second activity and start the first activity of a new instruction. This is called

- a. Performance
- b. Parallelism
- c. Pipelining
- d. All of the mentioned

Clear my choice

Which of the following statements are true for von Neumann architecture?

Select one:

- a. communication among components is handled by an external bus
- b. communication among components is handled by a high-speed bus
- c. communication among components is handled by a separate bus
- d. communication among components is handled by a shared system bus

What is the purpose of address bus?

The binary coded decimal BCD representation of 356 using 4 bits for each digit is 0011 0101 0110

Select one:

- True
- False

Which of the following statements are true for von Neumann architecture?

Using 10's complement subtraction, the final result of the following subtraction is :

$$\begin{array}{r} 8 \\ -\ 2 \\ \hline \boxed{?} \end{array}$$

- a. 6
- b. 8
- c. 16
- d. 3

○ d. 3

As soon as the first activity of an instruction is done you move it to the second activity and start the first activity of a new instruction. This is called

○ a. Performance

○ b. Parallelism

● c. Pipelining

○ d. All of the mentioned

Which of the following statement is true ?

- a. Magnetic tapes offer less capacity, more access time
- b. Magnetic tapes offer large capacity and short access time
- c. Registers are fast, inexpensive, and offer large amount of capacity
- d. Registers are fast, small, and expensive

Which of the following statements are true for von Neumann architecture?

c. slt

d. addi

Clear my choice

If a system is 64 bit machine, then the length of each word

Select one:

a. 2 bytes

b. 4 bytes

c. 16 bytes

d. 8 bytes

Clear my choice

Specify the destination register in the instruction

beq $t5, $t7, 24

Which of the following instructions is a J-format instruction?

- a. jal
- b. bne
- c. slt
- d. addi

Clear my choice

If a system is 64 bit machine, then the length of each word will be

Select one:

- a. 2 bytes
- b. 4 bytes
- c. 16 bytes
- d. 8 bytes

c. Accumulator

d. Cache

Clear my choice

Which of the following is **not** an I-type instruction?

Select one:

a. sll $t1, $t2, 3

b. slti $t1, $t2, 5

c. bne $t1, $t0, Label

d. addi $t1, $t2, 3

Clear my choice

If a system is 64 bit machine, then the length of each word will be _____

Select one:

a. 16 bytes

d. xor

Clear my choice

Which of the following instruction-format pairings is **incorrect?**

a. lw- R-format

b. j - J-format

c. slt- R-format

d. addi- I-format

Clear my choice

The complement of 5_8 equals to 2

Select one:

True

False

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When we want to load a register with 32 bits value, the assembler actually needs to perform two MIPS instructions. The first of these two instructions is **lui** *(load upper immediate)*, which takes the upper 16 bits provided and stores them as the upper 16 bits of the register. What is the other command?

- a. add
- b. addi
- c. and
- d. ori

c. slt

d. addi

Clear my choice

If a system is 64 bit machine, then the length

Select one:

a. 2 bytes

b. 4 bytes

c. 16 bytes

d. 8 bytes

Clear my choice

Specify the destination register in the instruction:

beq $t6, $t7, 24

a. $t8

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Question 25

Not yet answered

Marked out of 2

Flag question

The fastest data access is provided using _____

Select one:

- a. Caches
- b. DRAM's
- c. SRAM's
- d. Registers

Previous page

Previous activity

◀ Assignment2 (Deadline for submission 28/4/2021)

Jump to...

8086 assembly

Type here to search

on 13

The MIPS instruction for j 15 is:

Name	Format	
		6 bits
		op
j	J	2
jal	J	3

a. 000010 00000000000000000000001111

b. 000011 00000000000000000000001111

c. 000011 00000000000000000000001110

d. 000010 00000000000000000000001110

uestion 14

A 32 bit address generates an address space of _____ locations.

nswer saved

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b. SRAM's

c. DRAM's

d. Caches

Clear my choice

A 32 bit address generates an address space of _____ locations.

Select one:

- 4 gibibytes
- 16,777,216
- 1024
- 2048
- 2^{48}

Clear my choice

23 The complement of 5_8 equals to 2

b. 80

c. 10

d. 40

Clear my choice

The instruction used to cause unconditional jump is _____

Select one:

a. j address

b. move address

c. beq

d. bne

Clear my choice

There are 3 basic instruction formats in the MIPS instruction set architecture. They are:

R	opcode	rs	rt	rd	shamt	funct
I	opcode	rs	rt	immediate		
J	opcode	target address				

What aspect of the instruction's machine language encoding distinguishes between these different formats?

- a. The presence or absence of the constant field in the instruction
- b. The number of register fields in the instruction
- c. Either appending an "i" to the end of a normal instruction or beginning the instruction with a "j"
- d. None of the above

24 Let's say we have an Array with 64 integer elements. The address of the first

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The fastest data access is provided using _____

Select one:

- a. Registers
- b. SRAM's
- c. DRAM's
- d. Caches

Clear my choice

A 32 bit address generates an address space of _____ locations.

- addi $t1, $t2, 3
- andi $t0,$t1, 7
- jr $ra

Clear my choice

Which of the following instruction-format pairings is **incorrect**?

- a. j - J-format
- b. slt- R-format
- c. lw- R-format
- d. addi- I-format

Clear my choice

Assuming the content of $s5 0000000000001010, what woul executing this instruction?

sll $t2,$s5, 1

- a. 20
- b. 80
- c. 10
- d. 40

Clear my choice

The instruction used to cause unconditional jump is _____

Select one:

- a. j address
- b. move address
- c. beq
- d. bne

The MIPS instruction for j 15 is:

Name	Format	
		6 bits
		op
j	J	2
jal	J	3

- a. 000010 00000000000000000000001110
- b. 000010 00000000000000000000001111
- c. 000011 00000000000000000000001111
- d. 000011 00000000000000000000001110

Clear my choice

In IEEE754 format, the sign bit is followed by string of digits called as _ _

Select one:

a. Mantissa

d. 000011 00000000000000000000001110

Clear my choice

In IEEE754 format, the sign bit is followed by string of digits called

Select one:

a. Mantissa

b. Significant

c. Determinant

d. Exponent

Clear my choice

Which of the following is an R - type instruction?

Select one:

add $t0, $t0, $t1

addi $t1, $t2, 3