

United International University (UIU)

Dept. of Computer Science & Engineering (CSE) Computer Architecture -Class Test-2

1.	Use optimized multiplication algorithm to multiply a number Y by X. Where X is (last three digit of your Student ID %15 +1) and Y is 13. Now use 4 bit architecture to design a simulator for this multiplication.	[1+1+4]
2.	Assume there is only maximum of 8 bit registers available in your processor. Now design the Hardware Diagram for this optimized multiplication algorithm.	[1+3]