
# North South University

Department of Electrical & Computer Engineering

## LAB REPORT

Course Name: digital logic design

Section: 3

Project Name: Design a pattern based digital lock system

Group Number: 3


| Group members: | | Score |
|---|---|---|
| Mohammad Olid Afzal | ID- 2011831042 | |
| Ratul Dey | ID – 2014323642 | |
| Mohamad Ashraful Islam Chowdhury | ID – 2014318642 | |
| Ferdous Reza Niloy | ID- 2021281642 | |
| Ratul Bhattacharjee | ID- 2012996642 | |

***Project Contributions:***

1. Mohamad Olid Afzal

   ID- 2011831042

   Work: 20% (4bit Magnitude Comparator,  integration of pattern checker)

2.Ratul Dey

   ID- 2014323642

   Work: 15% (Decimal to BCD encoder and right shift register

3. Mohamad Ashraful Islam Chowdhury

   ID- 2014318642

   Work: 15% (7 Segment Display)

4. Ferdous Reza Niloy

   ID- 2021281642

   Work: 30% (Main circuit, pattern checker, clock multiplier, Enabler, 4 bit memory block)

5.Ratul Bhattacharjee

   ID- 2012996642

   Work: 20% (Decimal to excess-1, BCD to excess-11 , 7 segment display)

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## Objectives:

**Input:** The users will be provided with a keypad for giving input to the system.

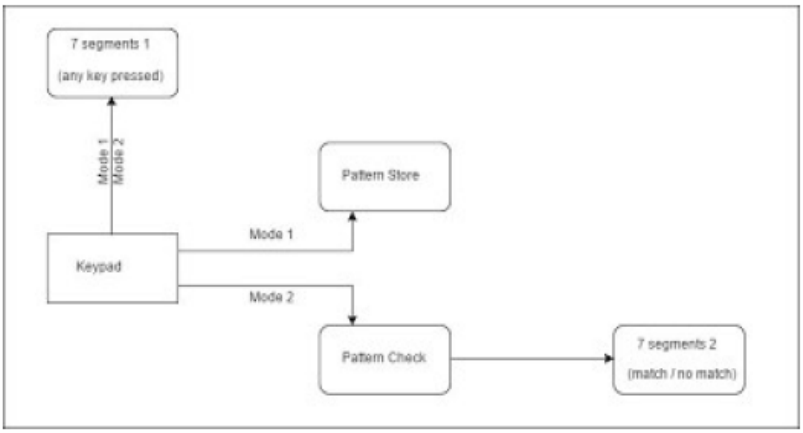
**Output :** There will be two types of 7 segments.

7 segment 1: Any input given through keypad will be displayed here.

7 segment 2: If the pattern is correct the result will be displayed in this 7 segment display. Result can be just a letter printed on the 7 segment (O/N).

**Modes:** A user will have two modes to operate the lock. In mode 1, the user can store a specific pattern. In mode 2, user can input a pattern that will be matched with stored pattern. Mode 1 is an advanced requirement and should be attempted only when mode 2 is complete. Mode 2 is the minimum requirement of the project.

**Sample pattern:** The pattern will be fixed for those completing only mode 1. It will consist of the 5 digits in following sequence - sec. no followed by group no and last 3 digits of ID. Say, If you are from Sec 5, Group 4 with an ID 13306996042 the fixed pattern will be 5 4 0 4 2. If different group members have different last 3 digits, you can pick one of them.




Block Diagram of the System

***Circuits:***

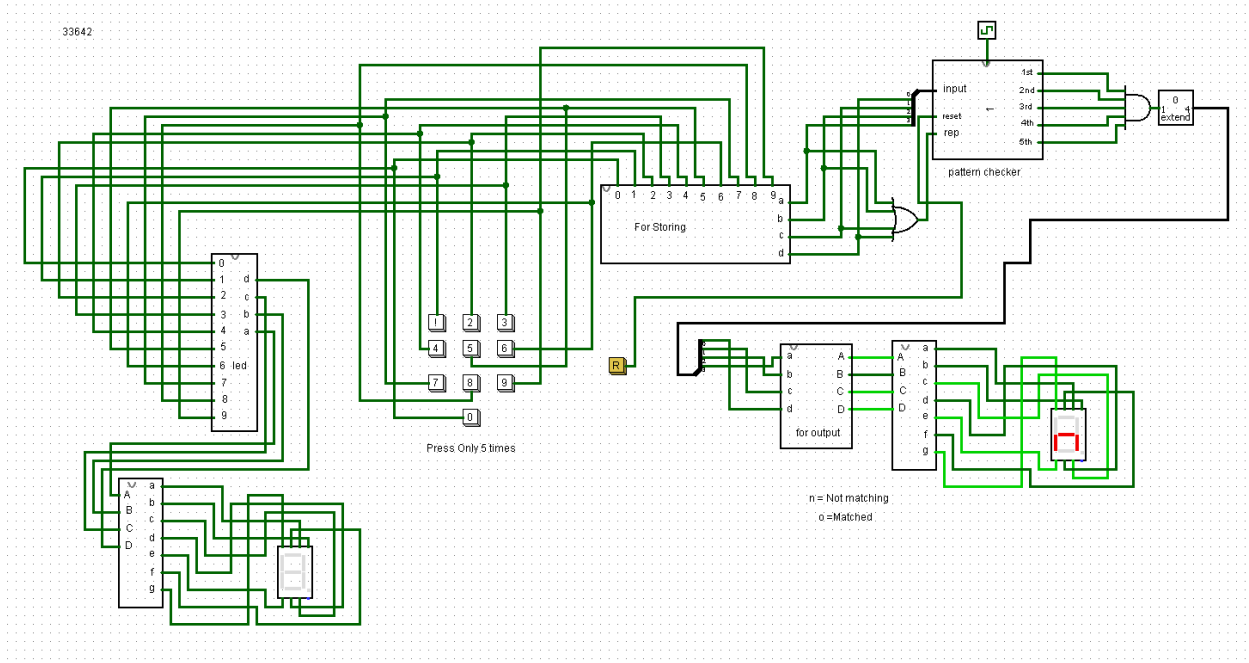



Figure: Main circuit

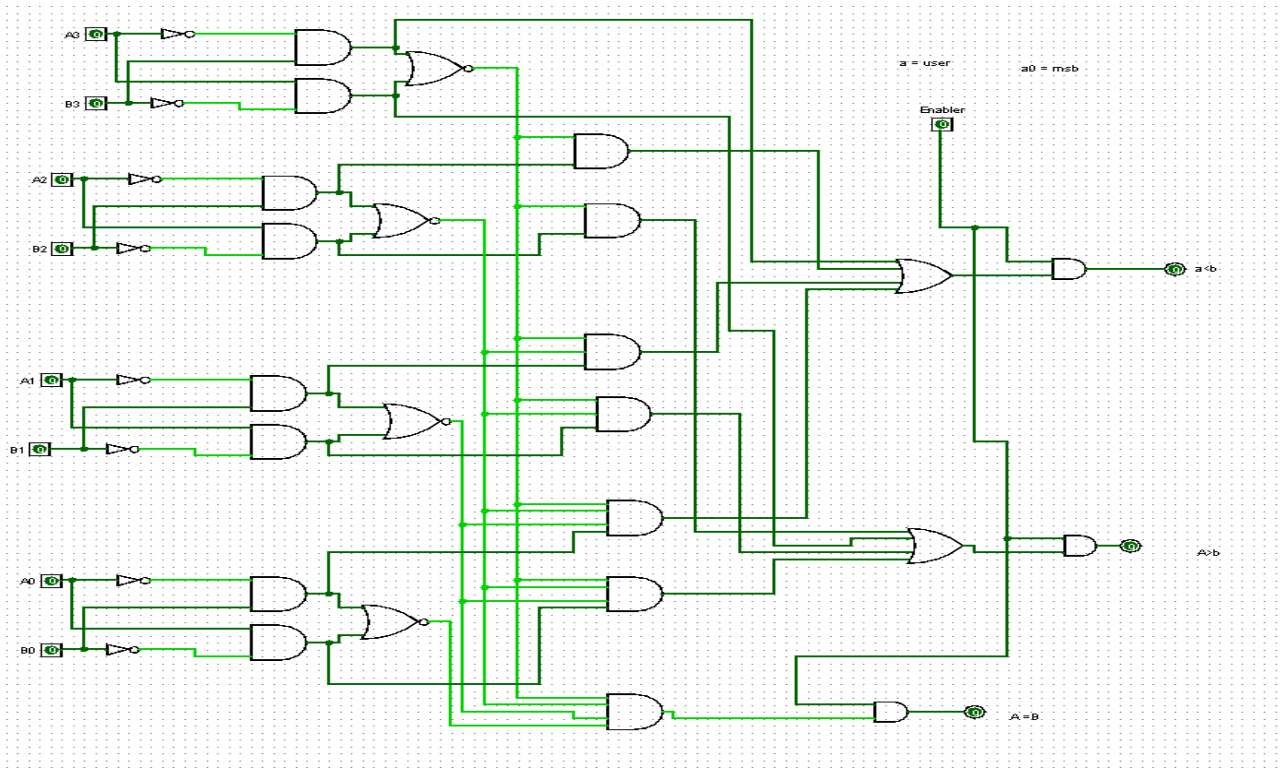
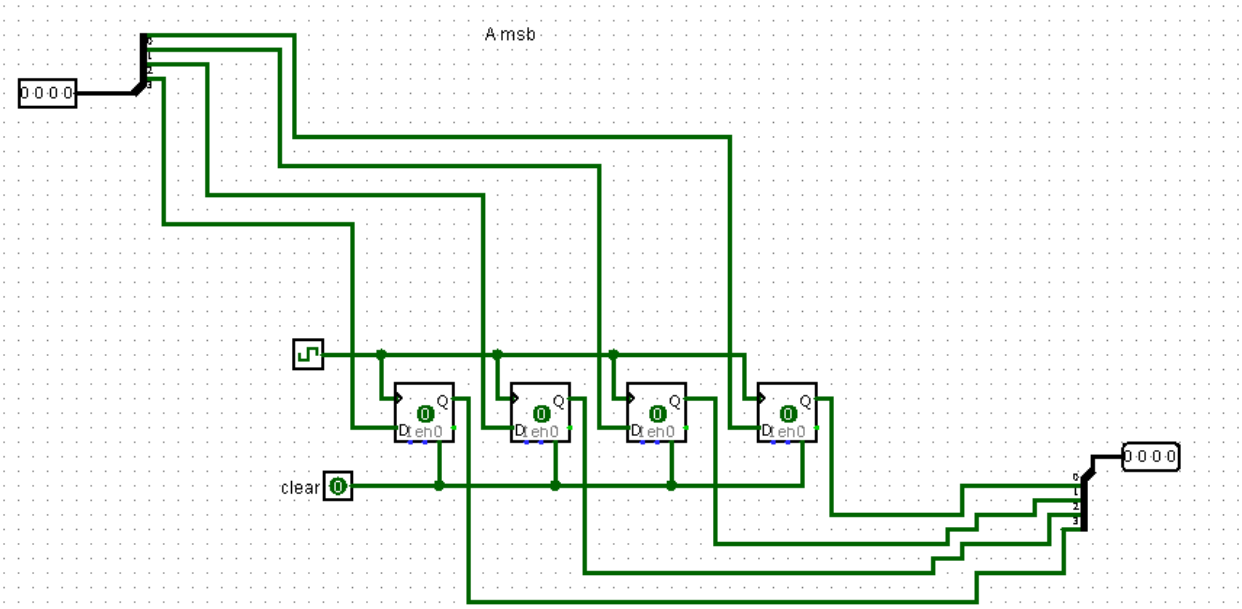
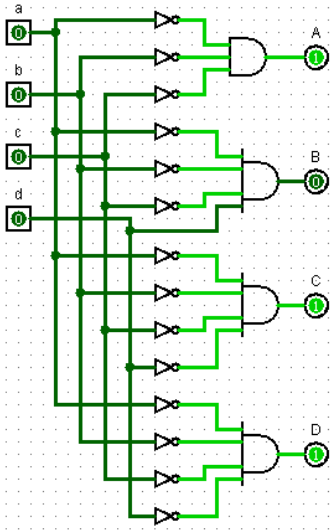



Figure: 4bit magnitude comparator




4 bit memory block (Modified right Shift register)

A:a = msb




to show output in LED

Figure:  bcd to excess 11

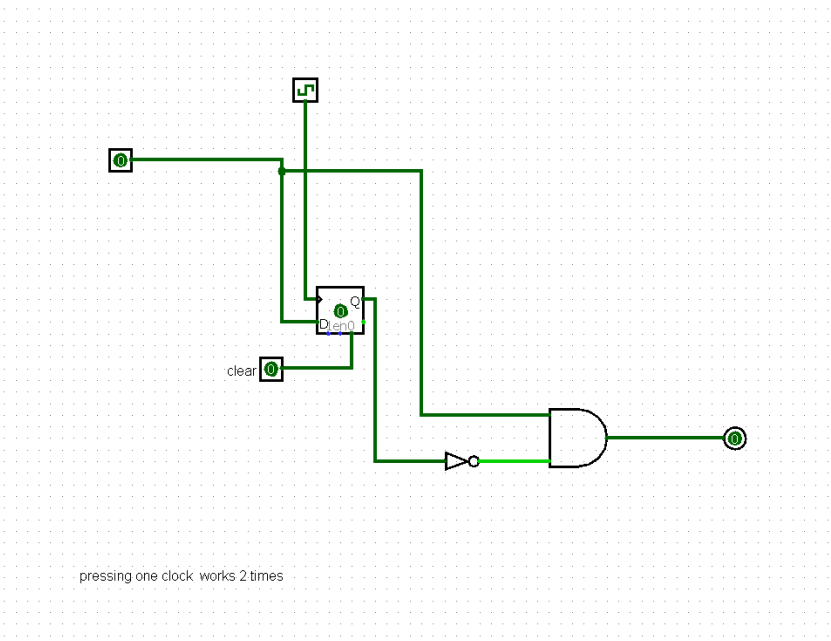



Figure:  Clock multiplier

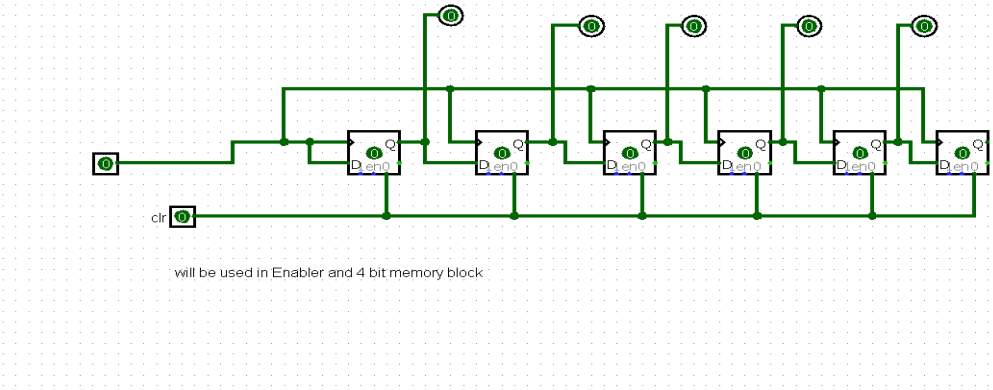



Figure:  Right shift register

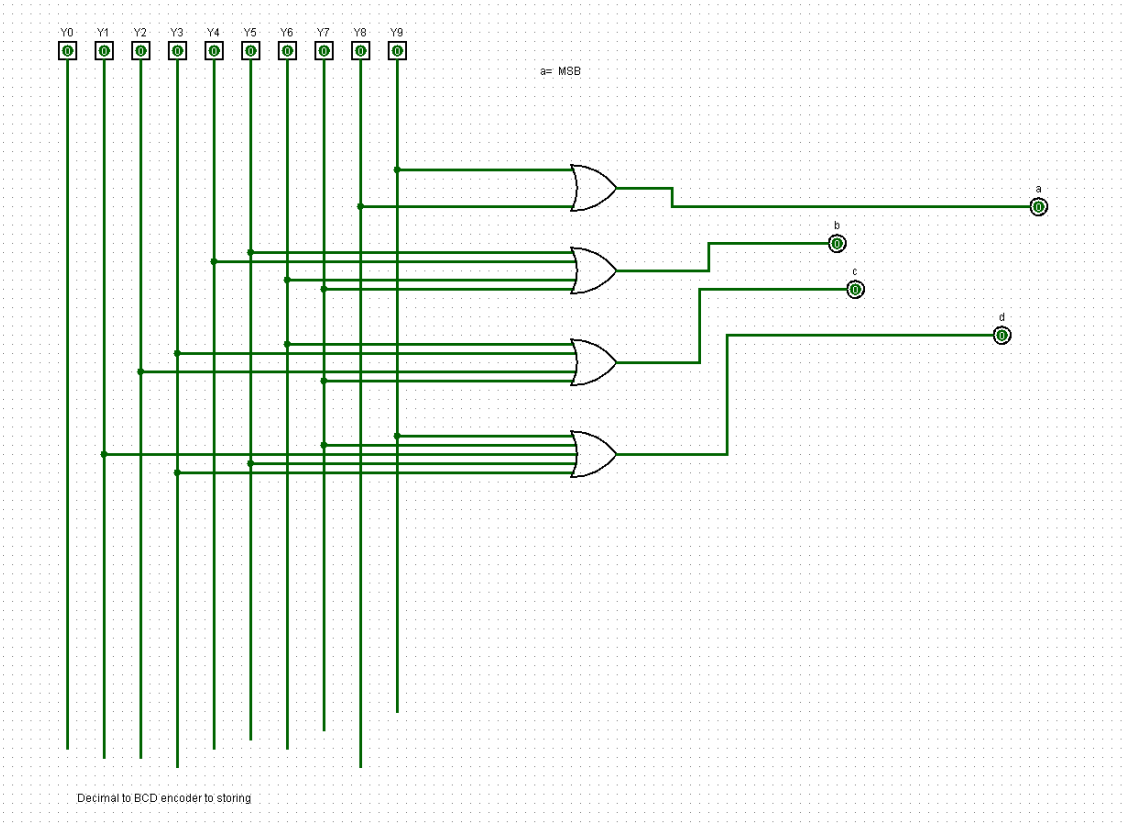



Figure: Decimal to bcd

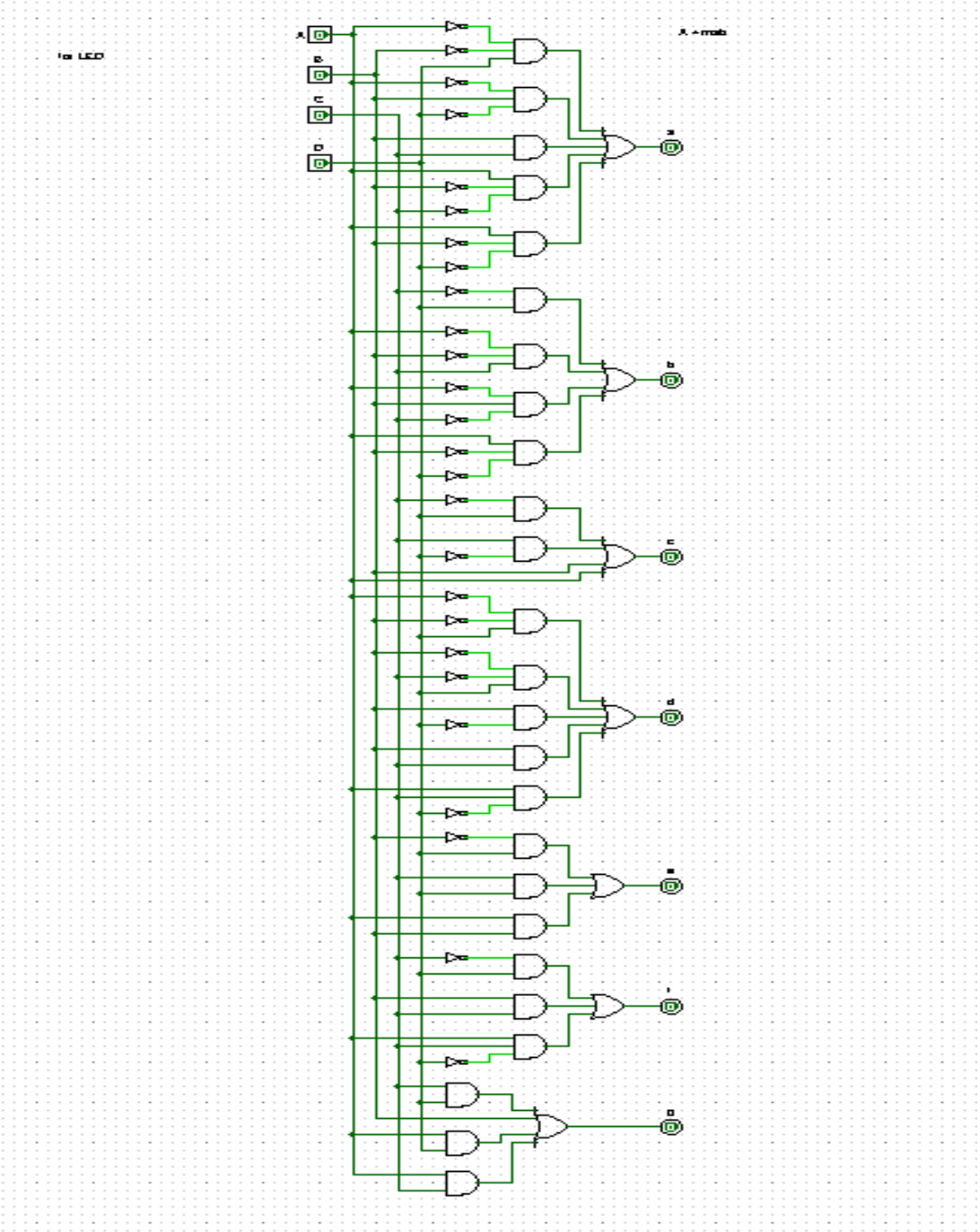


Figure:  7 segment display

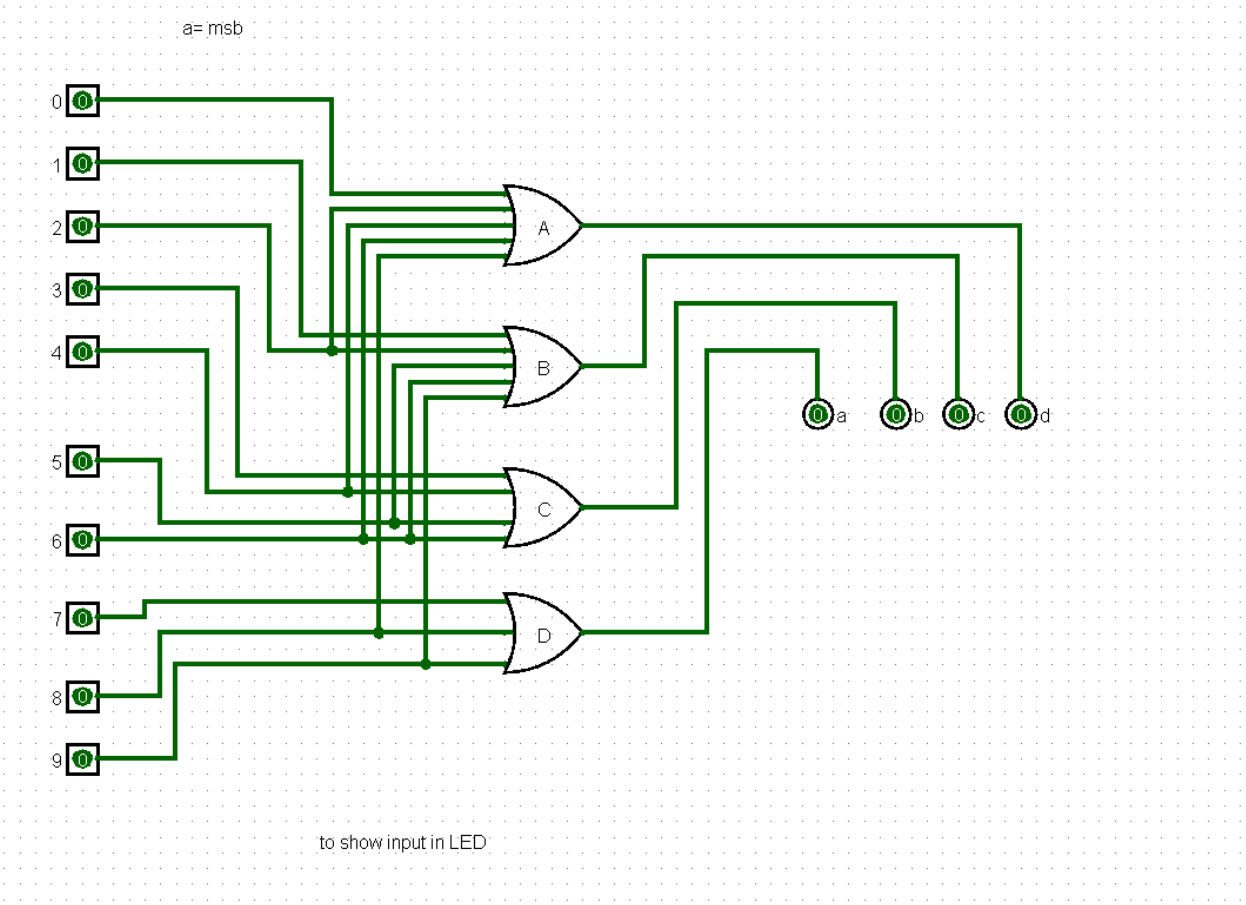



Figure: Decimal to excess 1

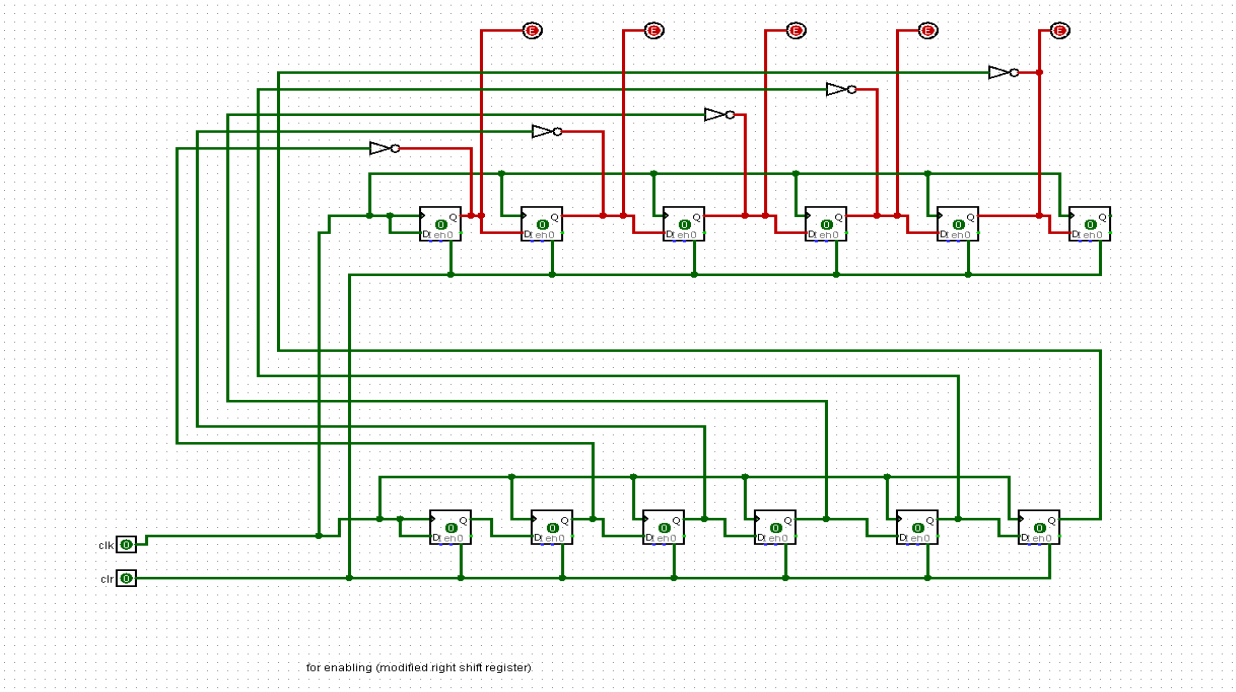



Figure: Enabler

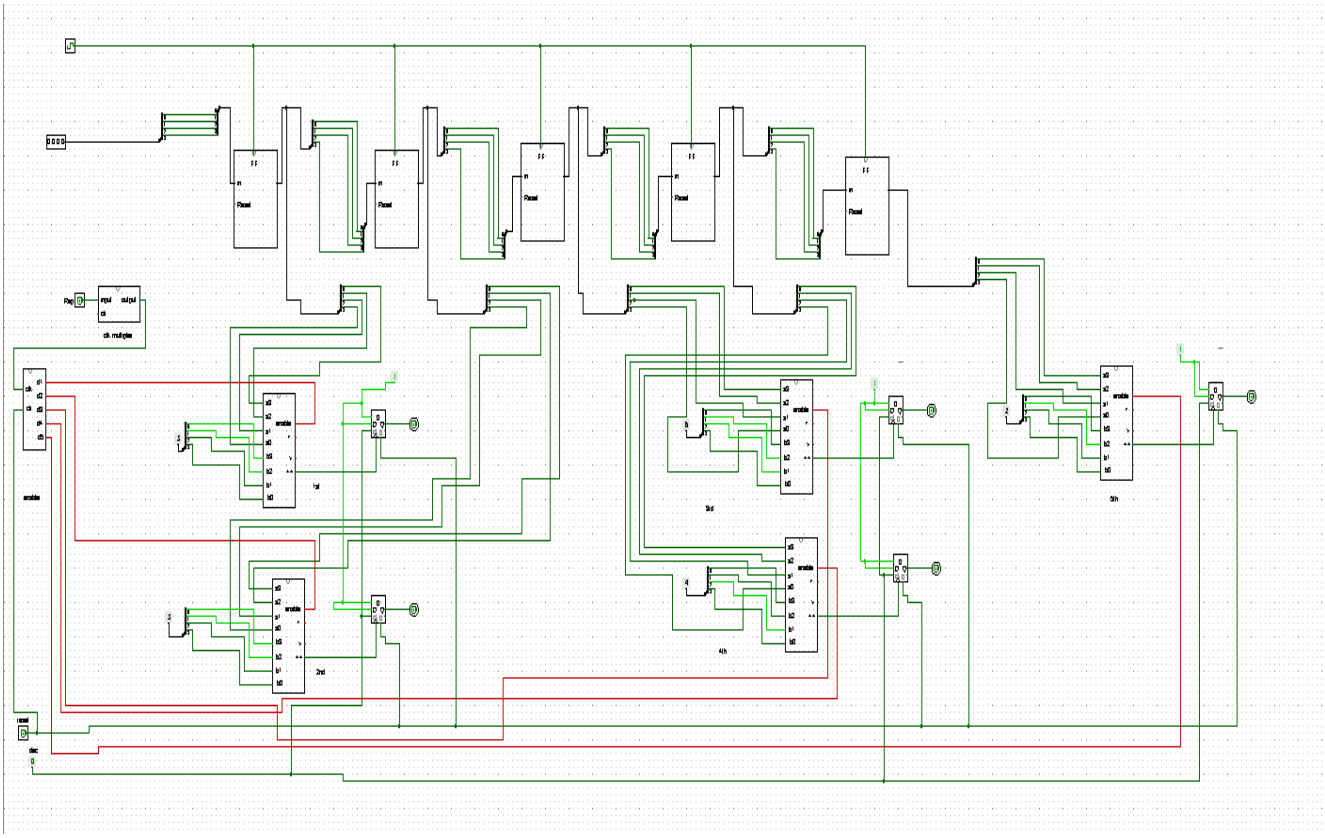
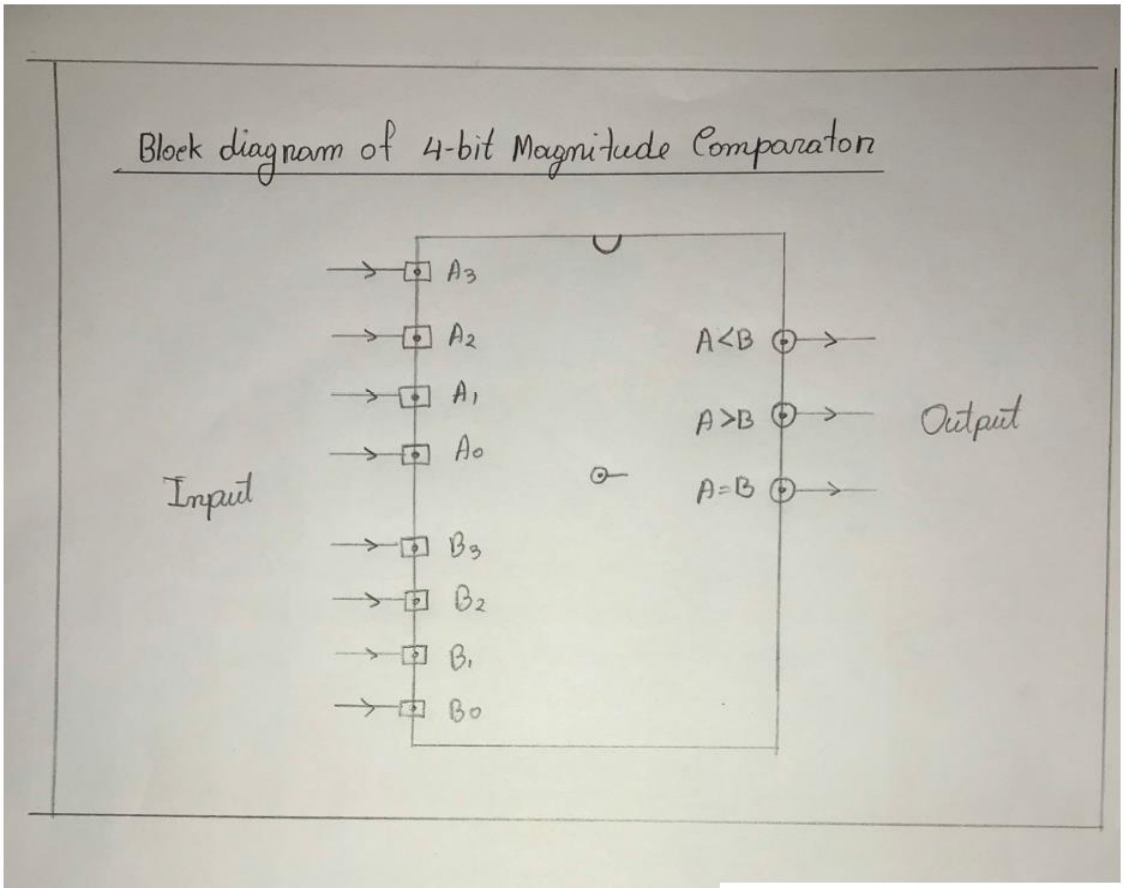


Figure: Pattern checker

**Data tables:**


Block diagram of 4-bit Magnitude Comparator
A3
A2
A1
A0
B3
B2
B1
B0
Input
A<B
A>B
A=B
Output

## Truth Table of 4-bit Magnitude Comparator

| Inputs | | | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | A<B | A>B | A=B |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| ⋮ | | | ⋮ | | ⋮ | | | ⋮ | | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

## Functions of 4-bit Magnitude Comparator

$A = A_3\ A_2\ A_1\ A_0$

$B = B_3\ B_2\ B_1\ B_0$

if $A < B \rightarrow A_3 < B_3$ $\quad [A_3 = 0, B_3 = 1]$

$\rightarrow A_3 = B_3,\ A_2 < B_2$

$\rightarrow A_3 = B_3,\ A_2 = B_2,\ A_1 < B_1$

$\rightarrow A_3 = B_3,\ A_2 = B_2,\ A_1 = B_1,\ A_0 < B_0$

$\therefore A < B = \bar{A}_3 B_3 + x_3 \bar{A}_2 B_2 + x_3 x_2 \bar{A}_1 B_1 + x_3 x_2 x_1 \bar{A}_0 B_0$

$$\begin{bmatrix} x_3 = \bar{A}_3 B_3 \\ x_2 = \bar{A}_2 B_2 \\ x_1 = \bar{A}_1 B_1 \end{bmatrix}$$

if $A > B \rightarrow A_3 > B_3$ $\quad [A_3 = 1, B_3 = 0]$

$\rightarrow A_3 = B_3,\ A_2 > B_2$

$\rightarrow A_3 = B_3,\ A_2 = B_2,\ A_1 > B_1$

$\rightarrow A_3 = B_3,\ A_2 = B_2,\ A_1 = B_1,\ A_0 > B_0$

$\therefore A > B = A_3 \bar{B}_3 + x_3 A_2 \bar{B}_2 + x_3 x_2 A_1 \bar{B}_1 + x_3 x_2 x_1 A_0 \bar{B}_0$

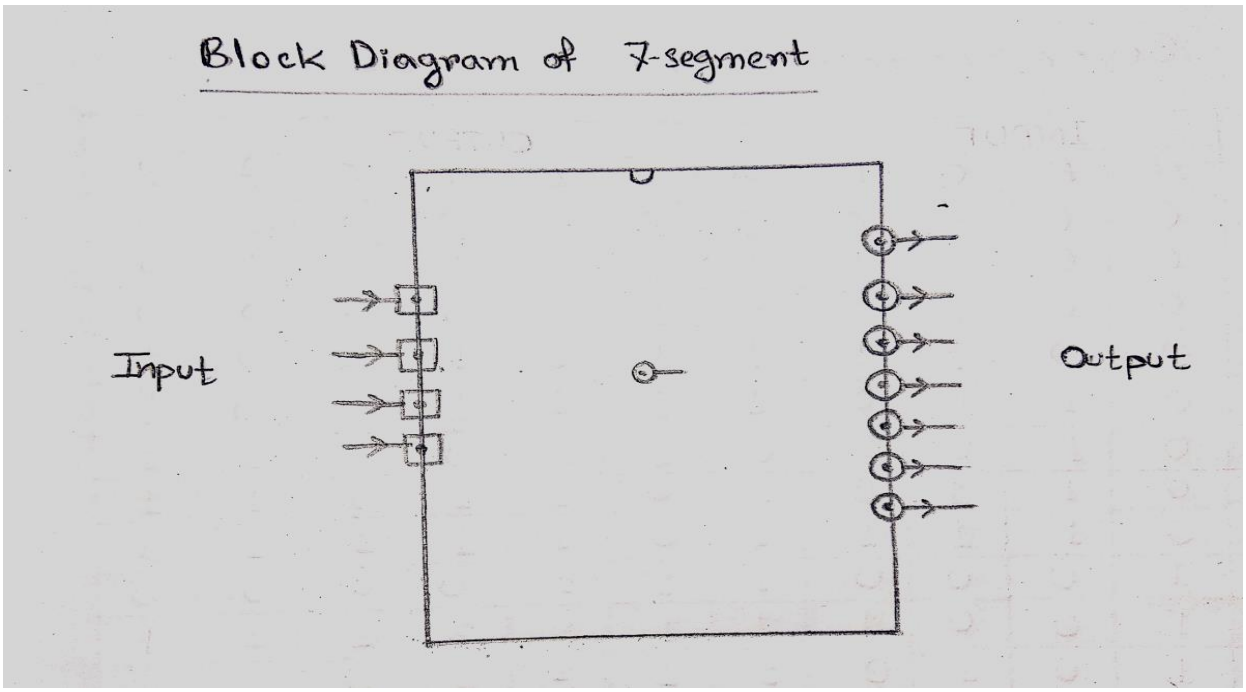
$$\begin{bmatrix} x_3 = A_3 \bar{B}_3 \\ x_2 = A_2 \bar{B}_2 \\ x_1 = A_1 \bar{B}_1 \end{bmatrix}$$

and if $A = B \rightarrow A_3 = B_3,\ A_2 = B_2,\ A_1 = B_1,\ A_0 = B_0$

$\rightarrow x_3 + x_2 + x_1 + x_0$

$$\begin{bmatrix} x_3 \Rightarrow A_3 = B_3 \\ x_2 \Rightarrow A_2 = B_2 \\ x_1 \Rightarrow x_1 = y_2 \\ x_0 \Rightarrow y_0 = x_0 \end{bmatrix}$$

## Block Diagram of 7-segment




## Seven Segment Decoder Truth Table

| | INPUT | | | | OUTPUT | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LED | A | B | C | D | a | b | c | d | e | f | g |
| NULL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 7 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 10 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 11 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 12 | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X |
| 13 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X |
| 14 | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X |

# Karnaugh Maps Simplification

| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 1 | 0 | 1 | 1 |
| 11 | 0 | X | X | X |
| 10 | 1 | 1 | 0 | 1 |

a= A'B'D + A'BD' + AB'C' + AB'D'

| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 1 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 0 | X | X | X |
| 10 | 1 | 0 | 0 | 1 |

b= C'D + A'B'C + A'BC' + AB'D'

| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 0 | 1 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | X | X | X |
| 10 | 1 | 1 | 1 | 1 |

c = C'D + CD' + B + A

| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 1 | 0 | 1 | 1 |
| 11 | 1 | X | X | X |
| 10 | 0 | 1 | 0 | 1 |

d = A'B'D + B'C'D + BD' + BC + ACD'

| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 1 | X | X | X |
| 10 | 0 | 1 | 1 | 0 |

$e = B'D + CD + AB$

| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 0 | 0 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | 0 | X | X | X |
| 10 | 0 | 1 | 0 | 1 |

$f = C'D + BC + ACD'$

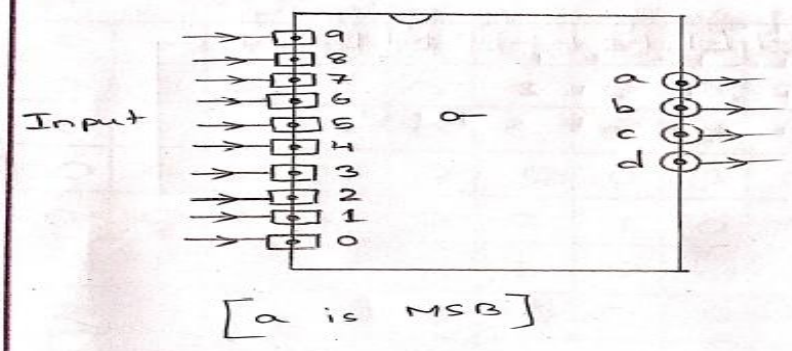
| AB/CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 0 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | X | X | X |
| 10 | 0 | 1 | 1 | 1 |

$g = CD + B + AD + AC$

## Truth table of Decimal to BCD encoder :-

| Inputs | | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | a | b | c | d |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

## Block diagram of Decimal to BCD encoder




[a is MSB]

## Expression of a, b, c, d :-

$a = 9 + 8$

$b = 7 + 6 + 5 + 4$

$c = 7 + 6 + 3 + 2$

$d = 9 + 7 + 5 + 3 + 1$

Truth table of Decimal to BCD - excess - 1.

| | | BCD Excess - 1 | | | |
|---|---|---|---|---|---|
| Decimal | BCD | $B_3$ | $B_2$ | $B_1$ | $B_0$ |
| 0 | 0000 | 0 | 0 | 0 | 1 |
| 1 | 0001 | 0 | 0 | 1 | 0 |
| 2 | 0010 | 0 | 0 | 1 | 1 |
| 3 | 0011 | 0 | 1 | 0 | 0 |
| 4 | 0100 | 0 | 1 | 0 | 1 |
| 5 | 0101 | 0 | 1 | 1 | 0 |
| 6 | 0110 | 0 | 1 | 1 | 1 |
| 7 | 0111 | 1 | 0 | 0 | 0 |
| 8 | 1000 | 1 | 0 | 0 | 1 |
| 9 | 1001 | 1 | 0 | 1 | 0 |

Expression for Circuit :

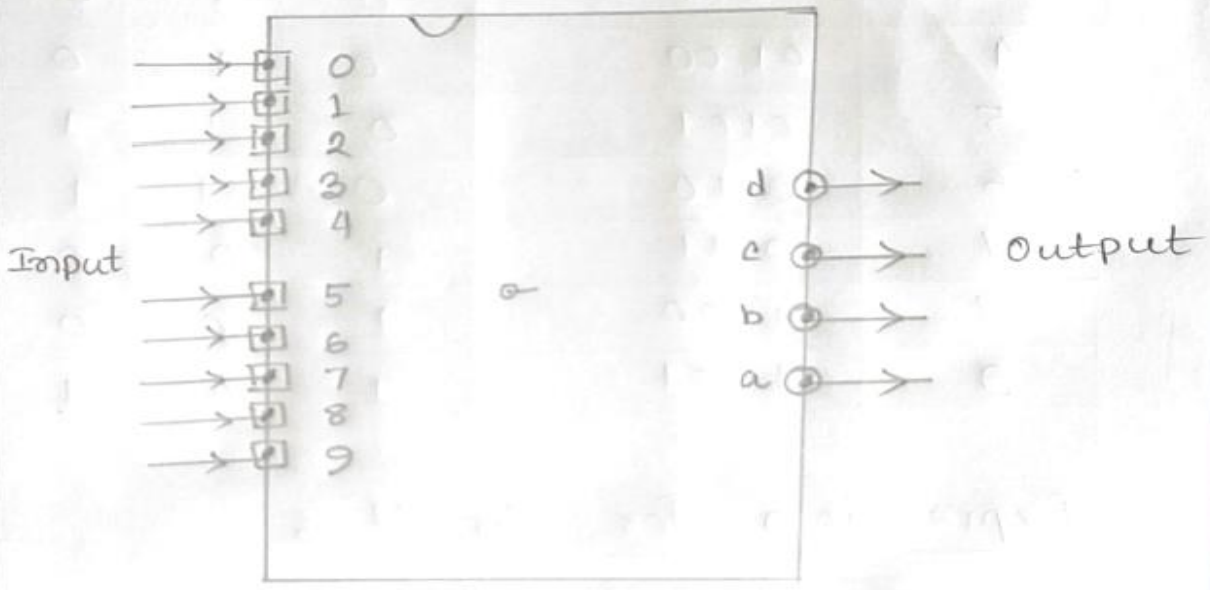
$B_0 = 0 + 2 + 4 + 6 + 8$

$B_1 = 1 + 2 + 5 + 6 + 9$

$B_2 = 3 + 4 + 5 + 6$

$B_3 = 7 + 8 + 9$

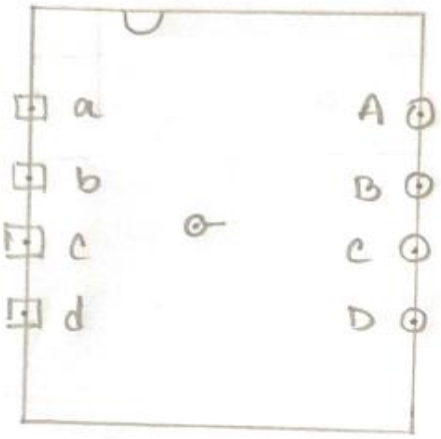
## Block diagram of Decimal to BCD Excess – 1 :




[Here, d is the MSB]

## Block Diagram:

A msb . a msb




Block Diagram of BCD to BCD excess 11

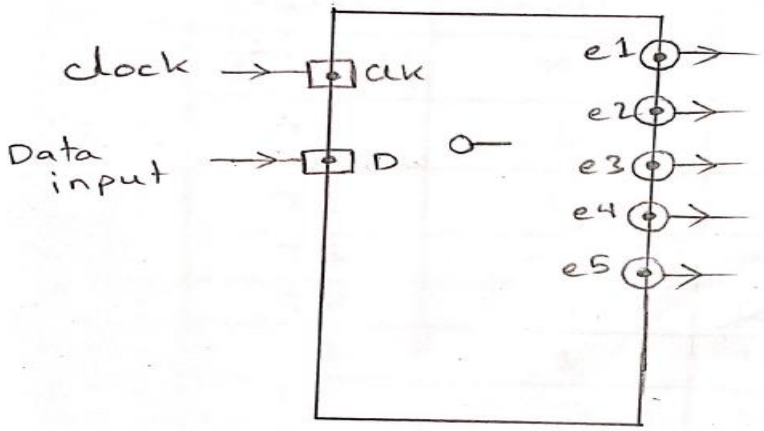
## BCD to BCD Excess-11

| Decimal | BCD | BCD Excess-11 | | | |
|---|---|---|---|---|---|
| | | B3 | B2 | B1 | B0 |
| 0 | 0 0 0 0 | 1 | 0 | 1 | 1 |
| 1 | 0 0 0 1 | 1 | 1 | 0 | 0 |

## Right Shifter using D flip-flops :

| States | Input | Output |
|---|---|---|
| Initial state | x | xxxxxx |
| T1 | 1 | 1xxxxx |
| T2 | 0 | 01xxxx |
| T3 | 1 | 101xxx |
| T4 | 0 | 0101xx |
| T5 | 1 | 10101x |
| T6 | 0 | 010101 |

## Block diagram for Right Shift register




right shift register