Block diagram for Right Shift register

clock → □ clk

Data input → □ D

e1
e2
e3
e4
e5
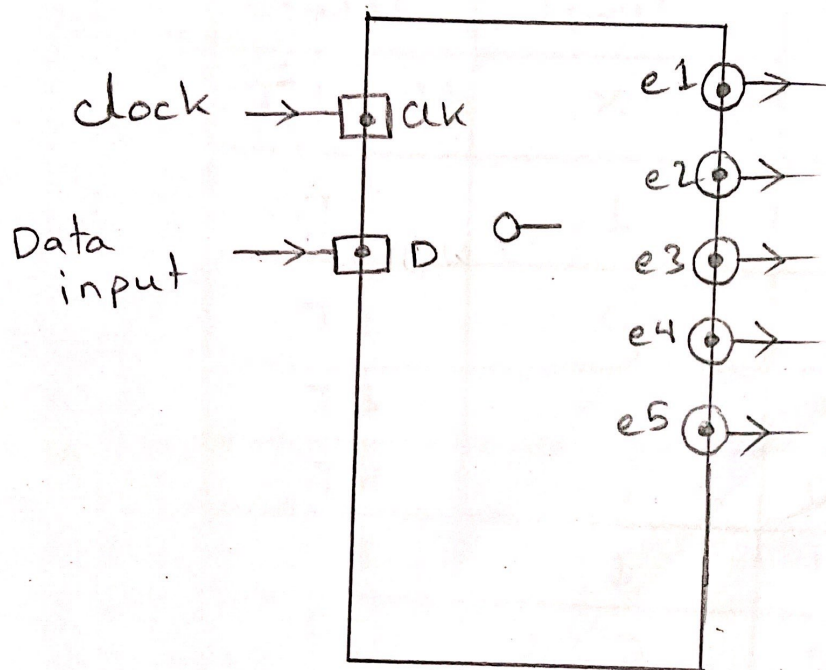
right shift register

Right shifter using D flip-flops:

States	Input	Output
Initial state	X	XXXXXX
T1	1	1XXXXX
T2	0	01XXXX
T3	1	101XXX
T4	0	0101XX
T5	1	10101X
T6	0	010101