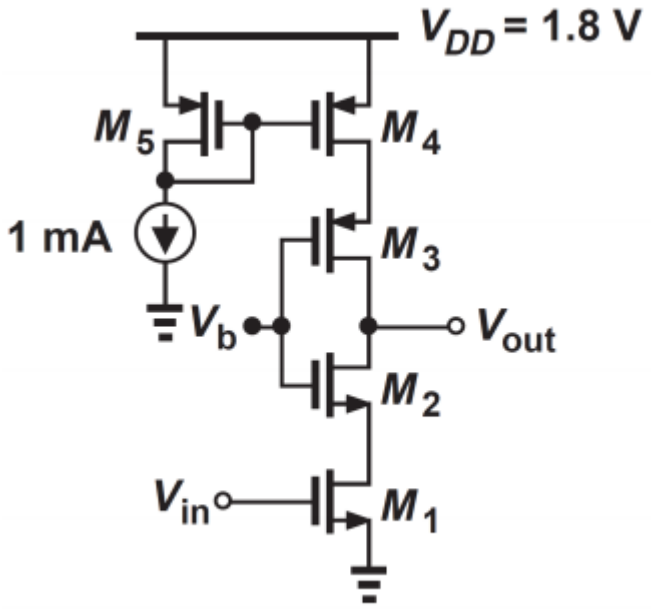
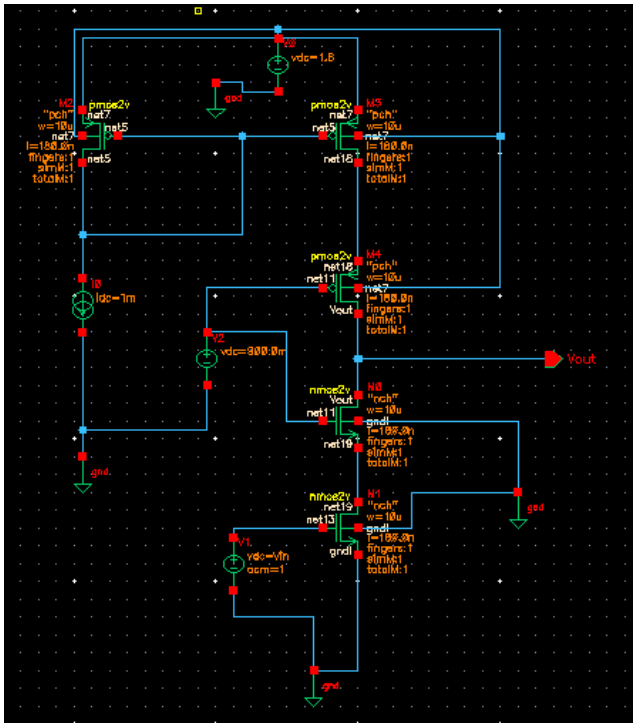
Analogue Integrated Circuits Report

Lab 3



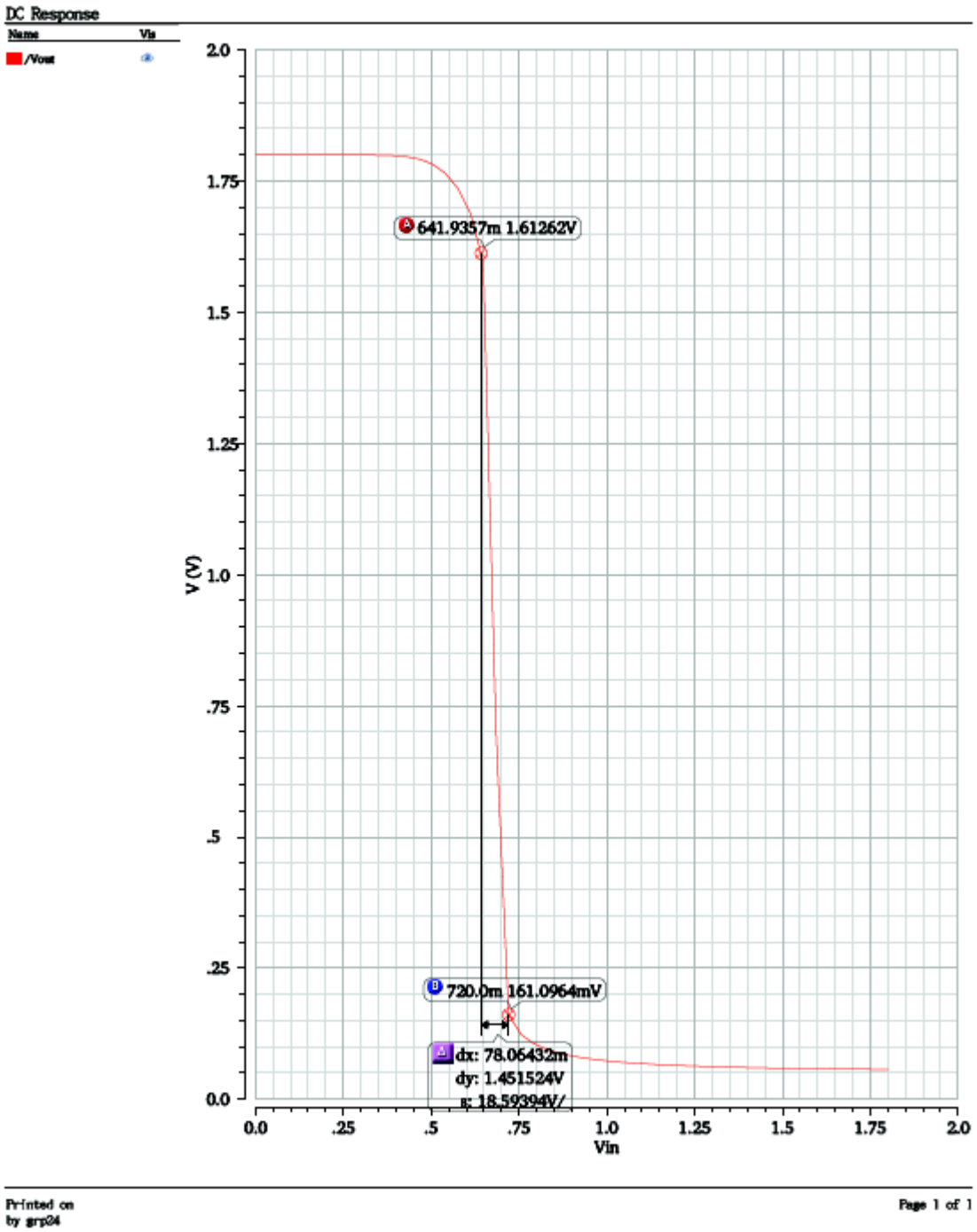
We were told to analyse the DC gain of the following circuit for DC voltages from 0-1.8V. We set each of the bulks of the NMOS transistors to ground and the bulks of the PMOS transistor to Vdd=1.8V. All the transistors had a channel width of 10µm and a channel length of 0.18µm. Our Vb was also set to a voltage of 0.9V. All transistors used were based on TSMC 180nm technology.

Our circuit was set up in cadence as shown.



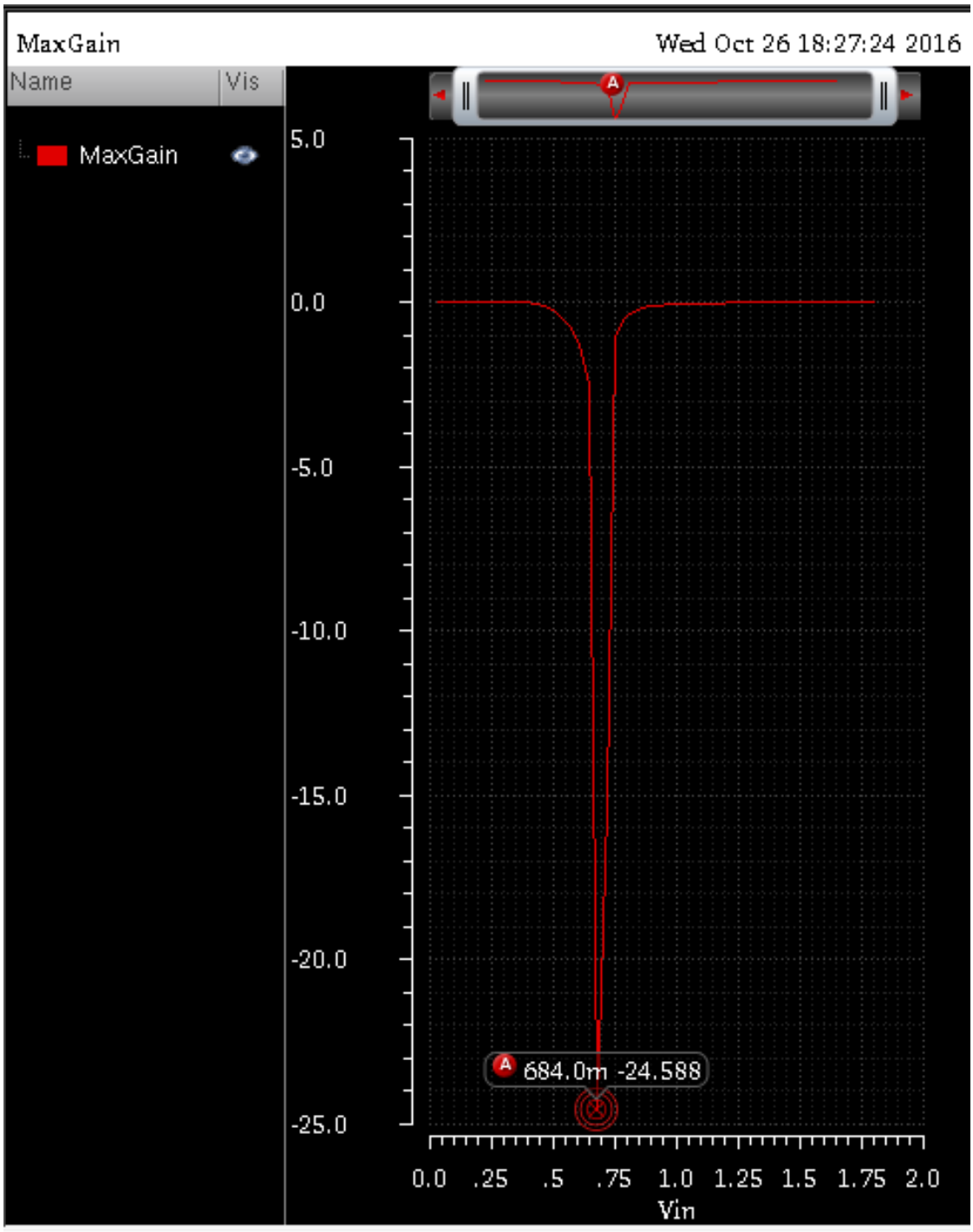
a.

We then ran a DC simulation for Vin values from 0-1.8V and we see that the circuit we have acts as an inverter where if Vin is less than the threshold voltage then the Value of Vout is equal to Vdd=1.8V. When the transistor begins to turn on we see a very rapid drop off in voltage for our Vout where in the space of 1V, from Vin = 0.4 to 1.4, the voltage at our output drops to 0.5V from 1.8V. Furthermore we notice that from Vin = 0.64V to Vin=0.72V the voltage at the output drops from 1.6V to 0.16 V. We see the slope is quite large at a value of -18.6 Vout/Vin. We can see that the circuit works very well as an inverter.



To find the max DC gain value we computed the derivative of our DC gain using the following formula. *deriv(v("/Vout" ?result "dc"))* This calculated the derivative of the graph which we then

plotted and found our max value to be at 0.684V. This is the point on our graph where the slope changes, denoting a max. We will then use this Value for the rest of our simulations.



b&c.

Finally we analysed how our small signal gain is affected by a +/- 20mV change in our DC value for Vin either side of the Max DC Gain when Vin=0.684V. We see that when Vin is at 0.684V the small signal output voltage is also at its max at 49.7 V. It also has quite a steep drop off point at around 0.1GHz. It starts to dip at 0.01GHz.

We also notice that a small change in DC input voltage can lead to a massive change in AC gain. If you decrease the input voltage by 20mV to 0.664V the output voltage is not even half that of our max gain voltage output at only 19.6V. However the voltage drop off does not occur until you are past 0.1GHz. so even though we have massively reduced our gain our voltage value is stable for longer.

Furthermore the same thing happens when we increase our DC voltage at Vin to 0.704V our AC voltage output is around a tenth of our Max gain voltage output at about 5V. However once again our voltage drop off point does not happen until 0.2GHz.

So we conclude that even though a relatively small change in input voltage can have detrimental effect on your output voltage, at voltage values further away from the Max DC gain input voltage of 0.684V we see that the output voltage will hold a steady value for a larger frequency range.