Analogue Integrated Circuits Report

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Lab 2

Introduction to choices for design parameters.

Why use gm/Id as a design parameter?

$$\frac{W}{L} = \frac{gm}{\mu CoxVov}$$

With our gm and L fixed, smaller Vov translates to a bigger (wider) device and a larger unwanted Cgs.

Therefore Vov isn't a good design parameter for our MOSFET so we use gm/Id.

gm/id is relevant for three reasons:

1. Strongly related to the performance of your analog circuit.
2. Gives a good indication of our device's operation region.
3. Provides a tool for calculating our transistor dimensions$\frac{W}{L}$.

How does it indicate our mode of operation?

$$\frac{gm}{Id} = \frac{1}{Id}\left(\frac{\partial Id}{\partial Vg}\right) = \frac{\partial(lnId)}{\partial Vg} = \frac{\partial\left\{\ln\left[\frac{Id}{\frac{W}{L}}\right]\right\}}{\partial Vg}$$

So our derivative is max in the inversion region. $\frac{gm}{Id}$ ratio decreases as the operating point moves towards strong inversion.

What do we want from our transistor?

- Large gm without investing too much current Id
- Large gm without a large Cgs

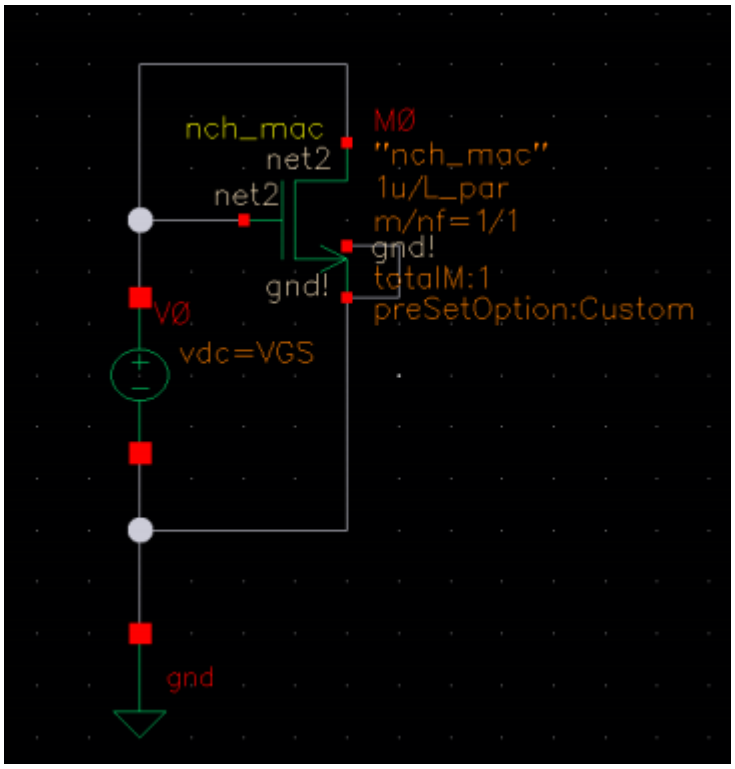
What performance metrics do we use?

- Transit frequency or Unity gain frequency
  $\omega_T = \frac{gm}{Cgs}$ Max frequency for which our MOSFET acts like an amplifier.
- Intrinsic gain
  gmr_o
- Transconductor efficiency (Want this to be Large)
  $$\frac{gm}{Id}$$
  Ability to translate current to transconductance.

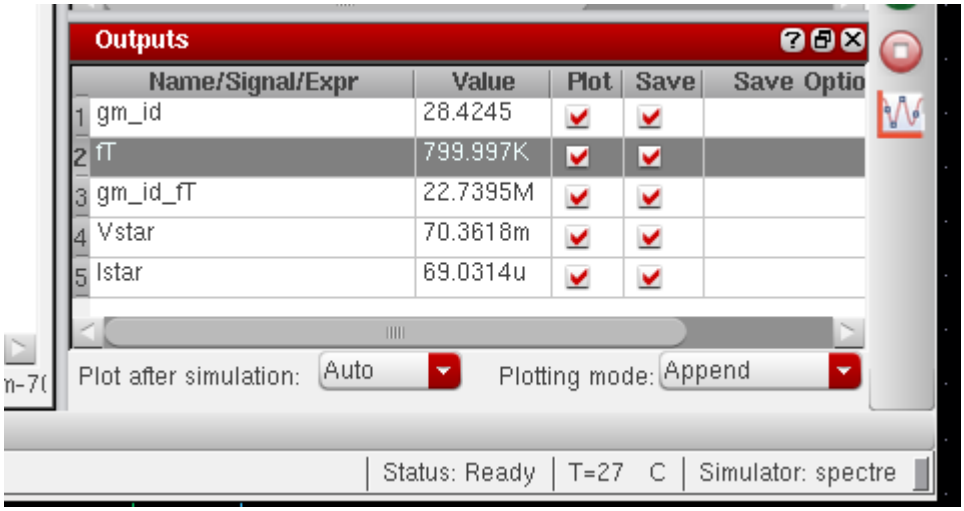
Lab work

The aim of our lab was to simulate 180nm TSMC MOSFETs by using simulations in Cadence ADE, and then to characterise a MOSFET by choosing appropriate design parameters to meet our specifications provided.

NMOS VSTAR TABLE



Our circuit consisted of a single NMOS TSMC MOSFET with its' bulk shorted to its' source which was set to ground. Our gate and drain our then set to a value Vdc from a voltage source which is at 1.8V. We then ran a DC analysis of the circuit at an operating point of 100mV and used the simulation to produce the following values.



For L = 200nm

Our equations are:

$$gm\_id = \frac{gm}{Id}$$

$$fT = \frac{gm}{Cgs\ 2\pi}$$

$$gm\_id\_fT = \frac{gm}{(\frac{Id}{fT})}$$

$$Vstar = \frac{2}{\frac{gm}{Id}}$$

$$Istar = \frac{Id}{W}$$

Our analysis sweeped the Vdc voltage source from 0.1V-1.8V, and then swept the transistor length from 200nm-1000nm.

Analysing the Graphs

Values for L (Mosfet Length):

- Red = 200nm
- Yellow = 400nm
- Green = 600nm
- Light Blue = 800nm
- Dark Blue= 1um

gm_id

Graph 1

At lower values of Vgs, our circuit has a much greater Transconductor efficiency. This is where our circuit has weak to moderate inversion. We also notice that varying the channel length has very little effect on this property.

ft

Graph 2

As our channel length decreases our transit frequency increases. Therefore shorter transistors are considered faster and can “switch” their voltage quicker. Furthermore if we increase the value of Vgs this will increase our transit frequency. We notice in particular that when Vgs is larger than 0.4-0.5V that the transit frequency rises quite rapidly. I think it is fair to assume that our threshold voltage lies around here.

gm_id_ft

Graph 3

This value is used to represent the average performance of a MOSFET. We can see that if you shorten your channel length you can vastly increase your MOSFET performance. Also the region of voltage Vgs for which the MOSFET performs best is between 0.5-1.25V, with the highest performance around 0.75V.

Vstar (V overdrive)

Graph 4

Vstar is equal to Vgs – Vth, so we see that once the value of Vgs exceeds our threshold, about 0.4V, That the relationship is practically linear. Our Vstar relationship is also greater in MOSFETs with shorter channel length but this is only apparent when the value for Vgs becomes quite large.

Istar

Graph 5

This shows the relationship of our current Id to our channel width. It increases when Vgs increases and when the channel length decreases.

NMOS IGAIN TABLE

This circuit was the same as before however there was now a fixed voltage of 0.91V on the gate. We then sweep Vds from100mV to 1.8V and again sweep our channel Length L from 200nm-1000nm.

GRAPH

gm_gds

This graph shows that as our Vds increases our Intrinsic gain increase accordingly. The relationship is almost linear once it becomes greater than 0.4-0.5V the Value of our threshold voltage. It is also clear that by increasing the length of your channel length L, you can achieve larger intrinsic gains. This mean that longer transistors are capable of amplifying greater.