Analogue Integrated Circuits- Final Project

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Hand calculations

We were given the following specifications for our transistors and design.

$$\mu_n C_{ox} = 200\mu AV^{-1}$$

$$\mu_p C_{ox} = 100\mu AV^{-1}$$

$$PM = 70°$$

$$GBW = 120MHz$$

$$Gain = 2000$$

$$Therefore\ bandwidth = 60\ KHz$$

$$Slew\ rate = 160V\mu s^{-1}$$

$$\lambda_n = 0.1V^{-1}, \lambda_p = 0.15V^{-1}$$

$$V_{th_n} = 0.55V, V_{th_p} = 0.5V$$

$$C_m = 2pF$$

And all transistors should be on and in saturation.

The following is the circuit topology we were given to design the OTA. We not the voltage dividers, current sources and differential amplifiers in the circuit. We were advised to start at the second stage of our OTA, find its' gain then utilise that to find the gain needed from the first stage, and pick voltages, $\frac{W}{L}$ values and bias currents accordingly.

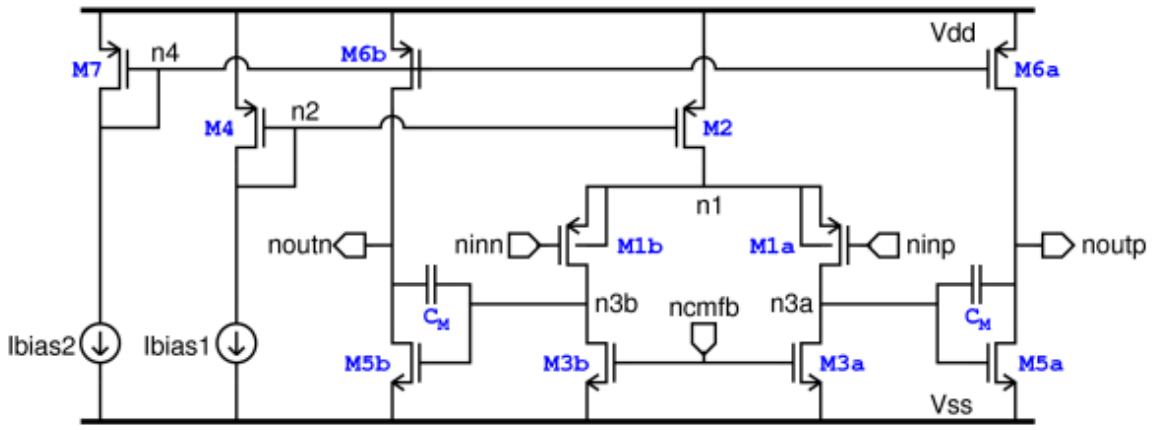


Figure 3.1: A differential Miller OTA

We know that the gain off the second stage of the circuit is $gm_5(r_{0_5}||r_{0_6})$. Therefore I will calculate g_{m_5}, the transconductance of my M_5 transistor.

$$g_{m_5} = 4GBW * 2\pi C_L = 6.0319mS$$

$$I_{d_5} = SR * C_l = 0.32mA\ (rearranging\ SR\ formula)$$

$$V_{gs_5} = \frac{2I_{d_5}}{g_{m_5}} + V_{th_n} = 0.6561V\ (rearranging\ g_m\ formula)$$

$$\frac{W}{L}_5 = \frac{g_{m_5}}{\mu_n C_{ox}(V_{ov})} = 284.25 = \frac{52.17\mu m}{0.18\mu m}$$

$$C_{gs_5} \approx 1pF$$

$$Cm = 3C_{gs_5} \approx 3pF$$

$$r_{0_5} = \frac{1}{\lambda_n I_{d_5}} = 22.17k\Omega$$

$$r_6 = \frac{1}{\lambda_p I_{d_5}} = 20.2k\Omega$$

The second stage gain $A_{V_2} = g_{m_5}(r_{0_5}||r_{0_6}) = 23.95$, and so my first stage gain is equal to $A_{V_1} = \frac{A_{V_{total}}}{A_{V_2}} = 83.47$

I then got the values for my M_1 transistor.

$$g_{m_1} = GBW * 2\pi C_m = 2.2619mS$$

$$I_{d_1} = SR_{int} C_m > 0.48mA$$

And $A_{V_1} = g_{m_1}(r_{0_1}||r_{0_3})\ but\ r_{0_1} = r_{0_3}\ therefore\ r_{0_1} = r_{0_3} = 73.8k\Omega \therefore I_{d_1} = \frac{1}{\lambda_p r_{0_1}} = 19.5\mu A\ choose\ 20\mu A$.

$$V_{sg_1} = \frac{2I_{d_1}}{g_{m_1}} + V_{d_p} = 0.9713V$$

To keep M_3 in saturation we set its gate equal to 0.7V. Using current formula it's $\frac{W}{L} = \frac{42.64\mu m}{0.18\mu m}$

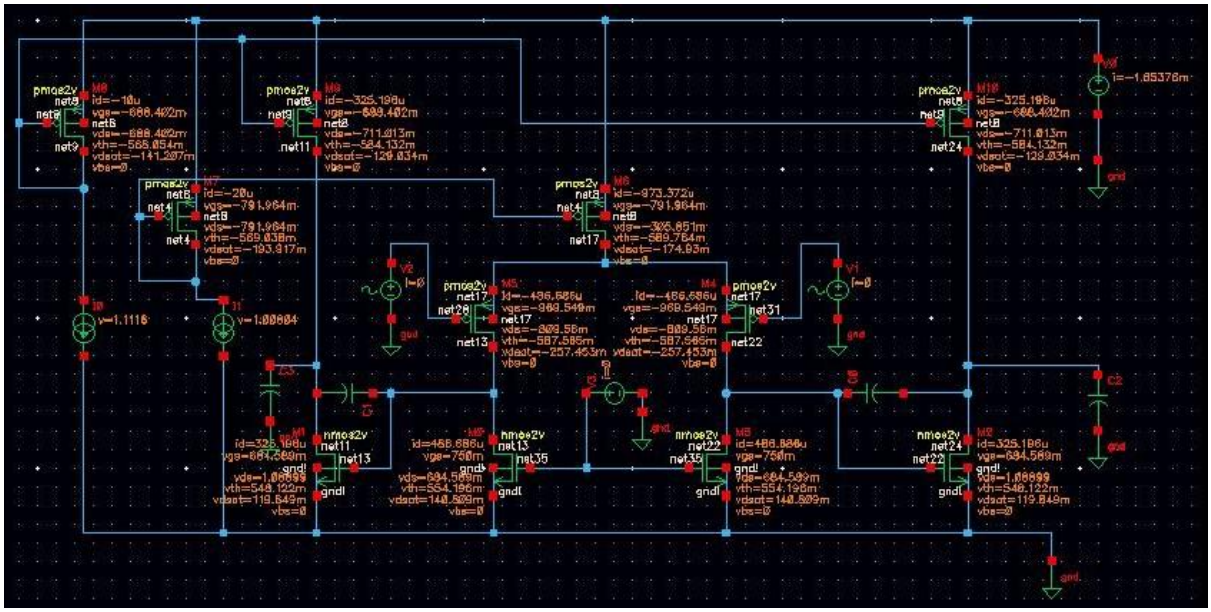
To find the values of $M_2\ and\ M_4$ I found them saying

$$\frac{W}{L}_2 = \frac{W}{L}_4 \left(\frac{2I_{d_1}}{I_{bias_1}}\right) = 266.5 = \frac{48\mu}{0.18\mu}\ as \frac{W}{L}_4\ was\ calculated\ usind\ I_d\ formula\ to\ be \frac{0.9\mu}{0.18\mu}.$$

Using similar calculations $\frac{W}{L}_7 = \frac{0.95\mu}{0.18\mu}\ and\ \frac{W}{L}_6 = \frac{28.8\mu}{0.18\mu}$ for an $I_{bias_2} = 10\mu A$

I set my Vin_{cm} to 0.9V and my V_{cmfb}=0.9V as I knew this would keep both transistors in saturation, also the 0.9V was chosen as it was halfway between our V_{dd} and ground to provide the best voltage swing.

The following circuit is my implemented design in Cadence where I simulated my design.



Despite my hand calculations being correct my gains were not close to the 2000 value I wanted. So I tweaked my values.

All transistors were over 180nm, as we were told not to change the length parameters of the transistors and maintain their factory spec values, and their widths were as follows.

$$W_1 = 12.5\mu m$$

$$W_2 = 50\mu m$$

$$W_3 = 4.5\mu m$$

$$W_5 = 62\mu m$$

$$W_5 = 62\mu m$$

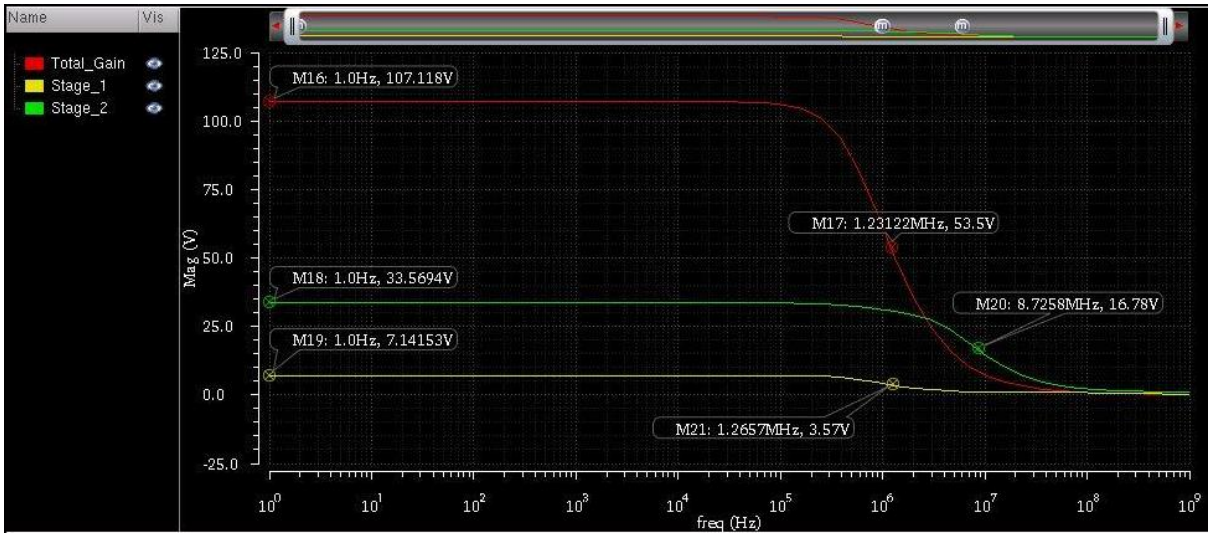
$$W_6 = 120\mu m$$

$$W_7 = 86\mu m$$

I changed my bias currents to $I_{bias_1} = 18mA \; and \; I_{bias_2} = 330\mu A$.

For my common mode voltage DC was 0.7V, AC was -0.5V for $M_{1_B} \; and + 0.5V$ forM_{1_A}

This gave me the highest gain with the circuit topology I used of 107.



This is obviously well below the value we wished for of 2000 and no matter how I changed the values of the transistors, currents or voltages I could not achieve a higher gain.

I then looked at it from a different point of view tried to place all my differential amplifier transistors close to the edge of saturation in order to provide maximum voltage swing and increase our gain however this also did now work.

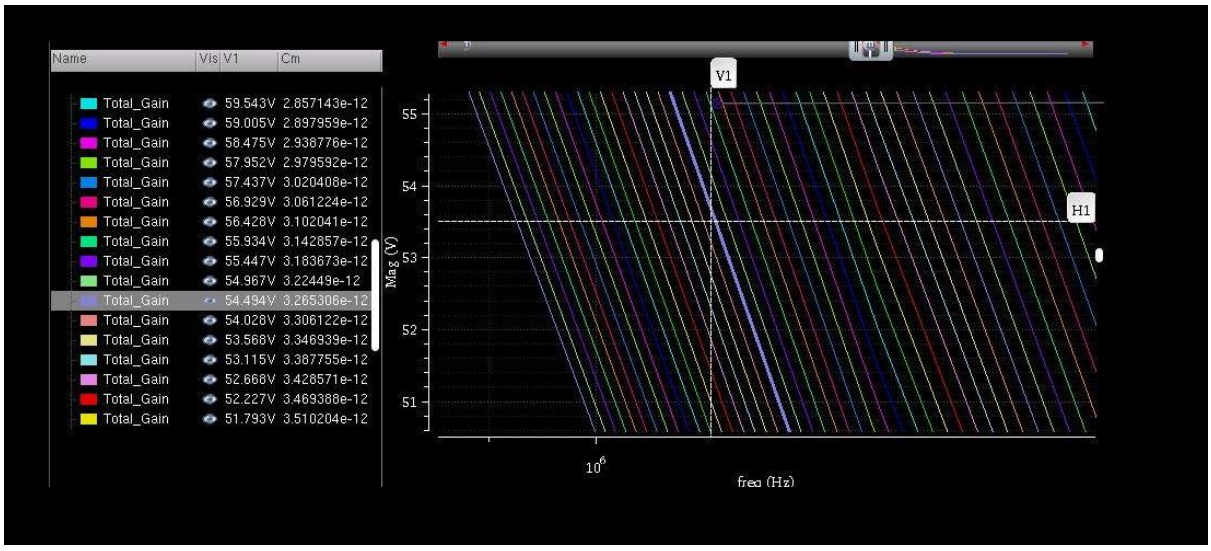
I have noticed a few things about the circuit though.

Firstly your gain is decided by your M1, M3 and M5 transistors. Changing the other values obviously manipulates the bias of your circuit but these three transistors, or 6 due to there being a copy of all of them for diff amp, are the values that really affect your gain.

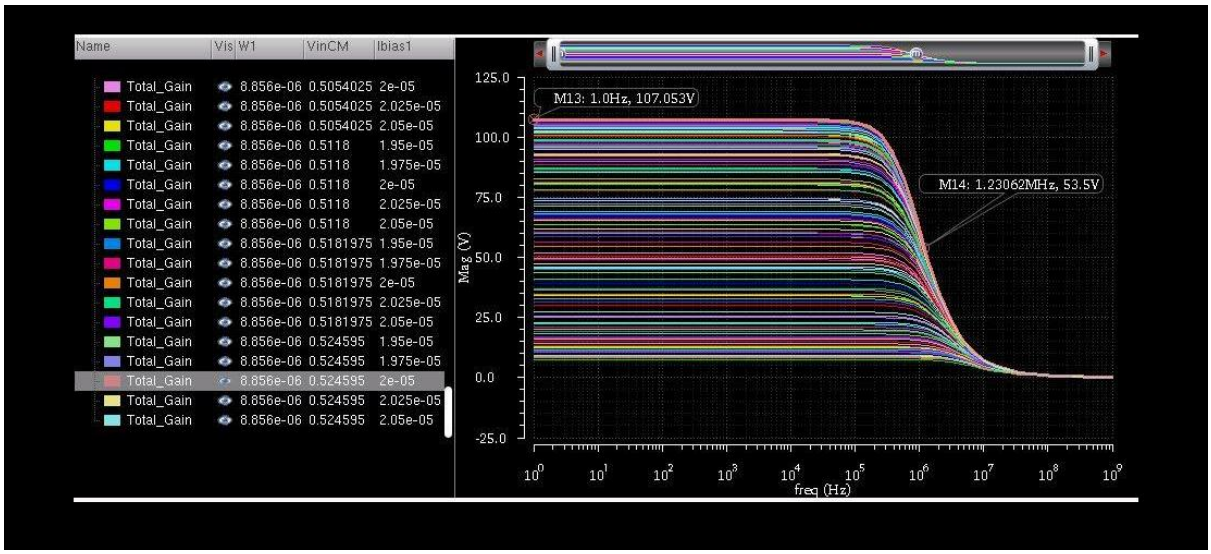
Decreasing the width of M3 increases your gain but does not affect your gain band width.

Similarly increasing the length of M1 increases your gain however it also reduces your gain bandwidth.

I decided to run some parametric analysis on the circuit in order to see how changes in key components or key values affected our gain as this was the first design criterion I wished to achieve.

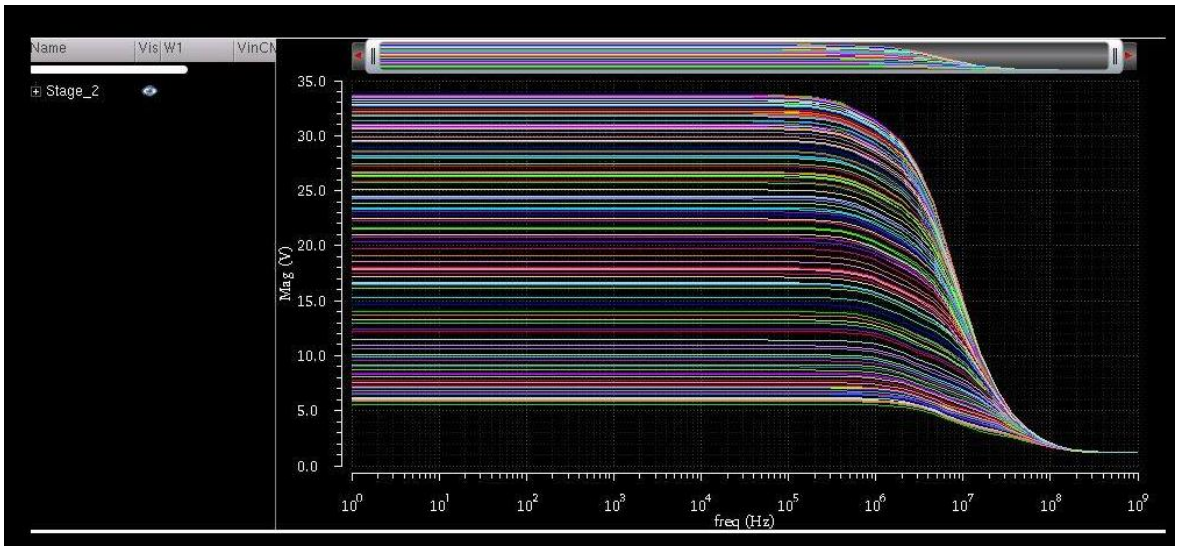


The first of these was to see how an increase or decrease in the width of the M1 transistor affects the gain of the circuit. The input voltage is 1V so the gain is relative. We note that as explained earlier to a point increasing the width of M1 increases the gain however doing this too much turns off the M3 transistor.

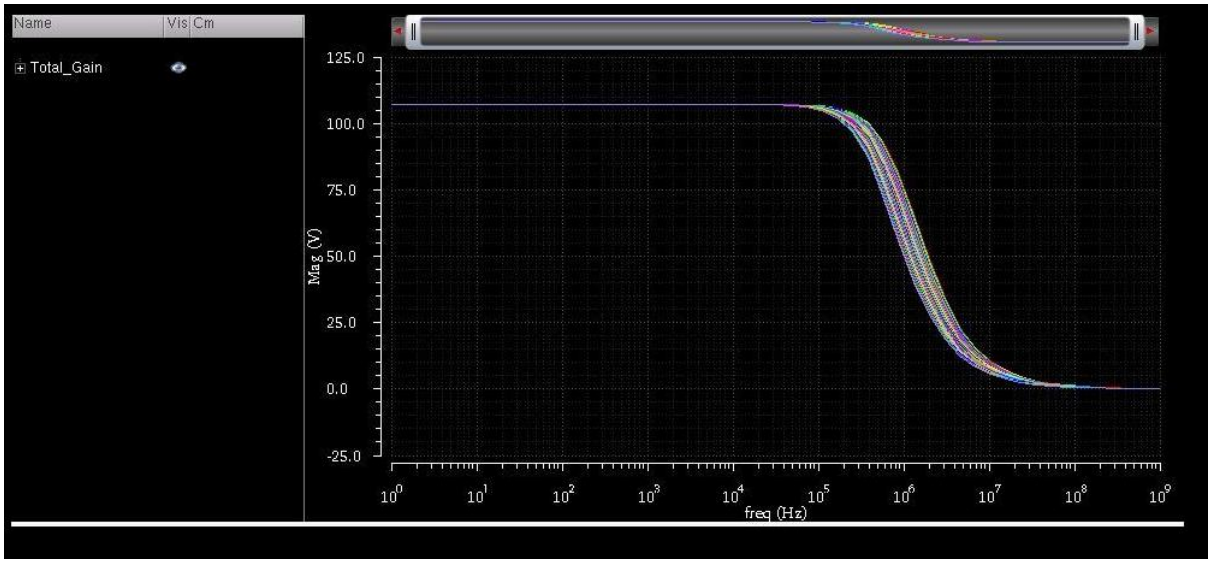


I then decided to zoom in and see how it affects the gain of specifically just my first stage. We note that again it increases fairly linearly until M3 turns off.

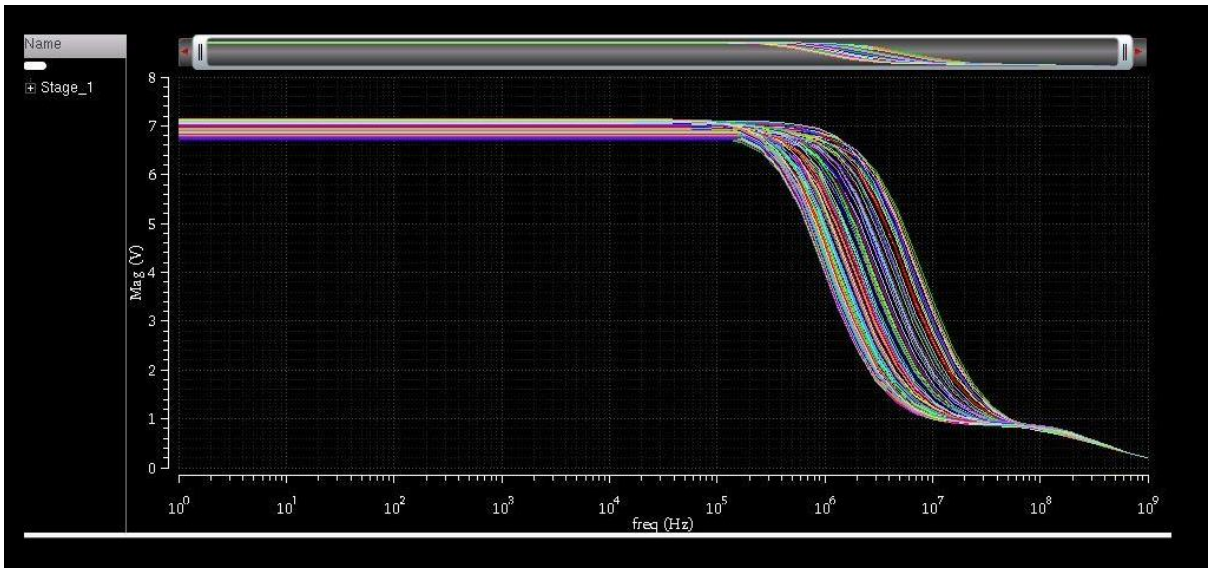
The same thing happens width M3 and M5 if you increase M5 you increase the gain until it or M6 are turned off. If you decrease M3 you increase the gain until M3 turns off.



I was then interested to see how different values of Cm would affect the circuit. We note that it slightly affects the dropoff and bandwidth of our filter but not drastically, then again the change I made were simply +/- 10%.



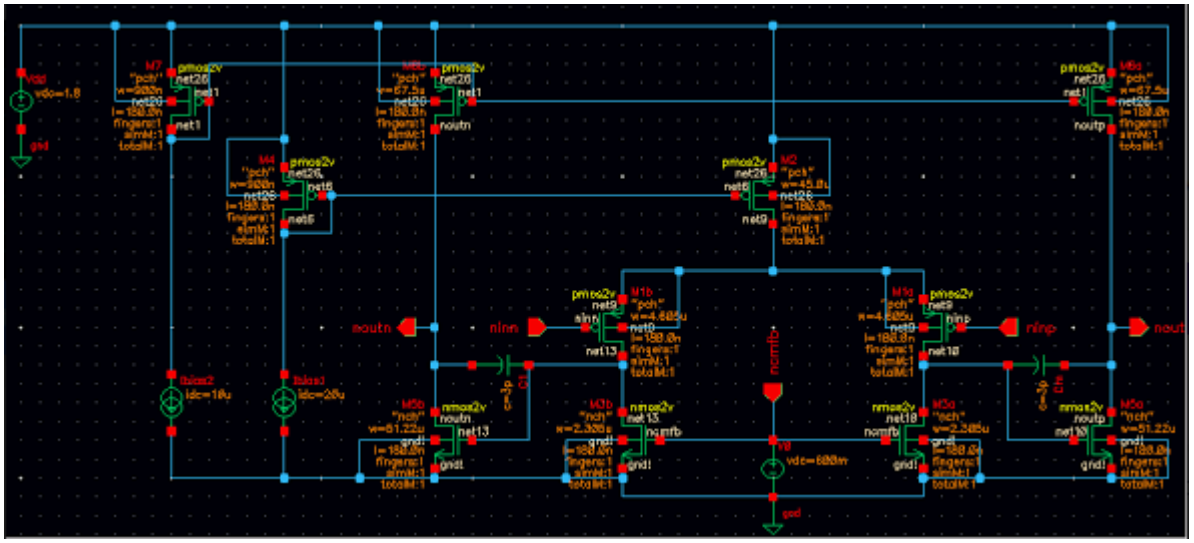
Here we see how it affects the gain of our the first stage of our amplifier. We note there are very small vaiations in gain however the band width changes considerably more drastically at this stage.



As I did not get the gain to work I couldn't really justify attempting to fix the phase margin of the circuit which would involve taking the Miller effect of the capacitor Cm into account as.

As stated before it is quite obvious that something is affecting the voltage swing from the first stage of my amplifier however I do not know what that is. By assuming 0.1V were dropped across V_{DS} of my transistors in my differential amplifier I could not get a gain larger than the gain I specified or one of the transistors would slip into the triode region.

The reason I wished to increase the swing is due to the formula $-\left(\frac{g_m r_0}{2}\right)^2$.



I accounted for the feedback at one stage but without an appropriate gain value I did not pursue this too far. The feedback would have been a Voltage-Voltage Feedback, in a series-shunt topology. It would also have had to have negative feedback or else the circuit would turn into an oscillator.

To calculate my phase I would have had to consider the two miller capacitors and two poles in the circuit, and draw the corresponding bode. Using this I would find my phase and alter it to fit my phase margin by introducing a dominant pole. $PM = \tan^{-1}\left(\frac{\omega_{p2}}{\omega_c}\right)$. There would also be a zero introduced in the circuit that would have to be accounted for depending on whether it was in the RHP or LHP. This would help me pick the value of my capacitors and also the series resistances added with those capacitors used to vary omega. The resistances, called nulling resistors, would move the pole over the zero effectively cancelling it.

My power consumption on my circuit was quite small at 2.98mW, however as the gain doesn't work, and the currents are small, this would surely increase if the gain was 2000.

My slew rate is also quite small but as the gain is not correct the value is rather irrelevant.

Finally it occurred to me extremely late on the 24th of December that to increase the gain of your circuit, you must alter your value of the transistor lengths as well as the widths in order to maintain the same W/L relationship so as to not affect currents or voltages. By increasing the length of M3 you increase your gain and do not affect your gain band width, and by reducing the length of your M1 transistor you can also increase your gain slightly, but it does increase your gain band width.

To be honest I discovered this after flicking through material online and realised that it was imperative to getting the correct gain of our circuit. Simply increasing or decreasing W is not enough to affect your gain. As it changes your ratios and as a result your currents and voltages. By being specifically instructed regularly to only use the 180nm technology and in so discouraging students from manipulating their lengths, I believe this was incredibly unfair. I then consulted with students from the year above who are taking the class and managed to get the gain, and they informed me that from their work placements they learned to do this, work placements which the majority of students have yet to complete.

I feel that under different circumstances I would definitely have completed this project, but given the time and the material given to assist us with its design I was unable.