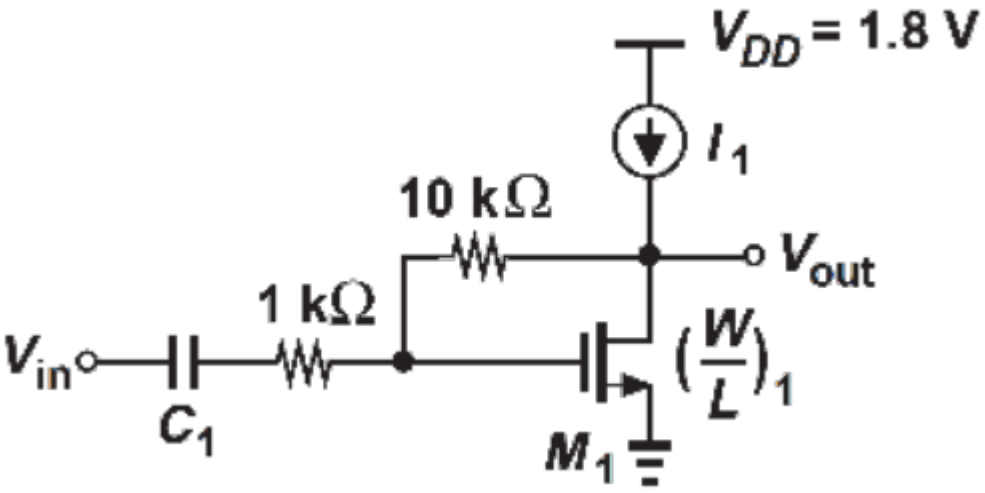
Analogue Integrated Circuits Report

Lab 3

Task 1



a.

For the circuit above we set I1 = 1mA. We were told that our $\mu_n C_{ox} = 200\mu A/V^2$ and that our Vth was 0.4V. The following are my hand calculations, which determine a value of W/L such that our $gm1 = \frac{1}{100\Omega}$ where $gm1 = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$.

Therefore $\frac{W}{L} = \frac{gm_1^2}{2\mu_n C_{ox} I_D} = \frac{(100^{-1})^2}{2(200x10^{-6})(1x10^{-3})}$ = 250. Seeing as the L is set at 180nm we calculated our W value should be 45µm.

b.

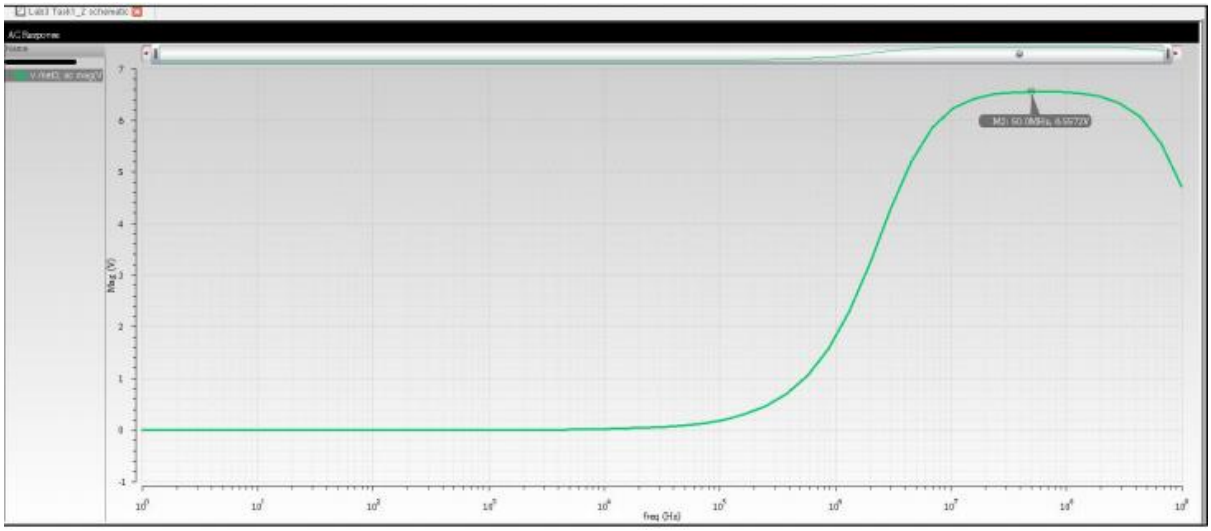
Now we must select a suitable capacitance for C_1 so that its' impedance is ≈ 100Ω (<< 1k Ω) at 50 MHz.

$$\left|\frac{1}{j\omega C}\right| = 100$$

$$C = \frac{1}{2\pi(50x10^6)100} = 31.84pF$$

C.

We set the magnitude of our Vin AC voltage source to 1V and at 50 MHz our observed Vout, from our graph, is 6.56V. Therefore our Voltage gain at this frequency is $\frac{Vout}{Vin} = 6.56$.



We then proceeded to get the value of our output impedance $Rout = \frac{Vout}{Iout}$.

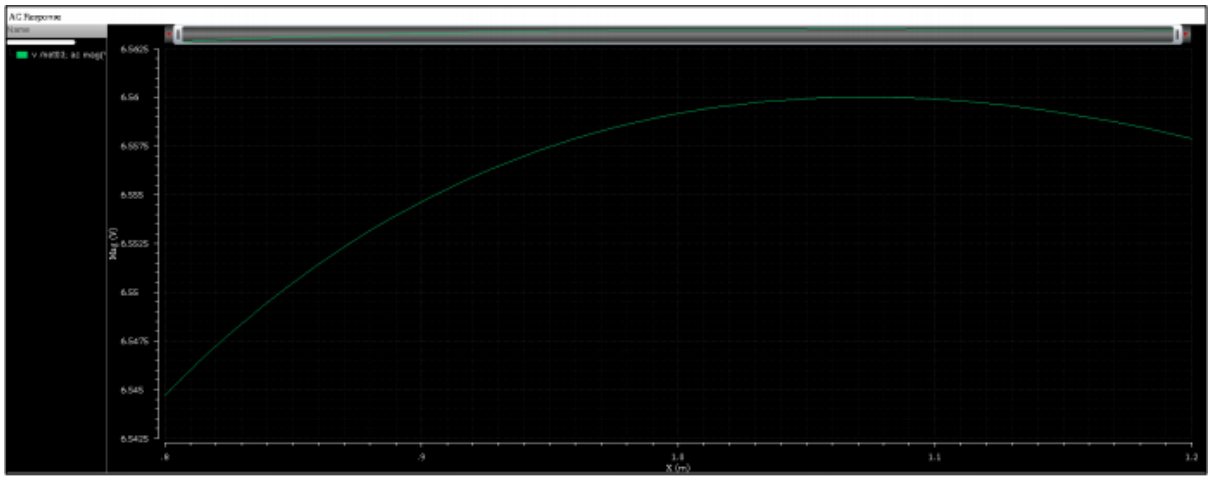
We grounded our input and injected a current at the output and measured the output voltage as a result of the current injected at the output. We generated the current using an AC voltage source with magnitude 1mV. The observed output voltage at 50MHz was 92.91nA. Therefore:

$$Rout = \frac{Vout}{Iout} = \frac{1m}{92.91n} = 10.76k\Omega$$

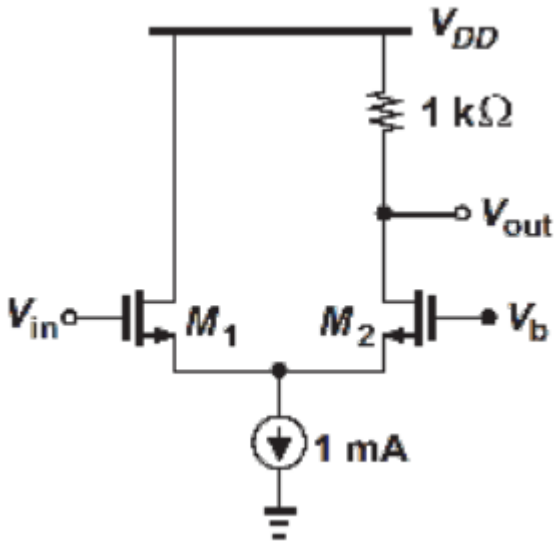
As the frequency increases the Iout will increase exponentially, therefore out Rout will tend to 0 as Iout increases.

d.

We then replaced our I1 value with the variable X and swept our current from 0.8nA to 1.2mA. We kept the magnitude of our AC Voltage source at our input is 1. Our peak gain appears circa 1.1mA and drops off for our other current values.



Task 2



For task 2 we set the value of $V_b = 1.2V$. Our $(\frac{W}{L})_1 = (\frac{W}{L})_2 = \frac{10\mu}{0.18\mu} m$

a.

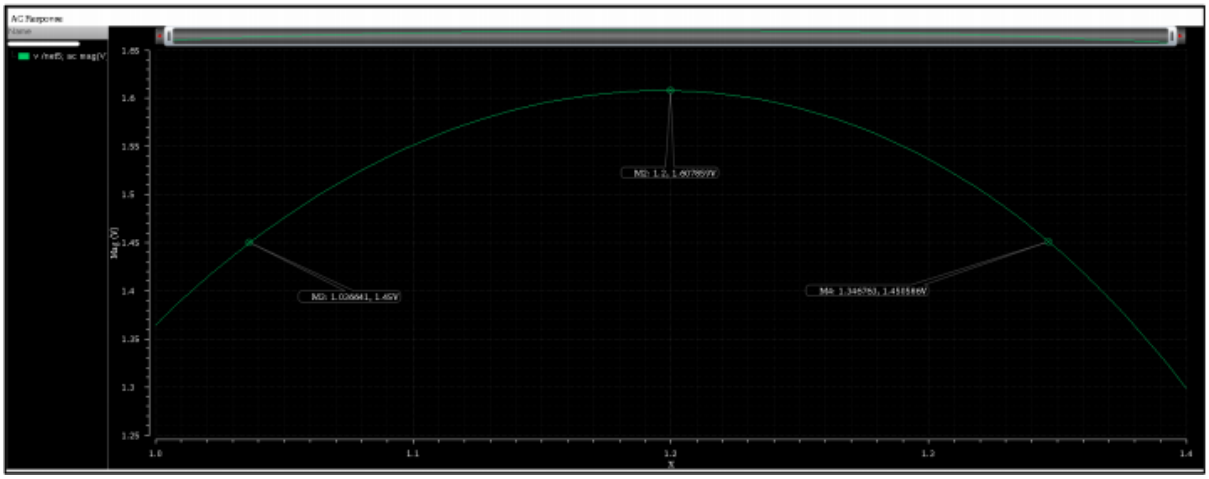
We set Vin to a DC value of 1.2V and measure our Vout/Vin to get our Voltage gain. From the plot we see our gain is approximately 1.60765 this is with an AC voltage magnitude of 1. We notice that the Gain drops sharply when the frequency passes 10^8Hz. This is most likely due to the high frequency response of the NMOS device where the internal capacitances of our device begin to have an adverse effect on the gain.

b.

We then swept the DC value from 1-1.4V and kept our frequency fixed at 50Mhz which was well within our constant gain region from (a). We notice that the gain is max when the DC value of Vin is equal to Vb

c.

c. What DC value at the input reduces the gain by 10% with respect to that obtained in



Gain = 1.45 @ Vin equal to 1.04 and 1.35