UCD School of Electrical & Electronic Engineering

RF Electronics Laboratory

Lab 6: Amplifier Design

Introduction

In the previous lab you performed various measurements on a high power transistor. These included biasing the device for a specified amplifier Class using ideal bias-tees. In this lab, you are required to replace the ideal bias-tees with more realistic components that are possible to manufacture, and to design matching networks for an amplifier to achieve maximum transducer gain.

Initial Setup

In this lab, you will again be using a nonlinear FET model. In order to simplify the lab somewhat, a perfectly unilateral model will be used rather than the almost-unilateral CGH40010 of Lab 5. To get the model, please download "Lab6Unilateral.emp" from Blackboard.

Task 1

Set your bias and project frequency as per the table, and add a Smith Chart graph with S11 and S22**.** As per previous labs, if you are working with a partner you need only select one value.

Last two digits of student number	Frequency	Bias
00-24	2 GHz	$V_{\mathrm{GS}} = -2.0, V_{\mathrm{DS}} = 28$
25-49	3 GHz	$V_{\mathrm{GS}} = -1.7, V_{\mathrm{DS}} = 28$
50-74	1 GHz	$V_{\mathrm{GS}} = -2.5, V_{\mathrm{DS}} = 28$
75-99	2.5 GHz	$V_{\mathrm{GS}} = -1.8, V_{\mathrm{DS}} = 28$

As you saw last week, the bias-tee (or Bias-T), allows the transistor to be biased from a constant voltage source – this means connecting a voltage source both to the gate and the drain – while also allowing an RF voltage to be superimposed on top of the bias at the gate terminal, and an amplified RF signal to be obtained at the drain terminal.

Without a bias-tee, the voltage at the gate would be unable to change (the voltage would be set by the DC supply), and even more disturbingly, the RF signal path may be exposed to very high voltages from the bias, particularly at the drain (so the output would have an undesired DC component equal to the drain-source bias voltage).

Examining the AWR element help for the ideal bias-tee in your circuit from last week will reveal the equivalent circuit model (also see diagram below).

Create a duplicate of "Amp", and replace the bias tees as per the help file.

Your task is to select capacitor and inductor values that will allow operation as per above – that blocks DC from reaching the RF path, and simultaneously blocks RF from the DC source.

Try to select values that are optimal for your needs – large capacitor and inductor values take up significant space and are more prone to unwanted resonances (in real circuit elements). However, if the values are too small, they may present undesirable impedances at RF. The capacitor reactance, X_{C}, should be significantly smaller, and the inductor reactance, X_{L}, significantly larger, than the magnitude of the relevant transistor impedance. In other words, we require

$$X_{\mathrm{C_{in}}} \ll |Z_{\mathrm{IN}}| \ll X_{L_{in}}$$

$$X_{\mathrm{C_{out}}} \ll |Z_{\mathrm{OUT}}| \ll X_{\mathrm{L_{out}}}$$

at the RF frequency of operation. The input and output impedance of the transistor may be determined from *S*-parameters taken at the appropriate frequency. Do not exceed

$$20 * X_{\mathrm{C_{in}}} \geq |Z_{\mathrm{IN}}| \geq X_{\mathrm{L_{in}}}/20$$

$$20 * X_{\mathrm{C_{out}}} \geq |Z_{\mathrm{OUT}}| \geq X_{\mathrm{L_{out}}}/20$$

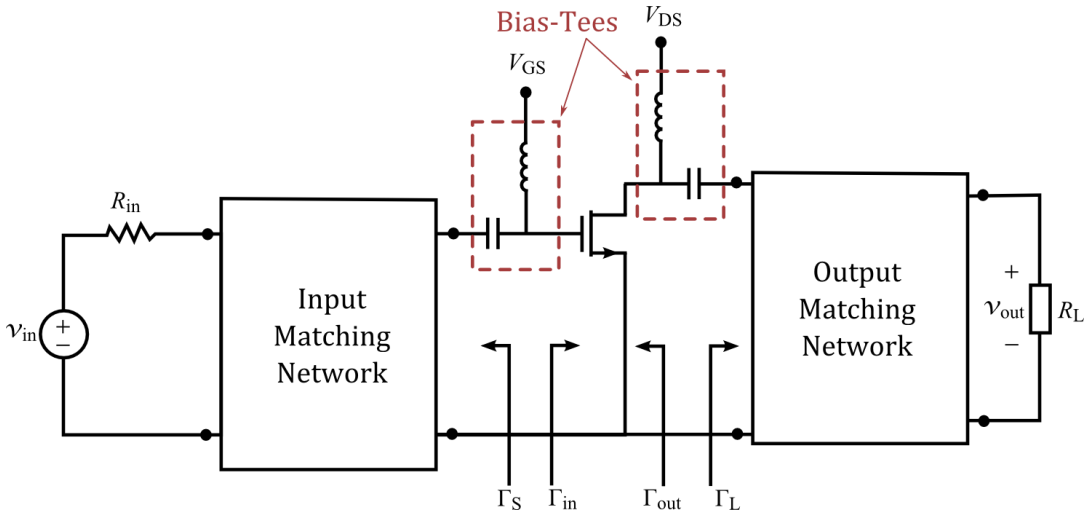
Compare the *S*-parameters of your circuit with realistic bias network design to the *S*-parameters of the circuit with ideal bias-tees. Are they as expected? If not, you must redesign your bias networks until they behave as required.

Task 2

The figure below shows the overall schematic of an amplifier (biasing also shown). As discussed in lectures, for small-signal matching (where *S*-parameters are valid), the maximum transducer power gain can be achieved when the following conditions are met:

$$\Gamma_S = \Gamma_{\mathrm{IN}}^* \text{ and } \Gamma_L = \Gamma_{\mathrm{OUT}}^*$$

that is, the reflection coefficient looking into the source must be the complex conjugate of the reflection coefficient looking into the transistor, and similarly for the output.



The lecture notes contain formulae which give the input and output reflection coefficients, Γ_{IN} and Γ_{OUT}, in terms of the *S*-parameters of the transistor. If the device is unilateral, $S_{12} = 0$, or even nearly so, the reflection coefficients take on a very simple form:

$$\Gamma_{\mathrm{in}} = S_{11} \text{ and } \Gamma_{\mathrm{out}} = S_{22}$$

Therefore, for a unilateral design, the following conditions must be met:

$$\Gamma_S = S_{11}^* \text{ and } \Gamma_L = S_{22}^*$$

In this task, you are required to design an input matching network to transfer $\Gamma_S = 0$ (R_S = 50 Ω) to S_{11}^* and an output matching network to transfer $\Gamma_L = 0$ (R_L = 50 Ω) to S_{22}^*, using

- Single-Stub Matching (all lines must have $Z_0 = 50\ \Omega$)

Sketch your design and put it into the simulator to simulate the complete circuit (incl. matching networks, bias networks and transistor). Make sure to include your smith chart in your report.

Using the formula given in the notes for the Unilateral Transducer Power Gain, calculate the theoretical maximum small signal transducer gain ($\Gamma_S = S_{11}^*,\ \Gamma_L = S_{22}^*$). You may verify your calculation using the Unilateral Gain measurement (GU). **Does the gain of your amplifier** (measured using either the GT measurement or $|S_{21}|$) **differ from this maximum value?**

Make sure you save a copy of your design, as it may be useful to have for Homework 2.