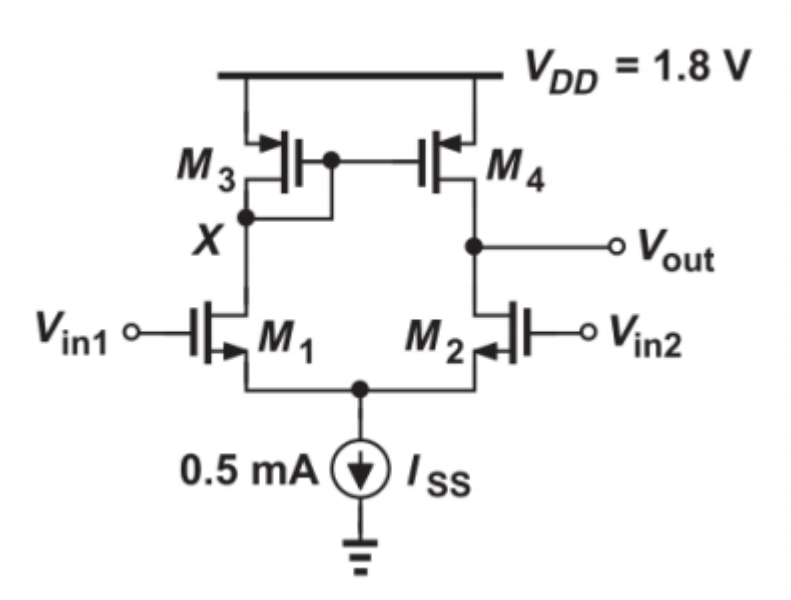
Analogue Integrated Circuits Report

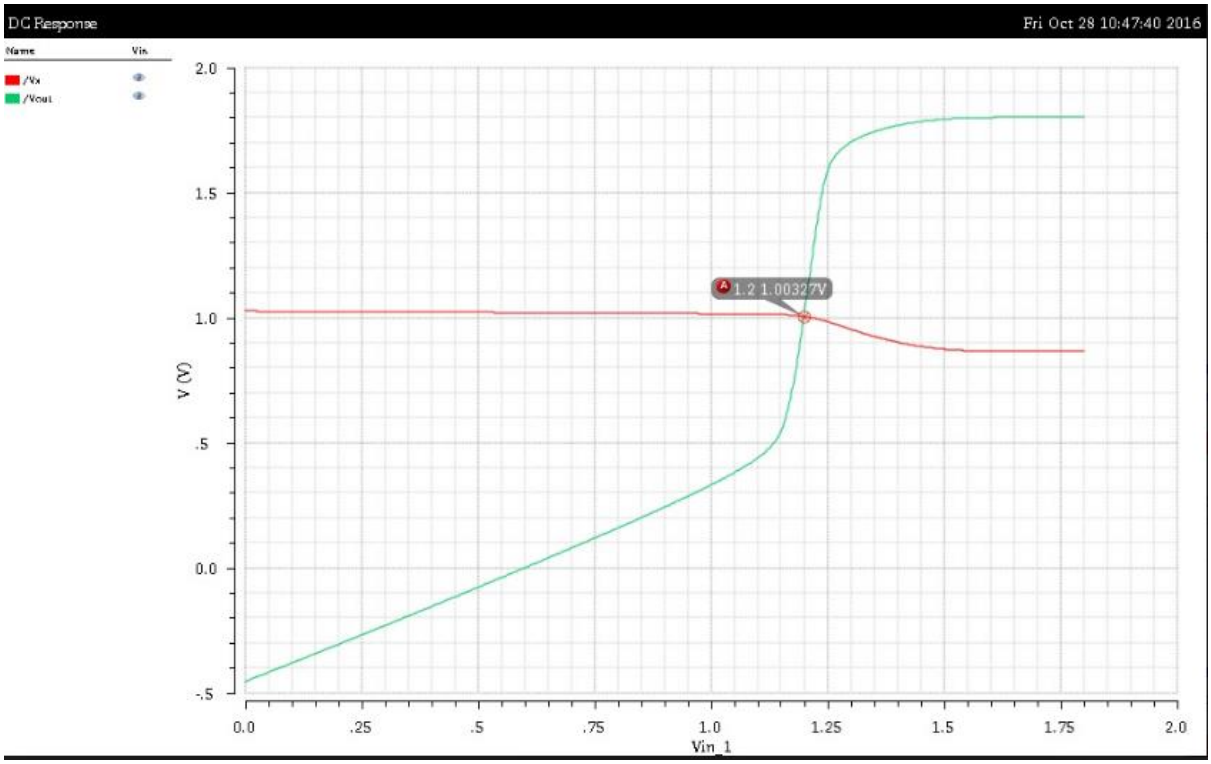
Lab 5



We were asked to measure the DC output of Vx and Vout when Vin1 and Vin2 were both equal to 1.2V, ie common mode. All transistor $\frac{W}{L} = \frac{10}{0.18}$. Therefore M3 and M4 are identical as they are both PMOS transistors, M1 and M2 are both identical NMOS transistors. Therefore at common mode the current going down the left hand branch of our circuit is equal to the current travelling down the right hand branch. This circuit is called a current mirror. The proof of this is in the hand calculations.

a.

We then ran a DC simulation for Vin1 values from 0-1.8V but kept Vin2 stable at 1.2Vand we see that the circuit we have returns a Vout and Vx that are equal when our Vin1 and Vin2 values are both equal. This is what we expected knowing what we know about common mode circuits and seeing that the currents through M1 and M2 are equal since VGS1 and VGS2 are equal and since VDS3 = VDS4 we also have the same current through M3 and M4 , since λ is the same for all the transistors so $r0_1$ and $r0_2$ are $equal$ as are $r0_3 and$ $r0_4$. The value at both nodes is 1.00327V.

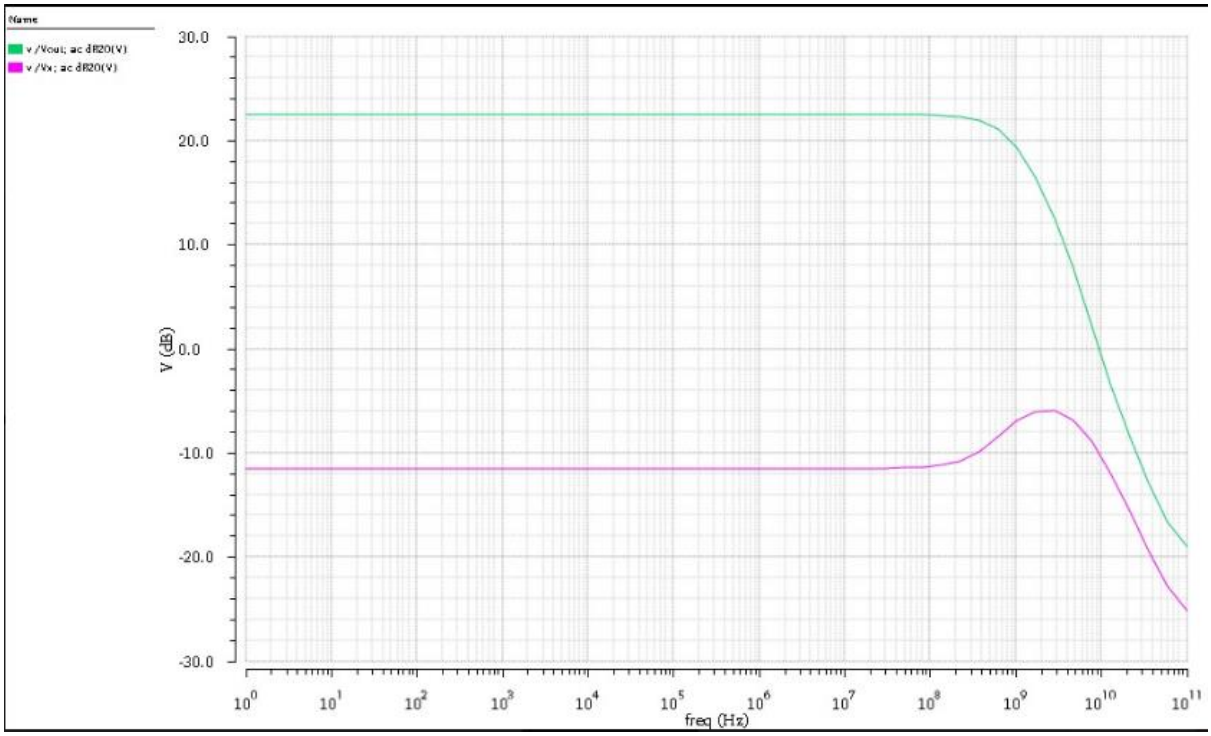


Vx is Red

Vout is Green

b.

We were then asked to find the small signal voltage gains Vout/(Vin1 −Vin2) and VX/(Vin1 −Vin2). To do this we set the AC magnitude of Vin1 equal to 0.5 and the AC magnitude of Vin1 equal to -0.5. Then when we run the simulation their combined AC magnitude will be 1 but they will be subtracted from each other as we want.



We see that the voltage gain at Vout (22.25dB) is much greater than that of Vx (-11.75dB). This is explained in the hand calculations were we get the equivalent resistances seen at each node. At Vout we have a the equivalent impedance is $r0_N||r0_P$ whereas at Vx the diode tied transistor M3 has an equivalent resistance of $\frac{1}{gm_3}$ which when placed in parallel with our $r0_N$ resistance from M1 is approximately equal to $\frac{1}{gm_3}$ which is much less than that at Vout. That is why its gain is much smaller.

C.

NMOS current equation.

$$I_{D(sat)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T$$

PMOS current equation

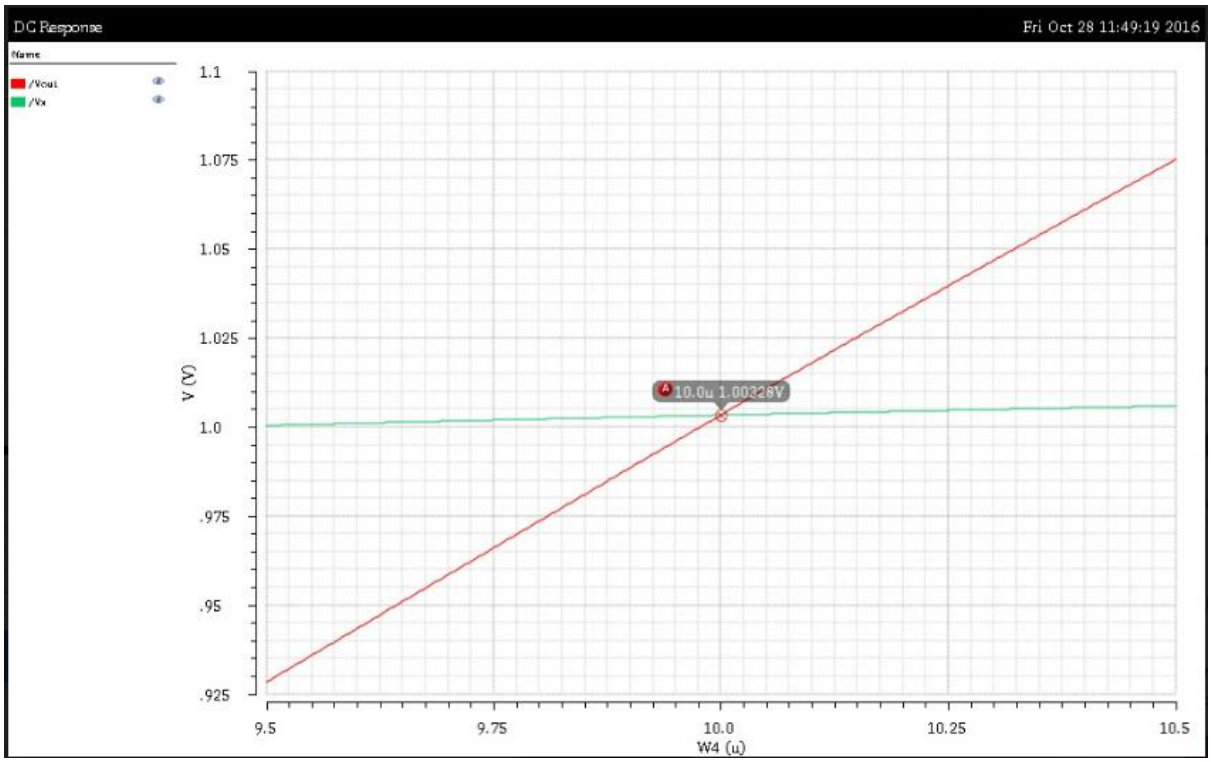
$$I_{D(sat)} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \leq V_T \text{ and } V_{DS} \leq V_{GS} - V_T$$

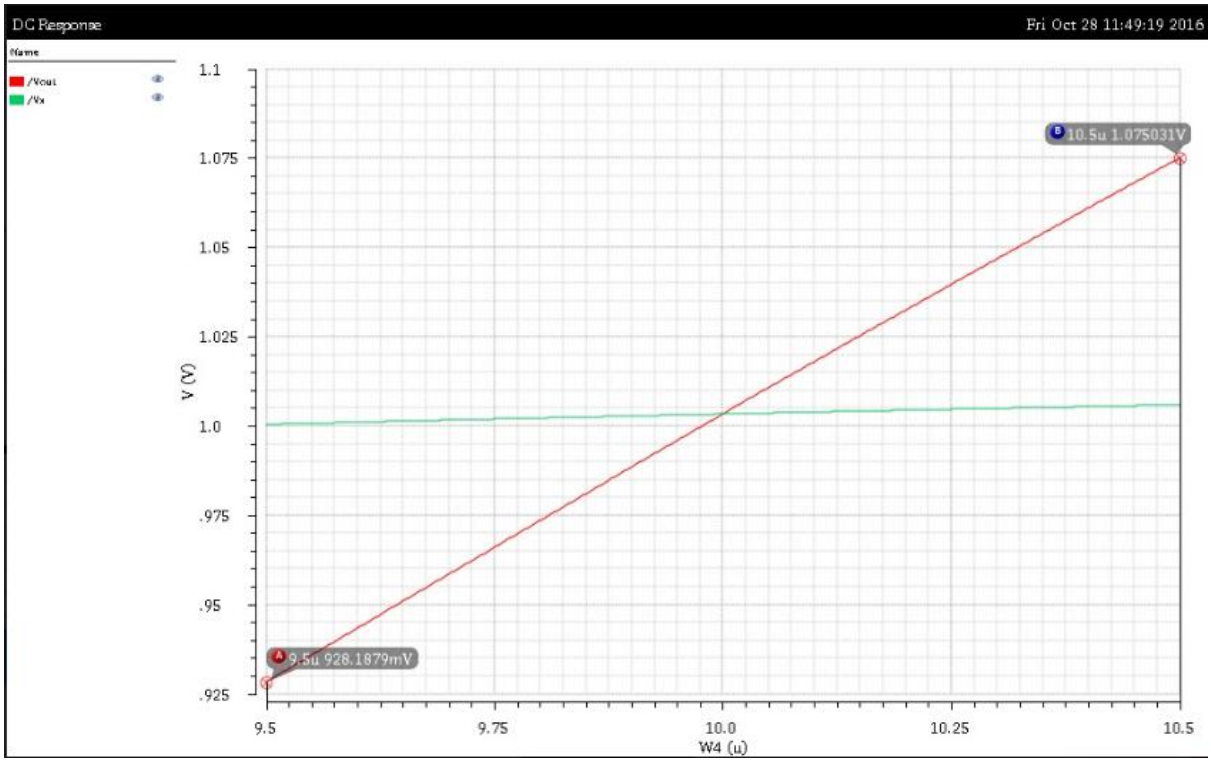
For PMOS swap VGS for VSG and VDS for VSD

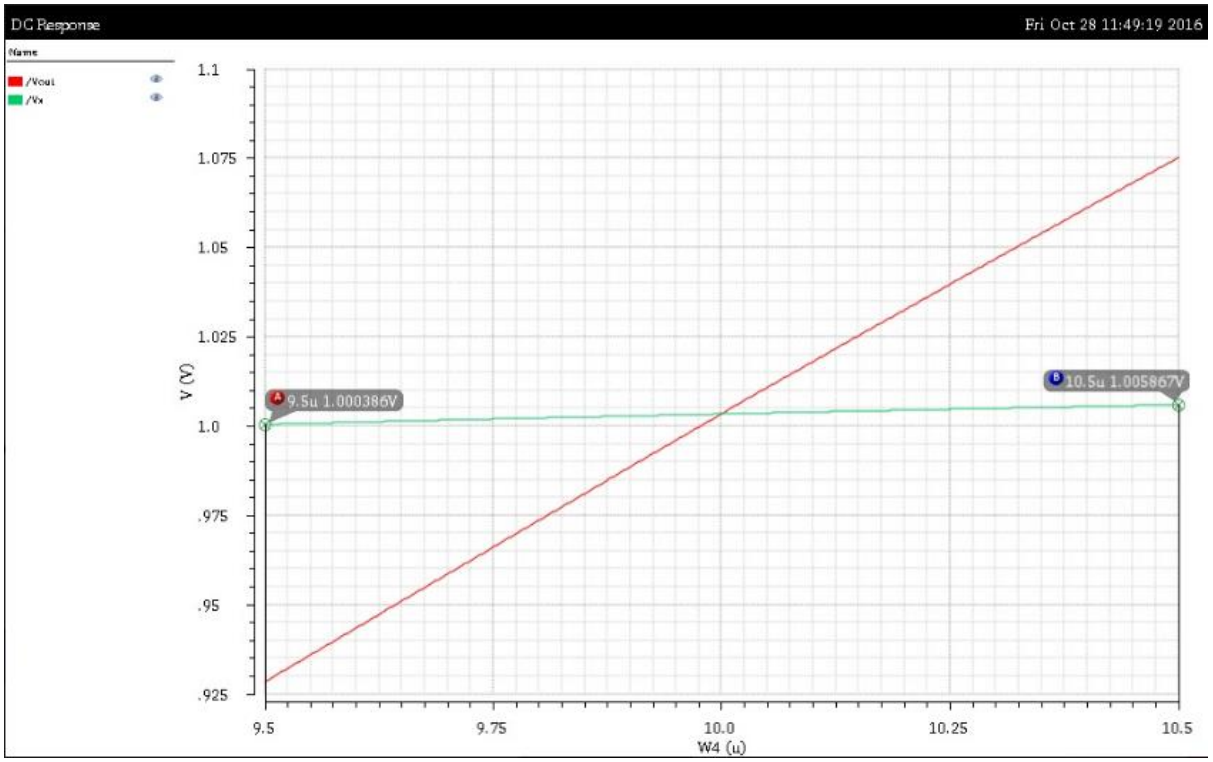
In the last part of lab 5 we varied the value of W in our M4 transistor by +/- 5%.

We see that changing the value of W should change the value of our current, however our current is fixed due to our current mirror circuit, therefore our VDS must change as all other parameters remain constant. As our VS must also remain constant our VD must increase to balance our equation as that will make VSD term smaller. This is what happens. Theoretically changing W in M4 should not change the value of our Vx however there are non-idealities in real MOSFETs which change the

voltage at Vx slightly. When our value for W at M4 is 10μm we see that the voltages are equal as then all transistor have same $\frac{W}{L} = \frac{10}{0.18}$.






DC Response
Fri Oct 28 11:49:19 2016
Name
/Vout
/Vx
1.1
1.075
1.05
1.025
1.0
.975
.95
.925
V (V)
9.5u 1.000386V
10.5u 1.005867V
9.5
9.75
10.0
10.25
10.5
W4 (u)