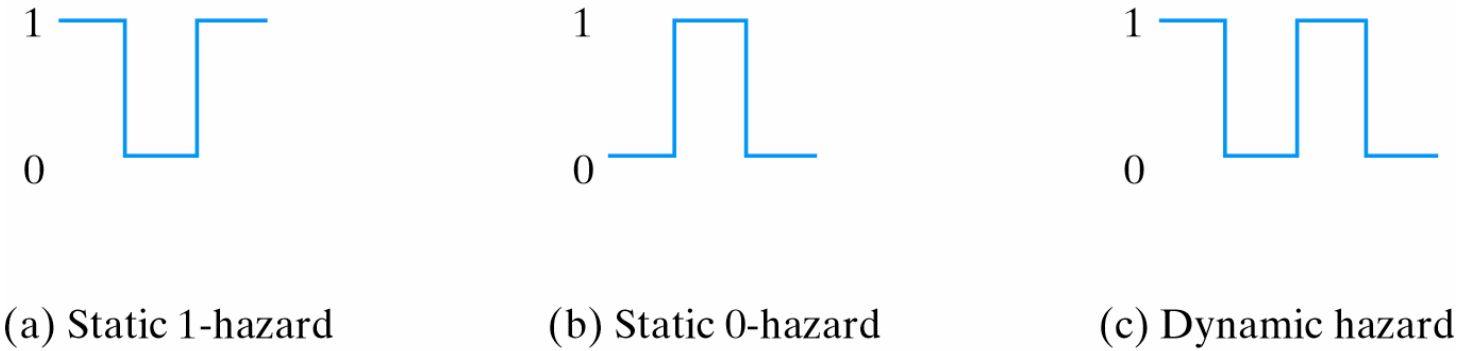
Asynchronous Logic II

Hazards

- In designing asynchronous sequential circuits, care must be taken to conform with certain restrictions and precautions to ensure that the circuits operate properly. The circuit must be operated in **fundamental mode** with only one input changing at any time and must be **free of critical races**.
- There is another phenomenon, called a **hazard**, that may cause the circuit to malfunction.
- Hazards are **unwanted switching transients** that may appear at the output of a circuit because different paths exhibit different propagation delays.

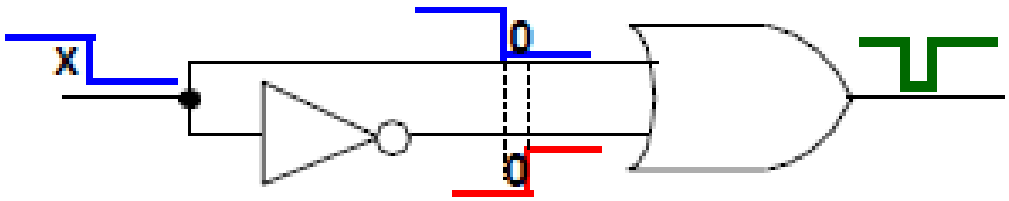
Hazards in Combinational Circuits

- Hazards occur in combinational logic, which may cause a temporary false output value.
- **Static hazard** is a momentary change in the output value when no change should occur.
- static-1 hazard: logic 1 momentarily goes to 0.
- static-0 hazard: logic 0 momentarily goes to 1.
- **Dynamic hazard**: logic level goes through three or more transitions.



(a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazard

Static-1 Hazards

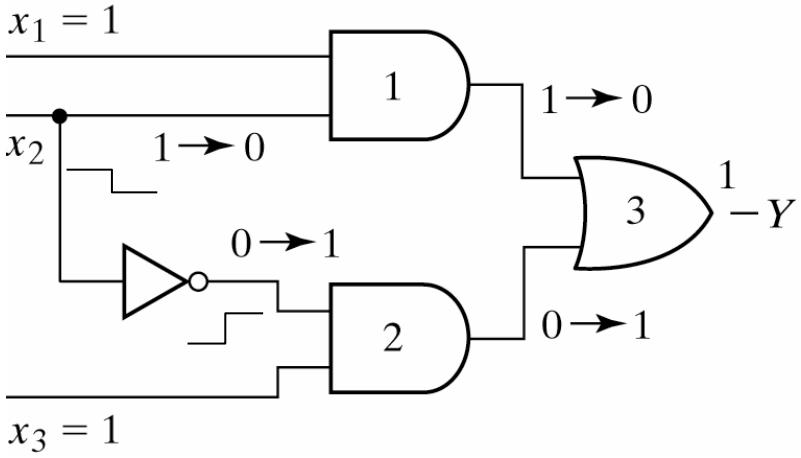


- Two parallel paths connected to an OR gate
- One path with an inverter.
- If x changes, different delays on two paths cause logic 1 momentarily goes to 0

Static-1 Hazards

- The **sum-of-products** (AND-OR circuit) may have a **static-1** hazard.

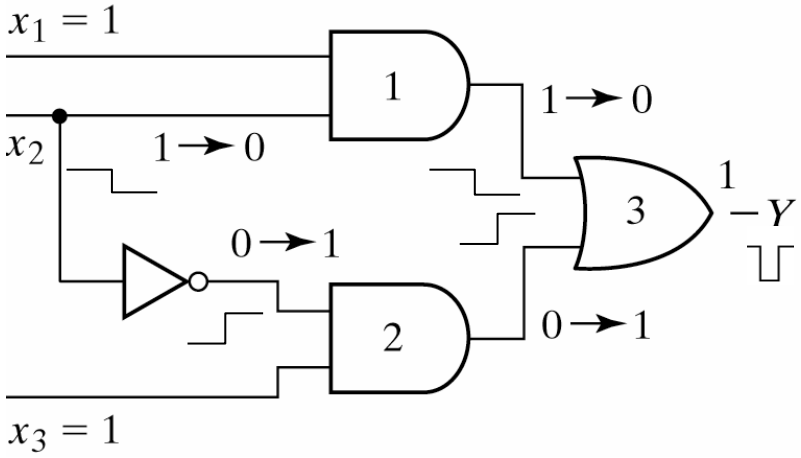
- Initially $x_1x_2x_3 = 111$,
  the output of the 1st gate is 1
  the output of the 2nd gate is 0
  the output of the 3rd gate is 1



- Then the input x_2 makes the transition from 1 to 0.

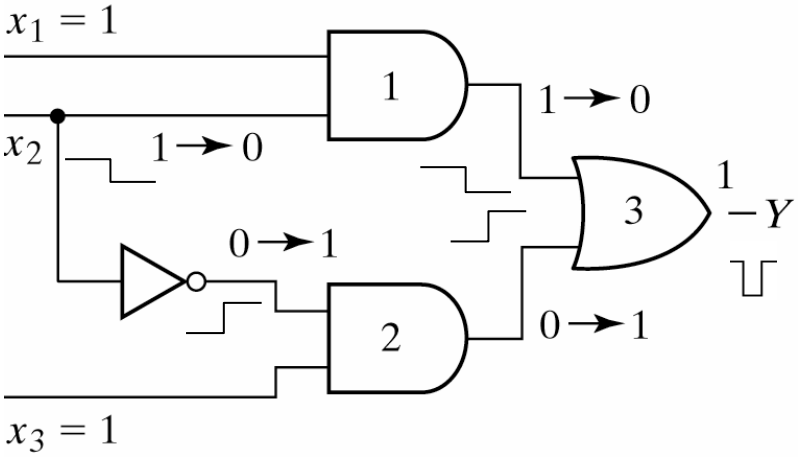
Static-1 Hazards

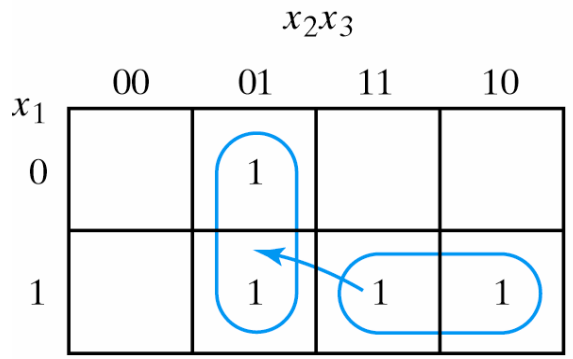
- Gate 1 output makes the transition $1 \rightarrow 0$
- Gate 2 output makes the transition $0 \rightarrow 1$
- Gate 2 does not respond as quickly because of the propagation delay through the inverter.
- As result there is a moment when both inputs to gate 3 are 0 and so the output will transition to 0 and then return to 1.



Static-1 Hazards

- The Karnaugh Map can be used to identify and remove hazards.
- In this circuit the transition of x_2 from 1 to 0 corresponds to the transition between the minterms 111 and 101

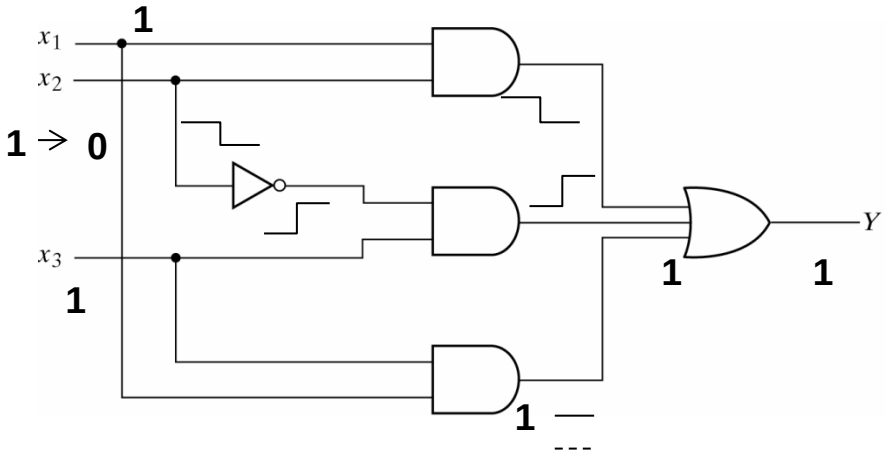


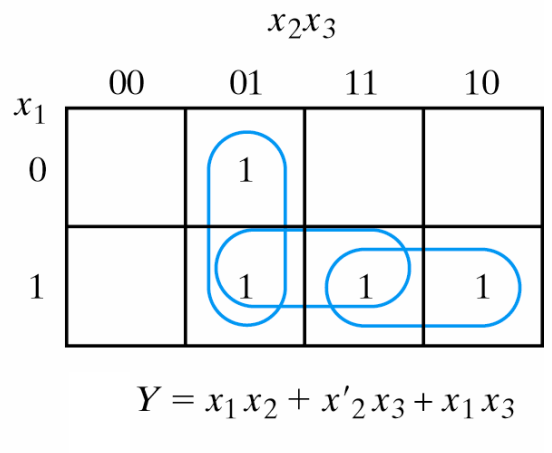


$$Y = x_1 x_2 + x'_2 x_3$$

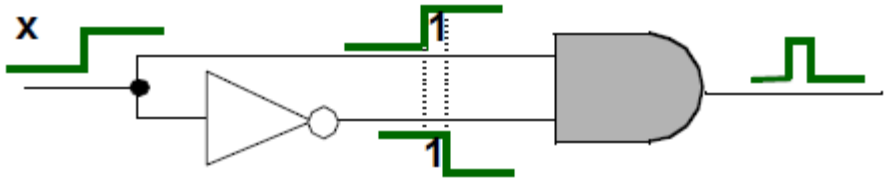
Static-1 Hazards

- If another gate is added to the circuit corresponding to the product term x_1x_3, the hazard is removed.
- This because the output of the new gate will keep the output at logic 1 despite the momentary transition.
- In general hazards can be removed by covering hazard minterms with a common product term.





Static-0 Hazards



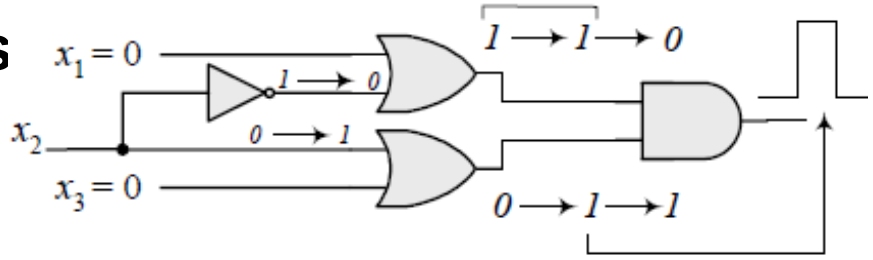
- Two parallel paths connected to an AND gate
- One path with an inverter.
- If x changes, different delays on two paths cause logic 0 momentarily goes to 1

Static-0 Hazards

- If circuit in **product-of-sums** form:

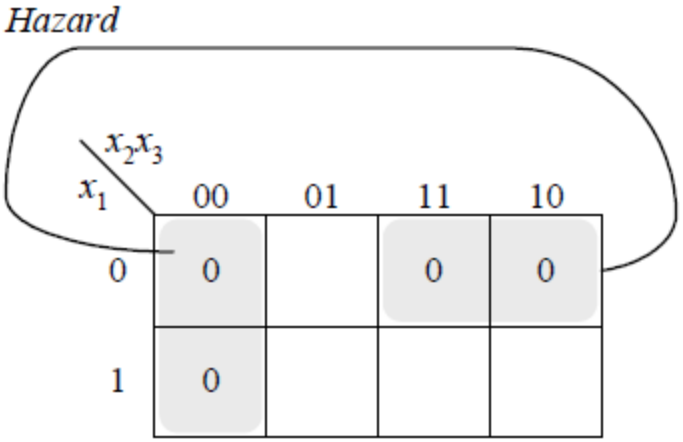
  $Y=(x_1 + x_2')(x_2 + x_3)$

  Cause **static-0** hazard.



- Add extra redundant terms to fill the gap:

  $Y=(x_1 + x_2')(x_2 + x_3)(x_1 + x_3)$

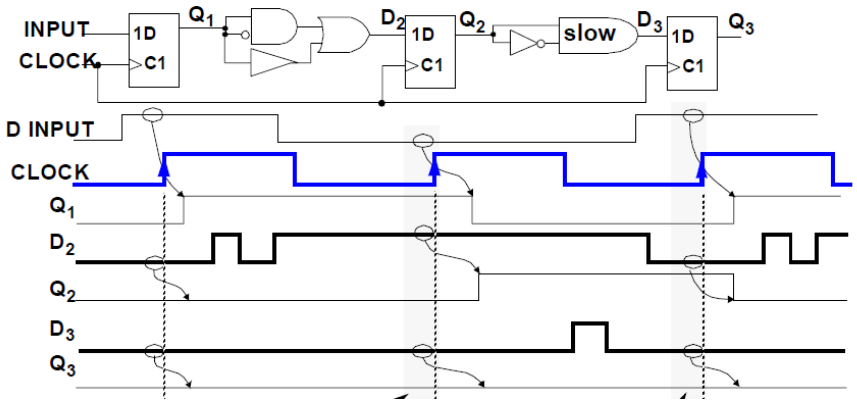


$Y=(x_1 + x_2')(x_2 + x_3)(x_1 + x_3)$

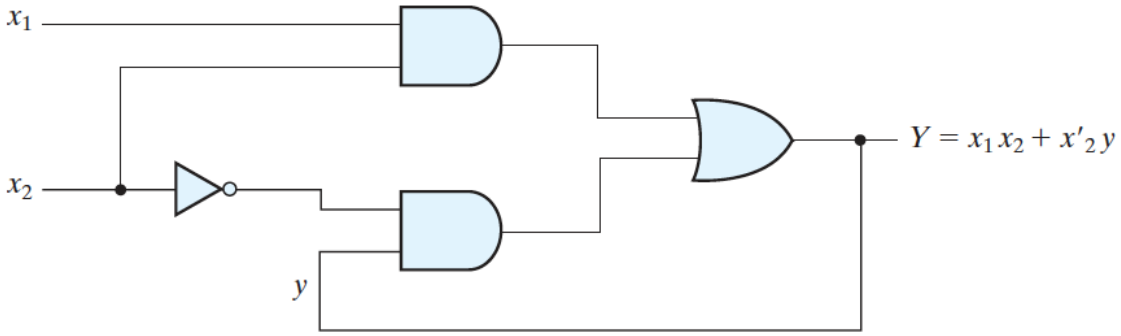
Add another term to remove hazard

Hazards in Sequential Circuits

- In normal combinational-circuit design associated with **synchronous** sequential circuits, hazards are of **no concern**, since momentary erroneous signals are not generally troublesome.



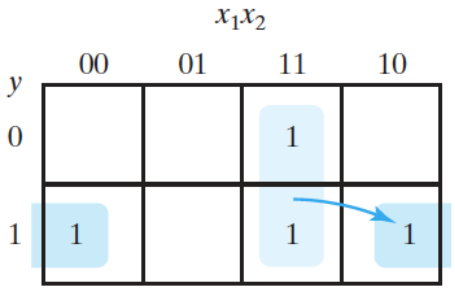
- However, if a momentary incorrect signal is **fed back** in an asynchronous sequential circuit, it may cause the circuit to go to the **wrong stable state**.



(a) Logic diagram

x_1x_2 / y	00	01	11	10
0	0	0	1	0
1	1	0	1	1

(b) Transition table



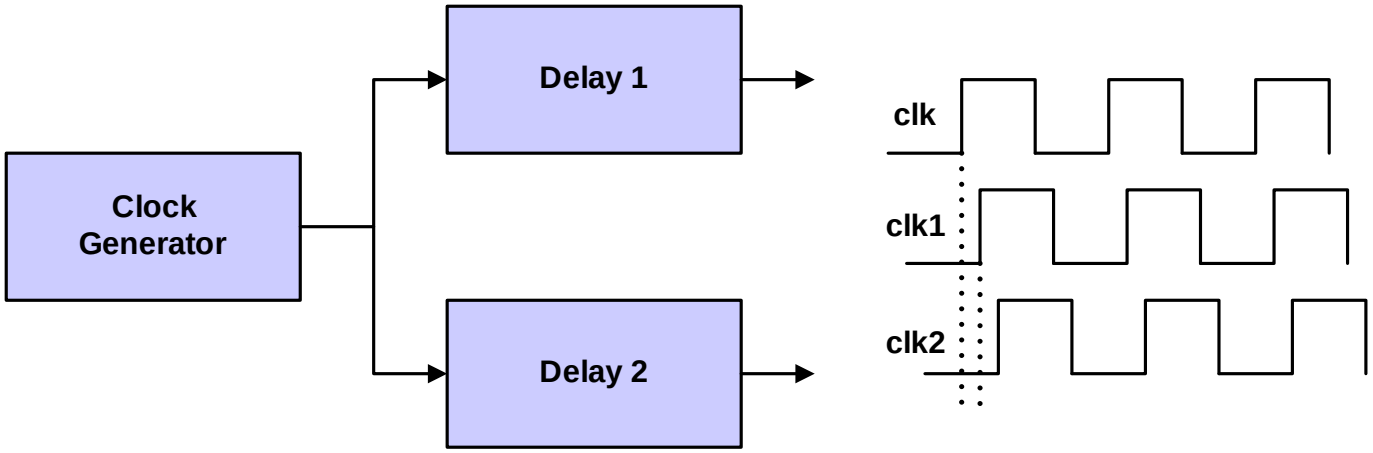
(c) Map for Y

Need to add an extra gate $Y=x_1x_2+x_2'y+x_1y$

- If the circuit is in total stable state $yx_1x_2=111$ and input x_2 changes from 1 to 0, the next total stable state should be 110.
- However, because of the hazard, output Y may go to 0 momentarily. If this false signal feeds back into gate 2 before the output of the inverter goes to 1, the output of gate 2 will remain at 0 and the circuit switch to the incorrect total stable state 010.

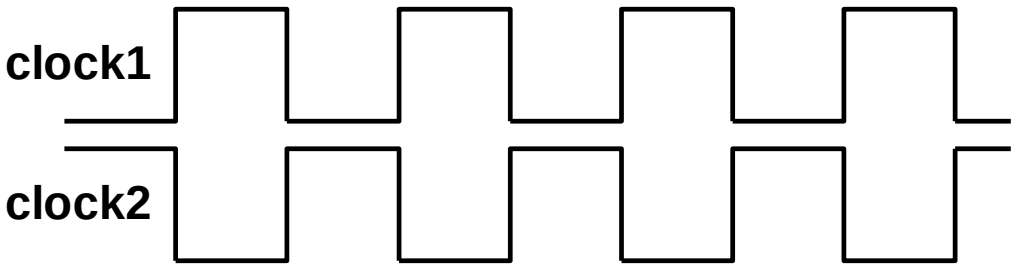
Clock Skew

- A single clock generator is producing a waveform for distribution to two parts of a digital system
  - Both clock waveforms should be occurring at the same time however due to the different logic paths, one clock lags behind the other.
  - The time delay between the two clock pulses is called **clock skew**.



Clock Skew

- Clock skew is not a problem at low frequencies, but at high frequencies it becomes a major problem.
- At 100MHz positive clock pulse occurs every 10 nanoseconds.
- If the clock skew is 5 nanoseconds, clock 1 and clock 2 are completely out of phase and the circuit becomes inoperative.



Clock Skew

- In very fast systems, the length of the conductors carrying clock signals must be considered.
- In such cases the sub-units may operate best asynchronously with respect to one another.

For example:

- Consider the transmission of data between one digital system and another.
- Distance may be too great to send data in parallel format along with a clock signal.
- In such cases, the data transmission must be done asynchronously.

Summary

- Asynchronous Logic circuits do not rely on synchronising clock signals and so are difficult to design.
- Fundamental mode ensures stability.
- Race Conditions may be non-critical or critical. Critical race conditions must be avoided.
- Static Hazards may be removed by introducing redundant logic corresponding to additional Karnaugh Map minterms/maxterms.