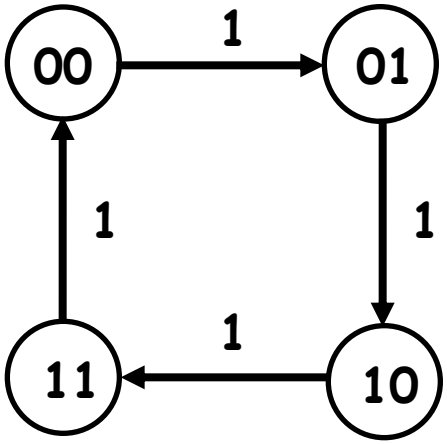
Synchronous Sequential Circuits I

Counters

Counters

- Counters are a special type of sequential circuits.
- The internal states (i.e., the flip-flop outputs) themselves serve as the “output”.
- In a count-up counter, the output value increases by one at each clock cycle. After the largest value, the output “wraps” back to 0.
- For instance, a 2-bit binary counter is something like this:

Present State		Next State	
A	B	A	B
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0



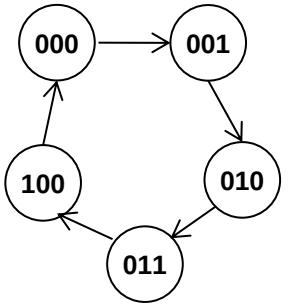
Counters

- Counters are available in two categories: **synchronous counters** and **ripple counters.**
- In a synchronous counter, the clock inputs of all flip-flops receive the common clock.
- In a ripple counter, a flip-flop output transition serves as a source for triggering other flop-flops. In other words, the clock input of some or all flip-flops are triggered, not by the common clock pulse, but rather by the transition that occurs in other flip-flop outputs.

Synchronous Binary Counter

- In a synchronous counter, the clock inputs of all flip-flops receive the common clock.
- We can design a synchronous counter following the sequential logic design procedures introduced in Lecture 8.
- e.g. consider a modulo-5 counter. The five output states of the counter are given by the table on the right.
- Our design will consist of three JK flip-flops (the outputs of which will be labelled A, B and C) and the connecting logic.

	A	B	C
t_0	0	0	0
t_1	0	0	1
t_2	0	1	0
t_3	0	1	1
t_4	1	0	0



Synchronous Binary Counter

- Since we know the next states of the counter from the time sequence transition, no need to list the next states separately.
- E.g., the transition of the B output from t_2 to t_3 is highlighted.
- To make this transition the corresponding J_B and K_B inputs can be known from the JK excitation table.

	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
t_0	0	0	0	0	X	0	X	1	X
t_1	0	0	1	0	X	1	X	X	1
t_2	0	1	0	0	X	X	0	1	X
t_3	0	1	1	1	X	X	1	X	1
t_4	1	0	0	X	1	0	X	0	X

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Synchronous Binary Counter

- Six Karnaugh maps corresponding to the inputs

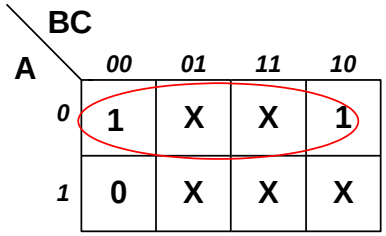
  $\{J_A, K_A, J_B, K_B, J_C, K_C\}$

  are created.
- For the J_A input the map is given as.

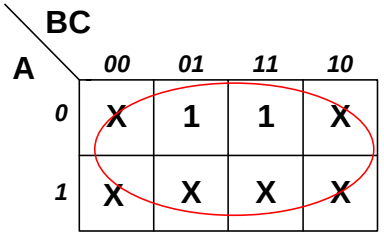
A \ BC	00	01	11	10
0	0	0	1	0
1	X	X	X	X

	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
t_0	0	0	0	0	X	0	X	1	X
t_1	0	0	1	0	X	1	X	X	1
t_2	0	1	0	0	X	X	0	1	X
t_3	0	1	1	1	X	X	1	X	1
t_4	1	0	0	X	1	0	X	0	X

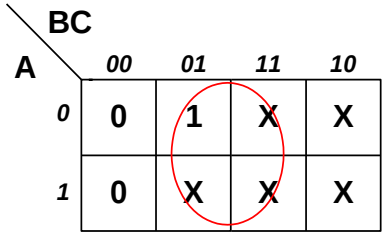
Synchronous Binary Counter



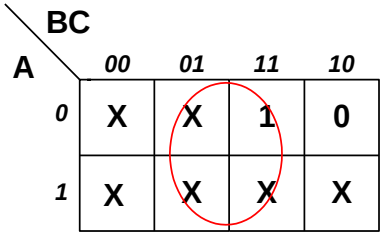
$$J_C = \overline{A}$$



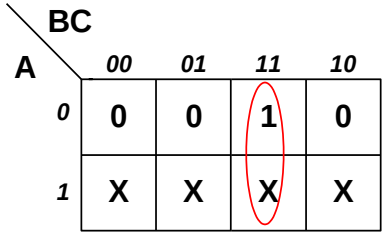
$$K_C = 1$$



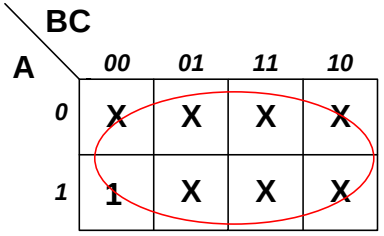
$$J_B = C$$



$$K_B = C$$



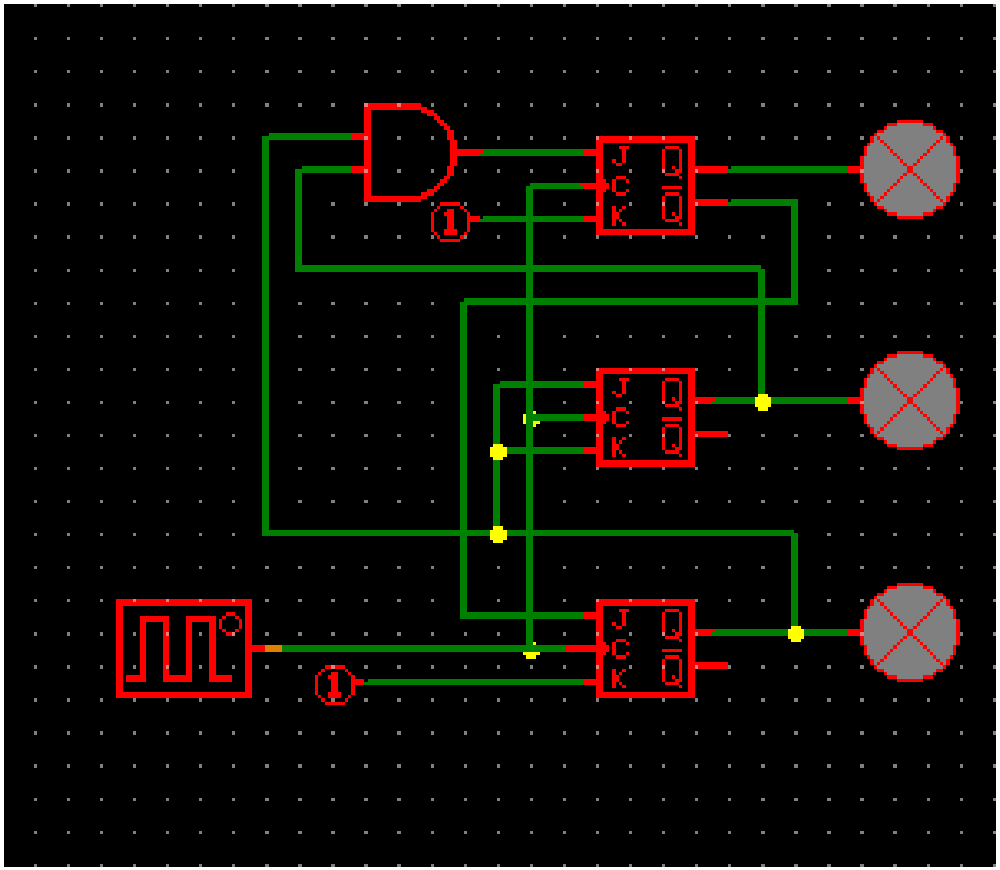
$$J_A = BC$$



$$K_A = 1$$

Synchronous Binary Counter

- The logic diagram of the counter shown in the right
  - lamps are connected to the flip-flop outputs and
  - a synchronising clock is connected.



Counter with Unused States

- A circuit with ***n*** flip-flops has 2^n binary states, but often not all of these states are used.
- In simplifying the input equations, the **unused states** may be treated as **don't care** conditions, which may cause the circuit to enter one of unused states.
- In that case, it is necessary to check if the circuit can eventually **return** to one of the valid states.
- If the circuit cannot return to the valid states, the unused state must be **re-assigned** to a specific state and **re-design** the circuit to force the return.

Counter with Unused States

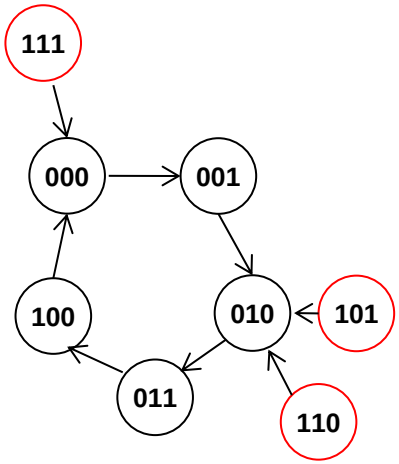
- For example, the modulo-5 counter only uses five states.
- 101,110,111 are not used. These states must be checked.

$$J_A = BC \qquad K_A = 1$$

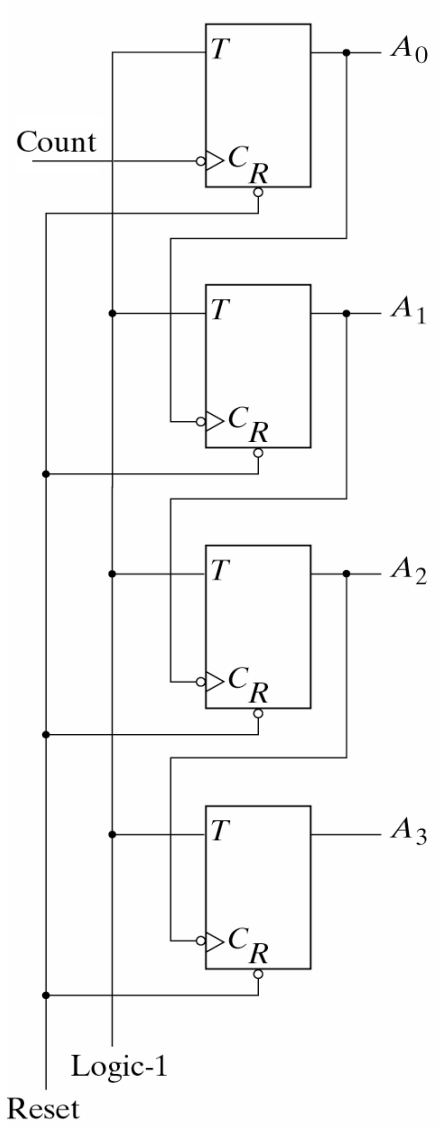
$$J_B = C \qquad K_B = C$$

$$J_C = \overline{A} \qquad K_C = 1$$

Present State			Flip-Flop Input						Next State		
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C	A	B	C
1	0	1	0	1	1	1	0	1	0	1	0
1	1	0	0	1	0	0	0	1	0	1	0
1	1	1	1	1	1	1	0	1	0	0	0



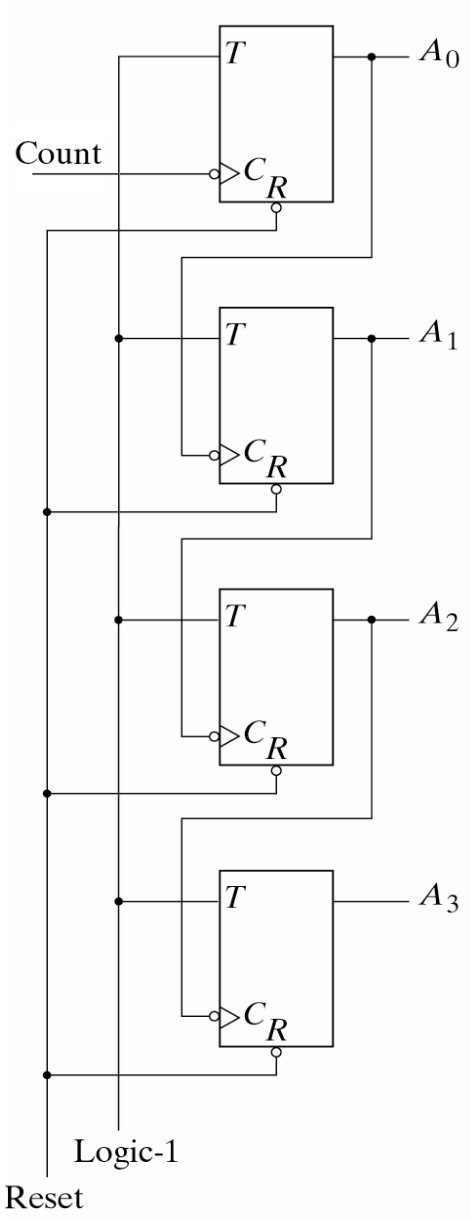
Binary Ripple Counter



- A ripple counter consists of a series connection of flip-flops.
- Logic 1 is inputted into each T-type flip-flop, so the output is toggled upon each clock edge.
- The first flip-flop is clocked by a count sequence.
- The output of each flip-flop is fed into the clock of the next flip-flop.

Binary Ripple Counter

- The counter output is initially set to $A_3A_2A_1A_0$=0000
- Upon the first negative clock edge the output of the first flip-flop is toggled, i.e. $A_3A_2A_1A_0$=0001
- Upon the second negative edge the output of the first flip-flop is toggled again.
- As this output transitions from high to low the second flip-flop toggles, i.e. $A_3A_2A_1A_0$=0010

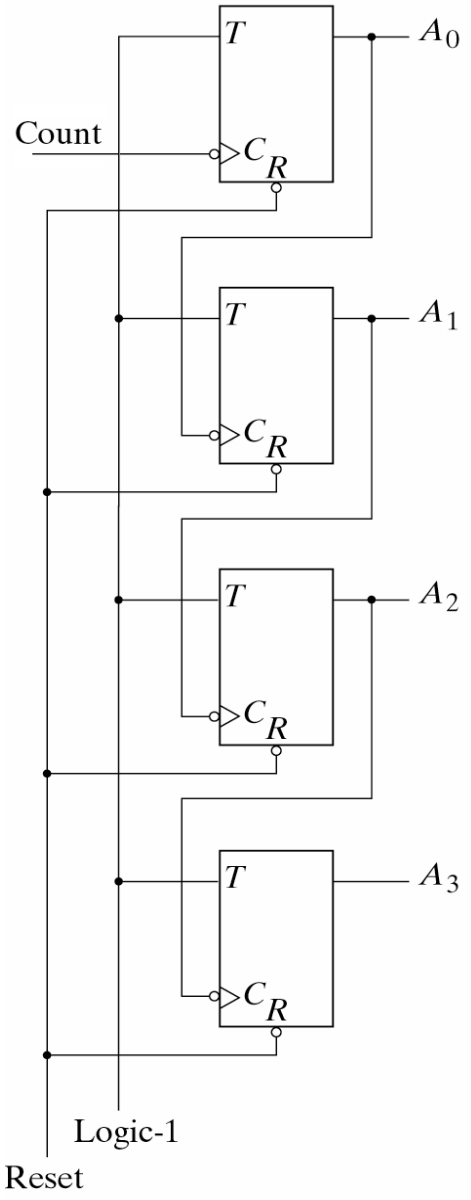


Binary Ripple Counter

- In three steps the output of the counter $A_3A_2A_1A_0$ transitions from
  0000 ⟶ 0001 ⟶ 0010

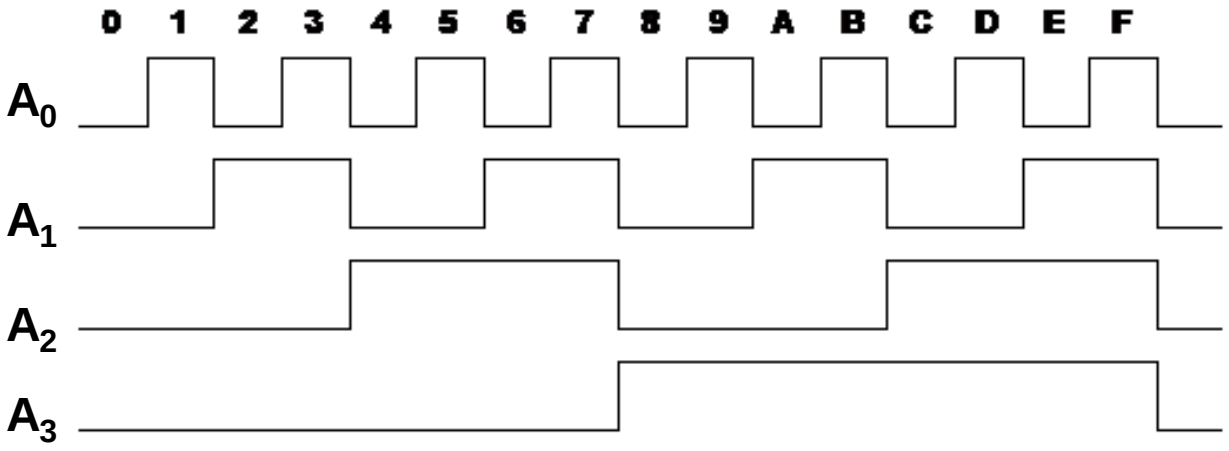
- In effect this circuit counts in binary.

- The counter is known as a ripple counter because of the way the clock signal ripples through the flip-flops.



Binary Ripple Counter

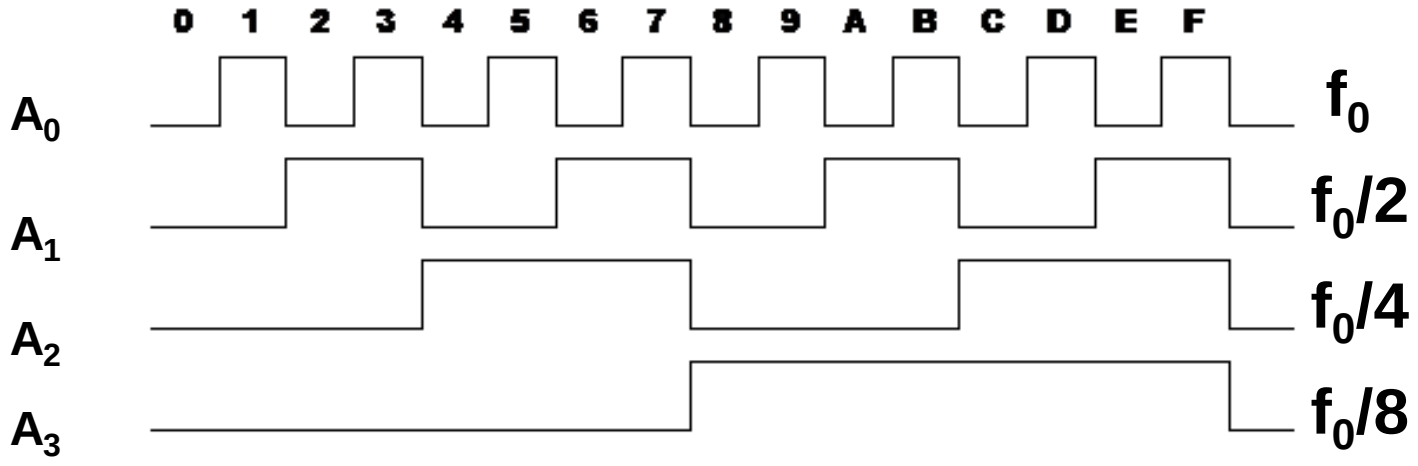
- As the count progresses the sequence
  0, 1, 2, 3, 4, 5, 6, 7, 8, …, 13, 14, 15
  is counted before the counter resets.



	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1
0	0	0	0	0

Binary Ripple Counter

- Ripple Counters are also known as divide by 2,4,8 counter, i.e. the original clock signal of frequency f_0 is used to produce clock signals of frequencies $f_0/2$, $f_0/4$ and $f_0/8$.



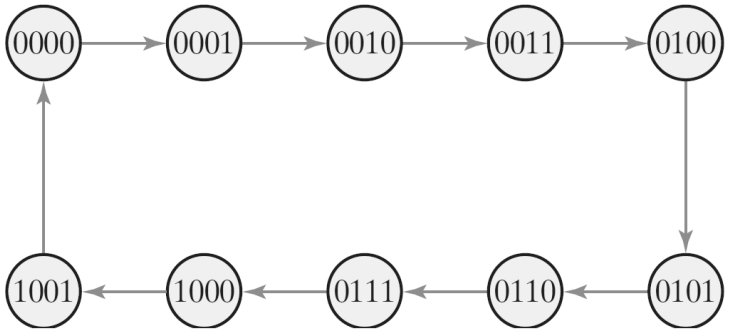
Binary Ripple Counter

Exercise

- How would the design change for a count-down counter?
- What connections would you use to implement a ripple counter with:
  - D flip-flops?
  - JK flip-flops?

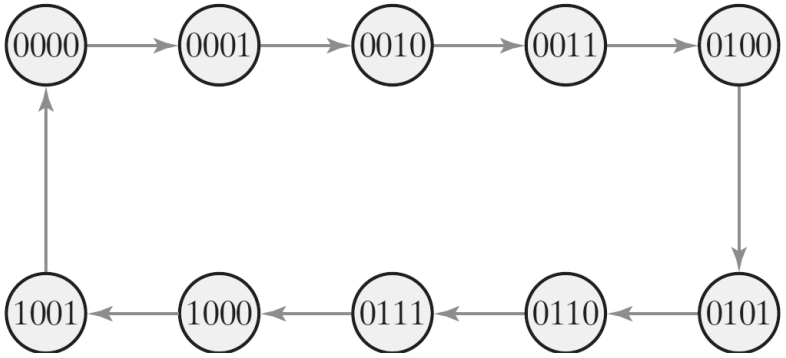
BCD Ripple Counter

- BCD: Binary Coded Decimal
- A decimal counter follows a sequence of 10 states and returns to 0 after the count of 9.
- It is similar to a binary counter, except that the state after 1001 is 0000.



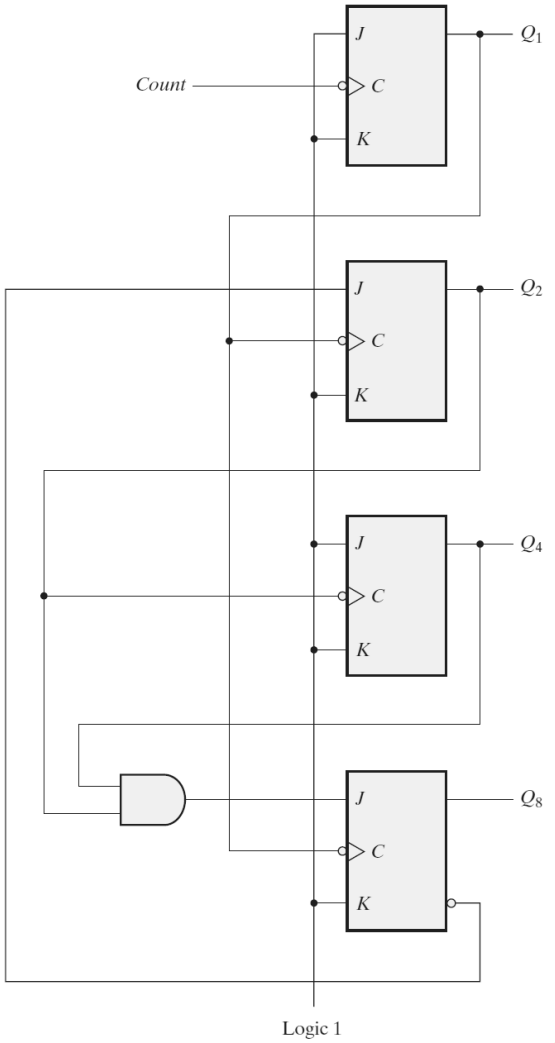
BCD Ripple Counter

- Q1 changes state after each clock pulse.
- Q2 complements every time Q1 goes from 1 to 0, as long as Q8=0. When Q8 becomes 1, Q2 remains at 0.
- Q4 complements every time Q2 goes from 1 to 0.
- Q8 remains at 0 as long as Q2 or Q4 is 0. When both Q2 and Q4 become 1, Q8 complements when Q1 goes from 1 to 0. Q8 is cleared on the next transition of Q1.



BCD Ripple Counter

- Four JK flip-flops can be used to represent 10 decimal digits.
- Remember that when the C (clock) input goes from 1 to 0, the flip-flops is set if J=1, is cleared if K=1, is complemented if J=K=1, and is left unchanged if J=K=0.
- The output of Q1 is applied to the C(clock) inputs of both Q2 and Q8 and output of Q2 is applied to the C(clock) input of Q4.
- The J and K inputs are connected either to a permanent 1 signal or to outputs of other flip-flops.



Multi-Decade Ripple Counter

- The 4-JK flip-flops BCD counter only can count from 0 to 9, which is called a **decade** counter.
- Multiple-decade counters can be constructed by connecting BCD counts in cascade, one for each decade.