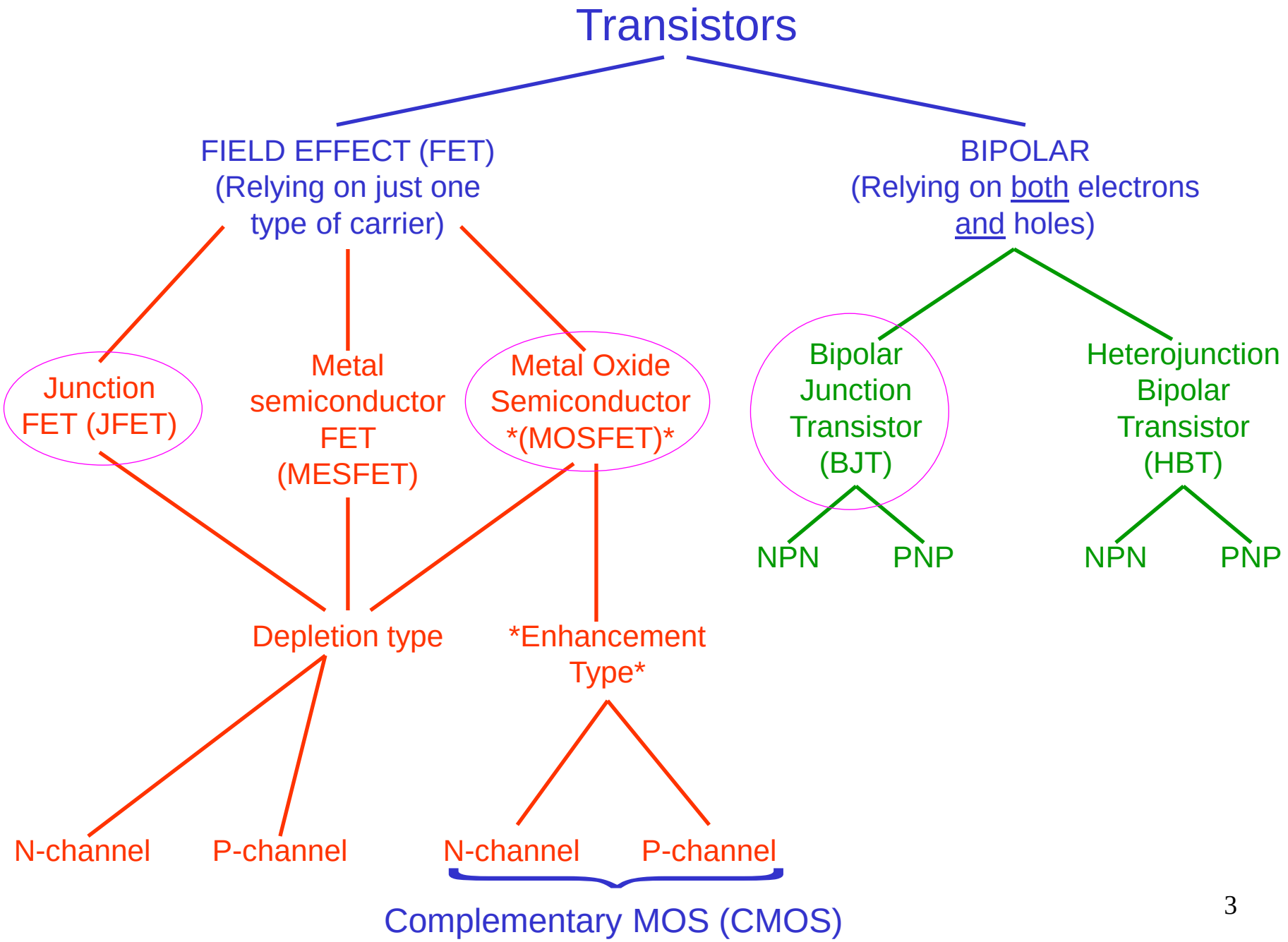
Chapter 10

Transistors

The JFET

Transistors - General Comments

- Transistors are enormously useful in Electrical & Electronic Engineering. They are versatile and provide extremely valuable functions in electronic circuits;
- The PN junction has just 2 terminals, transistors generally have 3;
- The first transistor was invented in Bell Labs in 1947 and there are now numerous different kinds of transistor;
- Transistors tend to be used for two basic kinds of purpose:
  - As **signal amplifiers**: When suitable DC bias is applied, a transistor can be used to increase the amplitude of a time-varying signal (voltage or current), i.e. to magnify a signal. Often, the product of signal current and voltage (the signal power) is magnified, as in a *power amplifier*. With feedback, an amplifier can be converted to an *oscillator* - a free-running circuit producing a continuous (e.g.) sinusoidal signal from the DC power;
  - As **an electronic switch**: Transistors can use the voltage (or current) at one of their terminals to switch the flow of perhaps a much larger current through the other two. These two states 'ON' and 'OFF' of a transistor can also be used in digital electronics to represent the binary digits '0' and '1' enabling transistors to store and process digital signals.


Transistors
FIELD EFFECT (FET)
(Relying on just one type of carrier)
BIPOLAR
(Relying on both electrons and holes)
Junction FET (JFET)
Metal semiconductor FET (MESFET)
Metal Oxide Semiconductor *(MOSFET)*
Bipolar Junction Transistor (BJT)
Heterojunction Bipolar Transistor (HBT)
NPN
PNP
NPN
PNP
Depletion type
Enhancement Type
N-channel
P-channel
N-channel
P-channel
Complementary MOS (CMOS)

Field Effect Transistors (FETs)

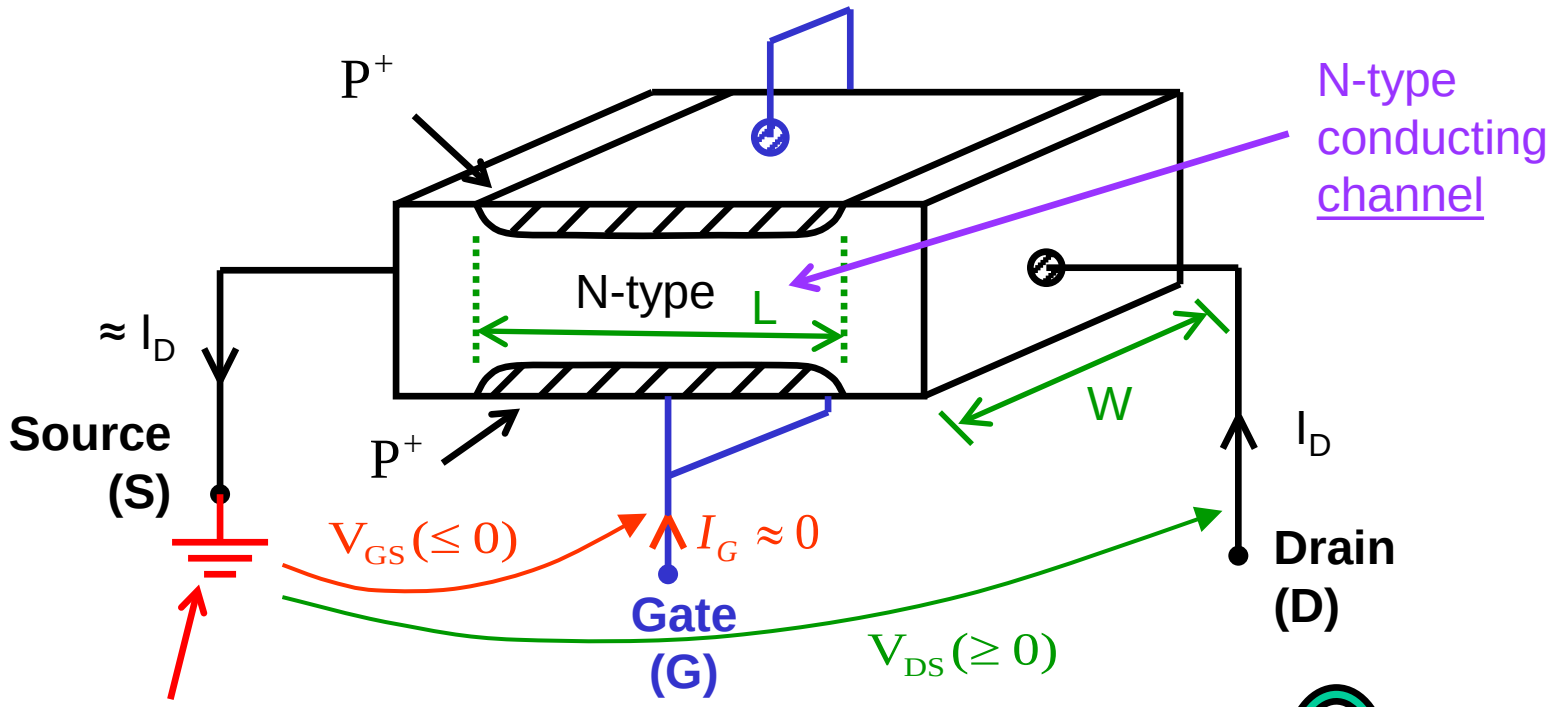
- This is the oldest transistor concept, originating in a patent by Lilienfeld in the 1920s, although practical realisation had to wait until the 1950s;
- All FETs share some common features: current may flow in a conducting channel connecting a Source (S) region to a Drain (D) region.
- The current flowing is controlled by the voltage (or electric field) applied to a third Gate (G) electrode, which under normal conditions is electrically isolated from the remainder of the structure (i.e. no DC current should normally flow through the Gate terminal). Exactly how this control is exercised varies between different kinds of FET;
- If the channel is naturally open-circuit, and the Gate voltage causes current to flow, the FET is said to be "enhancement type" (e.g. MOSFET)
- Conversely, if current flow tends to be suppressed by the Gate voltage the FET is described as "depletion type" (e.g. JFET)
- In an N-channel FET, electrons dominate the flow in the channel whereas holes dominate the flow in a P-channel FET.

The Junction FET (JFET)

The Junction FET

- The Junction FET or **JFET** is conceptually the simplest kind of transistor, although its usefulness in practical applications (in Silicon) is rather limited;
- The JFET is closely related to a family of advanced high-frequency microwave transistors including the MESFET (METal-Semiconductor FET), often made with GaAs or even more elaborate material systems;
- In a JFET, the **control of the conducting channel is effected by using the voltage on the Gate to vary the width of a reverse-biased PN junction depletion layer**, thereby changing (reducing) the cross-sectional area of the channel . JFETs are thus *depletion mode FETs*

Idealised Structure of an N-Channel JFET (Using Reverse-Biased Gate P^+N Junction)

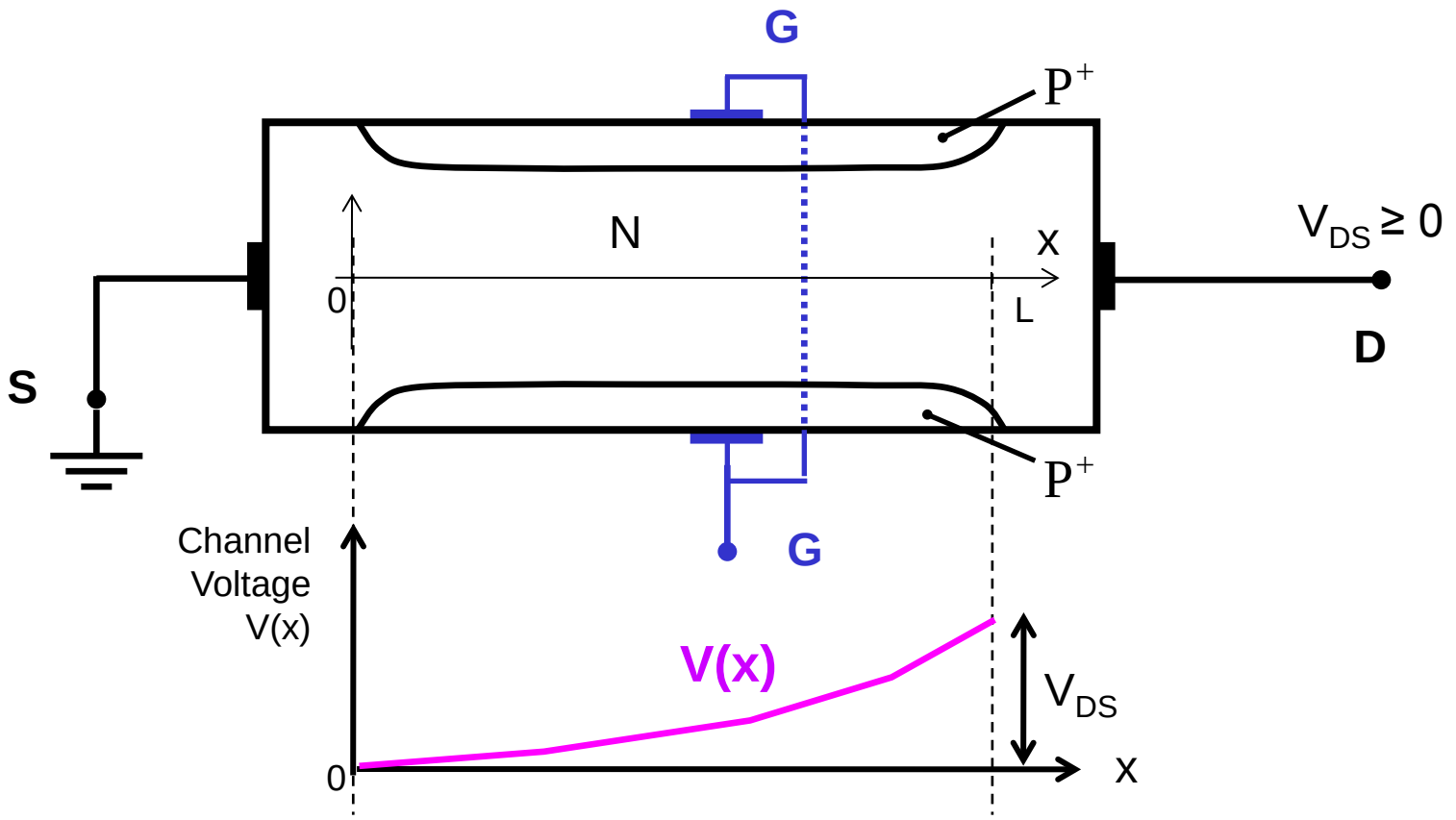


We will always assume that the Source is grounded here i.e. "Common Source" configuration

L : channel length
W : channel width

** *Key FET* ***Geometrical*** *Parameters*

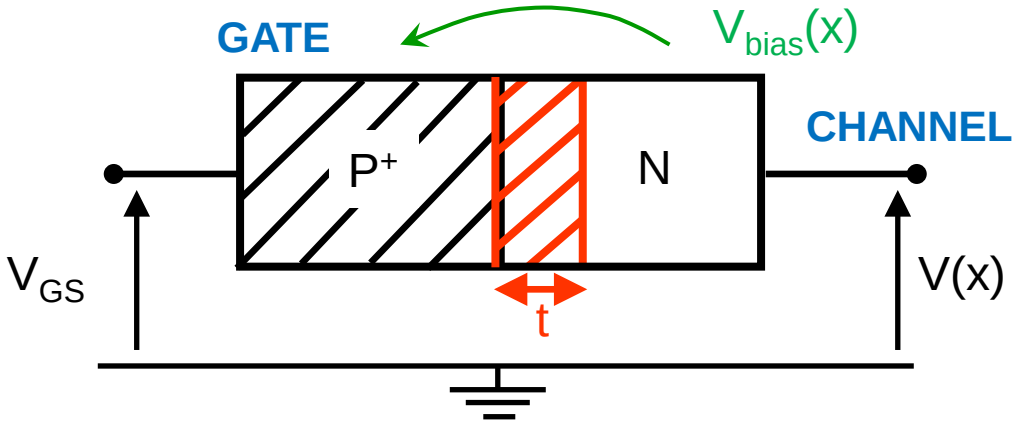
Assume $V_{DS} > 0$: *Channel Voltage V(x)*



- The displacement along the centre-line of the channel is 'x', ranging between x=0 and x=L. The channel voltage at any 'x' is V(x) and must vary from V(0) = 0 to V(L) = V_{DS} (> 0, i.e. it is always positive, at any x)

Shape of the Depletion Layer in a JFET

- If V_{GS} is < 0 and V_{DS} > 0, then the voltage V(x) along the channel from S to D is always positive, and so each of the two (one-sided) P^+N junctions is *continuously reverse-biased* along the channel.
- To determine how much reverse bias exists we can use the following picture at any channel position 'x':



We will use "t" to represent depletion layer width here, to avoid confusion with the channel width "W"

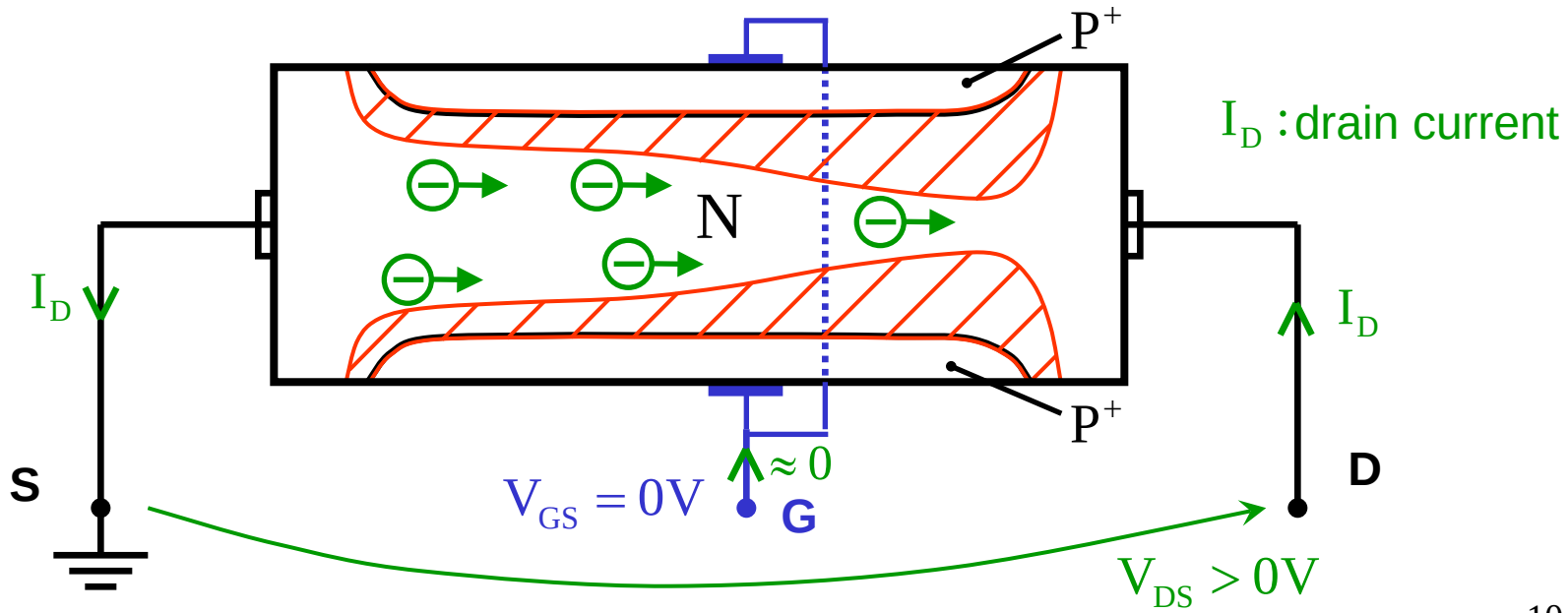
- By KVL, $V_{GS} = (V_{bias}(x) + V(x)) \Rightarrow V_{bias}(x) = (V_{GS} - V(x))$, so that (1-sided):

$$t(x) = \sqrt{\frac{2\varepsilon(\phi_i - V_{bias})}{qN_D}} = \sqrt{\frac{2\varepsilon(\phi_i - V_{GS} + V(x))}{qN_D}}$$

$\Rightarrow$ Depletion layer widens at drain end

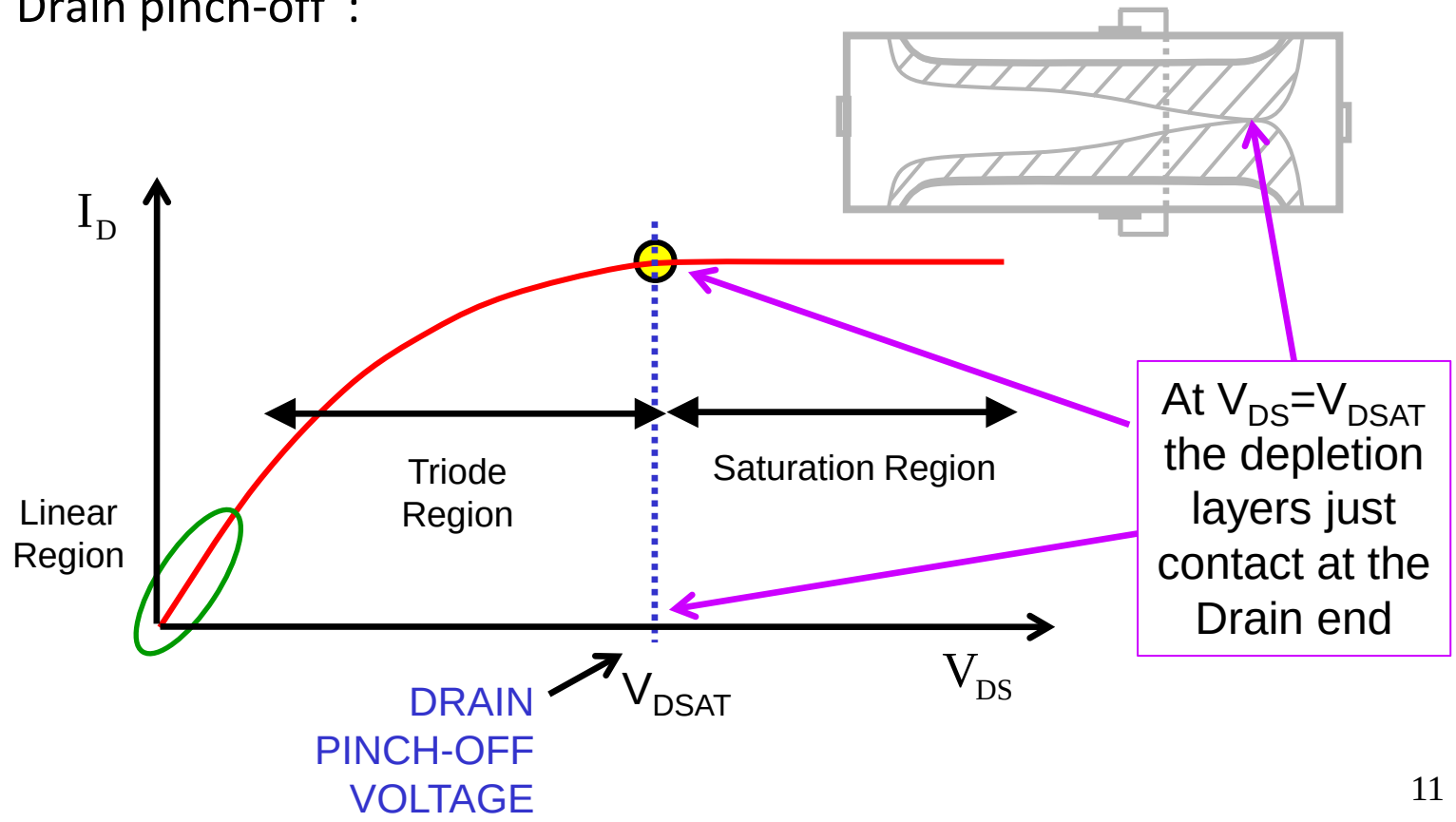
Depletion Layers in N-channel JFET

- The channel voltage V(x) varies from V(x=0)=0 (Source end) to V(x=L) = V_{DS} (Drain end). Therefore, the depletion layer width is narrowest at the Source end and widest at the Drain end;
- As V_{DS} is increased for a fixed (negative) V_{GS}, the *channel* tends to become narrower (or become "pinched-off") towards the Drain end, causing the Drain current I_D to increase sub-linearly with > V_{DS}:



Drain Current Characteristic (fixed V_{GS})

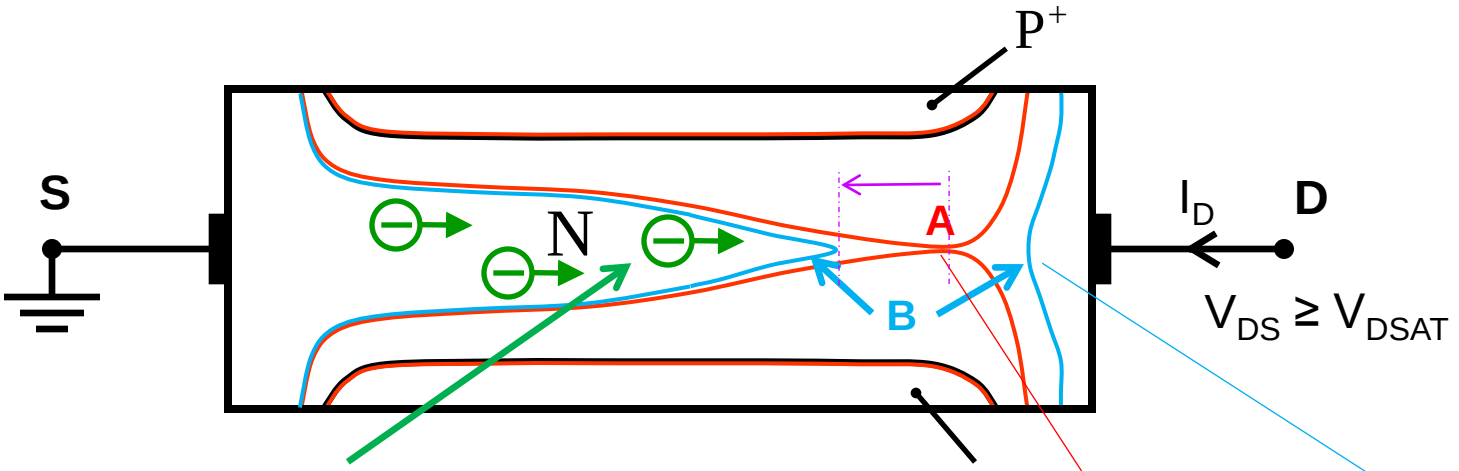
- For a fixed $V_{GS} < 0$, as V_{DS} is increased from zero, the drain current in the JFET (I_D) varies with V_{DS} as follows, showing 3 general regions: ***linear***, ***triode*** (or sub-linear) and ***saturation***, the latter beginning at "Drain pinch-off":



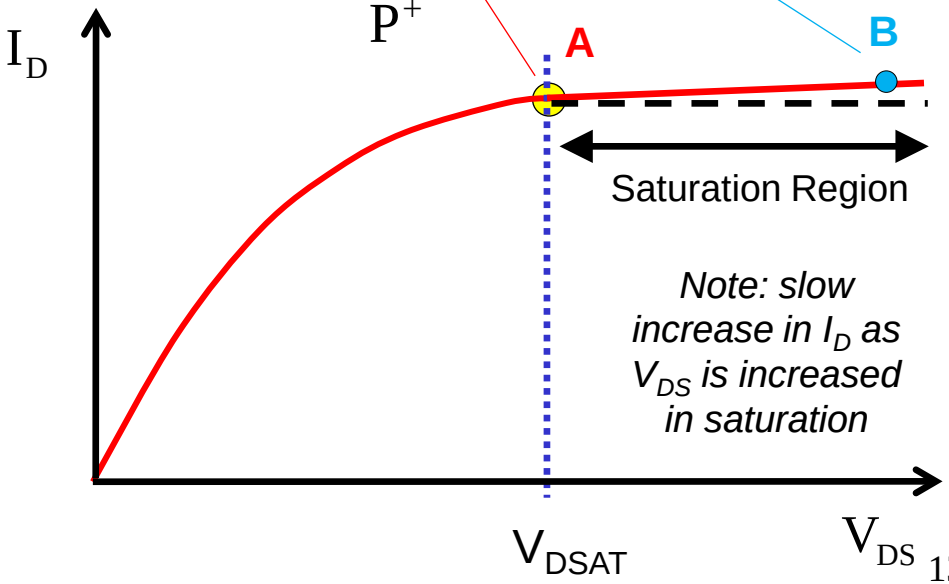
Why Does Drain Current Not Switch to Zero for $V_{DS} >= V_{DSAT}$?

- Behaviour in the saturation region is quite complex. Electrons are accelerated along conducting channel before the point at which the two depletion layers meet;
- These "hot" electrons are injected into the high electric field region of the (merged) depletion layers, where they drift at their *saturation* or *scattering limited* velocity (v_{ns});
- The current density then "saturates" to an approximate value: $J_{sat} \approx q.n.v_{ns}$, leading to current saturation
- As V_{DS} is increased beyond V_{DSAT}, the merged depletion layer simply widens at the Drain end, although the fact that the initial point of contact moves slightly towards the Source, causes a small increase of the current in saturation

Behaviour Beyond Drain Pinch-Off

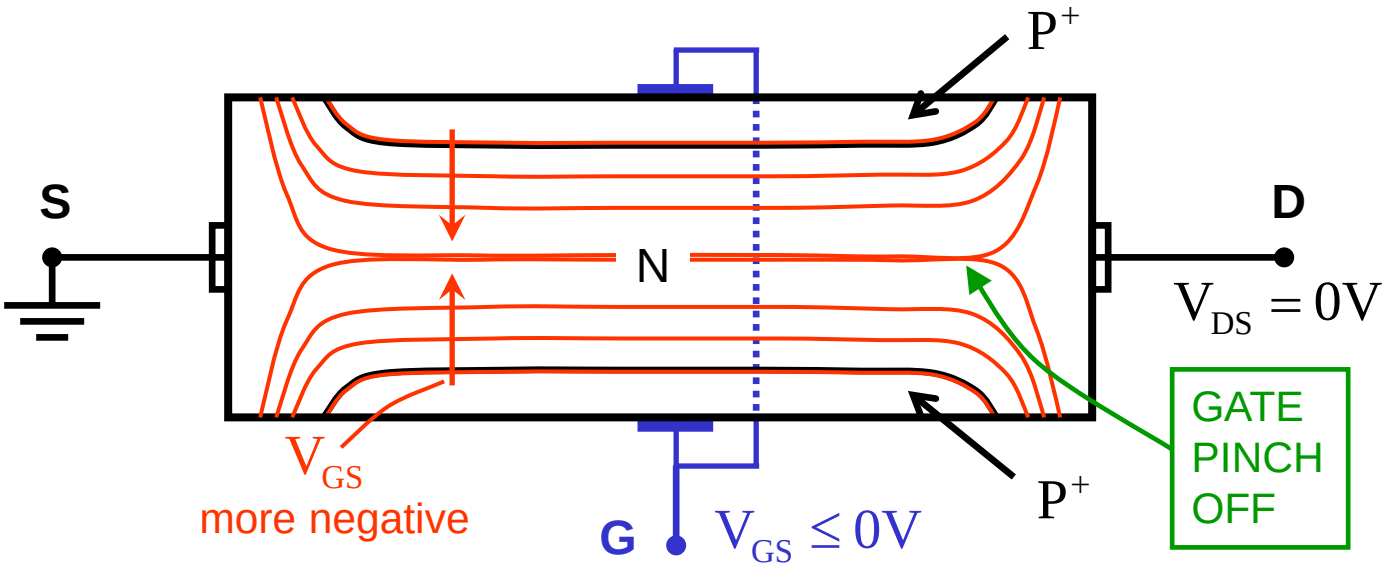


Hot electrons travelling at saturated velocity: can be injected across high field region at contact between two depletion layers.



Gate Pinch-Off and the Pinch-Off Voltage

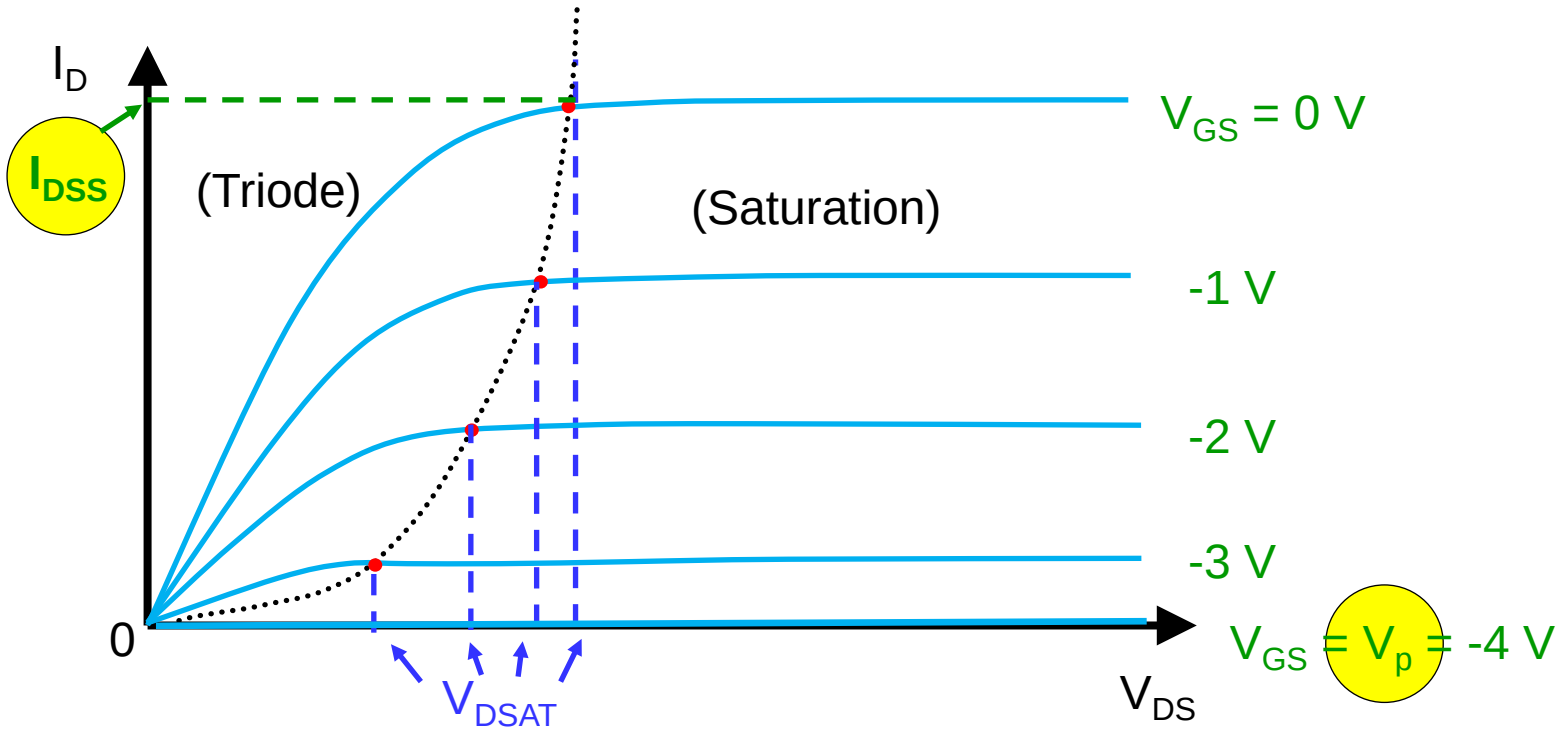
- Now consider a different bias condition: apply **zero bias** to the **Drain** ($V_{DS} = 0$) and systematically make V_{GS} more negative ($V_{GS} \leq 0$);
- Eventually, the depletion layers contact continuously along the channel: the device is then completely cut off;
- This condition is called **Gate pinch-off**, and the value of V_{GS} at which it occurs is called the **Pinch-Off Voltage $V_{GS} = V_P$**



See Applet: http://jas.eng.buffalo.edu/education/jfet/index.html

JFET DC Drain Characteristics

- Putting all this together, we find the following static Drain Characteristics for the N-Channel JFET (for illustration, a typical value is assumed for the Pinch-off Voltage: V_P = -4.0V)

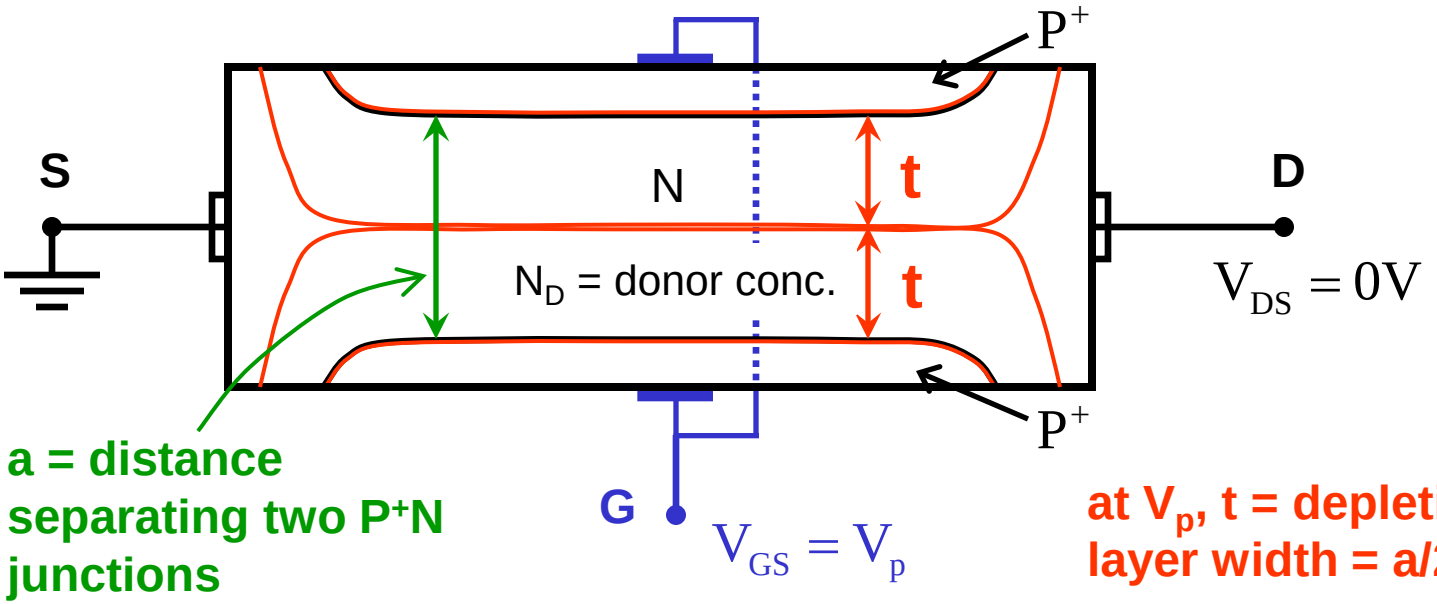


*** I_{DSS} and V_P are key **circuit-level** parameters for the JFET*

http://jas.eng.buffalo.edu/education/jfet/

Formula to Calculate Pinch-Off Voltage V_P

- Let the vertical displacement separating the two P^+N junctions be "a";
- It is clear that when $V_{GS} = V_P$, the depletion layer width "W" for each junction must be t = (a/2)



$$t = (W) = \sqrt{\frac{2\varepsilon \cdot (\phi_i - V_{GS} + V(x))}{qN_D}} \qquad \Rightarrow \frac{a}{2} = \sqrt{\frac{2\varepsilon(\phi_i - V_p + 0)}{qN_D}}$$

Expression for JFET Pinch-Off Voltage

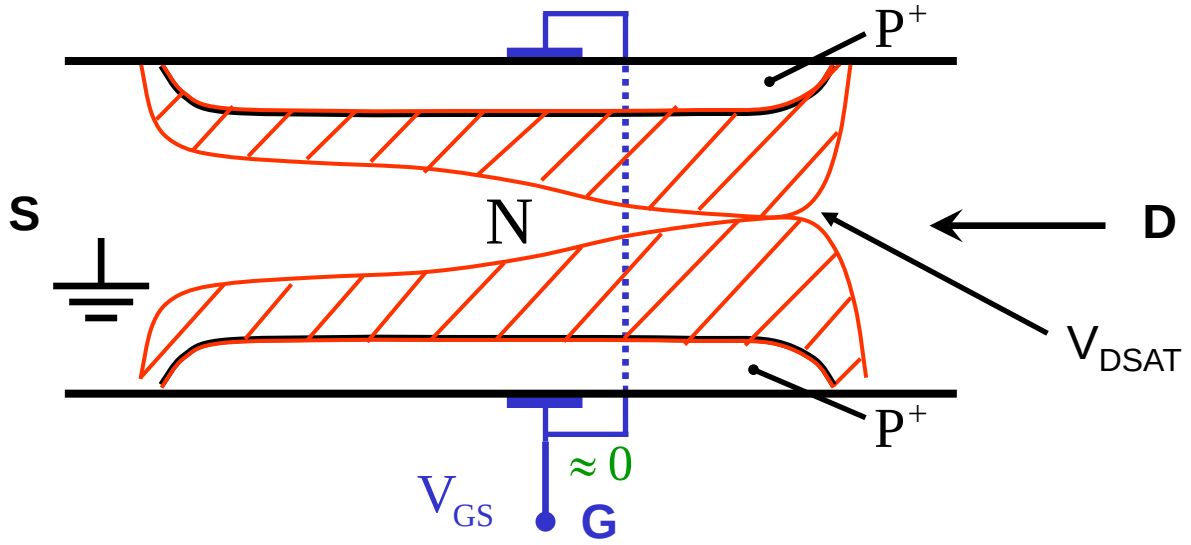
- Re-arranging the last equation, it is easy to derive the following expression for the Pinch-Off Voltage (V_P) (prove this result as an exercise):

$$V_P = \varphi_i - \frac{q \cdot N_D \cdot a^2}{8 \cdot \epsilon}$$

do not remember

- For an N-channel JFET, the value calculated will always turn out to be negative, and will typically be a few V in magnitude.

Relationship Between V_{DSAT} and V_P



- Suppose $V_{DS} = V_{DSAT}$ at some V_{GS}. Then at the point of contact between the 2 depletion layers:

$$t = \frac{a}{2} = \sqrt{\frac{2\varepsilon(\phi_i - V_{GS} + V_{DSAT})}{qN_D}}$$

- Comparing with the earlier expression for V_P, we find a simple relationship connecting V_{DSAT} and V_P at a given V_{GS}: $(V_{GS} - V_{DSAT}) = V_P$, or

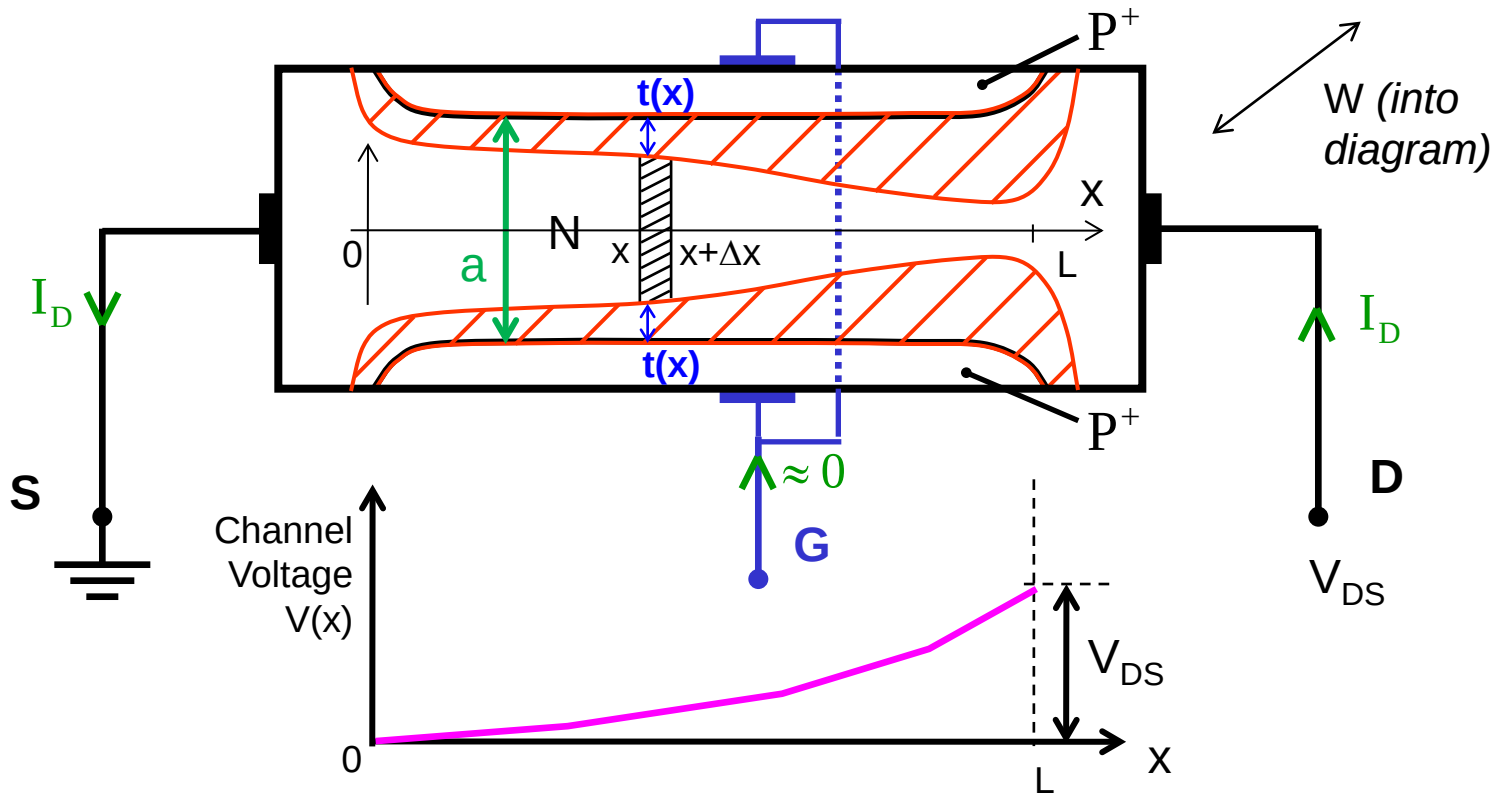
$$\boxed{V_{DSAT} = (V_{GS} - V_P)}$$

[e.g. V_P = -4V; V_{GS} = -1V => V_{DSAT} = +3V]

Example 10.1

Analysis for JFET DC Current in Triode Region

- We restrict the bias voltages such that: $V_P \le V_{GS} \le 0$ and $0 \le V_{DS} \le V_{DSAT}$. This means the device is operated in the triode region



Assumptions

- Assume current flow in channel is essentially 1-D (valid if L >> a). This is called the "Gradual Channel Approximation" (originally made by Schockley);
- Neglect diffusion and assume constant mobility in channel;
- Note that I_D is independent of 'x'. Thus we can then apply Ohm's Law to the shaded elemental section of the channel between "x" and "(x+Δx)":

$$\Delta V(x) = I_D.\Delta R(x)$$

- Where ΔR(x) is the resistance of the elemental section. Use:

$$R = \frac{"\rho \cdot l"}{A} = \frac{l}{\sigma \cdot A} = \frac{l}{(q \cdot N_D \cdot \mu_n) \cdot A}$$

Analysis in Triode Region (Study Optional)

- Substitute for length: l = Δx and area: A = (a-2.t(x)).W to obtain:

$$\Delta R(x) = \frac{\Delta x}{qN_D\mu_n(a-2t(x))\cdot W}$$

$$\Rightarrow \Delta V(x) = \frac{I_D\cdot\Delta x}{qN_D\mu_n(a-2t(x))\cdot W}$$

- Now divide across by Δx and take limit as Δx $\rightarrow$ 0:

$$I_D = qN_D\mu_n(a-2t(x))\cdot W\cdot\frac{dV}{dx}$$

...where:

$$t(x) = \sqrt{\frac{2\varepsilon(\phi_i - V_{GS} + V(x))}{qN_D}}$$

Analysis in Triode Region (Study Optional)

- Substitute for t(x):

$$\Rightarrow I_D = qN_D\mu_n\left(a - 2\sqrt{\frac{2\varepsilon(\phi_i - V_{GS} + V(x))}{qN_D}}\right).W\frac{dV(x)}{dx}$$

- Now integrate both sides wrt "x" between the limits of 0 and L and divide by L:

$$\Rightarrow \frac{1}{L}\cdot\int_0^L I_D\cdot dx = I_D = \frac{qN_D\mu_n}{L}\int_0^L\left(a - 2\sqrt{\frac{2\varepsilon(\phi_i - V_{GS} + V(x))}{qN_D}}\right)\cdot W\cdot\frac{dV(x)}{dx}\cdot dx$$

- Change variable of integration on RHS from "x" to "V":

$$\Rightarrow I_D = \frac{qN_D\mu_n W}{L}\cdot\int_{V(0)}^{V(L)}\left(a - 2\sqrt{\frac{2\varepsilon\cdot(\phi_i - V_{GS} + V)}{qN_D}}\right)\cdot dV$$

- But V(0)=0 and V(L)=V_{DS}:

$$\Rightarrow I_D = \frac{qN_D\mu_n W}{L}\cdot\int_0^{V_{DS}}\left(a - \sqrt{\frac{8\varepsilon}{qN_D}}\cdot\sqrt{(\phi_i - V_{GS} + V)}\right)\cdot dV$$

Final Result for Static Current

- This can be integrated (optional exercise) to give the final result:

do not remember

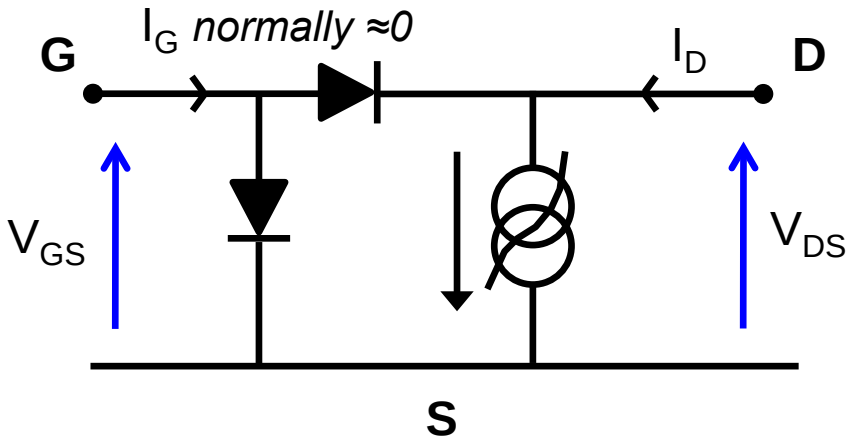
$$I_D = \frac{qN_D\mu_n Wa}{L}\cdot\left[V_{DS} - \frac{2}{3}\sqrt{\frac{8\varepsilon}{qN_D a^2}}\cdot\left\{\left(\phi_i + V_{DS} - V_{GS}\right)^{3/2} - \left(\phi_i - V_{GS}\right)^{3/2}\right\}\right]$$

- This equation can be used for V_{DS} up to V_{GS}-V_P (=V_{DSAT}). Beyond this point, the saturation current can be simply approximated as a constant equal to the value at $V_{DS} = V_{DSAT}$:

do not remember

$$I_D^{(sat)} = \frac{qN_D\mu_n Wa}{L}\cdot\left[V_{DSAT} - \frac{2}{3}\sqrt{\frac{8\varepsilon}{qN_D a^2}}\cdot\left\{\left(\phi_i + V_{DSAT} - V_{GS}\right)^{3/2} - \left(\phi_i - V_{GS}\right)^{3/2}\right\}\right]$$

DC Equivalent Circuit Model for JFET



Small-Signal JFET Analysis

- Generalise the DC result for channel-current to *time-varying signals*:

$$i_D(t) = f\left(v_{GS}(t), v_{DS}(t)\right)$$

- Replace each signal with the sum of a DC part and a small-signal part:

$$I_D + \mathrm{Im}\left\{I_d \cdot e^{j\omega t}\right\} = f\left(V_{GS} + \mathrm{Im}\left\{V_{gs} \cdot e^{j\omega t}\right\}, V_{DS} + \mathrm{Im}\left\{V_{ds} \cdot e^{j\omega t}\right\}\right)$$

$$\cong f\left(V_{GS}, V_{DS}\right) + \mathrm{Im}\left\{V_{gs} \cdot \left.\frac{\partial f}{\partial v_{GS}}\right|_{DC} \cdot e^{j\omega t}\right\} + \mathrm{Im}\left\{V_{ds} \cdot \left.\frac{\partial f}{\partial v_{DS}}\right|_{DC} \cdot e^{j\omega t}\right\}$$

$$\Rightarrow I_d = g_m \cdot V_{gs} + g_{ds} \cdot V_{ds}$$

2-D First-Order Taylor Series

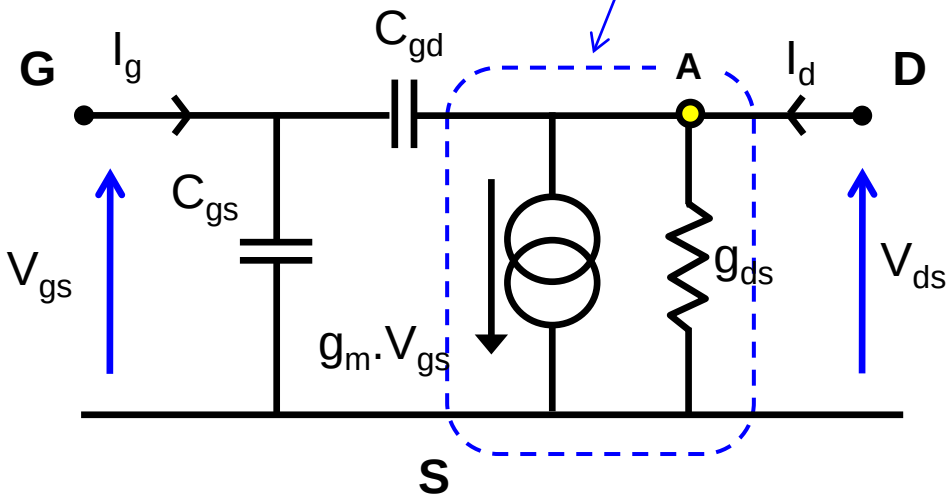
- Where: $g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{DC}$ and: $g_{ds} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{DC}$

transconductance

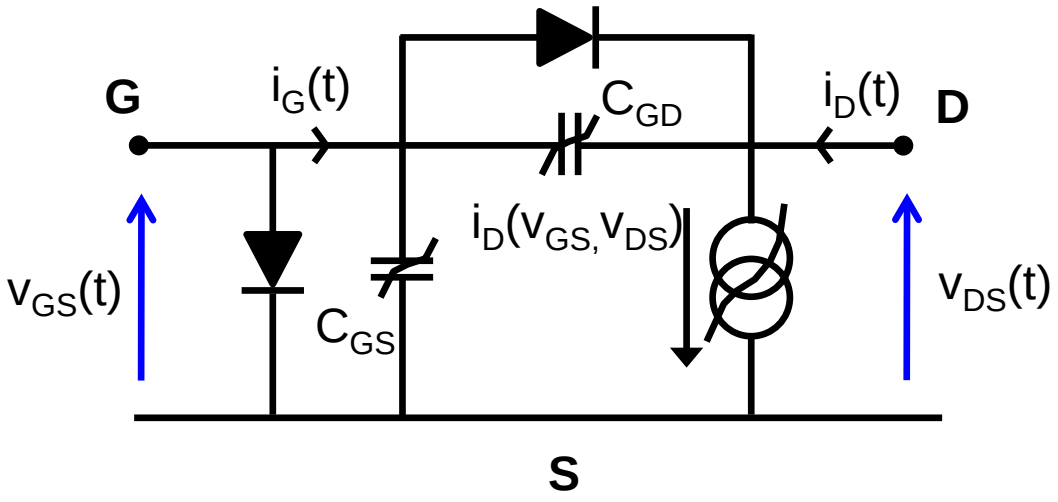
drain-source conductance

Small-Signal JFET Equivalent Circuit

- The result from the previous slide: $I_d = (g_m.V_{gs} + g_{ds}.V_{ds})$ can be seen as an instance of KCL at node "A" below, leading to a small-signal equivalent circuit for the drain-source channel as a linear voltage-controlled current source in shunt with a linear conductance;
- Adding in capacitances to represent the depletion layer capacitances (and ignoring parasitic resistances):, we arrive at the following small-signal equivalent circuit for the JFET:



Large-Signal JFET Equivalent Circuit



Note:

- JFETs have inferior analogue properties to bipolar transistors and inferior digital properties to those of MOS transistors.
- Their very high impedance at DC/low-frequencies is sometimes useful in circuit design, and they also tend to have better linearity performance at radio frequencies (RF)