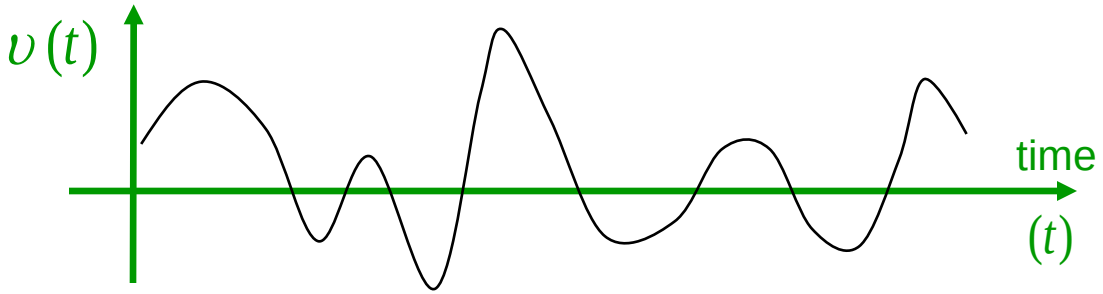
Chapter 9

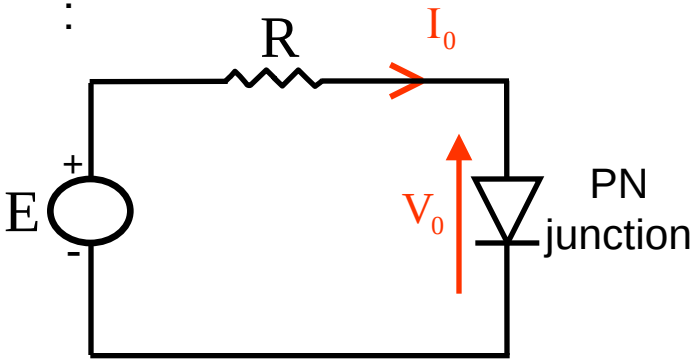
Small-Signal and Large-Signal Analysis of the PN Junction.

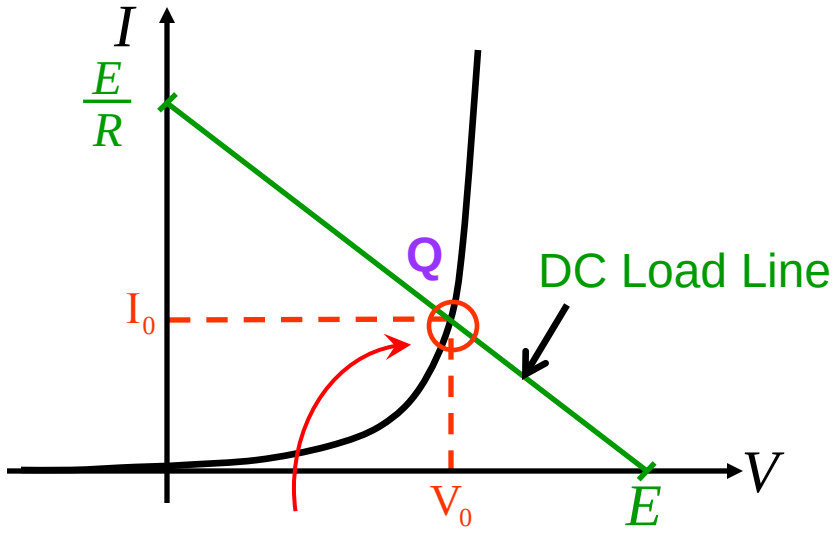
PN Junction and Signals

Electronic Engineering is largely concerned with “signals” – i.e. information in electrical form. e.g. (analogue) voltage waveform



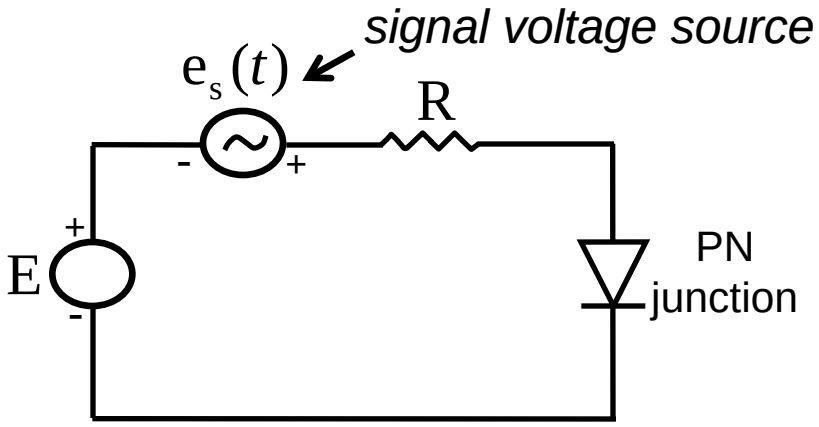
DC Circuit Analysis :





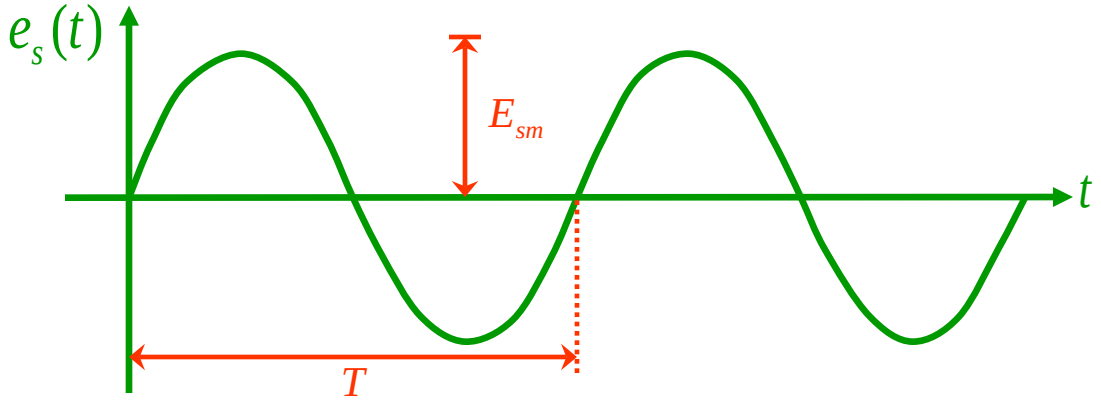
(I_0, V_0) DC bias point or Quiescent or Q-point

PN Junction and Signals



$e_s(t)$: AC signal source.

Consider this to be a sine wave :



T : period, f : frequency

$f = 1/T$ cycles/sec (Hz)

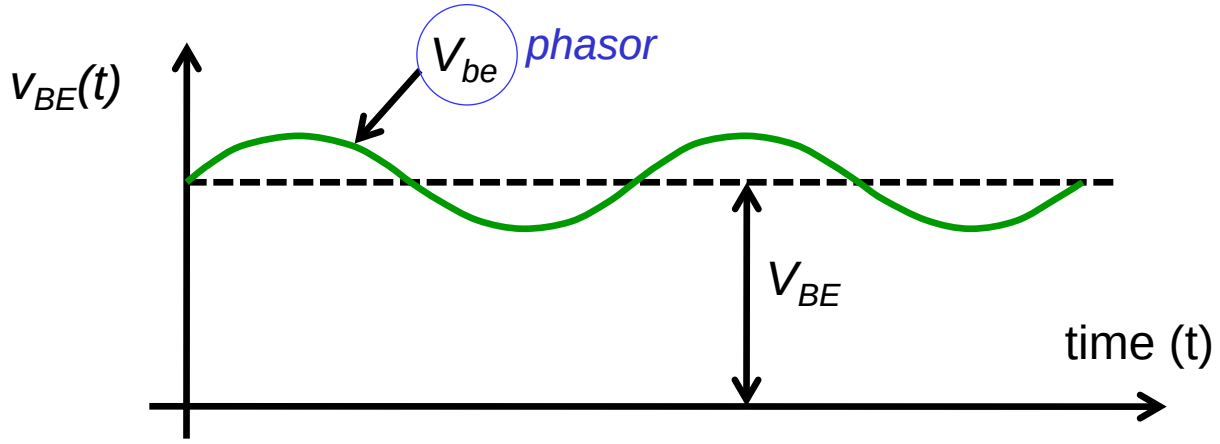
Angular frequency $\boxed{\omega = 2\pi f}$

$$e_s(t) = \mathrm{Im}\left\{E_{sm} e^{j\omega t}\right\} = E_{sm} Sin(\omega t)$$

$E_s = E_{sm} e^{j\omega t}$ is a phasor (complex – valued) representing this signal

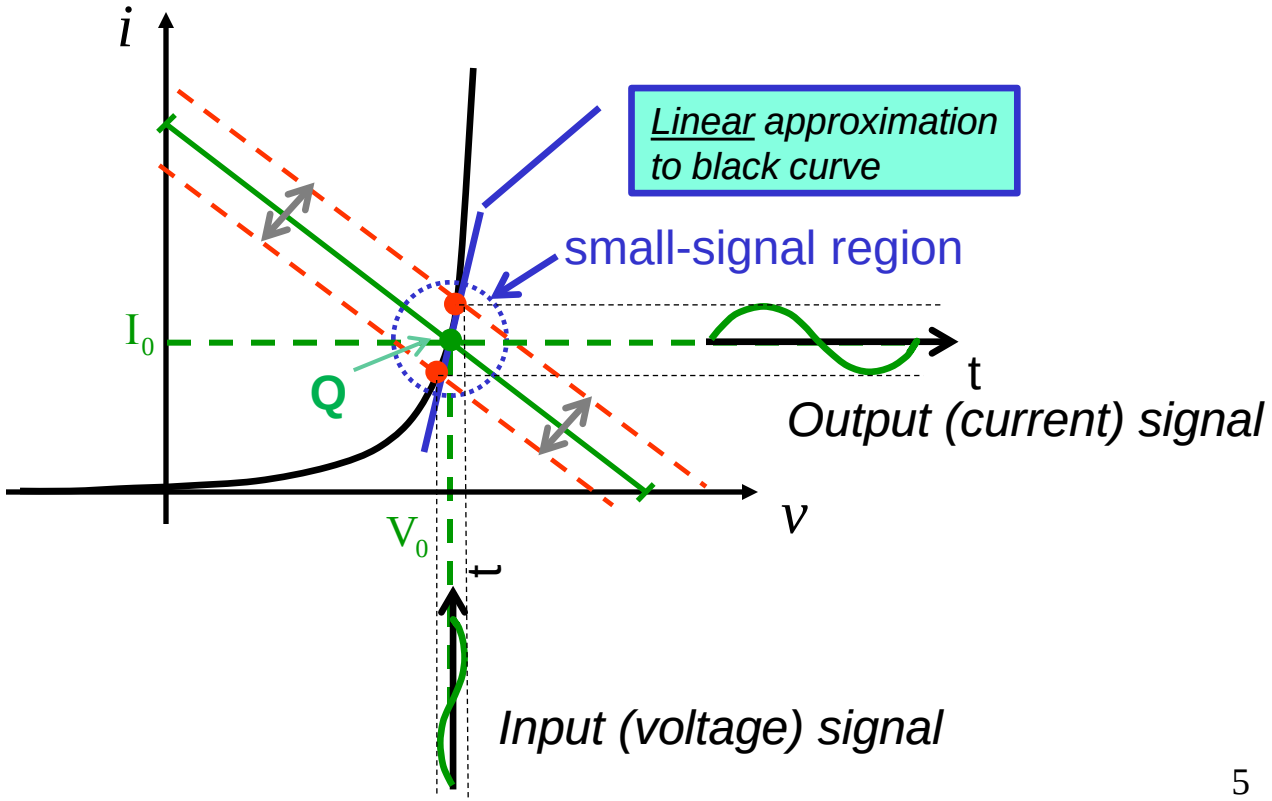
Notation

- We use capital letters with capital subscripts to represent DC or static quantities, e.g. V_{BE} or I_D;
- We use lower case letters with capital letter subscripts to represent the total (time-varying) voltage or current, e.g $v_{BE}(t)$, $i_D(t)$ ...
- We use lower case letters with lower case subscripts to represent the time-varying part of a signal – e.g. $v_{BE}(t) = V_{BE} + v_{be}(t)$
- We use capital letters with lower case subscripts to denote the special case of steady-state sinusoids or phasors (complex-valued, amplitude and phase), e.g. V_{be} or I_d.



Small – Signal Analysis

- Here we assume that the amplitude of signals is sufficiently small compared to Q-point values that the device (non-linear) characteristics can be approximated by a (linear) first-order Taylor series expansion.

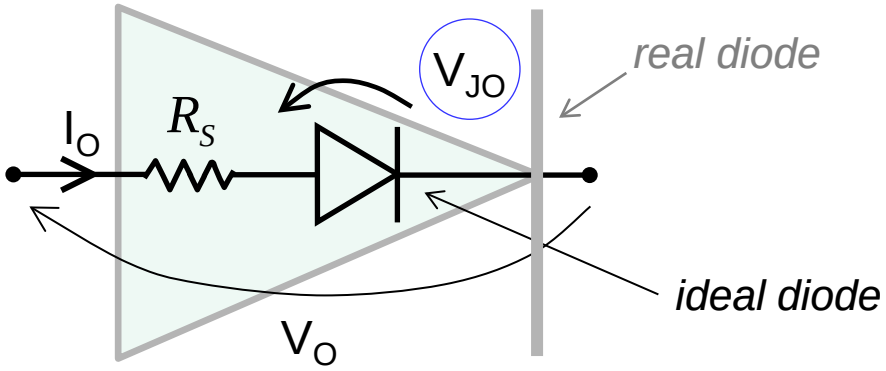


Kinds of Device Circuit Models

- **DC Model**
  - Valid for static (non-time-varying) signals only;
- **Small-Signal Model**
  - Valid for time varying signals around a given DC operating point (as determined by using a DC model), but only if the amplitude of the signals is small. Linear analysis methods sufficient;
- **Large-Signal Model**
  - In principle the most general kind of model (but the most difficult to construct and use). Includes the DC and Small-Signal Models as special cases. Valid for essentially arbitrary signals. Requires non-linear analysis techniques, usually involving computer simulation.

Reminder: DC Equivalent Circuit Model

- As we saw previously, a simple DC equivalent circuit for the PN junction allowing for parasitic resistance effects can be constructed as follows:

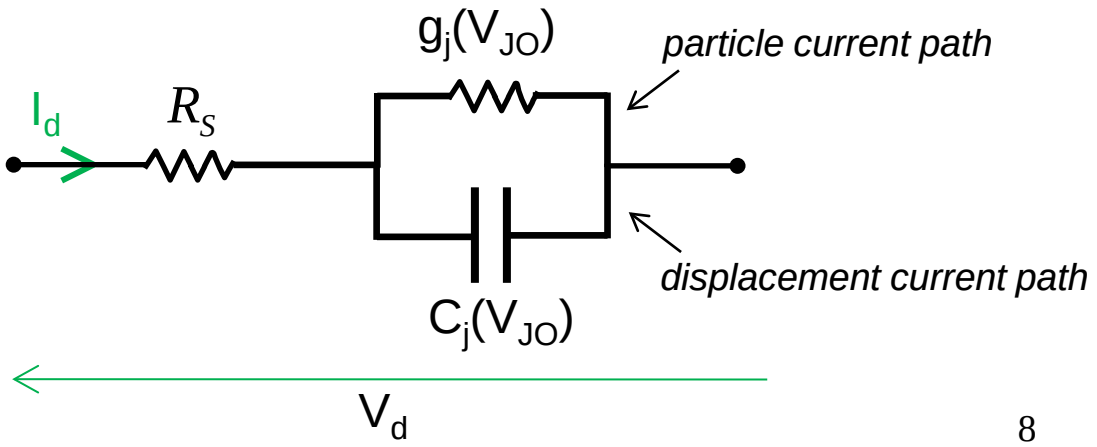


- When this circuit is solved (with given external conditions) it defines the DC or Q-point (I_O, V_O).
- A small-signal model for the device can only be constructed once the associated Q-point is known.

Small-Signal Equivalent Circuit Model

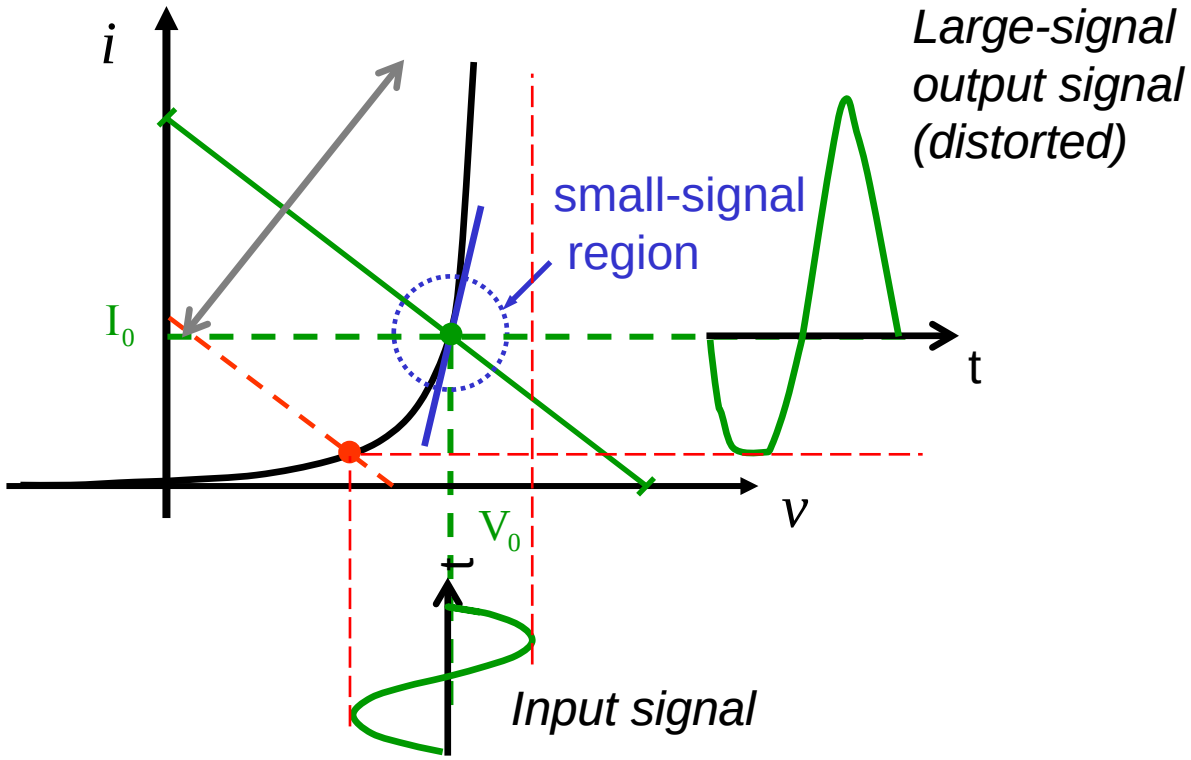
- This is an assembly of linear circuit elements that represent the terminal electrical behaviour of a device **within the small-signal zone around Q** with acceptable accuracy. Generally, these elements can be directly related to underlying physical aspects of the device operation;
- The model is only valid in the vicinity of a given Q-point and the values of at least some of the elements will depend on the quiescent or DC conditions (e.g. (I_o,V_o))
- If sinusoidal signal is applied to a small-signal equivalent circuit, only sinusoidal signals are produced, i.e. no new frequencies are generated

Example: small-signal model of PN junction (at DC point (I_o, V_o)):



Large-Signal or Nonlinear Analysis

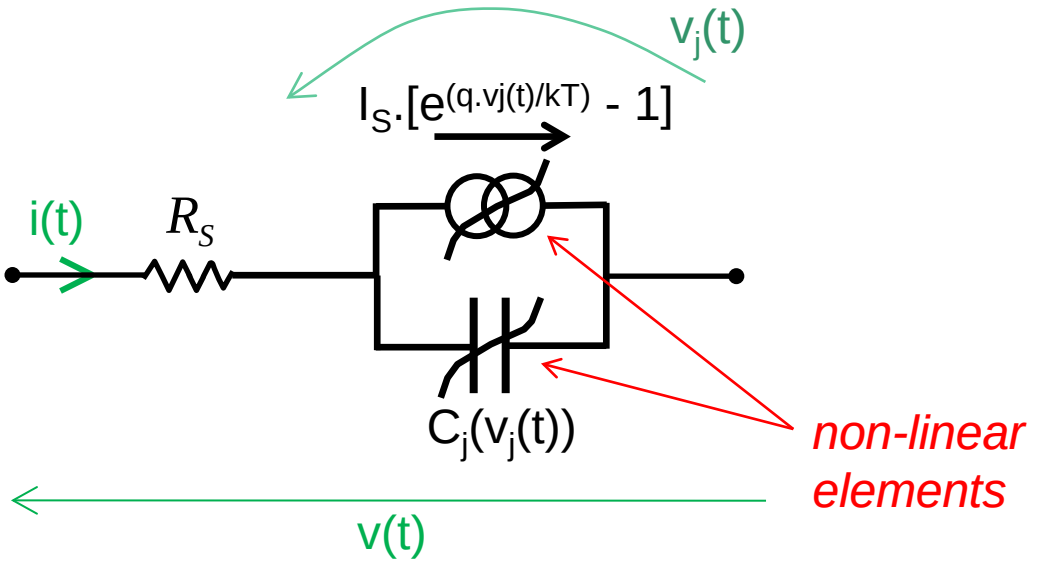
- In this case, the input amplitude becomes large and the small-signal approximation breaks down
- **Nonlinear** effects become evident whenever the device (such as the PN junction) is fundamentally non-linear: new frequencies (e.g. harmonics) are usually generated



Large-Signal Equivalent Circuit Model

- Again the model seeks to represent the large-signal terminal electrical behaviour of a device with acceptable accuracy using circuit elements, some of which will be non-linear functions of their controlling voltages (or currents);
- The large-signal model of a device is the most general kind of model, but also the most difficult to construct. In principle, it should reduce to a DC or a small-signal model at any bias point.

Example: large-signal model of PN junction:



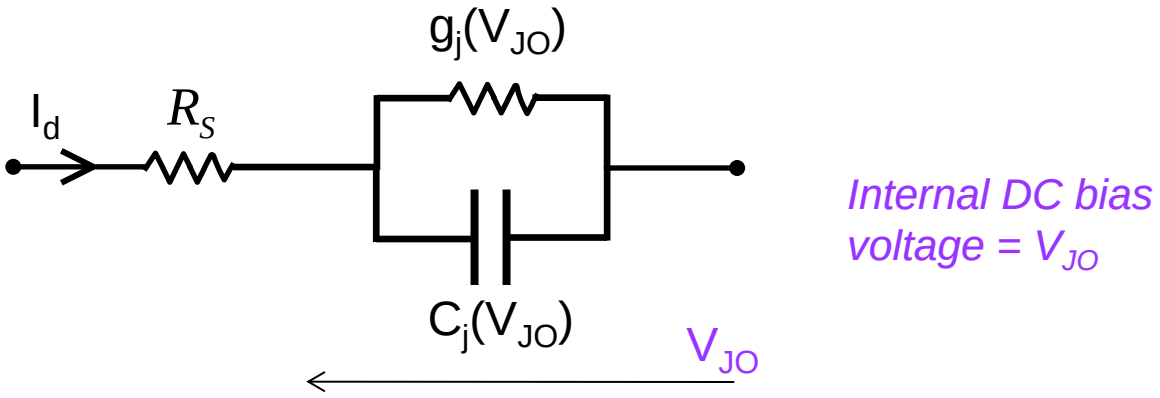
Non-linear Circuit Analysis and SPICE

- Few circuits containing non-linear elements can be solved analytically: numerical solutions using Computer-Aided Design (CAD) software or design tools becomes essential;
- The SPICE program (widely available and free) is the most successful circuit simulation program of its kind, but many other examples exist. SPICE was developed at the the University of California, Berkeley in early 1970's and has been added to and refined over the years[1].
- SPICE uses equivalent circuit models to represent a wide range of semiconductor devices. It can perform DC, small-signal or large-signal/transient analysis of complex circuits with many 100,000's of transistors
- Circuit simulation is important in CAD for EE but just element of the general field of ***EDA (Electronic Design Automation)***. This is a large global industry, and key players include Synopsys, Cadence, (who have operations in Ireland), Mentor, ADS etc

[1] *e.g. see* http://sss-mag.com/spice.html

Small-Signal Analysis of PN Junction

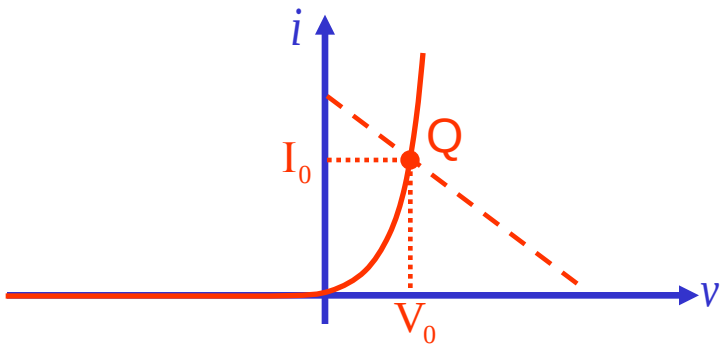
- We will now investigate the small-signal model of the PN junction in more detail, in particular the elements $g_j(I_O)$ and $C_j(V_{JO})$ and their dependence on DC bias conditions.



- Physically, the conductance g_j arises from the flow of particle current across the PN junction, whereas the capacitance C_j arises from the charges stored within the depletion layer. R_S is the parasitic resistance.

(1) Analysis for PN Junction Small-Signal Conductance g_j

- For simplicity, we will ignore the effects of the parasitic resistance R_s here, and also, for now, the displacement current flowing though C_j



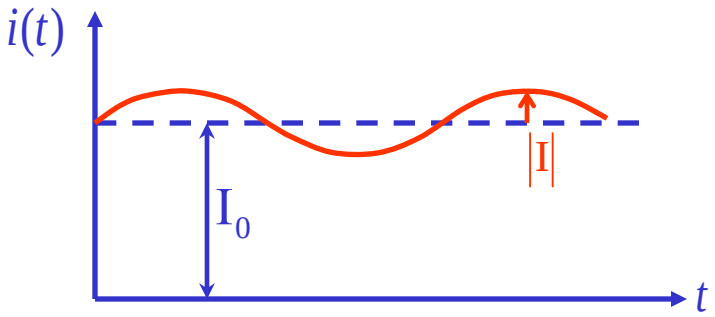
DC:

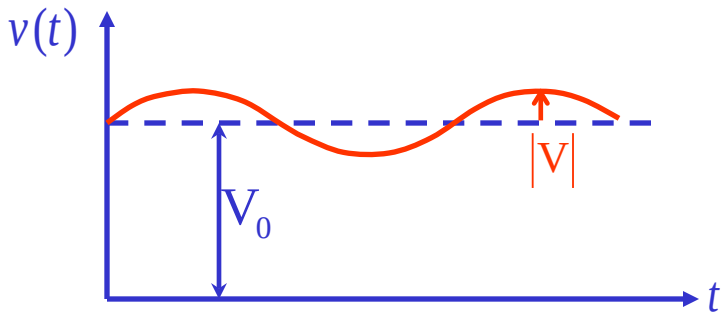
$$I_0 = I_s\left[e^{(qV_0/kT)} - 1\right]$$

In General:

$$i(t) = f(v(t)) = I_s\left[e^{(qv(t)/kT)} - 1\right]$$

Time-varying signals (low-freq.)





The Taylor Series

- The Taylor Series is a result in mathematics that allows the value of a function at a point "x" (nearby) a given location "x_o" to be determined in terms of a series expansion using derivatives at the given location x_o:

$$f(x) = f(x_o) + (x - x_o) \cdot \left.\frac{df}{dx}\right|_o + \frac{1}{2} \cdot (x - x_o)^2 \cdot \left.\frac{d^2 f}{dx^2}\right|_o + \cdots$$

- If the two values are quite close, then we can truncate this expansion as a First-Order Taylor Series. This is exactly what is done in "small-signal" device analysis:

$$f(x) = f(x_o) + (x - x_o) \cdot \left.\frac{df}{dx}\right|_o$$

First-Order Taylor Series Expansion

$$i(t) = I_0 + \mathrm{Im}\left\{ Ie^{j\omega t} \right\} \qquad v(t) = V_0 + \mathrm{Im}\left\{ Ve^{j\omega t} \right\}$$

1st order Taylor series of $i(t) = f\left(v(t)\right)$:

$$i(t) = \underbrace{f\left(V_0\right)}_{= I_0} + \underbrace{\left.\frac{df}{dv}\right|_0} \cdot \left(v(t) - V_0\right)$$

$$\cancel{I_0} + \mathrm{Im}\left\{ Ie^{j\omega t} \right\} = \cancel{I_0} + \underbrace{\left[\frac{qI_s}{kT} e^{qV_0/kT} \right]} \cdot \underbrace{\left(v(t) - V_0\right)}_{= \mathrm{Im}\left\{ Ve^{j\omega t} \right\}}$$

$$\Rightarrow I = \underbrace{\left[\frac{qI_s}{kT} e^{qV_0/kT} \right]} \cdot V$$

depends on Q

I : small-signal current

V : small-signal voltage

or $\quad I = g_j \cdot V$ .. where g_j is defined as the small signal conductance of the PN junction at the bias point Q (depends on V_o)

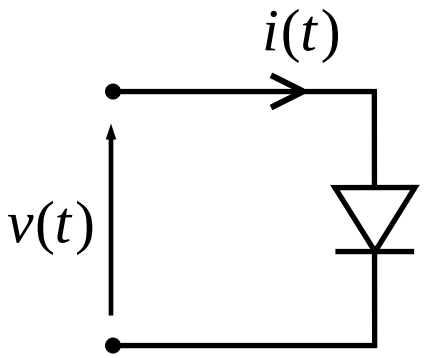
Forward and Reverse Small-Signal Conductance of PN Junction

- **Reverse Bias:**
  - Here g_j will quickly become extremely small (i.e. very high resistance) so that we can often use the approximation $g_j \approx 0$ in reverse bias once V is below ≈ -100mV
- **Forward Bias:**
  - We have shown: $$g_j = \frac{q \cdot I_S}{kT} \cdot e^{q.V_o / kT}$$
  - If $V_o >> kT/q$, we can use the approximation $$I_o \cong I_S \cdot e^{qV_o / kT}$$
  - Which leads to the simple result and important result:

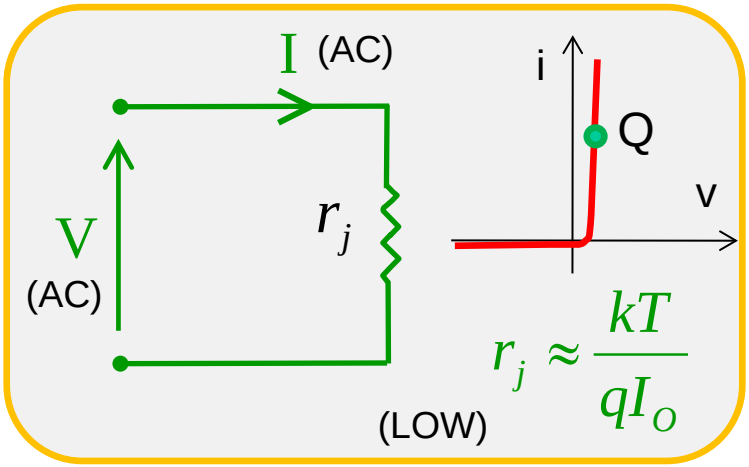
$$g_j = \frac{q \cdot I_O}{kT} \quad or\ (at\ 300K) \quad r_j = \frac{1}{g_j} \approx \frac{26}{I_O(mA)}\ \Omega$$

e.g. I_O=10mA $r_j \approx 2.6\Omega$

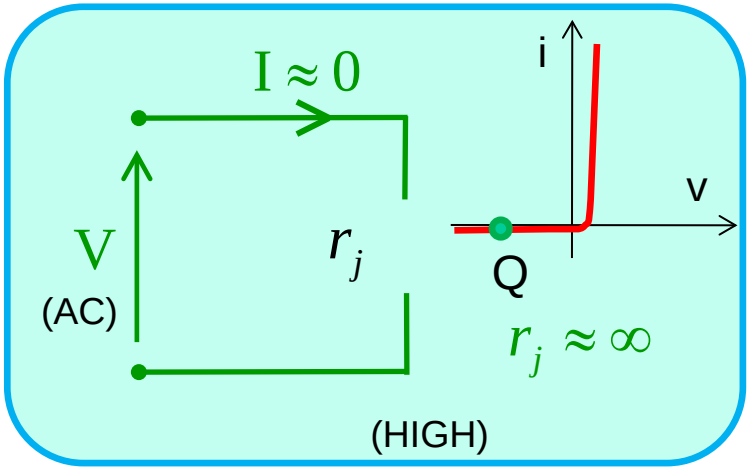
Simplified Small Signal Equivalent Circuits for PN Junction



Forward Bias:



Reverse Bias:

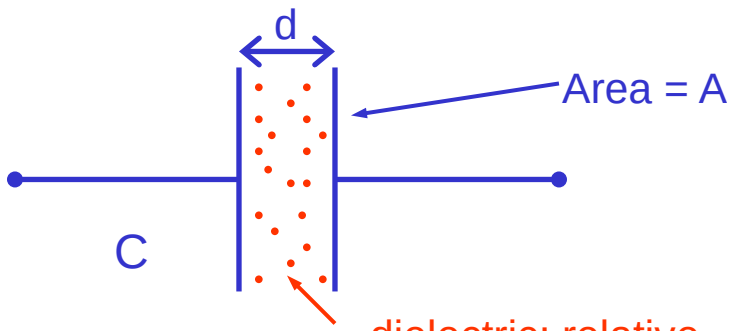


NB: Parasitic resistance neglected; Depletion capacitance neglected (reasonable at low frequencies)

EXAMPLE 9.1

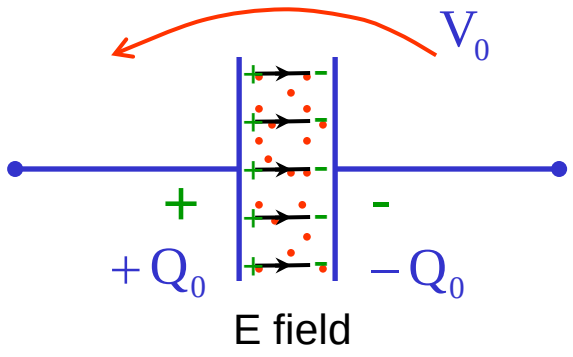
(2) Analysis for PN Junction Small-Signal Capacitance C_j

Reminder: the normal parallel plate capacitor :



$$C = \frac{\varepsilon A}{d} = \frac{\varepsilon_r \varepsilon_0 A}{d}$$

Apply a DC Voltage V_o:



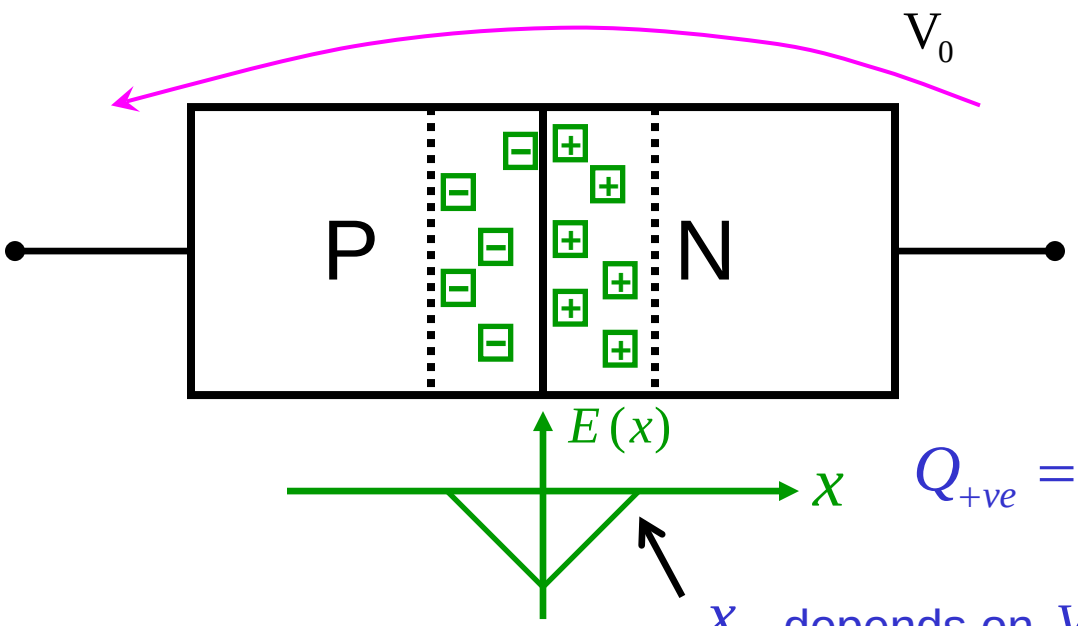
A **linear** relationship exists between charge and voltage

$$Q_o = C \cdot V_o$$

Q_O : charge

V_O: voltage

Depletion Layer Charge in PN Junction



...hence the depletion layer charge is a nonlinear function of the applied voltage. When we have a nonlinear Q(V) relationship like this, the small signal "junction" capacitance at a DC bias point V_o is defined as:

$$C_j = \left.\frac{dQ}{dV}\right|_0$$

Small-Signal Capacitance in PN Junction

PN Junction $Q = qN_D x_n A$

Earlier we found a relationship between x_n and V_0 Substitute this in:

$$Q = qN_D A \underbrace{\left[\frac{2\varepsilon N_A(\phi_i - V_o)}{qN_D(N_A + N_D)} \right]^{1/2}}_{x_n}$$

$$\Rightarrow C_j = \left. \frac{dQ}{dV} \right|_o = \left[\frac{q\varepsilon N_A N_D}{2(N_A + N_D)} \right]^{\frac{1}{2}} \times \frac{A}{\sqrt{\phi_i - V_o}}$$

$$= \frac{\varepsilon A}{\left[\frac{2\varepsilon(\phi_i - V_o)}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}} = \frac{\varepsilon A}{W}$$

W : depletion layer width

same as parallel plate capacitor!

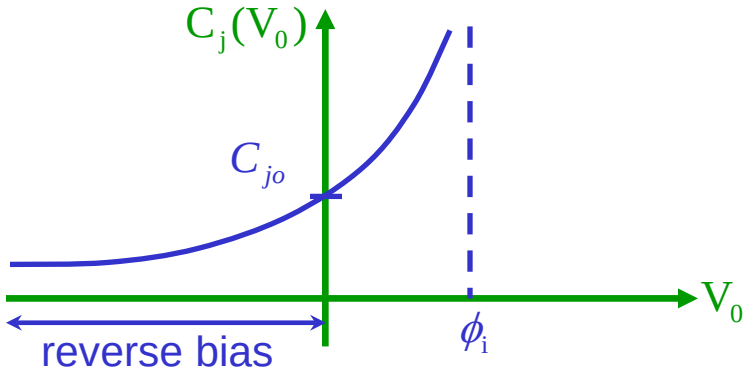
Formula for Depletion Layer Capacitance

- We can re-write this result as follows:

$$C_j(V_o) = \frac{\varepsilon A}{\left[\frac{2\varepsilon\phi_i}{q}\left(\frac{N_A + N_D}{N_A \cdot N_D}\right)\right]^{1/2} \cdot \left(1 - \frac{V_o}{\phi_i}\right)^{1/2}}$$

- This shows that the PN junction depletion capacitance is a *non-linear* function of the DC bias voltage V_o. Denoting the capacitance at zero bias $C(V_o=0)$ as C_{jo}, we arrive at the final more compact form:

$$C_j(V_o) = \frac{C_{jo}}{\left(1 - \frac{V_o}{\phi_i}\right)^{1/2}}$$



More General Forms of Small-Signal Capacitance

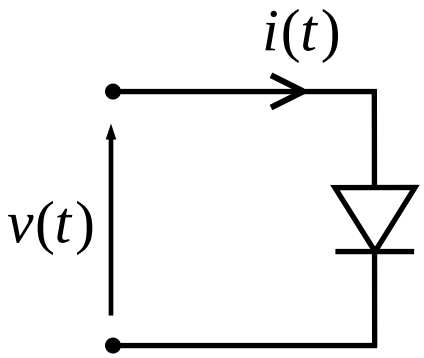
- This result is valid for a step-change doping profile at the junction. Other kinds of doping profile are possible: for example, a linearly-graded profile leads to the power in the denominator changing from ½ to ⅓. The SPICE program uses the following general form:

$$C_j(V_o) = \frac{C_{jo}}{\left(1 - \frac{V_o}{\phi_i}\right)^m}$$

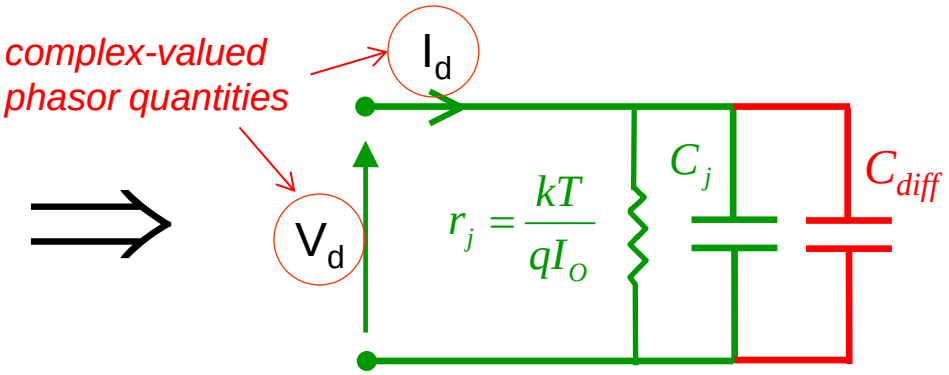
... where 'm' is an adjustable number that can be fitted to the measured data and allows for quite general doping profiles.

- There is another component of capacitance that exists in PN junctions and this is associated with the storage of minority carriers in the neutral regions under forward bias. It is called the **Diffusion Capacitance (C_{diff})** and has a complex dependence on DC current and the frequency of the signal. It is more important under forward bias.

Small Signal Equivalent Circuits for PN Junction



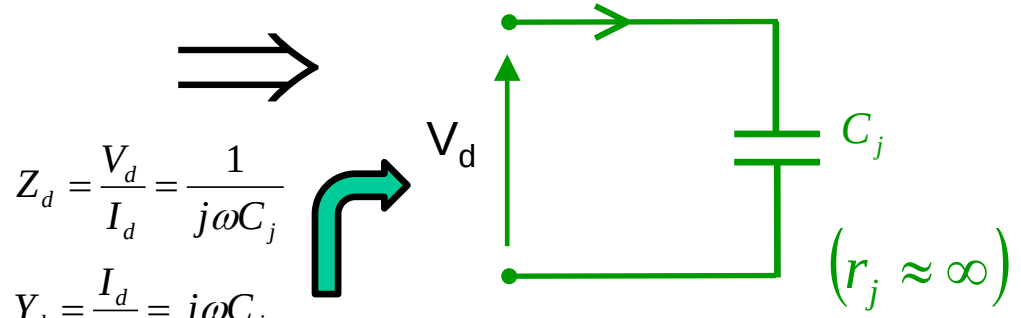
Forward Bias:



NB: Parasitic resistance effects neglected.

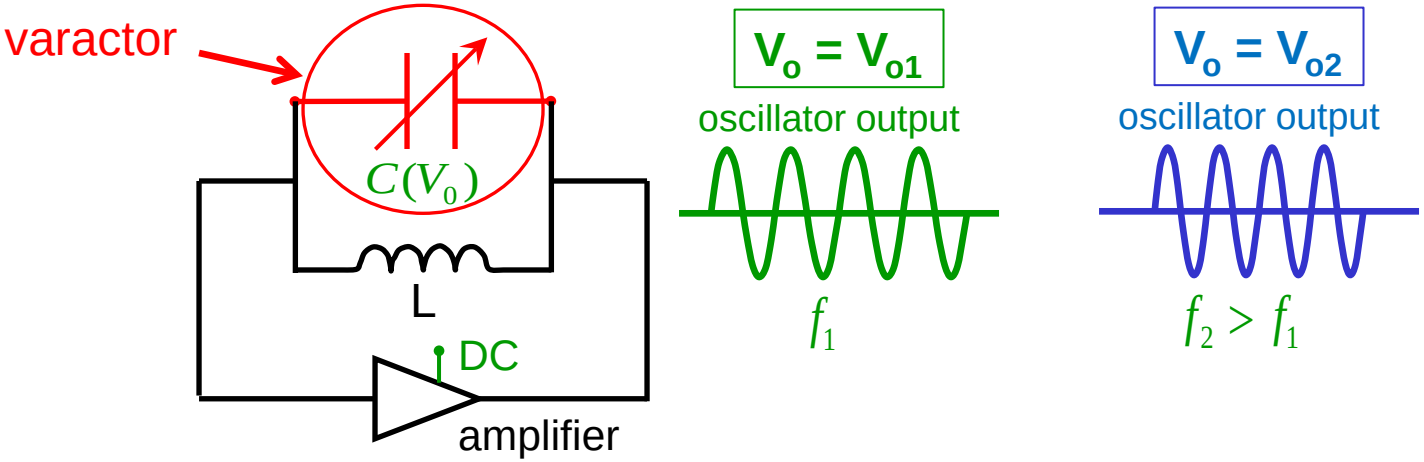
Reverse Bias:

$$I_d = Y_d . V_d = j\omega C_j . V_d$$



The Varactor Diode

- The fact that a reverse-biased PN junction has a low-loss, electronically-variable capacitance can be put to good use;
- **Varactor diodes** have special doping profiles designed to ensure the maximum range of tunability of C_j as the controlling voltage is changed
- For example, Voltage Controlled Oscillators (VCOs) are widely used in communications, and are electronic oscillators whose resonant frequencies can be changed with the voltage bias. They are a key part of very stable signal sources called frequency synthesisers



EXAMPLE 9.2