Sample Final Exam

Answer Any Three Questions

1. (i) When can a circuit be described as a two-port? Briefly outline the advantages and limitations of the two-port description in circuit analysis. 20%

(ii) Find the admittance (Y) matrix of the two-port in Figure 1(a). 40%

(iii) A linear time-invariant two-port is terminated at port 1 in the series combination of a 6 V voltage source and a 1 Ω resistance. If port 2 is terminated in an open circuit, as in Figure 1(b), $i_1 = 1.5$ A and $v_2 = 3$ V. If port 2 is terminated in a 1 Ω resistance, as in Figure 1(c), $i_1 = 2$ A and $v_2 = 1$ V. Find the impedance (Z) matrix of the two-port. 40%

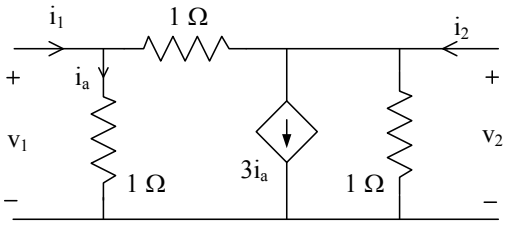

Figure 1(a)

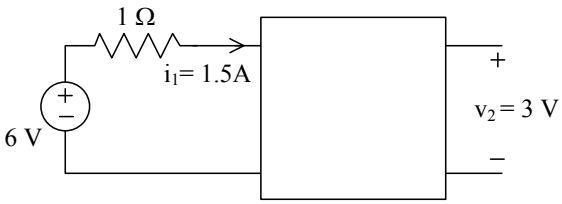

Figure 1(b)

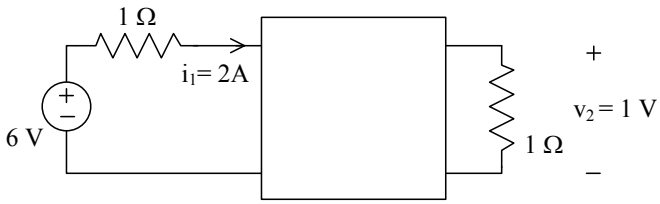

Figure 1(c)

2. (i) If the Laplace transform of f(t) is F(s), write down an expression for the Laplace transform of the time derivative df(t)/dt. Use this result to show how capacitors are transformed when the Laplace transform is applied to a circuit. 20%

(ii) What is the (s-domain) impedance seen by the voltage source in the circuit of Figure 2? 20%

(iii) Find i(t) for $t \geq 0$ in the circuit of Figure 2, if $v_i(t) = 1$ V for $t \geq 0$ and there is no energy stored in the circuit at $t = 0^-$. 30%

(iv) By decomposing Z(s) using the partial fraction expansion, draw a circuit whose input impedance Z(s) is

$$\frac{2s+5}{(s+2)(s+3)}$$

30%

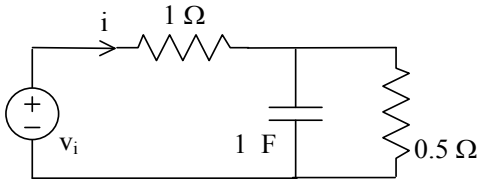

Figure 2

3. (i) Find the transfer function $V_2(s)/V_1(s)$ for each of the circuits given in Figure 3. The op amps are ideal with infinite gain and operating in the linear region.

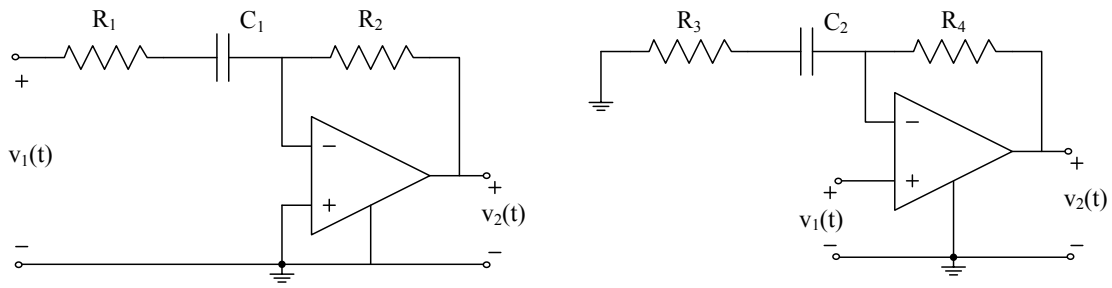

Figure 3

(ii) Use a cascade connection of the circuits from (i) to design a circuit with transfer function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-2s(s+3)}{(s+2)(s+4)}$$

Give the values of all circuit elements in your design.

(iii) Find the output voltage $v_{out}(t)$ of the circuit from (ii) for $t \geq 0$ if its input voltage $v_{in}(t)$ is the unit step and all initial capacitor voltages are zero.

4. (i) Discuss, giving equations as appropriate, the process of impedance scaling in filter design. Indicate what it involves, why it is useful, and how it can be applied to an RLC circuit. 20%

(ii) Design an RLC filter with 1 kΩ terminating resistances to meet the specification shown in Figure 4. 80%

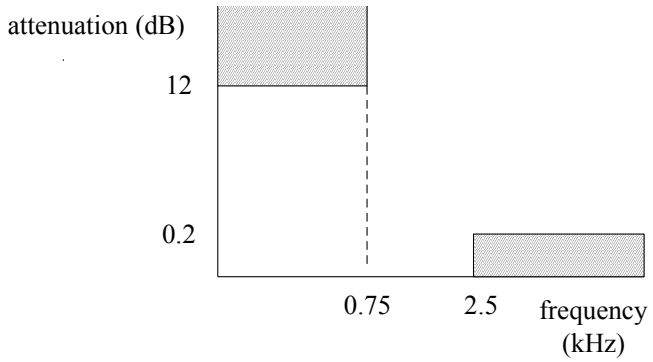

Figure 4