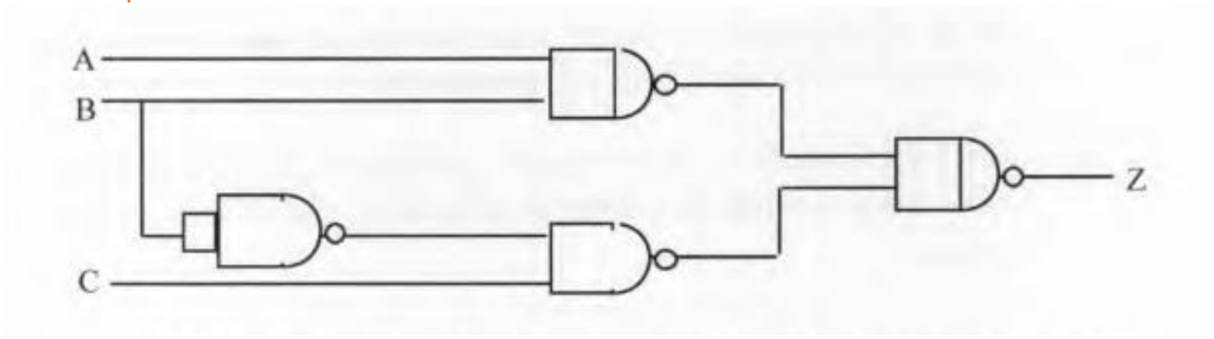
ECE 385 Fergal Lonergan AL1 flonerg2

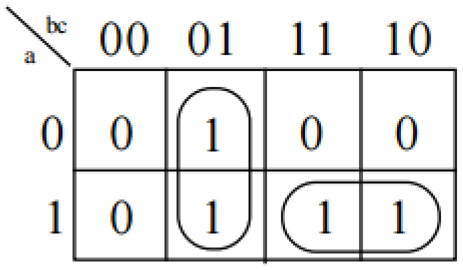
Lab Report 1

Introduction

In this lab we were tasked with testing a simple circuit containing four NAND gates. It has the following truth table. The circuit then acts like a 2-1 MUX or multiplexer. Multiplexers can be used for retrieving a single predetermined output from a series of inputs. We are also investigating the effect of glitches on digital circuits. We first test this in part A and then we redesign our circuit to negate our glitch in part B.

Description of the Circuits.





a \ bc	00	01	11	10
0	0	1	0	0
1	0	1	1	1

Circuit A.

Circuit A uses four NAND gates to create a MUX and it does its' job quite well, however there are a few glitches in it. Due to the fact that the B input has to be inverted it slows the gate by a small propagation delay and so causes a glitch when originally the values at the final NAND gate are not the actual Values we need/want for the circuit. As a result to fix this we review our Karnaugh map and realise that there is another term we can add. The AB'C term highlighted in the map below. This removes the glitches and so our circuit works exactly as designed. (Part B)

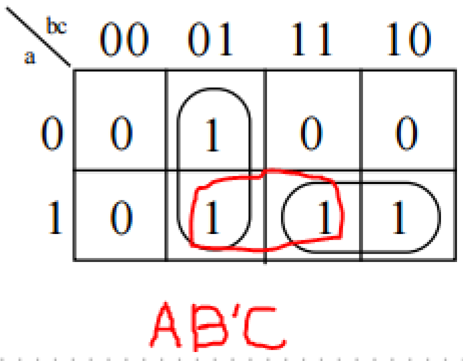
This circuits could be made quite simply using AND-OR logic however this requires the use of more transistors than NAND-NAND logic. This logic will also reduce the package count by two thirds as AND-OR logic implementation would require 3 chips.

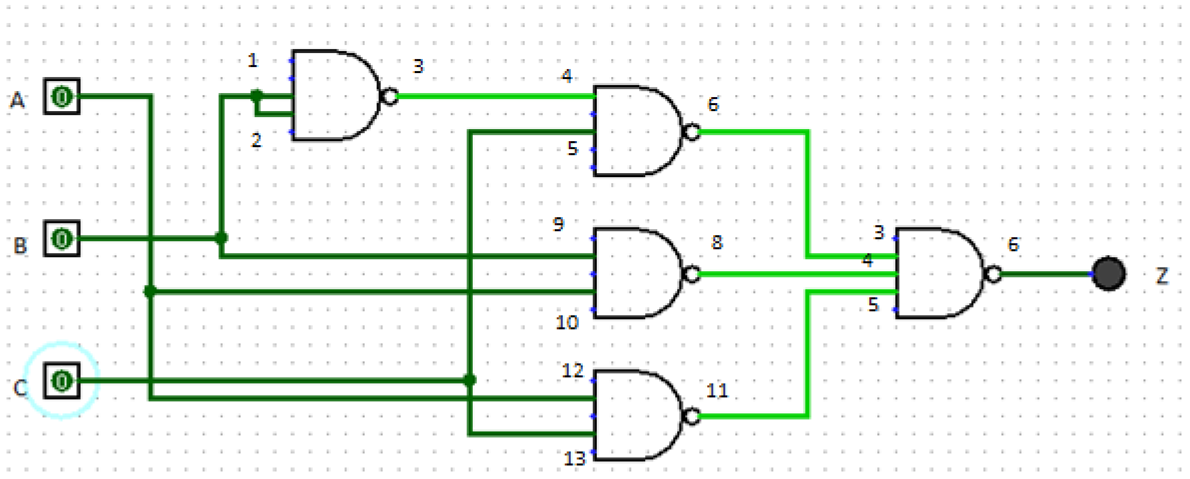
The conversion from AND-OR to NAND-NAND can be carried out on any two level AND-OR circuit simply by replacing each AND and OR gate with a NAND gate.

This K-map demonstrates the 2 to 1 multiplexor properties of this logic design. We were alerted to the fact that there could be delays arising from the propagation delay on the b line. In order to get rid of this static hazard the two adjacent min terms would need to be connected. This would add complexity to the circuit and a SN7410 chip would need to be used for a 3 input NAND gate. The adjusted k-map can be seen below.

This k-map with additionals give rise to the logic output

$$Z = [(B'C)'(AB)'(AC)']'$$





DONE ON LOGISIM

This gives us the following representation on logisim. Both circuits had the following truth table, this was tested by testing all possible combinations of switches connected to an output LED.

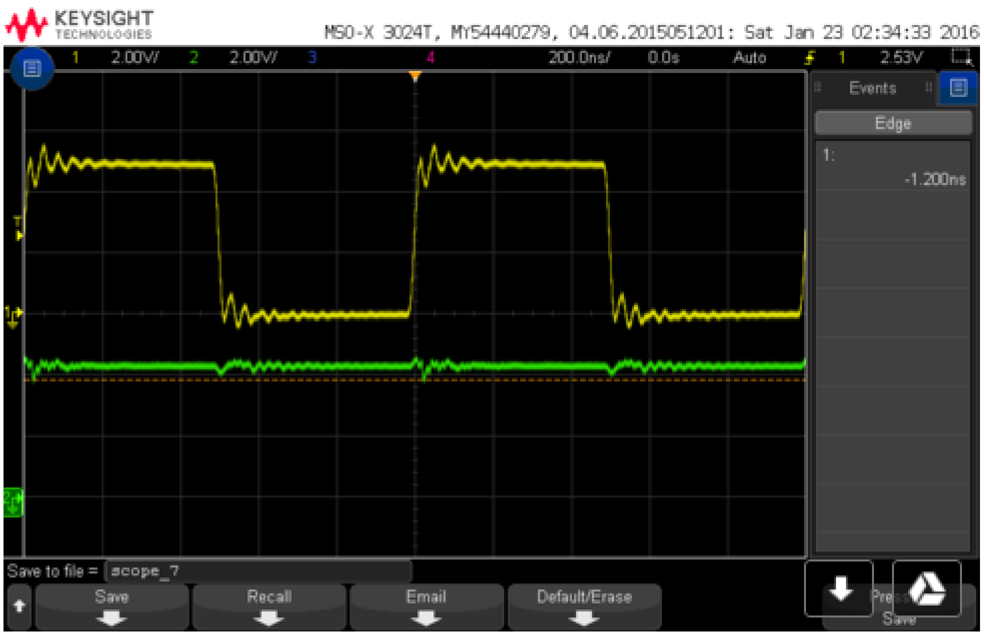
A	B	C	Z

0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

RESULTS & COMMENTS

The oscilloscope readings for initial circuit can be seen below. These demonstrate the multiplexing functions of the circuit and confirm the above truth table. The select of our multiplexer which was input b was connected to the clock. The yellow line shows the clock signal and the green signal shows the output of the circuit.

The first picture shows a and c at logic 0

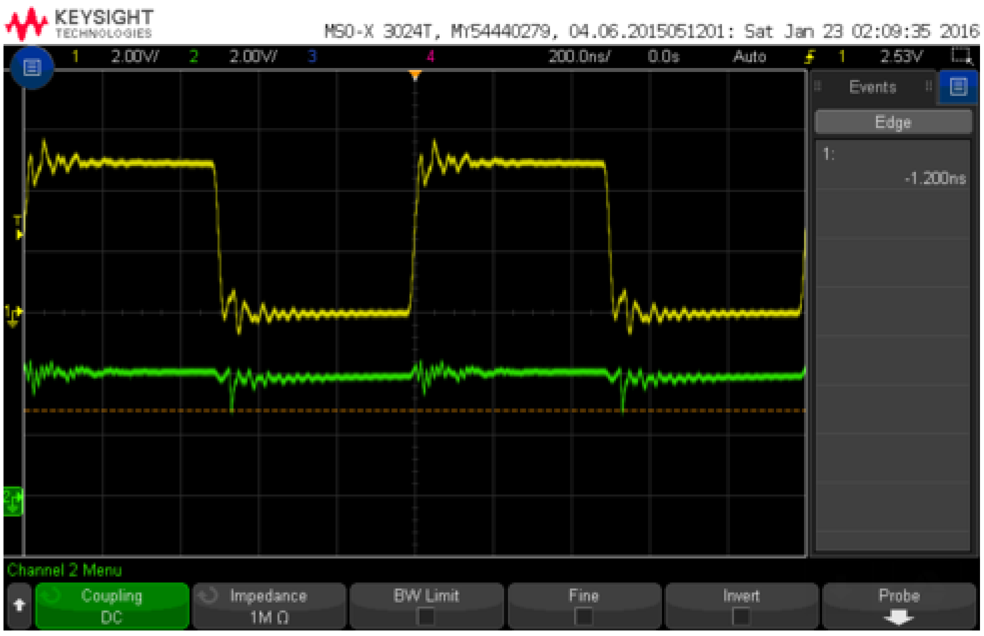

KEYSIGHT TECHNOLOGIES
MSO-X 3024T, MY54440279, 04.06.2015051201: Sat Jan 23 02:34:33 2016
1 2.00V/ 2 2.00V/ 3 4 200.0ns/ 0.0s Auto 1 2.53V
Events
Edge
1: -1.200ns
Save to file = scope_7
Save
Recall
Email
Default/Erase
Press to Save

B

A

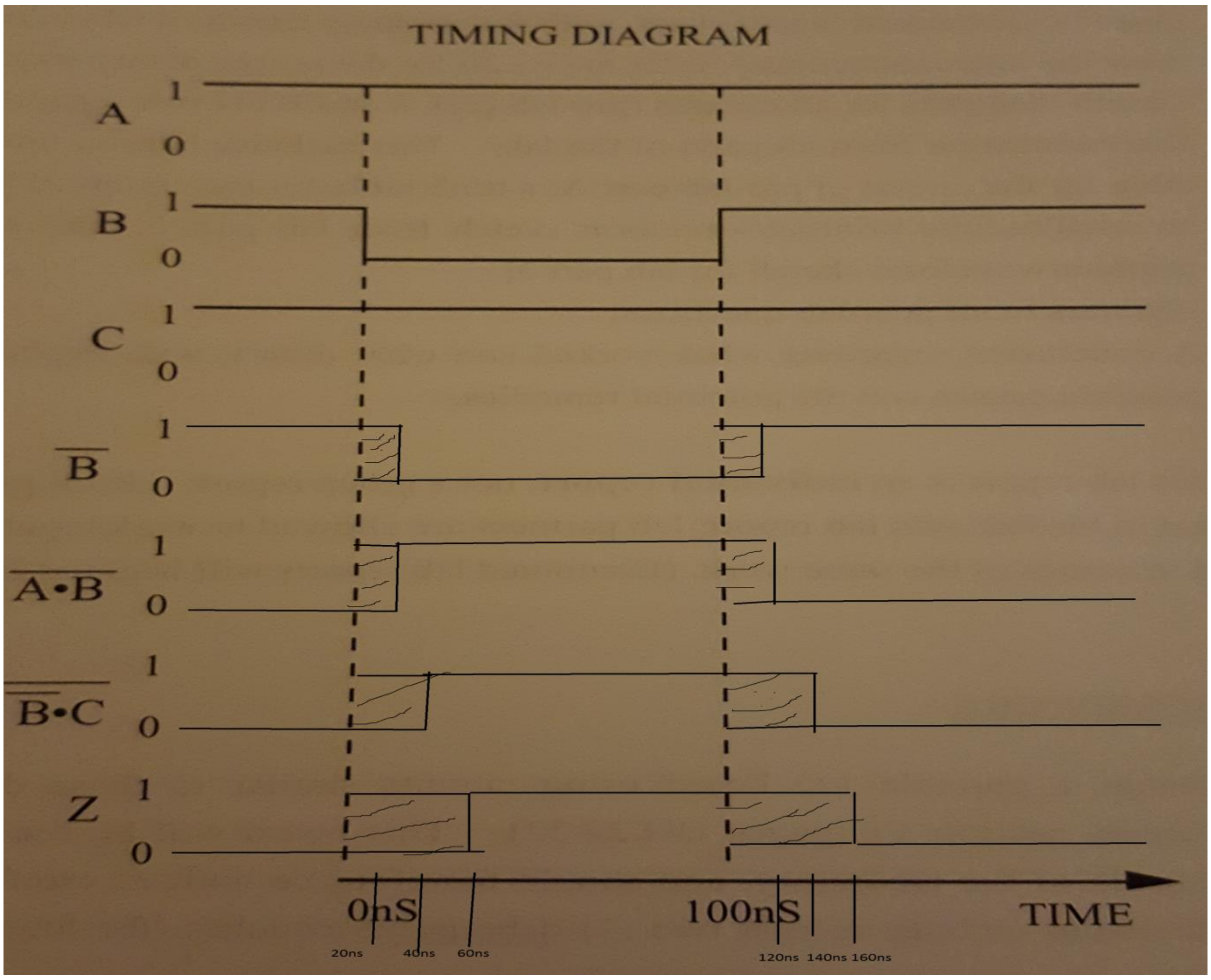
The following readings are from the second implementation with static hazards removed.

This reading shows a,b and c at logic 0.


KEYSIGHT TECHNOLOGIES
MSO-X 3024T, MY54440279, 04.06.2015051201: Sat Jan 23 02:09:35 2016
1 2.00V/ 2 2.00V/ 3 4 200.0ns/ 0.0s Auto 1 2.53V
Events
Edge
1: -1.200ns
Channel 2 Menu
Coupling DC
Impedance 1M Ω
BW Limit
Fine
Invert
Probe

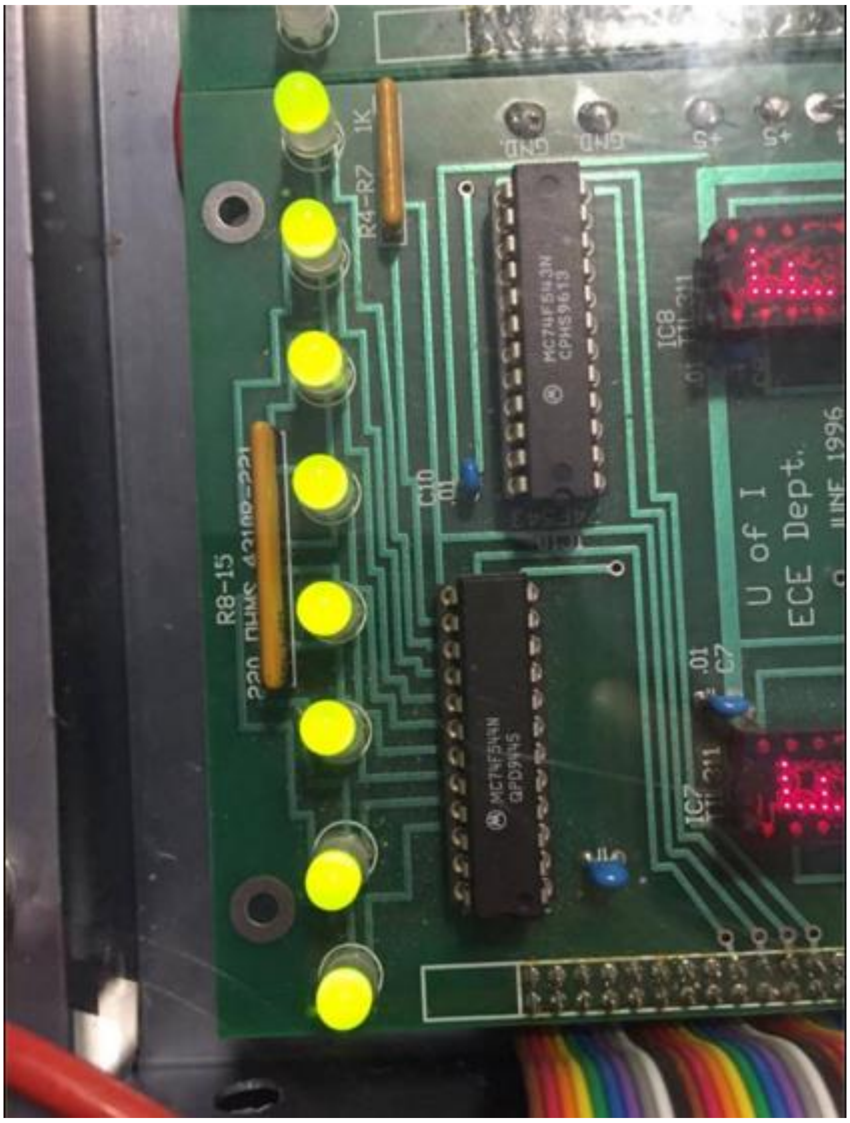
It is clear to see from circuit two that our glitch has now disappeared and our redesign worked perfectly.

POST LAB

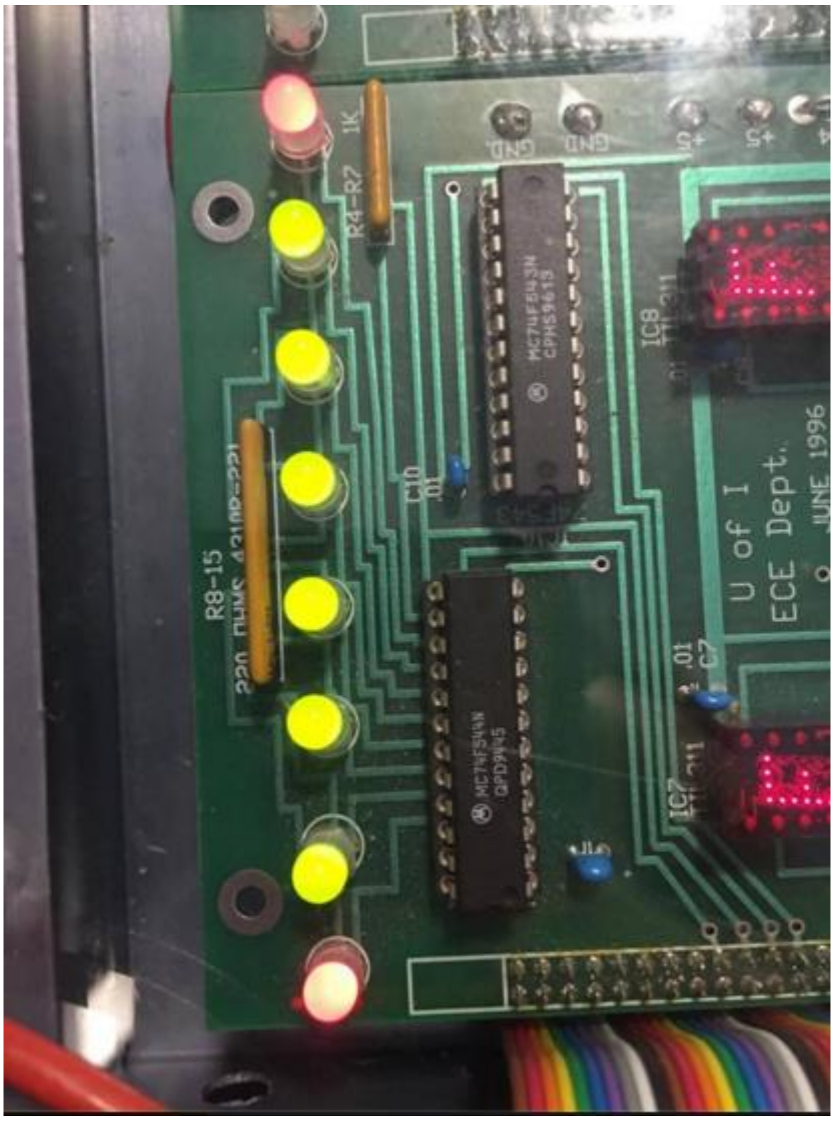


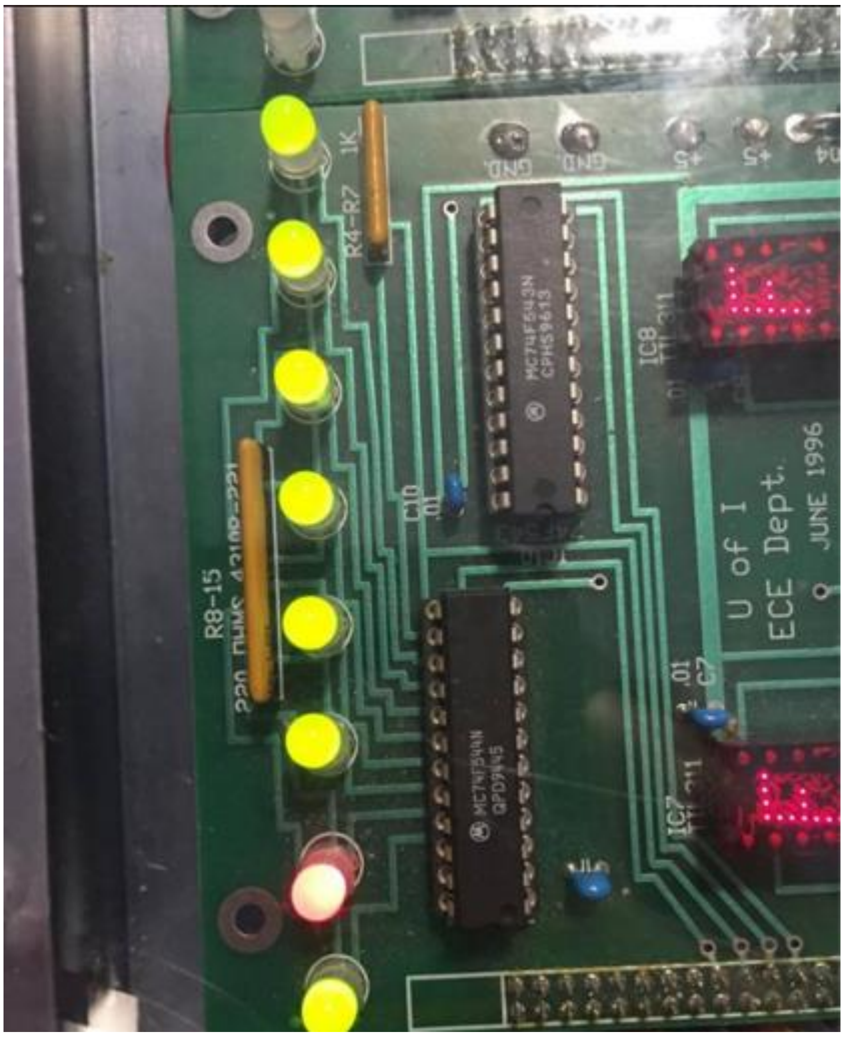
It takes 60ns for Z to stabilise on the falling edge of B. It also takes 60ns on the rising edge of B. When a mechanical switch is closed the components inside bounce; causing the switch to open for a brief amount of time. When the switch in the given debouncing circuit is in the up position the upper gates output must be a one. This and the logic one created by the pull-up resistor make the lower gate a zero. This switch may bounce however it is assumed that it will never bounce completely across the gap to the other side. This r latch will maintain its state if the switch is in-between the two terminals which eliminates the effects of bouncing.

Question 2



GND
GND
+5
+5
R4-R7
1K
R8-15
MC74F544N
IC8
TIL311
C10
.01
MC74F544N
.01
C7
IC7
TIL311
U of I
ECE Dept.
JUNE 1996


GND
GND
+5
+5
1K
R4-R7
R8-15
220 OHMS 4310R-221
MC74F543N
CPHS9613
IC8
TIL311
C10
.01
U of I
ECE Dept.
JUNE 1996
.01
C7
IC7
TIL311
MC74F544N
QPD9945



LED’s lighting and showing input and output.