Programmable Logic

PAL, PLA

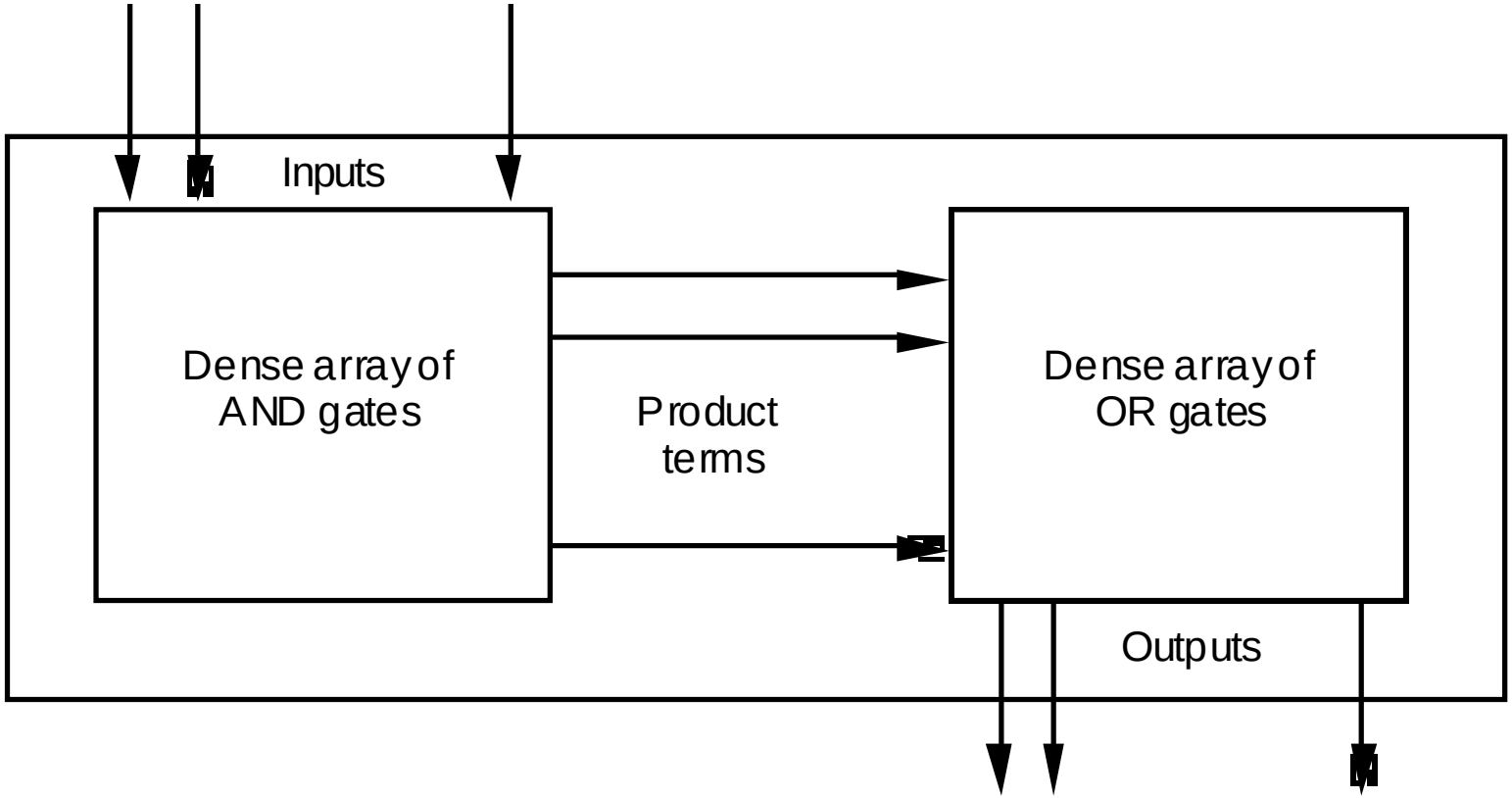
PLAs

Programmable Logic Array

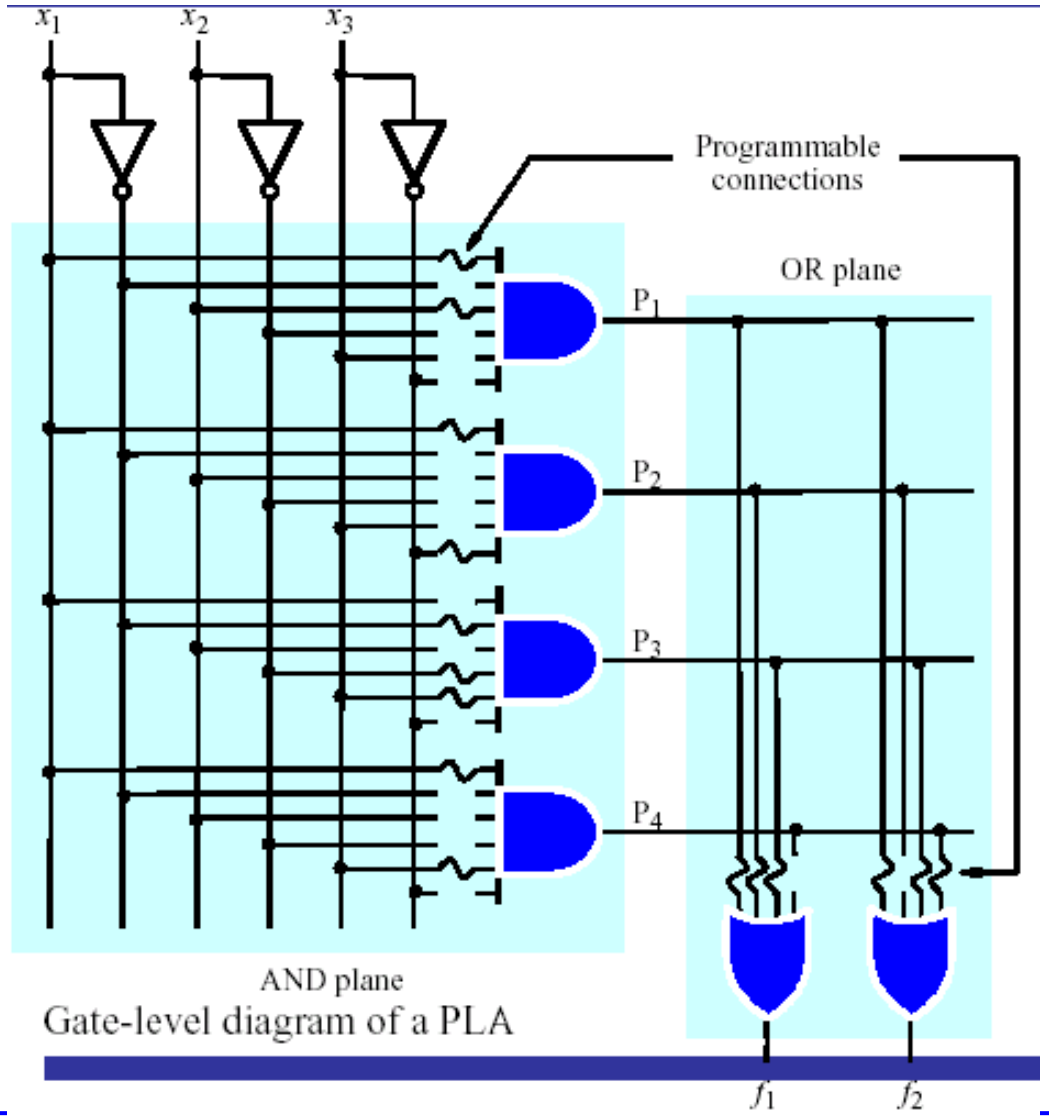
- Pre-fabricated building block of many AND/OR gates (or NOR, NAND)
- General purpose logic building blocks
- “Personalized” or “customized” by making/breaking connections among the gates
- This process is called “programming”

PLA

- **Realizes Sums of Products**

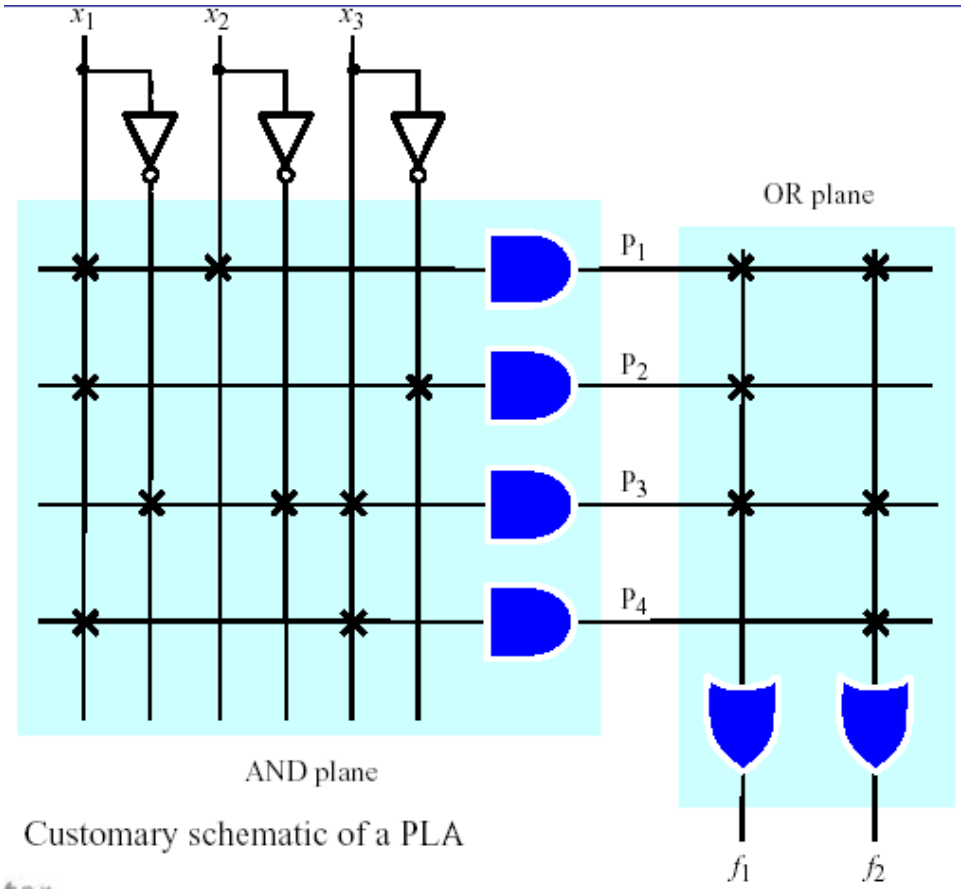


PLA



Gate-level diagram of a PLA

PLA



Customary schematic of a PLA

- **A 3×2 PLA with 4 product terms.**

Design for PLA: Example

- Implement the following functions using PLA

F0 = A + B' C'
F1 = A C' + A B
F2 = B' C' + A B
F3 = B' C + A

Personality Matrix

Product term	Inputs A	B	C	Outputs F_0	F_1	F_2	F_3
A B	1	1	-	0	1	1	0
$\overline{B}$ C	-	0	1	0	0	0	1
A $\overline{C}$	1	-	0	0	1	0	0
$\overline{B}$ $\overline{C}$	-	0	0	1	0	1	0
A	1	-	-	1	0	0	1

Input Side:

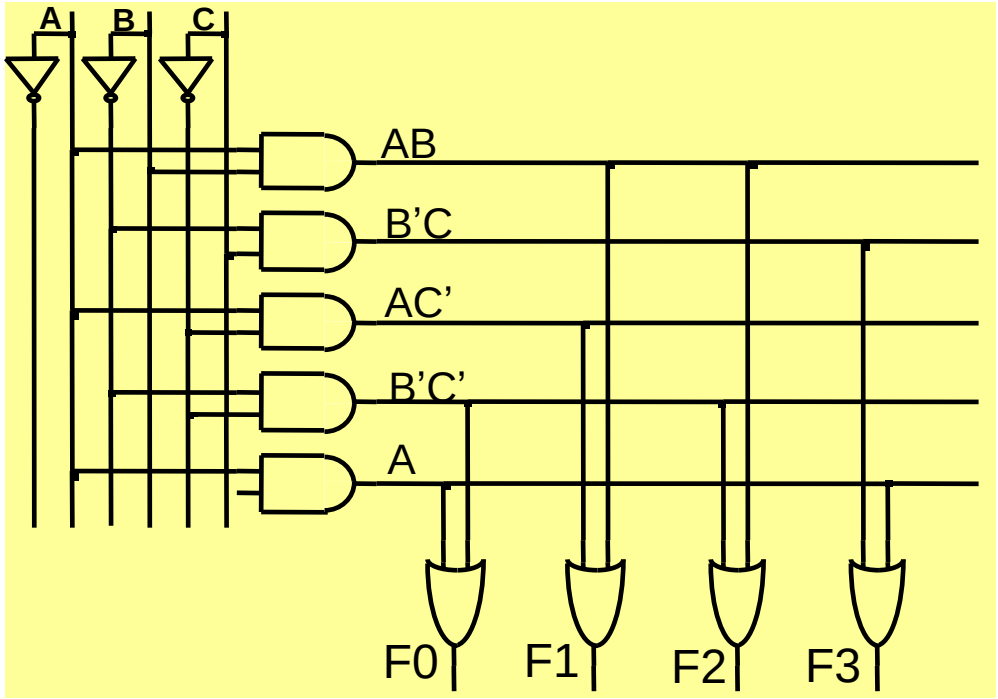
1 = asserted in term
0 = negated in term
- = does not participate

Output Side:

1 = term connected to output
0 = no connection to output

Example: Continued

F0 = A + B' C'
F1 = A C' + A B
F2 = B' C' + A B
F3 = B' C + A

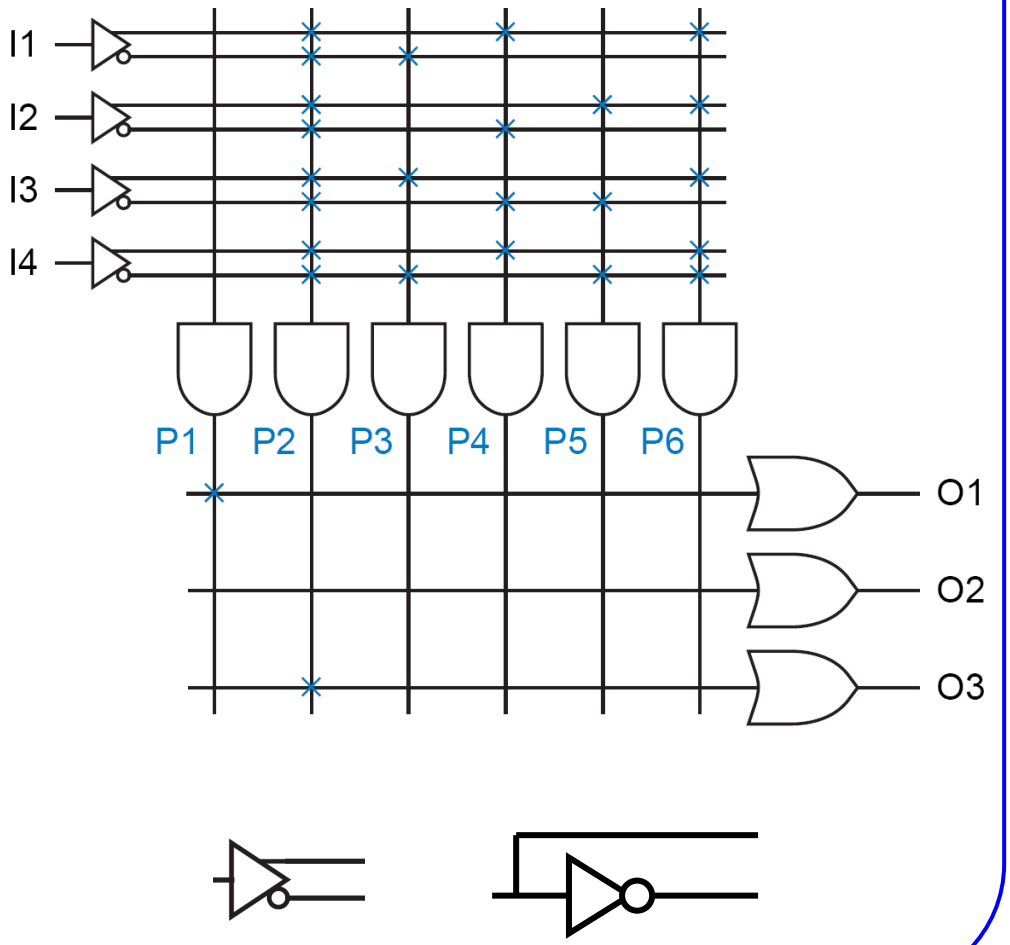


Personality Matrix

Product term	Inputs A	B	C	Outputs F_0	F_1	F_2	F_3
A B	1	1	-	0	(1)	(1)	0
$\overline{B}$ C	-	0	1	0	0	0	(1)
A $\overline{C}$	1	-	0	0	(1)	0	0
$\overline{B}$ $\overline{C}$	-	0	0	(1)	0	(1)	0
A	1	-	-	(1)	0	0	(1)

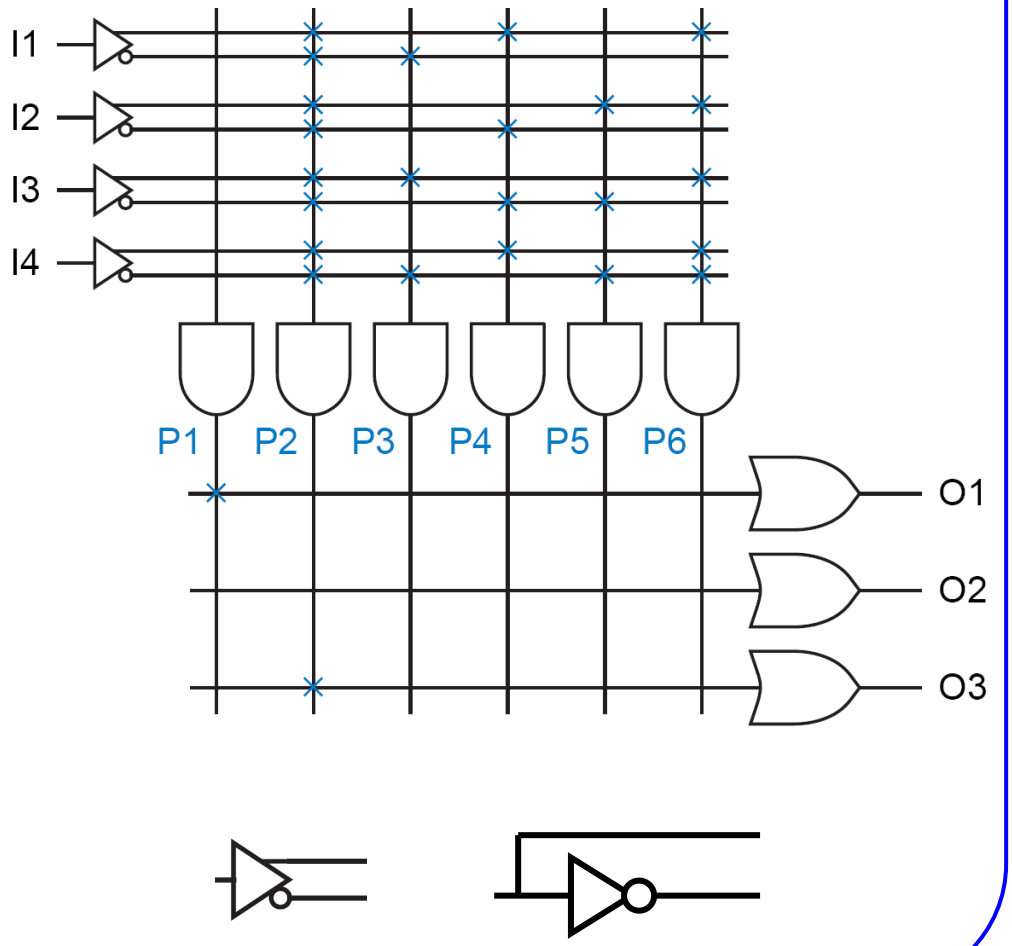
Generating Constant 1 at output

- Sometimes a PLA output must be programmed to be a constant 1 or a constant 0.
- Use OR gates to generate a constant 1



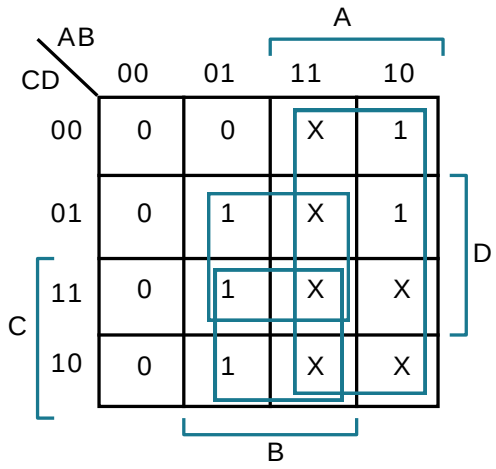
Generating Constant 0 at output

- Use one of the AND gates to generate a constant 0

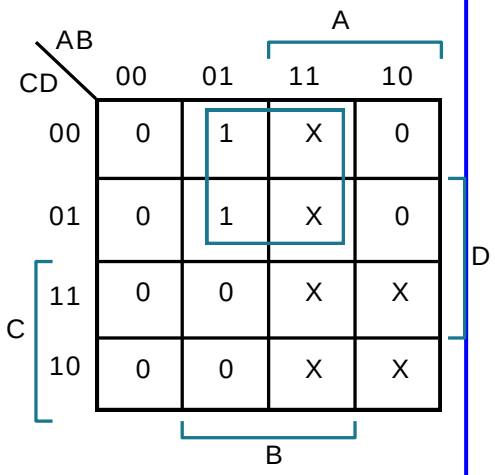


BCD to Gray Code Converter

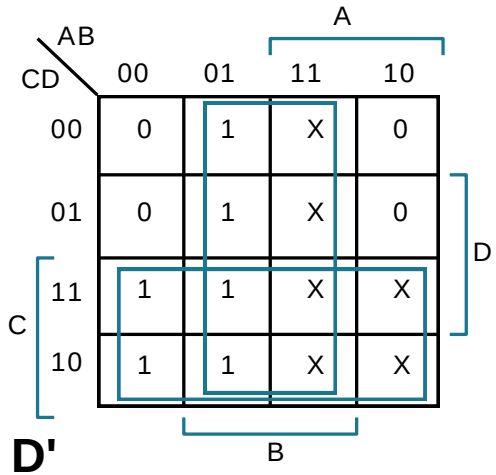
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X



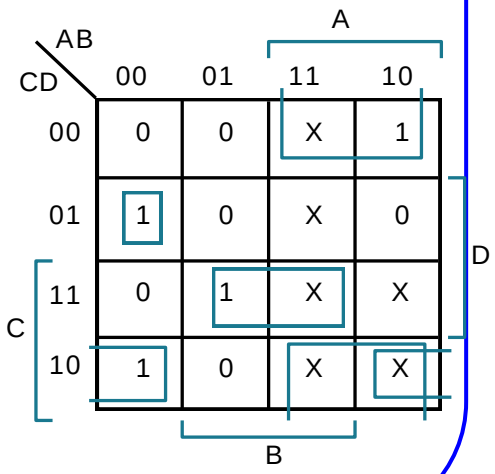
K-map for W



K-map for X



K-map for Y



K-map for Z

Minimized Functions:

W = A + B D + B C
X = B C'
Y = B + C
Z = A'B'C'D + B C D + A D' + B' C D'

Example (Continued)

Notes:

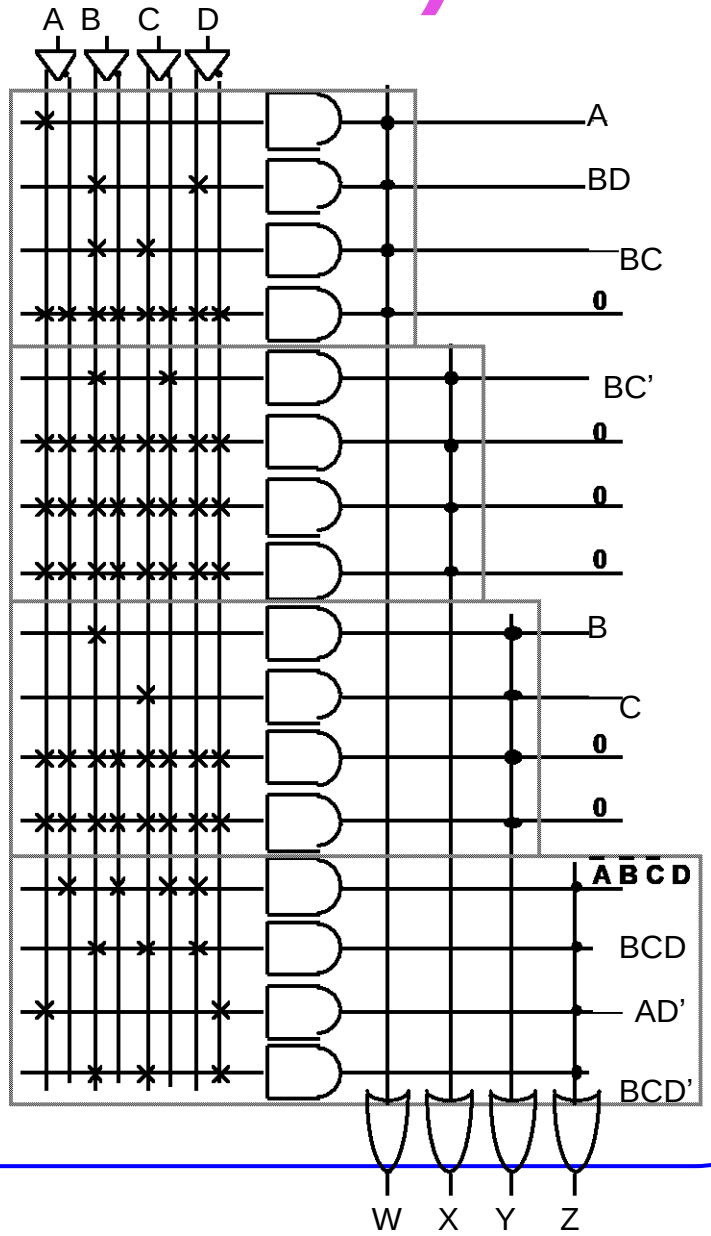
- 4 product terms preassigned to each OR gates' inputs

- The OR gates' inputs may or may not be internally pulled down by the manufacturer

- It is a safe engineering practice to not leave any OR input unconnected

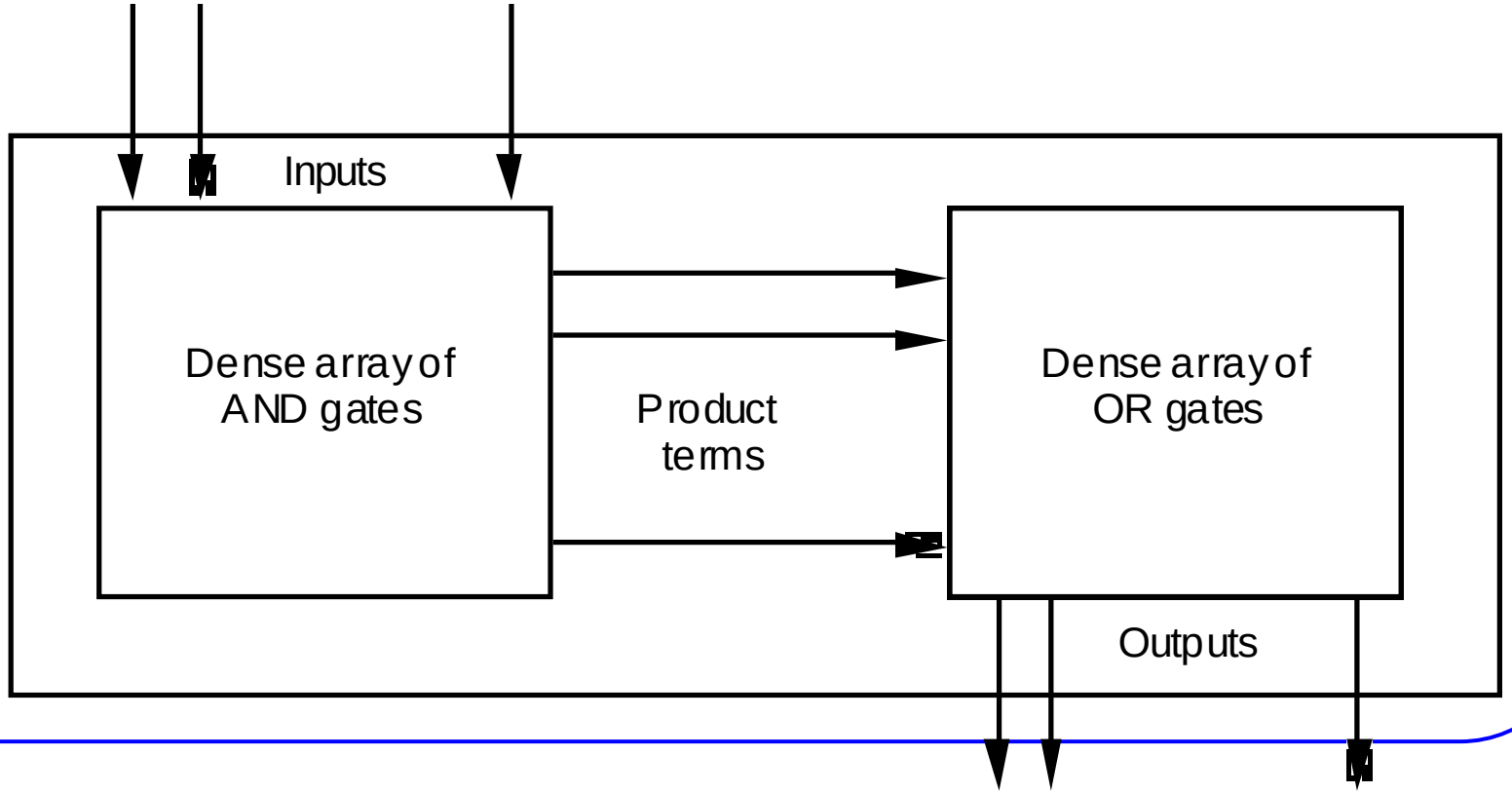
- A PLA achieves higher flexibility at the cost of lower speed!

- Too much programmability?



PALs

- **Programmable Array Logic**
  - Realizes Sums of Products but with a *fixed* OR array



PAL

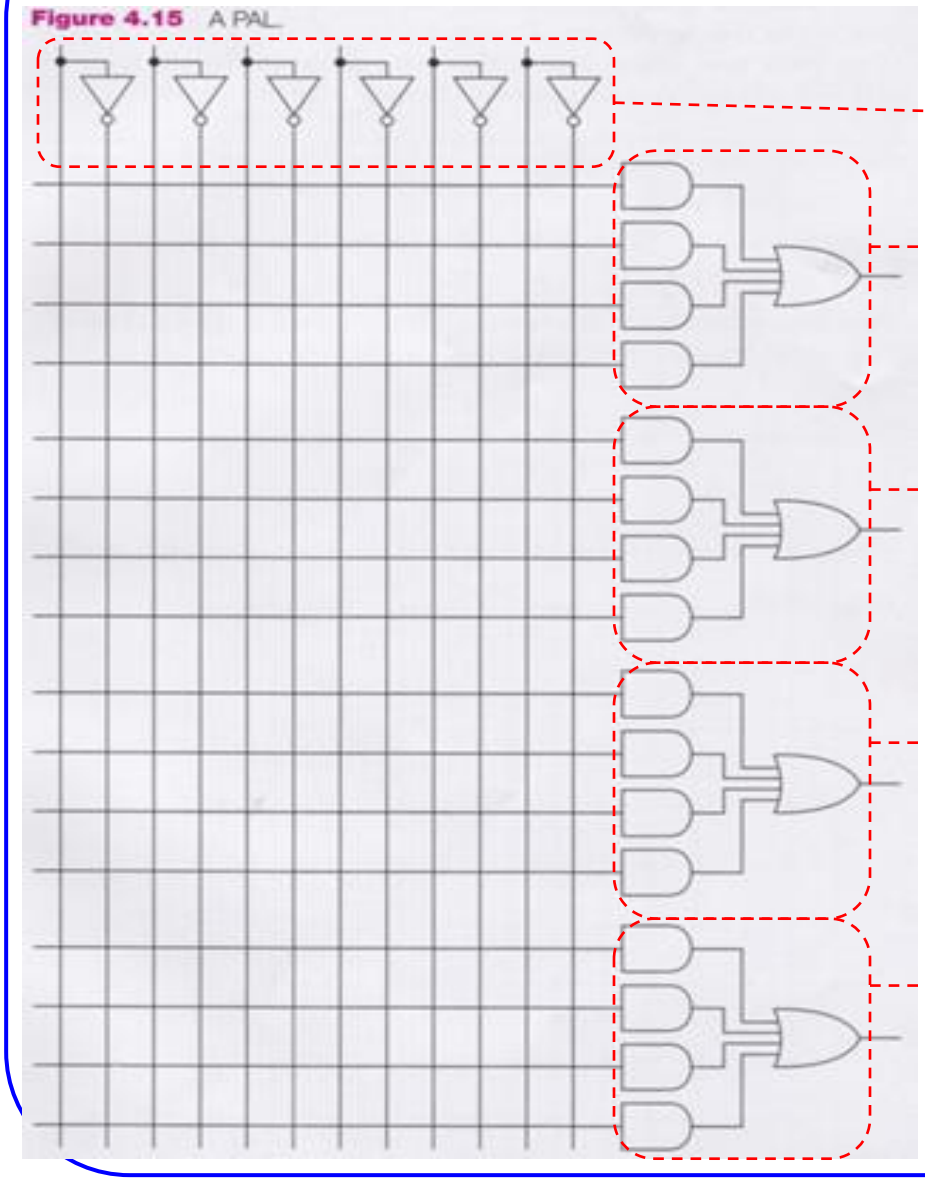
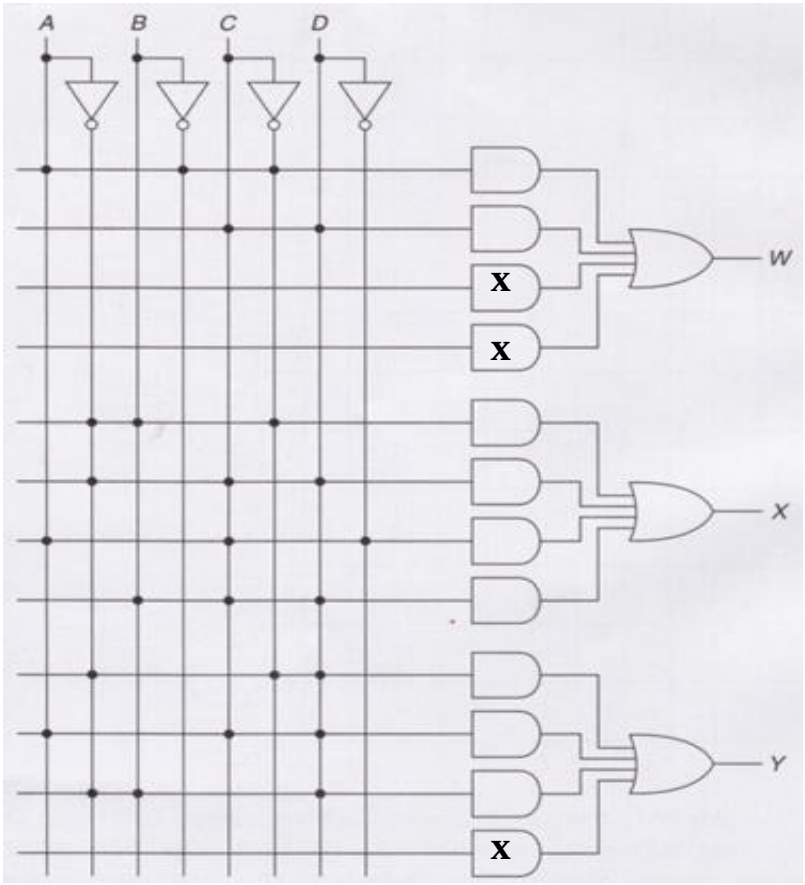


Figure 4.15 A PAL
inputs
1st output section
2nd output section
3rd output section
4th output section
Only functions with at most four products can be implemented

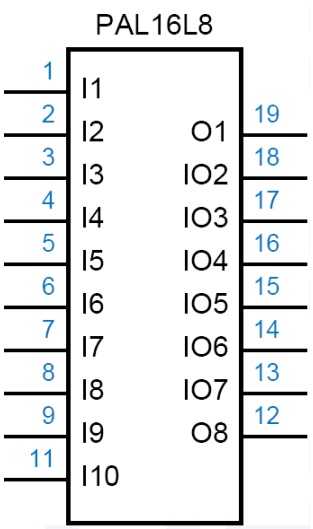
PAL

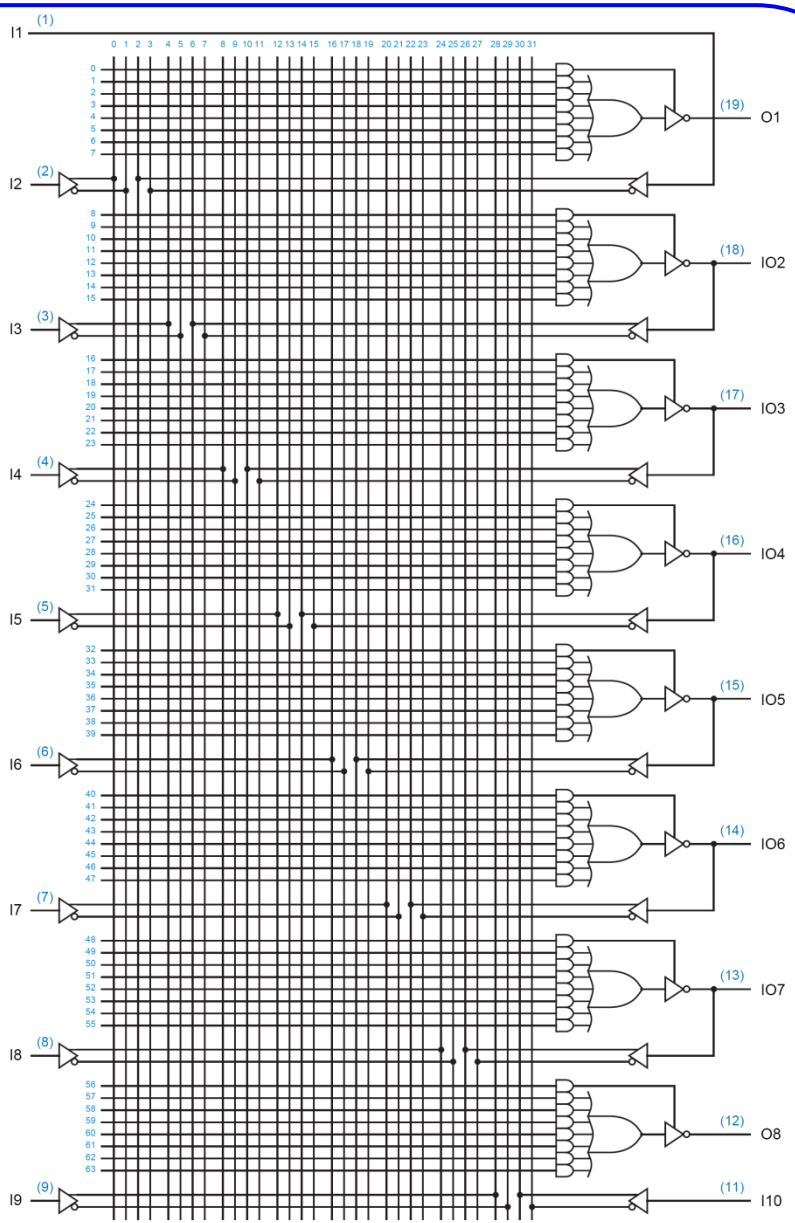


$W = AB'C' + CD$

$X = A'BC' + A'CD + ACD' + BCD$

$Y = A'C'D + ACD + A'BD$


PAL16L8
1
I1
2
I2
3
I3
4
I4
5
I5
6
I6
7
I7
8
I8
9
I9
11
I10
19
O1
18
IO2
17
IO3
16
IO4
15
IO5
14
IO6
13
IO7
12
O8


I1
(1)
I2
(2)
I3
(3)
I4
(4)
I5
(5)
I6
(6)
I7
(7)
I8
(8)
I9
(9)
(19)
O1
(18)
IO2
(17)
IO3
(16)
IO4
(15)
IO5
(14)
IO6
(13)
IO7
(12)
O8
(11)
I10

Helper Terms

- If an I/O pin's output-control gate produces a constant 1, → the output is always enabled, but the pin may still be used as an input too.
- → outputs can be used to generate first-pass "helper terms" for logic functions that cannot be performed in a single pass with the limited number of AND terms available for a single output.