فرهاد امان ۹۹۳۱۰۰۶ پیش گزارش ۴

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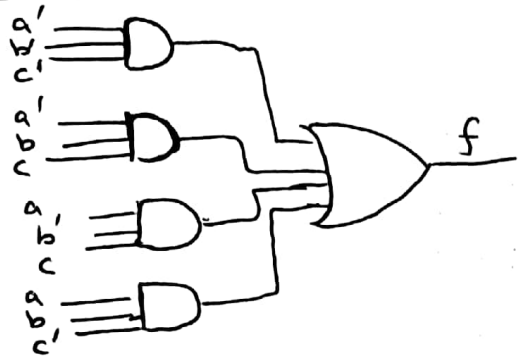
a	b	c	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

SOP: $a'b'c' + a'bc + ab'c + abc'$



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```
module parity_bit (A, B, C, f);
    input A, B, C;
    output f;
    wire w1, w2, w3, w4, A_bar, B_bar, C_bar;

    not n1(A_bar, A);
    not n2(B_bar, B);
    not n3(C_bar, C);

    and a1(w1, A_bar, B_bar, C_bar);
    and a2(w2, A_bar, B, C);
    and a3(w3, A, B_bar, C);
    and a4(w4, A, B, C_bar);

    or o(f, w1, w2, w3, w4);
end module
```