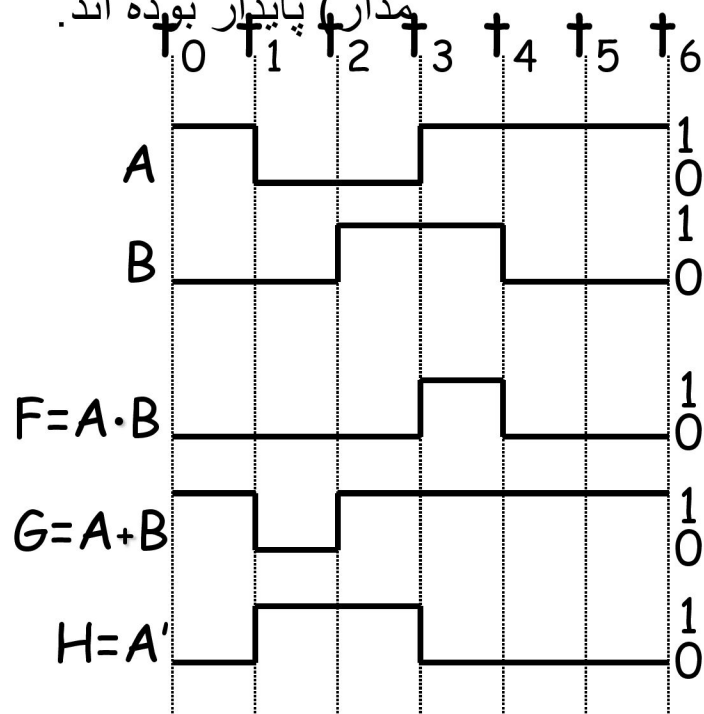


Hazard

شکل موج ها

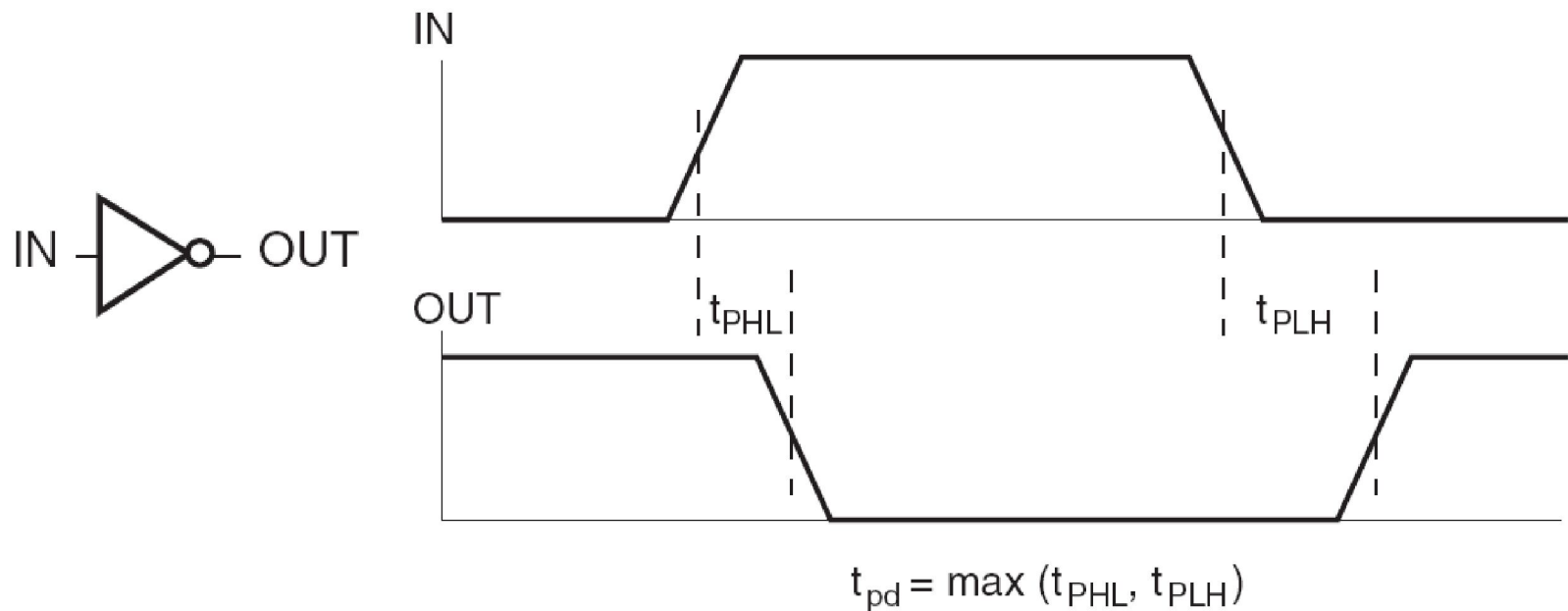
➤ تا به حال تاخیر گیت ها در نظر گرفته نمی شدند:

- تاخیر صفر: غیر واقعی
- یا علاقه به دانستن رفتار حالت پایدار
- فرض: ورودی ها برای مدت طولانی (نسبت به تاخیرالمان های مدار) پایدار بوده اند.



تاخیر

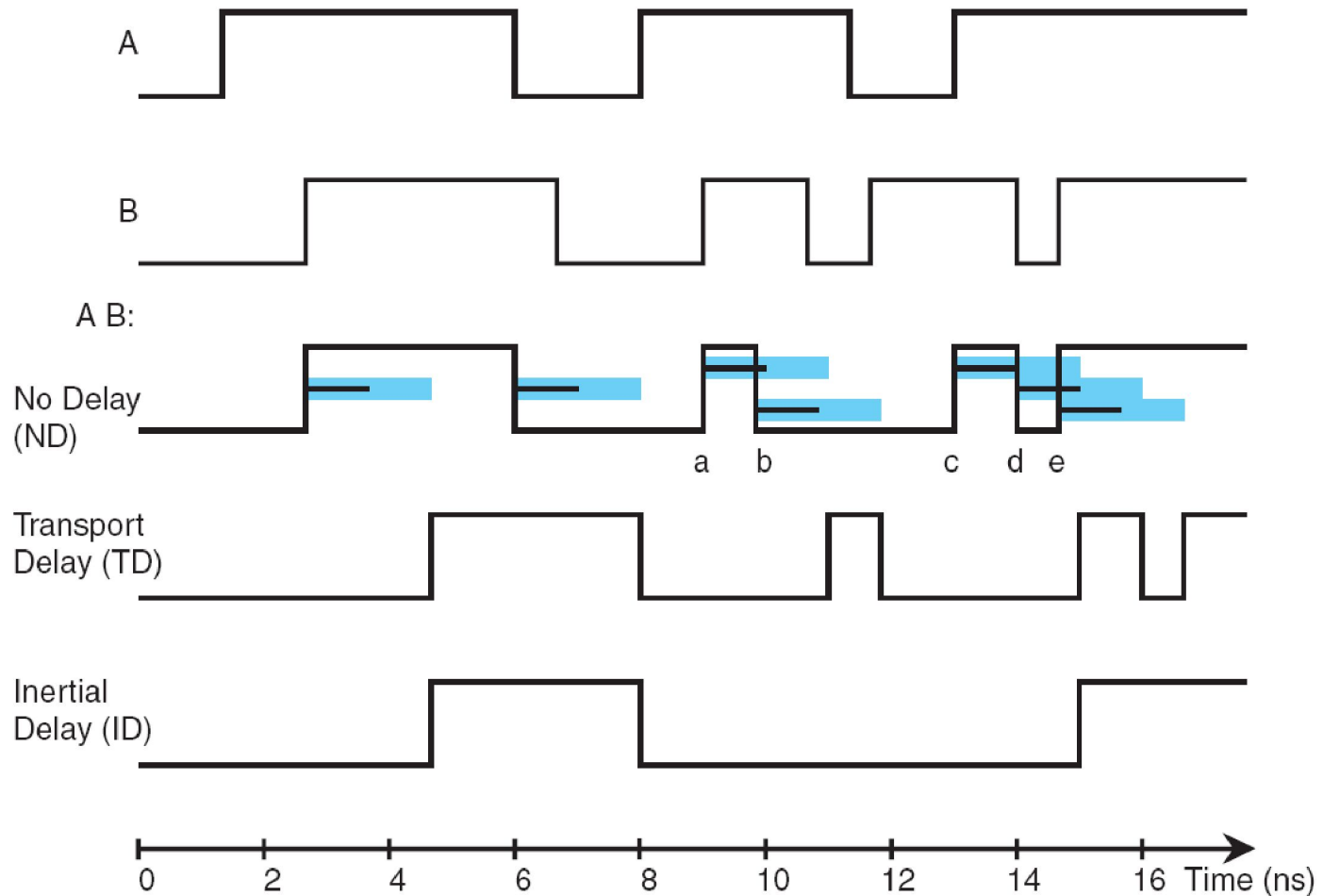
- تاخیر در مدارها



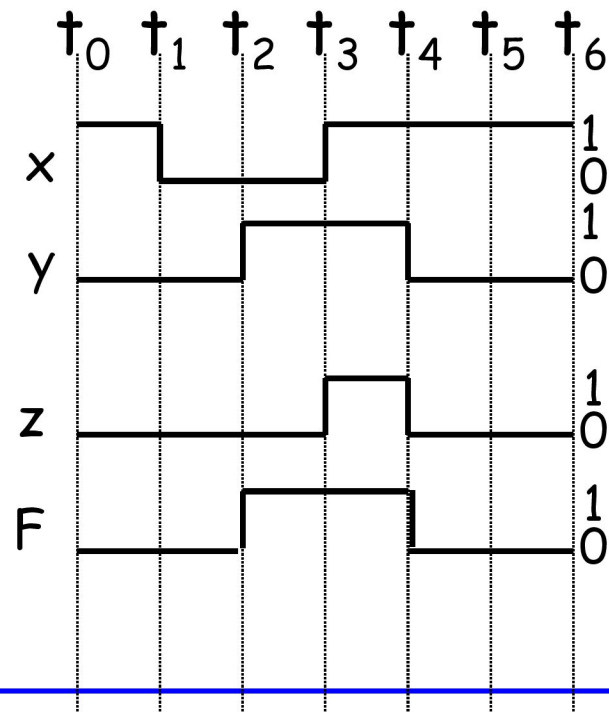
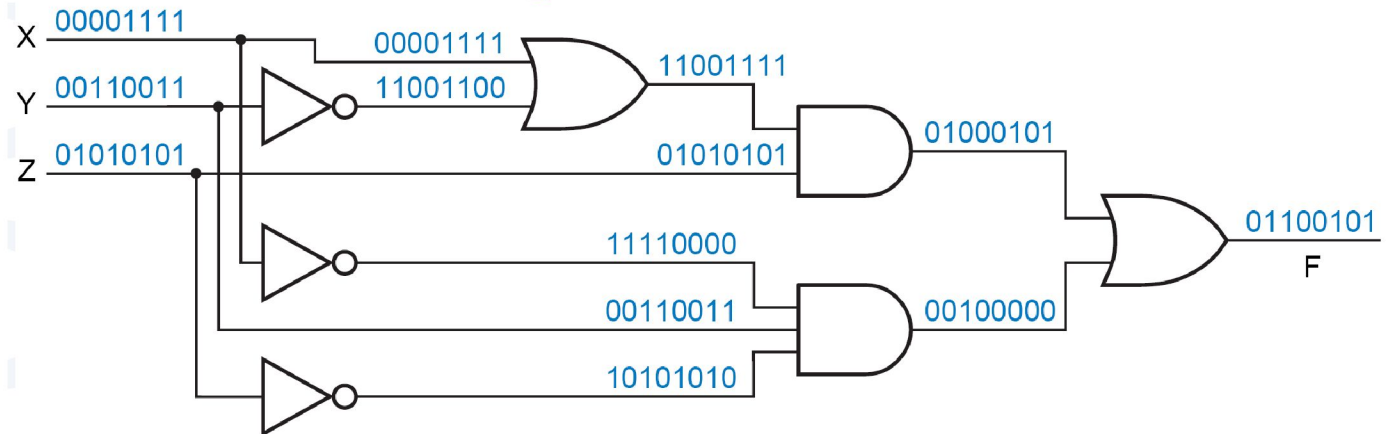
Propagation Delay for an Inverter

تاخیرها

- Inertial Delay
- Transport Delay



شکل موج ها



Hazard

➤ تاخیرها ممکن است باعث پالس‌های ناخواسته شوند

Glitch -

• هازارد:

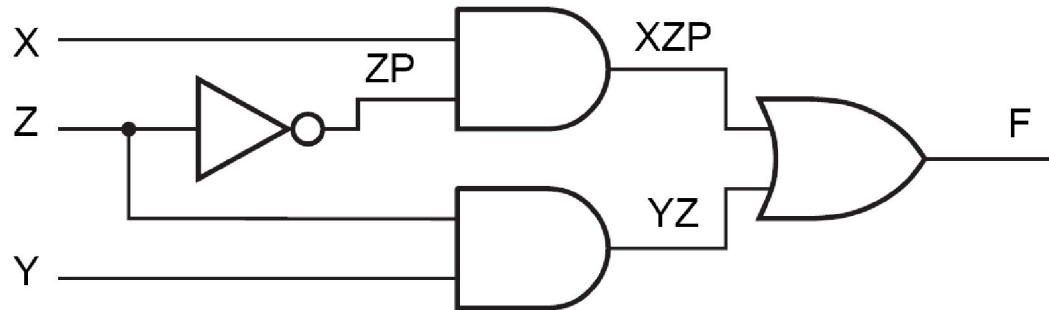
➤ مداری که احتمال ایجاد glitch در آن هست، هازارد دارد.

• دو نوع:

➤ استاتیک

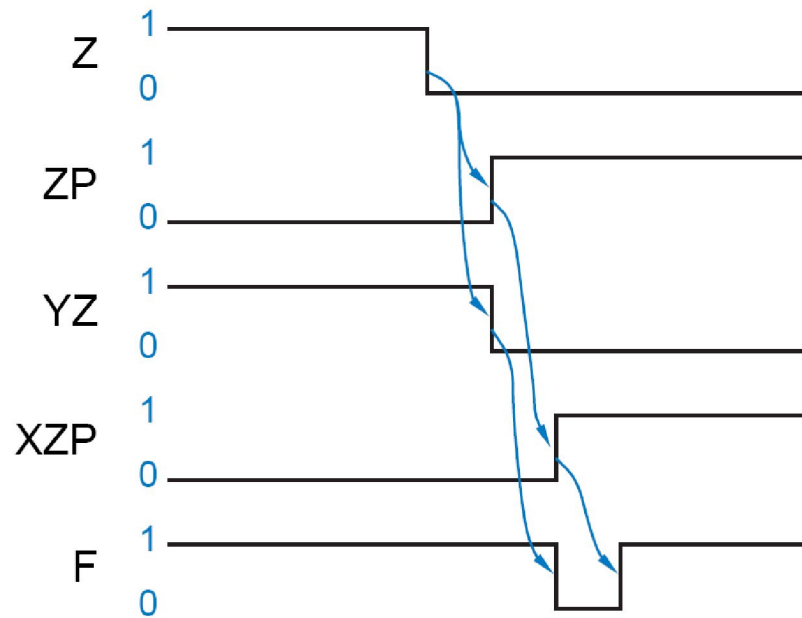
➤ دینامیک

مثال



Initially:

$$X=Y=Z=1$$



Static Hazard

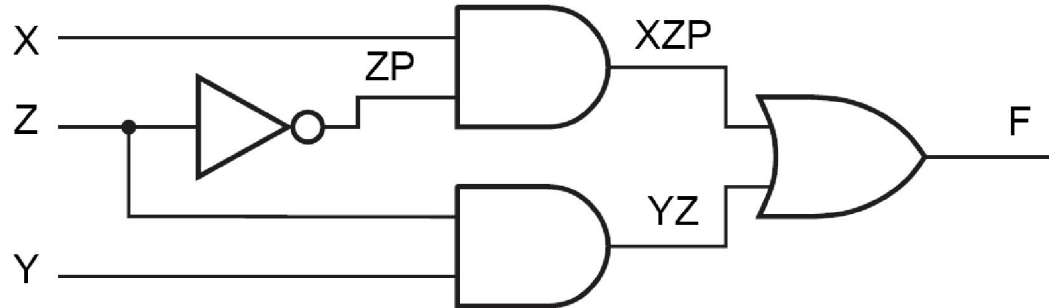
- **Informal Definition:**

- A static-1 hazard is the possibility of a 0 glitch when we expect the output to remain at a nice steady 1 based on a static analysis

- **Formal Definition:**

- A static-1 hazard is a pair of input combinations that:
 - (a) differ in only one input variable and
 - (b) both give a 1 output such that it is possible for a momentary 0 output to occur during a transition in the differing input variable.

مثال



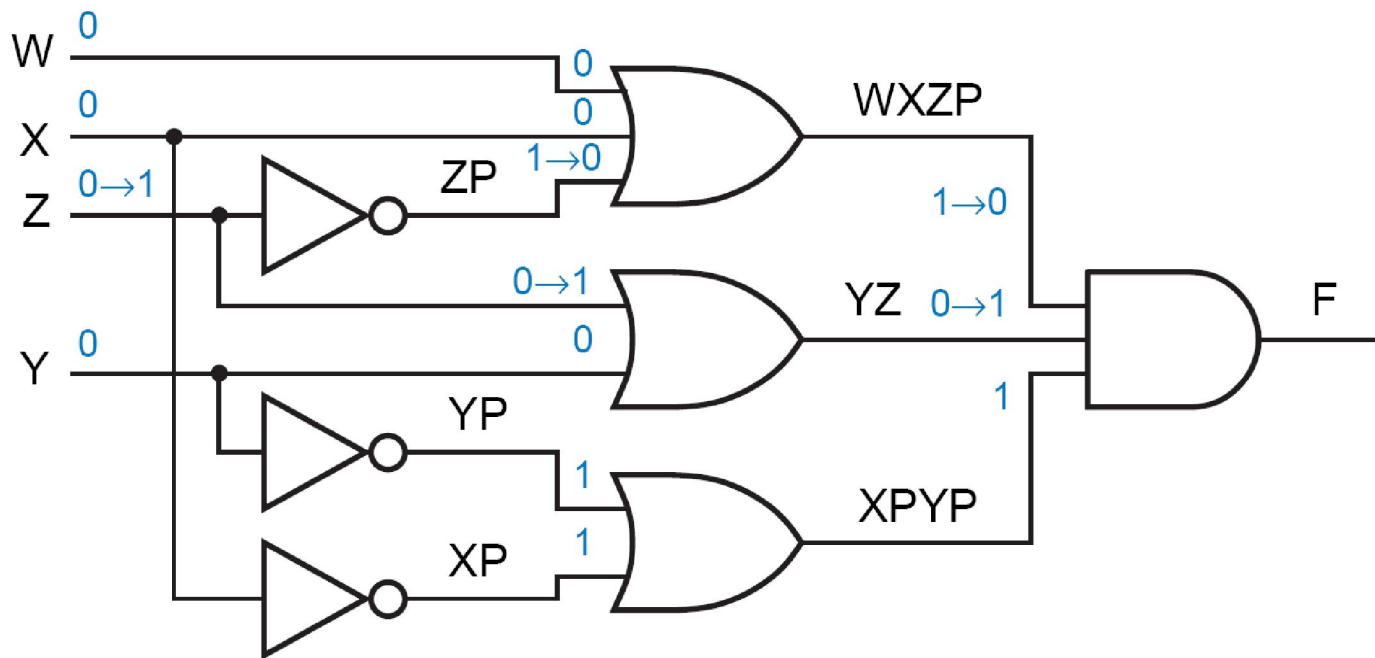
- Even though “static” analysis predicts that the output is 1 for both input combinations $X, Y, Z = 111$ and $X, Y, Z = 110$, F goes to 0 for one time unit.

Static-0 Hazard

- A static-0 hazard is just the **dual** of a static-1 hazard
- A properly designed **two-level sum-of-products** (AND-OR) circuit can have no static-0 hazards
- An **OR-AND circuit** that is the dual of the example circuit could potentially have a static-0 hazard

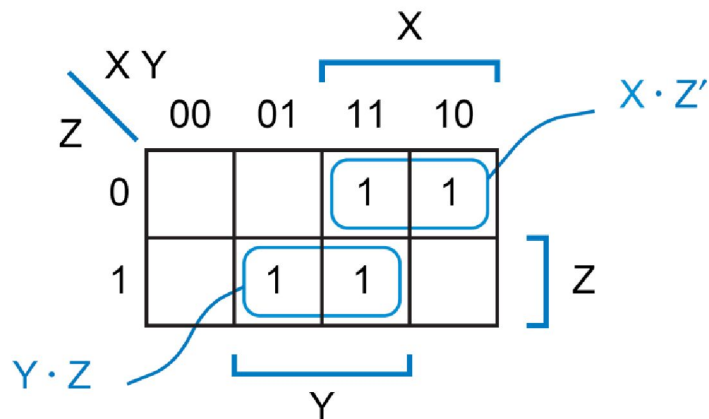
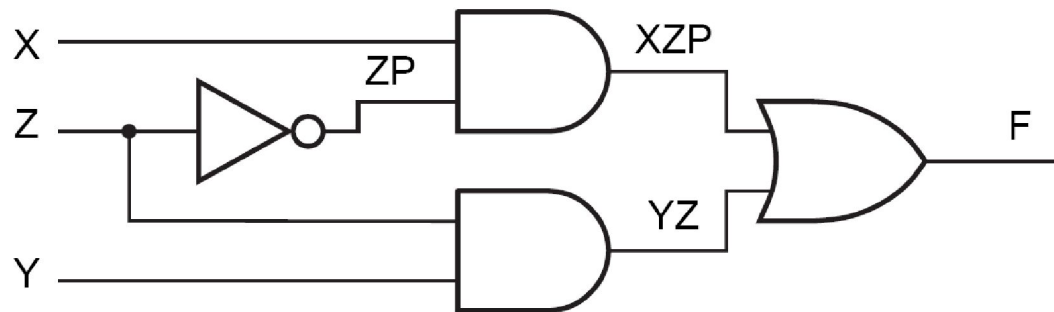
مثال

• تحلیل کنید:

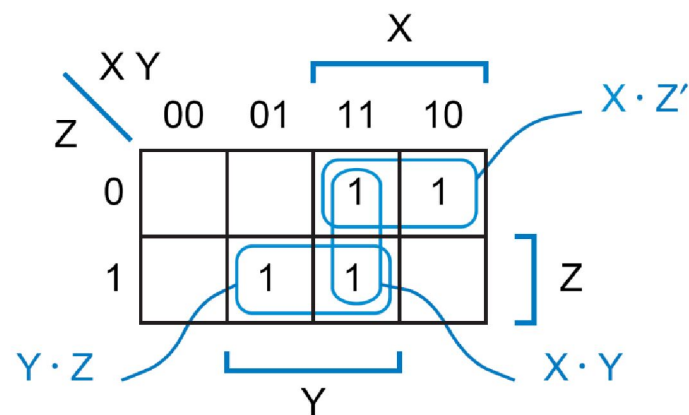


تشخیص هازارد

- A **Karnaugh map** can be used to detect static hazards in a two-level SoP or PoS circuit:

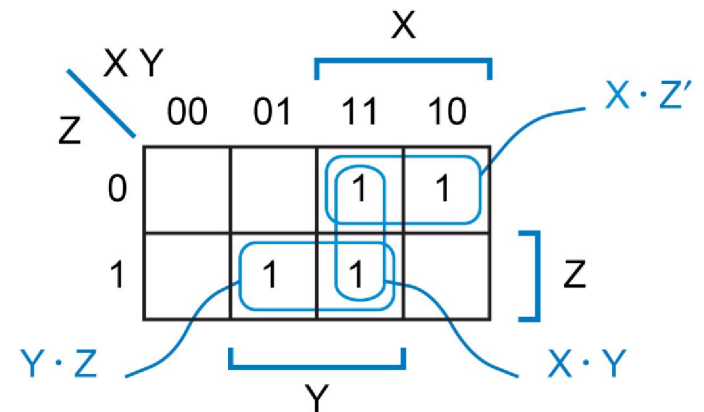
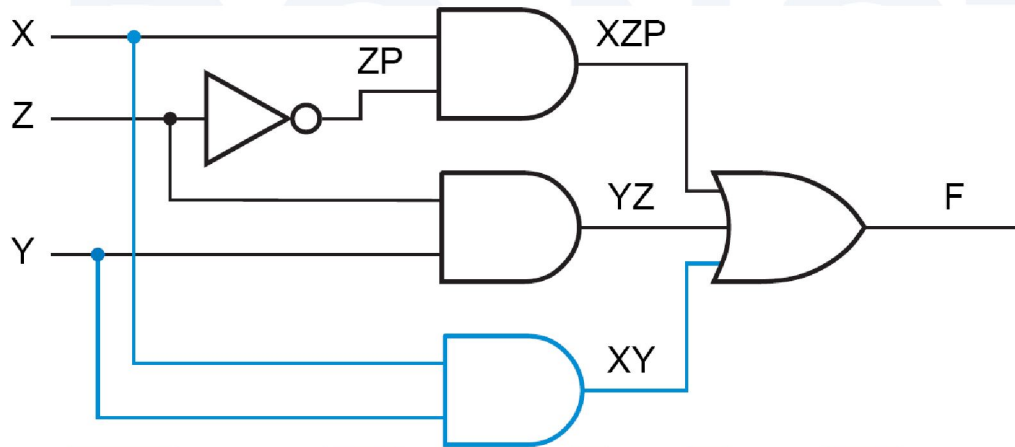


$$F = X \cdot Z' + Y \cdot Z$$



$$F = X \cdot Z' + Y \cdot Z + X \cdot Y$$

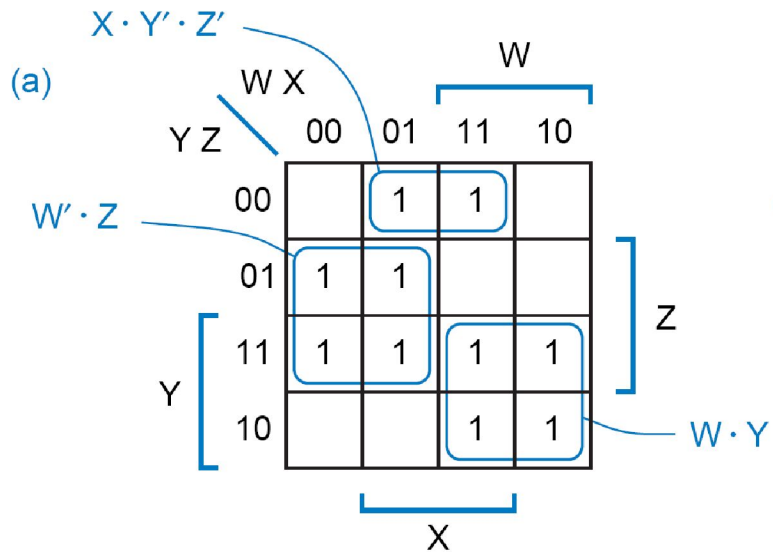
رفع هزارد



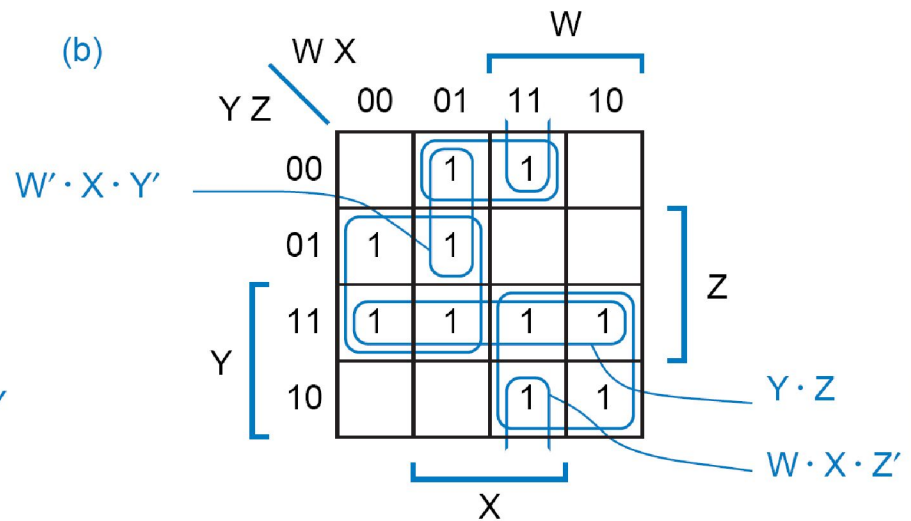
$$F = X \cdot Z' + Y \cdot Z + X \cdot Y$$

- Note the tradeoff between determinism and cost (number of gates)!

مثال



$$F = X \cdot Y' \cdot Z' + W' \cdot Z + W \cdot Y$$

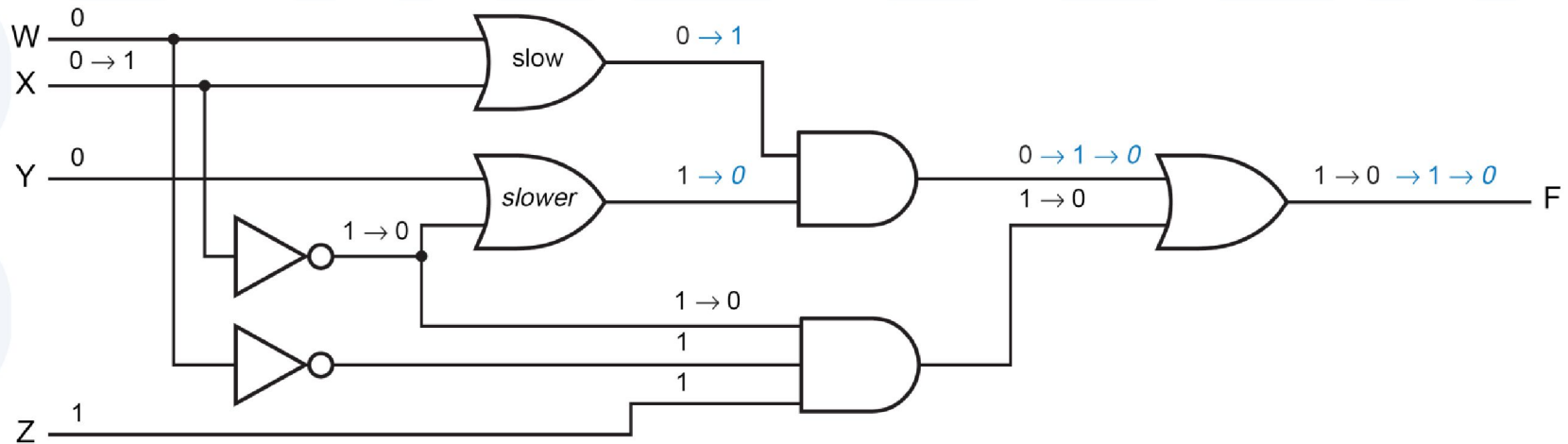


$$F = X \cdot Y' \cdot Z' + W' \cdot Z + W \cdot Y + W \cdot X \cdot Y' + Y \cdot Z' + W \cdot X \cdot Z'$$

Dynamic Hazard

- **Dynamic hazard:**
 - The possibility of an output changing **more than once** as the result of a single input transition.
 - Multiple output transitions can occur if there are **multiple paths with different delays** from the changing input to the changing output.

مثال



➤ سه مسیر از X به F با سه تاخیر مختلف

➤ $F=1 \leftarrow W, X, Y, Z = 0, 0, 0, 1$

➤ فرض: X یک شود.

➤ فرض: دو OR میانی کند و بقیه گیت‌ها عادی هستند.

- اول تغییرات مشکي $F=0 \leftarrow$

- بعد آبی غیر ایتالیکی

- بعد آبی ایتالیکی

Hazard-Free Design

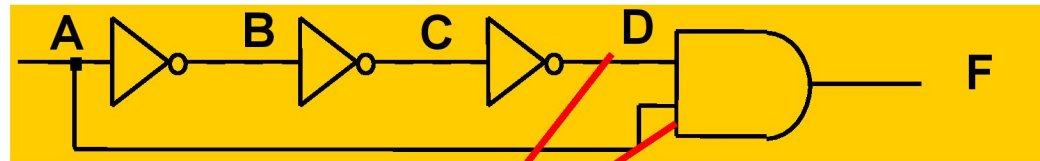
- Techniques for finding hazards in arbitrary circuits, are rather difficult to use.
 - → when you require a hazard-free design, it's best to use a circuit structure that is easy to analyze.
- In particular, two-level AND-OR circuit has no static-0 or dynamic hazards.
- Static-1 hazards may exist in such a circuit but they can be found and eliminated using K-map.

نکته

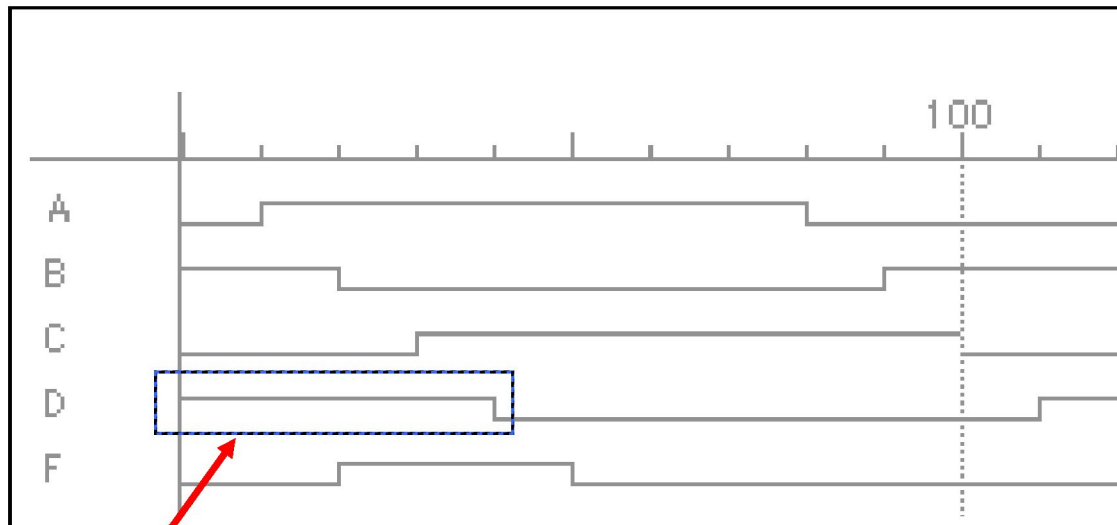
- **Most Hazards are not hazardous:**

- A well-designed, **synchronous** digital system is structured so that hazard analysis is not needed for most of its circuits.
- In a synchronous system, all of the inputs to a combinational circuit are changed at a particular time, and the outputs are not “looked at” until they have had time to settle to a steady-state value.
- Hazard analysis and elimination are typically needed only in the design of **asynchronous sequential** circuits.
- Asynchronous circuits are not the mainstream but if you want to design them, an understanding of hazards will be absolutely essential for a reliable result.

Pulse-Shaping Circuit



$$A' \cdot A = 0$$



3 gate delays

D remains high for
three gate delays after
A changes from low to high

F is not always 0!