فرهاد امان ۹۹۳۱۰۰۶ پیش گزارش ۸

```
module mux4X1 (
    input [3:0] w3,
    input [3:0] w2,
    input [3:0] w1,
    input [3:0] w0,
    input [1:0] sel,
    output [3:0] y
);
    assign y = sel[1] ? (sel[0] ? w3 : w2) : (sel[0] ? w1 : w0);
endmodule

module alu (
    input [1:0] A,
    input [1:0] B,
    input [1:0] sel,
    output [3:0] Y
);
    wire [3:0] Mul;
    wire [3:0] Add;
    wire [3:0] Nand;
    wire [3:0] Not;
    assign Mul = {A[1] & A[0] & B[1] & B[0], (A[1] & B[1] & ~B[0]) |
    (A[1] & B[1] & ~A[0]), (~A[1] & A[0] & B[1]) | (A[0] & B[1] & ~B[0]) |
    (A[1] & ~B[1] & B[0]) | (A[1] & ~A[0] & B[0]), A[0] & B[0]};
    assign Add = A + B;
    assign Nand = {0, 0, ~(A[1] & B[1]), ~(A[0] & B[0])};
    assign Not = {0, 0, ~A[1], ~A[0]};
    mux4X1 m1 (Mul, Add, Nand, Not, sel, Y);
```