Electrical Rules Check Report

Class	Document	Message
Warning	sample_board.SchDoc	Nets Wire SAMPLE-VH1_P has multiple names (Net Label SAMPLE-VH1_P, Net Labe SAMPLE-VH2_P)
Warning	sample_board.SchDoc	Off grid Net Label SAMPLE-I_P at 4841.509mil,4150mi
Warning	sample_board.SchDoc	Off grid Net Label SAMPLE-VH1_P at 4696.006mil,4550mi
Warning	sample_board.SchDoc	Off grid Net Label SAMPLE-VH2_N at 4678.671mil,4250mi
Warning	sample_board.SchDoc	Off grid Net Label SAMPLE-Vr_N at 4758.962mil,4650mi
Warning	sample_board.SchDoc	Off grid Net Label SAMPLE-Vr_P at 4776.297mil,4750mi

Design Rules Verification Report

Filename : C:\Users\Shadow\Desktop\Repos\ltk-hall-electronics\boards\sample\sample_l

Warnings 0
Rule Violations 6

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (Disabled)(All),(All)	0
Short-Circuit Constraint (Allowed=No) (Disabled)(All),(All)	0
Un-Routed Net Constraint ((All))	6
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=50mil) (Preferred=25mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=1mil) (Max=100mil) (Disabled)(All)	0
Hole To Hole Clearance (Gap=10mil) (Disabled)(All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (Disabled)(All),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Silk primitive without silk layer	0
Total	6

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Via (256mil,1870.001mil) from Top Layer to Bottom Layer Dead Copper - Net Not Assignec
Un-Routed Net Constraint: Via (510mil,1470mil) from Top Layer to Bottom Layer Dead Copper - Net Not Assignec
Un-Routed Net Constraint: Via (510mil,1560mil) from Top Layer to Bottom Layer Dead Copper - Net Not Assignec
Un-Routed Net Constraint: Via (630mil,1470mil) from Top Layer to Bottom Layer Dead Copper - Net Not Assignec
Un-Routed Net Constraint: Via (630mil,1560mil) from Top Layer to Bottom Layer Dead Copper - Net Not Assignec
Un-Routed Net Constraint: Via (887mil,1871.001mil) from Top Layer to Bottom Layer Dead Copper - Net Not Assignec