Electrical Rules Check Report

Class	Document	Message
		Successful Compile for probe.PrjPcb

Design Rules Verification Report

Filename : C:\Users\Shadow\Desktop\Repos\ltk-hall-electronics\boards\probe\probe.PcbDoc

Warnings 0
Rule Violations 34

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=6mil) (All),(All)	12
Short-Circuit Constraint (Allowed=No) (All),(All)	13
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=6mil) (Max=200mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=11.811mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	3
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	2
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All	0
Total	34

Clearance Constraint (Gap=6mil) (All),(All)
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-1(302.724mil,3542.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-1(302.724mil,3542.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-2(254.724mil,3541.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-2(254.724mil,3541.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-3(204.724mil,3543.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-3(204.724mil,3543.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-4(155.724mil,3542.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-4(155.724mil,3542.307mil) o
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Trac
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Trac
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Trac
Clearance Constraint: (Collision < 6mil) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Trac

Short-Circuit Constraint (Allowed=No) (All),(All)
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Board Cutout (Multi-Layer)Region (0 hole(s)
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-1(302.724mil,3542.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-1(302.724mil,3542.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-2(254.724mil,3541.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-2(254.724mil,3541.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-3(204.724mil,3543.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-3(204.724mil,3543.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-4(155.724mil,3542.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad U1-4(155.724mil,3542.307mil) on Multi-Laye
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (157.48mil,3456.693mil)(157.48mil,3602.132mil)
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (303.15mil,3456.693mil)(303.15mil,3598.95mi
Short-Circuit Constraint: Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track (303.15mil,3456.693mil)(303.15mil,3598.95mi

Hole Size Constraint (Min=11.811mil) (Max=100mil) (All)
Hole Size Constraint: (118.11mil > 100mil) Pad U1-1(302.724mil,3542.307mil) on Multi-Layer Actual Slot Hole Width = 118.11m
Hole Size Constraint: (118.11mil > 100mil) Pad U1-2(254.724mil,3541.307mil) on Multi-Layer Actual Slot Hole Width = 118.11m
Hole Size Constraint: (118.11mil > 100mil) Pad U1-3(204.724mil,3543.307mil) on Multi-Layer Actual Slot Hole Width = 118.11m
Hole Size Constraint: (118.11mil > 100mil) Pad U1-4(155.724mil,3542.307mil) on Multi-Layer Actual Slot Hole Width = 118.11m

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.63mil < 10mil) Between Pad U1-1(302.724mil,3542.307mil) on Multi-Layer And Pa
Minimum Solder Mask Sliver Constraint: (2.63mil < 10mil) Between Pad U1-2(254.724mil,3541.307mil) on Multi-Layer And Pa
Minimum Solder Mask Sliver Constraint: (1.63mil < 10mil) Between Pad U1-3(204.724mil,3543.307mil) on Multi-Layer And Pa

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.296mil < 10mil) Between Pad P1-1(232.425mil,686.646mil) on Multi-Layer And Trac
Silk To Solder Mask Clearance Constraint: (9.296mil < 10mil) Between Pad P1-2(119.425mil,655.646mil) on Multi-Layer And Trac