COSC2406 F18 – Assembly Language Programming

Assignment 2

Due: September 30th, 2018 by 11:55pm

Answer each question in full sentences. The point value is an indication as to how much work is required for each question. Most require very simple answers. Use complete sentences for descriptive answers and explanations. Show all your calculations where answers are derived.

1. [3] There are five steps in the instructions execution cycle: three required steps and two additional steps when a memory operand is used. Name the five steps, briefly describe each and indicate the three steps which are always required by placing [REQUIRED] at the end of the description.

2. [1] When a processor switches from one task to another, what values in the first task's state must be preserved? (This is a thinking question – you will not find a clear answer in the chapter).

3. [4] The x86 processors have 4 modes of operation, three of which are primary and one sub-mode. Name and briefly describe each mode.

4. [1] When running in 64-bit programming mode, two of the four modes of operation from Q4 above are not supported. Which modes are not supported?

5. [1] The 64-bit x86-64 processors use a 48-bit physical address space. How much RAM memory can these CPU's support?

6. [8] Name all eight 32-bit general purpose registers. Identify the special purpose of each register where one exists.

7. [1] Which flag is set when the result of an *unsigned* arithmetic operation is too large to fit into the destination?

8. [1] Which flag is set when the result of a *signed* arithmetic operation is either too large or too small to fit into the destination?

9. [4] Besides the two flags identified as the answers to Q8 & Q9 above, name the four additional CPU status flags identified in class as applicable to this course and briefly describe their purpose.

FOR QUESTIONS 10 to 17, provide your final answers in Assign2_SubmsissionSheet.docx provided and create a PDF document to show your calculations.

10. [3] In a 1-GHz processor, 1 billion clock cycles occur every second. Therefore, one clock cycle takes 1/1,000,000,000 seconds – or 1 nanosecond. What is the duration of single clock cycle, stated in nanoseconds, for each of the following processor speeds:
    a) 2.27 GHz b) 4.65 GHz c) 3.39 GHz

11. [4] Construct a truth table to solve the following Boolean expression: (AC + ~B) ⊕ (A · B + ~C)

12. [3] For each of the six numbers provided in Set#1, specify whether the parity bit will be set.

13. [3] Convert each of the three hexa-decimal segment-offset addresses in Set#2 to a 20-bit linear address stated as a HEX value.

14. [8] In real-address mode, list four different segment-offset address combinations for each of the two linear addresses provided in Set#3. For your answers, none of the offset values can contain a zero.

15. [2 x 5] For each of the three real numbers provided in Set #4, answer the questions which follow:
    a) [0.5] What is the sign bit?
    b) [0.5] What is the binary value of the whole number part of the number?
    c) [1.0] What is the binary value of the fractional part of the number?
    d) [1.0] What is the normalized representation of the number in binary (don't forget the sign)?
    e) [1.0] What is the biased exponent value as a binary number?
    f) [1.0] the Single Precision IEEE Binary Format Real number representation for each.

Example: Using -10.875 as the real number, we find the IEEE Single Precision format as follows:

a) Sign is negative – bit value is 1

b) 10d = 1010b

c) .875 X 2 = 1.75 → 1

.750 X 2 = 1.50 → 1

.500 X 2 = 1.00 → 1

.000 means we are done.

d) All together -10.875D = -1010.111B

Normalized: -1010.111B = -1.010111B x 2^3

e) Biased exponent: 127 + 3 = 130 = 10000010B

f) Answer: 1 10000010 0101 1100 0000 0000 0000 000

16. [2 x 5] Each of the numbers in Set #5 represent a real number stored in IEEE Single precision format. Convert each to their base 10 value.

    a) [0.5] What is the sign?

    b) [0.5] What is the biased exponent value?

    c) [0.5] What is the unbiased exponent value?

    d) [1.0] What is the normalized representation of the number in binary?

    e) [0.5] What is the unnormalized representation of the number in binary?

    f) [0.5] What is the decimal value of the whole number part of the number?

    g) [1.0] What is the decimal value of the fractional part of the number?

    h) [0.5] What is the real number in base 10 (don't forget the sign)?

17. [5] The IEEE-Double Precision format is similar to the IEEE-Single Precision format except that the biased exponent is 11 bits instead of 8, the bias value is 1023 instead of 127, and the fractional component is 53 bits instead of 23. Using this information, store the number in Set #6 into IEEE-Double Precision format.

    Just like in question #15, answer the questions which follow:

    a) [0.5] What is the sign bit?

    b) [0.5] What is the binary value of the whole number part of the number?

    c) [1.0] What is the binary value of the fractional part of the number?

    d) [1.0] What is the normalized representation of the number in binary (don't forget the sign)?

    e) [1.0] What is the biased exponent value as an 11-bit binary number?

    f) [1.0] the Double Precision IEEE Binary Format Real number representation.

Submit your completed assignment as a Word (or compatible) document electronically via the CMS. An upload link has been provided.