Python FPGA Development
(Where have you been!)

Python EcoSystem!!

Abstract

The goal of the MyHDL project is to empower hardware designers with the elegance and simplicity of the Python language.

MyHDL is a free, open-source package for using Python as a hardware description and verification language.

Modeling

Python's power and clarity make MyHDL an ideal solution for high level modeling. Python is famous for enabling elegant solutions to complex modeling problems.

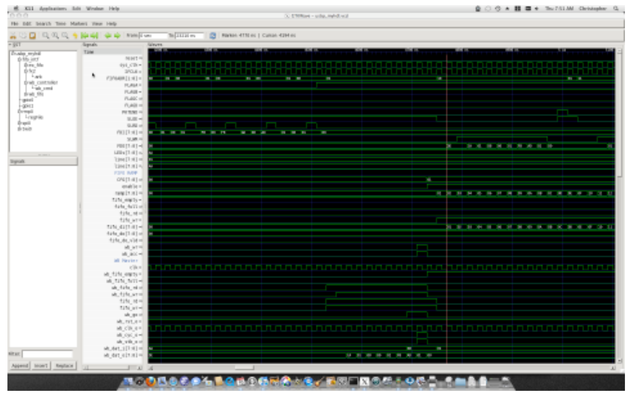
Simulation and Verification

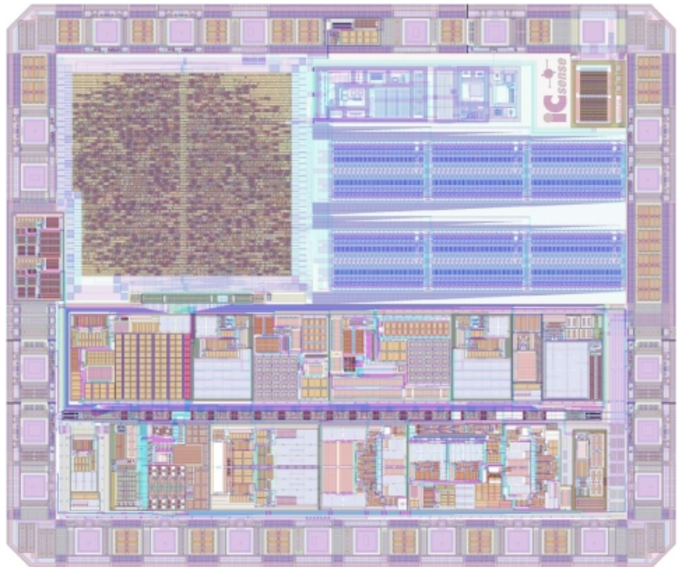
The built-in simulator runs on top of the Python interpreter. It supports waveform viewing by tracing signal changes in a VCD file.

With MyHDL, the Python unit test framework can be used on hardware designs.

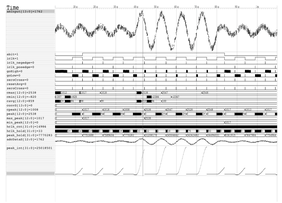
Conversion to Verilog and VHDL

Subject to some limitations, MyHDL designs can be converted to Verilog or VHDL. This provides a path into a traditional design flow.

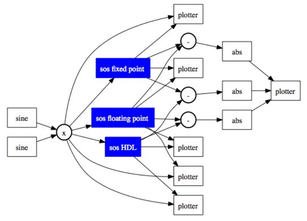


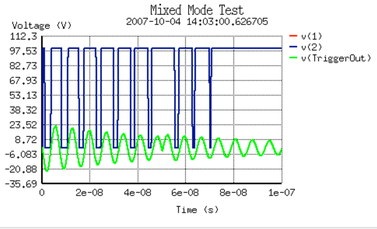


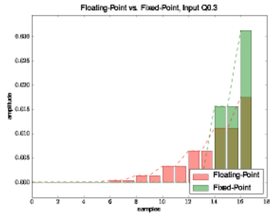
ASIC Proven, MyHDL Digital Macro

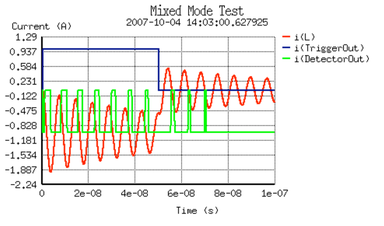


Complex Simulations

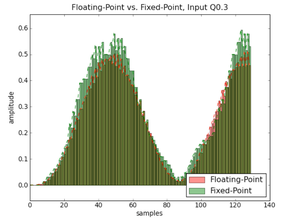








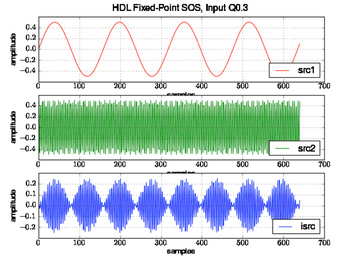
Cosimulation with Spice

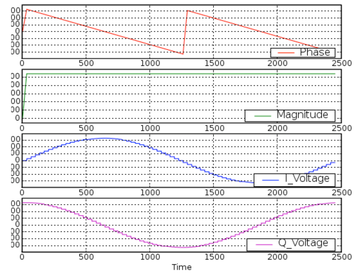


Fixed-Point Analysis

Why?

- New to Digital Hardware Design
- Scripting Languages Intensively Used
- Modern Software Development Techniques for Hardware Design
- Algorithm Development and HDL Design in One Environment
- Require Both Verilg and VHDL
- VHDL Too Verbose
- SystemVerilog Too Complicated
- You have been TCL'd too much
- Google uses Python





Resources

www.myhdl.org

www.jandecaluwe.com/hdldesign/digmac.html