CE 3320.001 Project

Name: Fernando Portillo

Project Title: Mealy State Machine

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1 Problem

Design a mealy state machine (1 input, 1 output) that is turned on when the input "1010" is obtained.

2 Mealy State Machine Designed

2.1 Description

Mealy state machine can take detect the sequence "1010" and turn on. It can also use previous bits to create a new sequence (overlaps). Resets if the reset is ON (0) mostly seen in the code. Using four states to determine the sequence.

2.2 Mealy State Machine Diagram

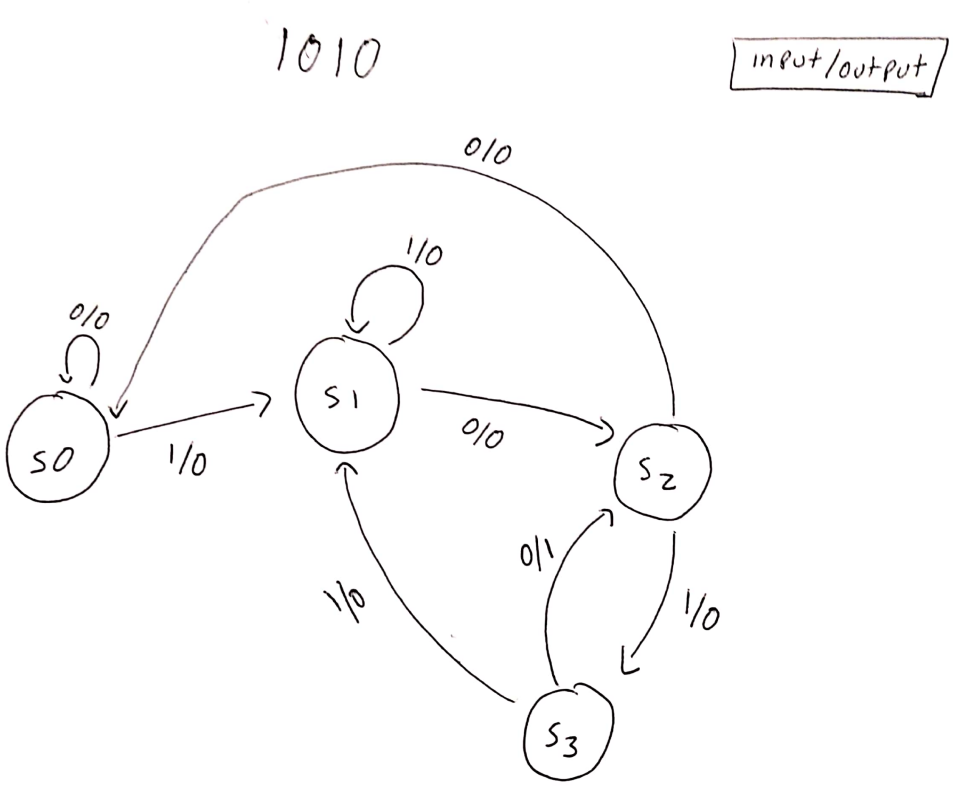

Figure 1: Mealy State Machine Diagram

3 Output

Output in Vivado differs from the output seen in the command line. Unfortunately, I could not get the Vivado Design Suite to work, it shows all the inputs changing but the output does not seem to change. Command line output if the sequence was detected based on the output wire turning on. That is the correct functionality of the design. The command line shows the sequence up the point it was detected or when the program ends.

3.1 Vivado

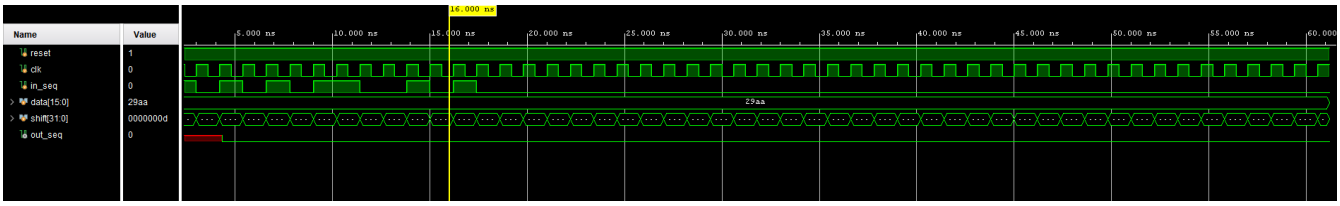

Figure 2: overall look of the vivado simulation output

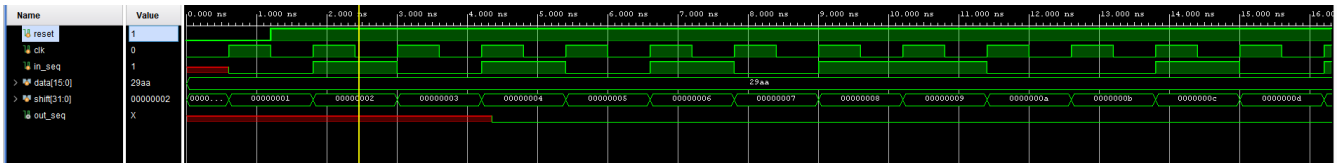

Figure 3: close up look of the vivado simulation output

3.2 Command Line (Icarus Verilog)

```
$ vvp project
01010
Sequence with or without overlap detected

10
Sequence with or without overlap detected

11001010
Sequence with or without overlap detected

00000000000000000000000000000000

testbench.v:25: $finish called at 61200 (1s)
```

Figure 4: icarus verilog command line output using display