Instrução	Versão DP	Classe	Mneumonico	Código binário	Reg2Loc	Uncondbranch	Branch	MemRead	MemtoReg	ALU control lines	MemWrite	ALUSrc	RegWrite	SetFlags	bcond	blink	bregister	bnz	zeroext0	zeroext1	zeroext2	exclusive	numBytes
Add	Core	Aritimética	ADD	10001011000	0	0	0	0	0	0010	0	0	1	0	0	0	0	0	0	0	0	0	00
Add Immediate	Core	Aritimética	ADDI	10010001000 10010001001	X	0	0	0	0	0010	0	1	1	0	0	0	0	0	0	0	0	0	00
Add Immediate & Set flags	Core	Aritimética	ADDIS	10110001000 10110001001	X	0	0	0	0	0010	0	1	1	1	0	0	0	0	0	0	0	0	00
Add & Set Flags	Core	Aritimética	ADDS	10101011000	0	0	0	0	0	0010	0	0	1	1	0	0	0	0	0	0	0	0	00
AND	Core	Aritimética	AND	10001010000	0	0	0	0	0	0000	0	0	1	0	0	0	0	0	0	0	0	0	00
AND Immediate	Core	Aritimética	ANDI	10010010000 10010010001	X	0	0	0	0	0000	0	1	1	0	0	0	0	0	0	0	0	0	00
AND Immediate & Set Flags	Core	Aritimética	ANDIS	11110010000 11110010001	0	0	0	0	0	0000	0	1	1	1	0	0	0	0	0	0	0	0	00
AND & Set Flags	Core	Aritimética	ANDS	11101010000	0	0	0	0	0	0000	0	0	1	1	0	0	0	0	0	0	0	0	00
Branch	Core	Branch	B	000101XXXXX	X	1	X	0	0	XXXX	0	0	0	0	0	0	0	0	0	0	0	0	00
Branch Conditionally	Extension	Branch	B.cond	01010100XXX	X	0	1	0	0	XXXX	0	0	0	0	0	0	0	0	0	0	0	0	00
Branch with Link	Extension	Branch	BL	100101XXXXX	x	1	x	0	0	0000	0	0	1	0	0	1	0	0	0	0	0	0	00
Branch to Register	Extension	Branch	BR	11010110000	x	1	x	0	0	0000	0	0	0	0	0	0	1	0	0	0	0	0	00
Compare & Branch if not zero	Core	Branch	CBNZ	10110101XXX	0	0	1	0	0	0110	0	0	0	0	0	0	0	1	0	0	0	0	00
Compare & Branch if zero	Core	Branch	CBZ	10110100XXX	0	0	1	0	0	0110	0	0	0	0	0	0	0	0	0	0	0	0	00
eXclusive OR	Extension	Aritimética	EOR	11001010000	0	0	0	0	0	1101	0	0	1	0	0	0	0	0	0	0	0	0	00
Exclusive OR Immediate	Extension	Aritimética	EORI	1101001000X	X	0	0	0	0	1101	0	1	1	0	0	0	0	0	0	0	0	0	00
Load Register Unscaled offset	Core	Load	LDUR	11111000010	X	0	0	1	1	0010	0	1	1	0	0	0	0	0	0	0	0	0	00
LoaD Byte Unscaled offset	Extension	Load	LDURB	00111000010	X	0	0	1	1	0010	0	1	1	0	0	0	0	0	1	1	1	0	00
Load HalfUnscaled offset	Extension	Load	LDURH	01111000010	X	0	0	1	1	0010	0	1	1	0	0	0	0	0	0	1	1	0	00
Load Signed Word Unscaled offset	Extension	Load	LDURSW	10111000100	X	0	0	1	1	0010	0	1	1	0	0	0	0	0	0	0	1	0	00
Load eXclusive Register	Extension	Load	LDXR	11001000010	X	0	0	1	1	0010	0	1	1	0	0	0	0	0	0	0	0	1	00
Logical Shift Left	Extension	Aritimética	LSL	11010011011	X	0	0	0	0	1111	0	X	1	0	0	0	0	0	0	0	0	0	00
Logical Shift Right	Extension	Aritimética	LSR	11010011010	X	0	0	0	0	1110	0	X	1	0	0	0	0	0	0	0	0	0	00
MOVe wide with Keep	Extension	Aritimética	MOVK	111100101XX	X	0	0	0	0	0110	0	1	1	0	0	0	0	0	0	0	0	0	00
MOVe wide with Zero	Extension	Aritimética	MOVZ	110100101XX	X	0	0	0	0	0110	0	1	1	0	0	0	0	0	0	0	0	0	00
Inclusive OR	Extension	Aritimética	ORR	10101010000	0	0	0	0	0	0011	0	0	1	0	0	0	0	0	0	0	0	0	00
Inclusive OR immediate	Extension	Aritimética	ORRI	1011001000X	X	0	0	0	0	0011	0	1	1	0	0	0	0	0	0	0	0	0	00
STore Register Unscaled offset	Core	Store	STUR	11111000000	1	0	0	0	0	0010	1	1	0	0	0	0	0	0	0	0	0	0	00
STore Byte Unscaled offset	Extension	Store	STURB	00111000000	1	0	0	0	0	0010	1	1	0	0	0	0	0	0	0	0	0	0	11
STore Word Unscaled offset	Extension	Store	STURW	10111000000	1	0	0	0	0	0010	1	1	0	0	0	0	0	0	0	0	0	0	01
STore HalfUnscaled offset	Extension	Store	STURH	01111000000	1	0	0	0	0	0010	1	1	0	0	0	0	0	0	0	0	0	0	10
STore eXclusive Register	Extension	Store	STXR	1100100000	1	0	0	0	0	0010	1	1	0	0	0	0	0	0	0	0	0	0	00
SUBtract	Core	Aritimética	SUB	11001011000	0	0	0	0	0	0110	0	0	1	0	0	0	0	0	0	0	0	0	00
SUBtract Immediate	Core	Aritimética	SUBI	1101000100X	X	0	0	0	0	0110	0	1	1	0	0	0	0	0	0	0	0	0	00
SUBtract Immediate & Set Flags	Core	Aritimética	SUBIS	1111000100X	X	0	0	0	0	0110	0	1	1	1	0	0	0	0	0	0	0	0	00
SUBtract & set flags	Core	Aritimética	SUBS	11101011000	0	0	0	0	0	0110	0	0	1	1	0	0	0	0	0	0	0	0	00