

DRV8301 Three-Phase Gate Driver With Dual Current Shunt Amplifiers and Buck Regulator

1 Features

- 6-V to 60-V Operating Supply Voltage Range
- 1.7-A Source and 2.3-A Sink Gate Drive Current Capability
- Slew Rate Control for EMI Reduction
- Bootstrap Gate Driver With 100% Duty Cycle Support
- 6- or 3-PWM Input Modes
- Dual Integrated Current Shunt Amplifiers With Adjustable Gain and Offset
- Integrated 1.5-A Buck Converter
- 3.3-V and 5-V Interface Support
- SPI
- Protection Features:
 - Programmable Dead Time Control (DTC)
 - Programmable Overcurrent Protection (OCP)
 - PVDD and GVDD Undervoltage Lockout (UVLO)
 - GVDD Overvoltage Lockout (OVLO)
 - Overtemperature Warning/Shutdown (OTW/OTS)
 - Reported Through nFAULT, nOCTW, and SPI Registers

2 Applications

- 3-Phase BLDC and PMSM Motors
- CPAPs and Pumps
- E-bikes
- Power Tools
- Robotics and RC Toys
- Industrial Automation

3 Description

The DRV8301 is a gate driver IC for three-phase motor drive applications. The device provides three half-bridge drivers, each capable of driving two N-channel MOSFETs. The DRV8301 supports up to 1.7-A source and 2.3-A peak current capability. The DRV8301 can operate off of a single power supply with a wide range from 6-V to 60-V. The device uses a bootstrap gate driver architecture with trickle charge circuitry to support 100% duty cycle. The DRV8301 uses automatic handshaking when the high-side or low-side MOSFET is switching to prevent flow of current. Integrated VDS sensing of the high-side and low-side MOSFETs is used to protect the external power stage against overcurrent conditions.

The DRV8301 includes two current shunt amplifiers for accurate current measurement. The amplifiers support bidirectional current sensing and provide an adjustable output offset up to 3 V.

The DRV8301 also includes an integrated switching mode buck converter with adjustable output and switching frequency. The buck converter can provide up to 1.5 A to support MCU or additional system power needs.

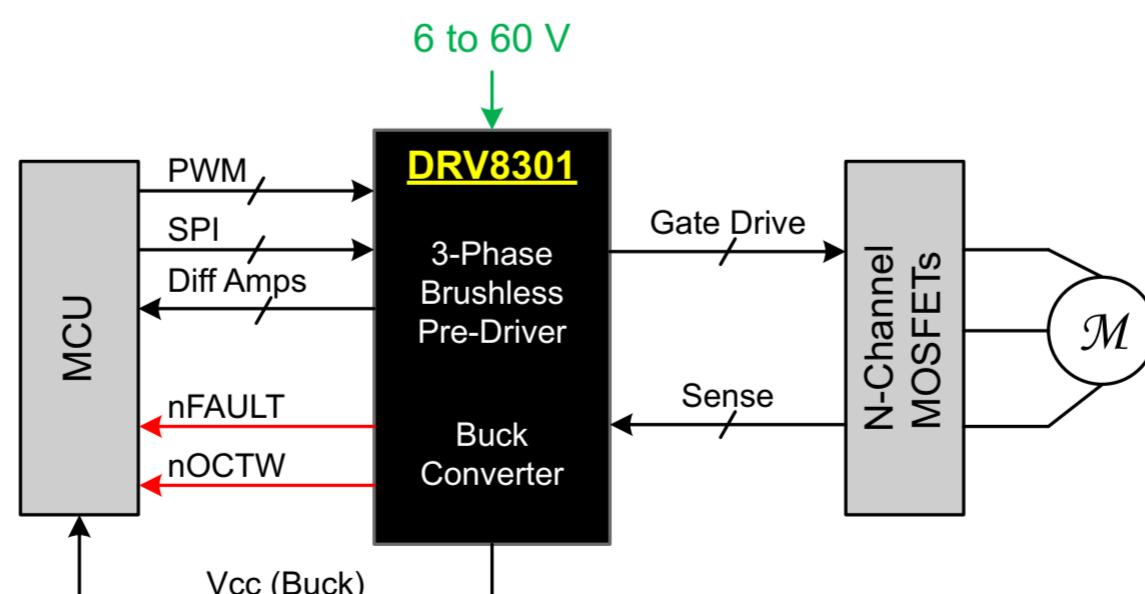
The SPI provides detailed fault reporting and flexible parameter settings such as gain options for the current shunt amplifiers and slew rate control of the gate drivers.

Device Information⁽¹⁾

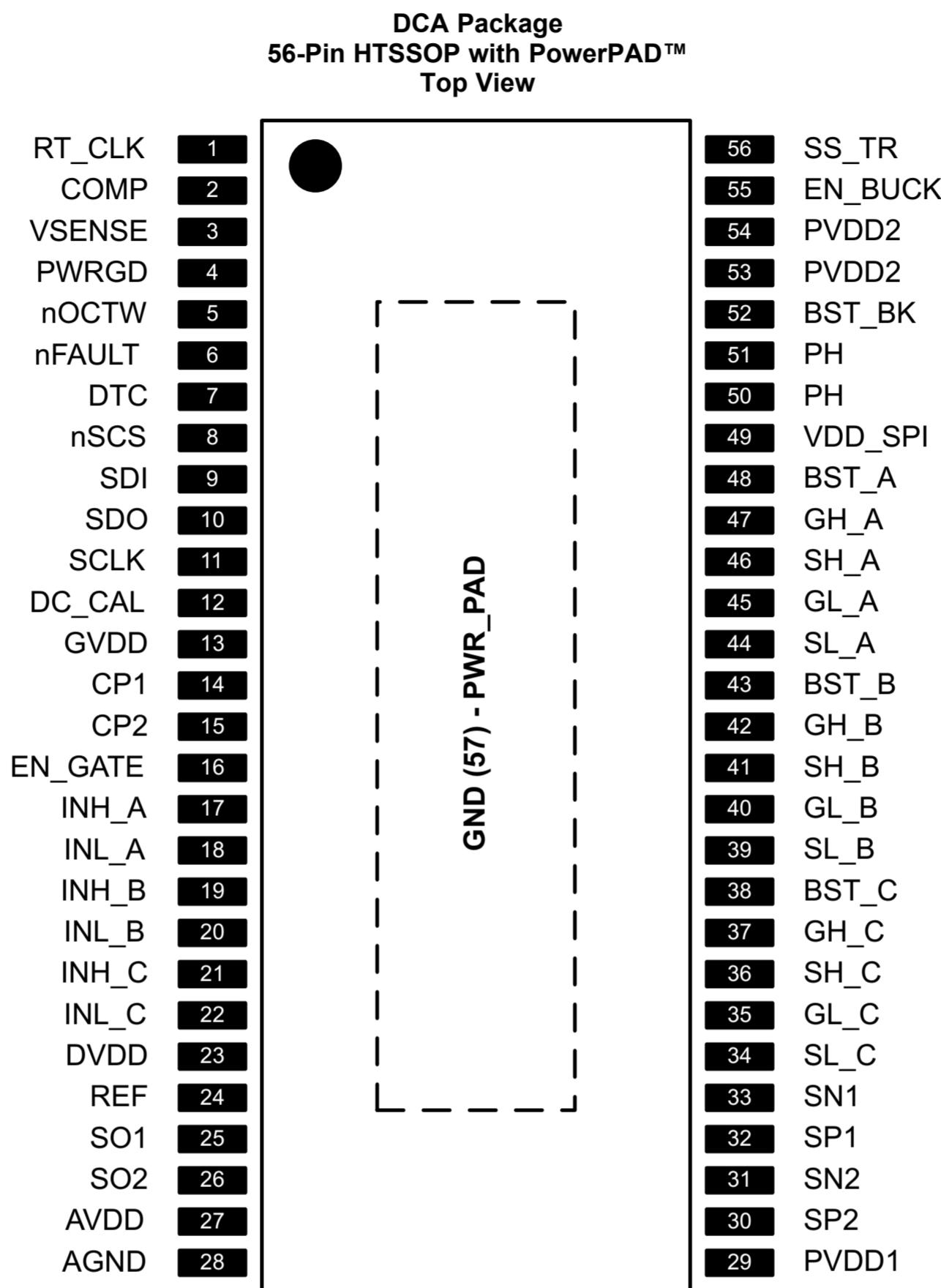
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8301	HTSSOP (56)	14.00 mm × 8.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
RT_CLK	1	I	Resistor timing and external clock for buck regulator. Resistor should connect to GND (PowerPAD™) with very short trace to reduce the potential clock jitter due to noise.
COMP	2	O	Buck error amplifier output and input to the output switch current comparator.
VSENSE	3	I	Buck output voltage sense pin. Inverting node of error amplifier.
PWRGD	4	O	An open-drain output with external pullup resistor required. Asserts low if buck output voltage is low due to thermal shutdown, dropout, overvoltage, or EN_BUCK shut down
nOCTW	5	O	Overcurrent and/or overtemperature warning indicator. This output is open drain with external pullup resistor required. Programmable output mode via SPI registers.
nFAULT	6	O	Fault report indicator. This output is open drain with external pullup resistor required.
DTC	7	I	Dead-time adjustment with external resistor to GND
nSCS	8	I	SPI chip select
SDI	9	I	SPI input
SDO	10	O	SPI output

(1) KEY: I = Input, O = Output, P = Power

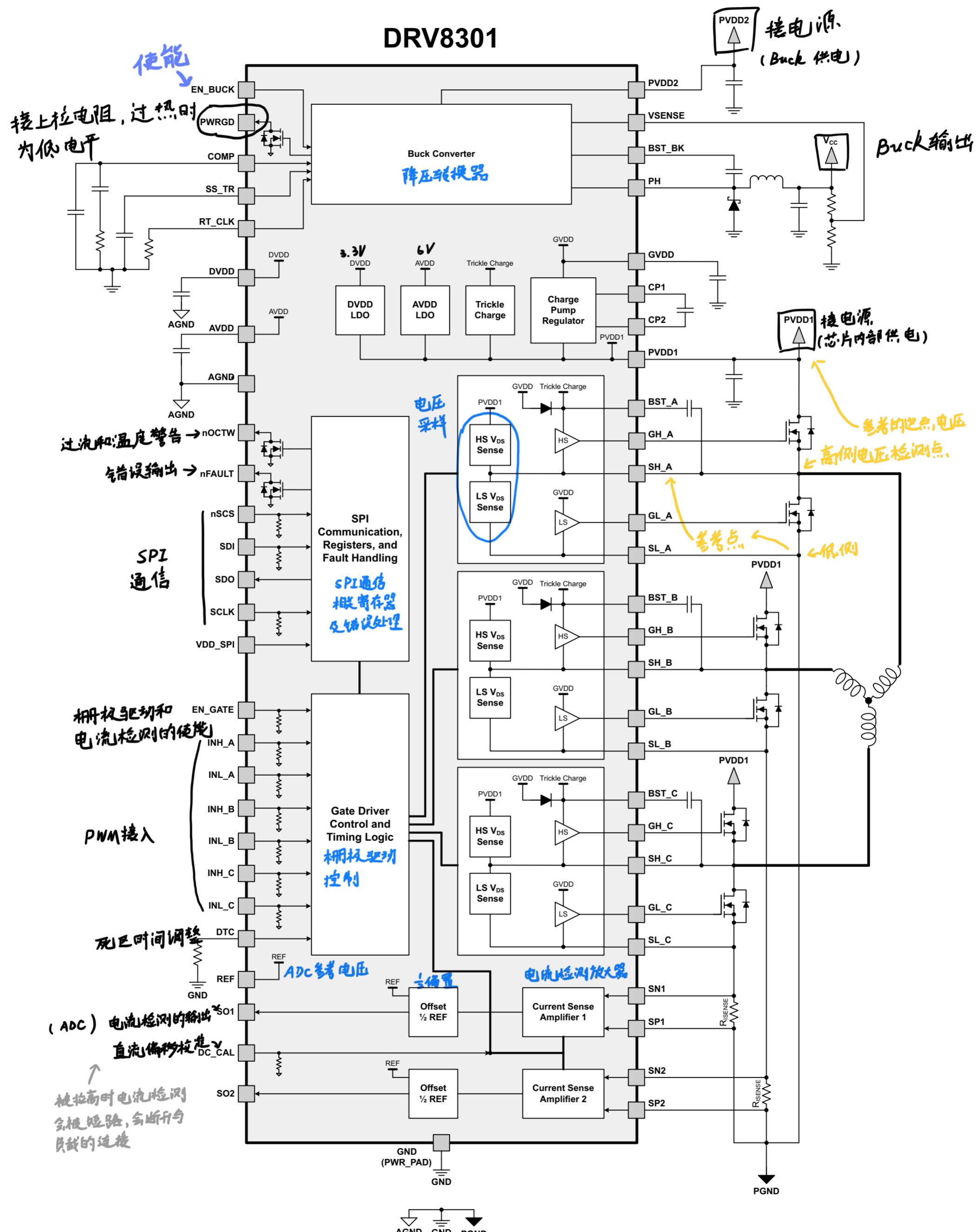
Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
SCLK	11	I	SPI clock signal
DC_CAL	12	I	When DC_CAL is high, device shorts inputs of shunt amplifiers and disconnects loads. DC offset calibration can be done through external microcontroller.
GVDD	13	P	Internal gate driver voltage regulator. GVDD cap should connect to GND
CP1	14	P	Charge pump pin 1, ceramic capacitor should be used between CP1 and CP2
CP2	15	P	Charge pump pin 2, ceramic capacitor should be used between CP1 and CP2
EN_GATE	16	I	Enable gate driver and current shunt amplifiers. Control buck through EN_BUCK pin.
INH_A	17	I	PWM input signal (high side), half-bridge A
INL_A	18	I	PWM input signal (low side), half-bridge A
INH_B	19	I	PWM input signal (high side), half-bridge B
INL_B	20	I	PWM input signal (low side), half-bridge B
INH_C	21	I	PWM input signal (high side), half-bridge C
INL_C	22	I	PWM input signal (low side), half-bridge C
DVDD	23	P	Internal 3.3-V supply voltage. DVDD cap should connect to AGND. This is an output, but not specified to drive external circuitry.
REF	24	I	Reference voltage to set output of shunt amplifiers with a bias voltage which equals to half of the voltage set on this pin. Connect to ADC reference in microcontroller.
SO1	25	O	Output of current amplifier 1
SO2	26	O	Output of current amplifier 2
AVDD	27	P	Internal 6-V supply voltage, AVDD cap should always be installed and connected to AGND. This is an output, but not specified to drive external circuitry.
AGND	28	P	Analog ground pin. Connect directly to GND (PowerPAD).
PVDD1	29	P	Power supply pin for gate driver, current shunt amplifier, and SPI communication. PVDD1 is independent of buck power supply, PVDD2. PVDD1 cap should connect to GND
SP2	30	I	Input of current amplifier 2 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best common mode rejection.
SN2	31	I	Input of current amplifier 2 (connecting to negative input of amplifier).
SP1	32	I	Input of current amplifier 1 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best common mode rejection.
SN1	33	I	Input of current amplifier 1 (connecting to negative input of amplifier).
SL_C	34	I	Low-Side MOSFET source connection, half-bridge C. Low-side V _{DS} measured between this pin and SH_C.
GL_C	35	O	Gate drive output for low-side MOSFET, half-bridge C
SH_C	36	I	High-side MOSFET source connection, half-bridge C. High-side V _{DS} measured between this pin and PVDD1.
GH_C	37	O	Gate drive output for high-side MOSFET, half-bridge C
BST_C	38	P	Bootstrap cap pin for half-bridge C
SL_B	39	I	Low-side MOSFET source connection, half-bridge B. Low-side V _{DS} measured between this pin and SH_B.
GL_B	40	O	Gate drive output for low-side MOSFET, half-bridge B
SH_B	41	I	High-side MOSFET source connection, half-bridge B. High-side V _{DS} measured between this pin and PVDD1.
GH_B	42	O	Gate drive output for high-side MOSFET, half-bridge B
BST_B	43	P	Bootstrap cap pin for half-bridge B
SL_A	44	I	Low-side MOSFET source connection, half-bridge A. Low-side V _{DS} measured between this pin and SH_A.
GL_A	45	O	Gate drive output for low-side MOSFET, half-bridge A
SH_A	46	I	High-side MOSFET source connection, half-bridge A. High-side V _{DS} measured between this pin and PVDD1.
GH_A	47	O	Gate drive output for high-side MOSFET, half-bridge A

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BST_A	48	P	Bootstrap cap pin for half-bridge A
VDD_SPI	49	I	SPI supply pin to support 3.3-V or 5-V logic. Connect to the same supply that the MCU uses for SPI operation.
PH	50, 51	O	The source of the internal high side MOSFET of buck converter
BST_BK	52	P	Bootstrap cap pin for buck converter
PVDD2	53, 54	P	Power supply pin for buck converter, PVDD2 cap should connect to GND.
EN_BUCK	55	I	Enable buck converter. Internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors
SS_TR	56	I	Buck soft-start and tracking. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. Cap should connect to GND
GND (PowerPAD)	57	P	GND pin. The exposed power pad must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Three-Phase Gate Driver

The half-bridge drivers use a bootstrap configuration with a trickle charge pump to support 100% duty cycle operation. Each half-bridge is configured to drive two N-channel MOSFETs, one for the high-side and one for the low-side. The half-bridge drivers can be used in combination to drive a 3-phase motor or separately to drive various other loads.

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The peak gate drive current and internal dead times are adjustable to accommodate a variety of external MOSFETs and applications. The peak gate drive current is set through a register setting and the dead time is adjusted with an external resistor on the DTC pin. Shorting the DTC pin to ground will provide the minimum dead time (50ns). There is an internal hand shake between the high side and low side MOSFETs during switching transitions to prevent current shoot through.

The three-phase gate driver can provide up to 30mA of average gate drive current. This will support switching frequencies up to 200 kHz when the MOSFET $Q_g = 25\text{nC}$.

Each MOSFET gate driver has a VDS sensing circuit for overcurrent protection. The sense circuit measures the voltage from the drain to the source of the external MOSFETs while the MOSFET is enabled. This voltage is compared against the programmed trip point to determine if an overcurrent event has occurred. The high-side sense is between the PVDD1 and SH_X pins. The low-side sense is between the SH_X and SL_X pins. Ensuring a differential, low impedance connection to the external MOSFETs for these lines will help provide accurate VDS sensing.

The DRV8301 allows for both 6-PWM and 3-PWM control through a register setting.

Table 1. 6-PWM Mode

INL_X	INH_X	GL_X	GH_X
0	0	L	L
0	1	L	H
1	0	H	L
1	1	L	L

Table 2. 3-PWM Mode

INL_X	INH_X	GL_X	GH_X
X	0	H	L
X	1	L	H

Table 3. Gate Driver External Components

NAME	PIN 1	PIN 2	RECOMMENDED
R _{nOCTW}	nOCTW	V _{CC} ⁽¹⁾	≥10 kΩ
R _{nFAULT}	nFAULT	V _{CC} ⁽¹⁾	≥10 kΩ
R _{DTC}	DTC	GND (PowerPAD)	0 to 150 kΩ (50 ns to 500 ns)
C _{GVDD}	GVDD	GND (PowerPAD)	2.2 μF (20%) ceramic, ≥ 16 V
C _{CP}	CP1	CP2	0.022 μF (20%) ceramic, rated for PVDD1
C _{DVDD}	DVDD	AGND	1 μF (20%) ceramic, ≥ 6.3 V
C _{AVDD}	AVDD	AGND	1 μF (20%) ceramic, ≥ 10 V
C _{PVDD1}	PVDD1	GND (PowerPAD)	≥4.7 μF (20%) ceramic, rated for PVDD1
C _{BST_X}	BST_X	SH_X	0.1 μF (20%) ceramic, ≥ 16 V

(1) V_{CC} is the logic supply to the MCU

8.2 Typical Application

The following design is a common application of the DRV8301.

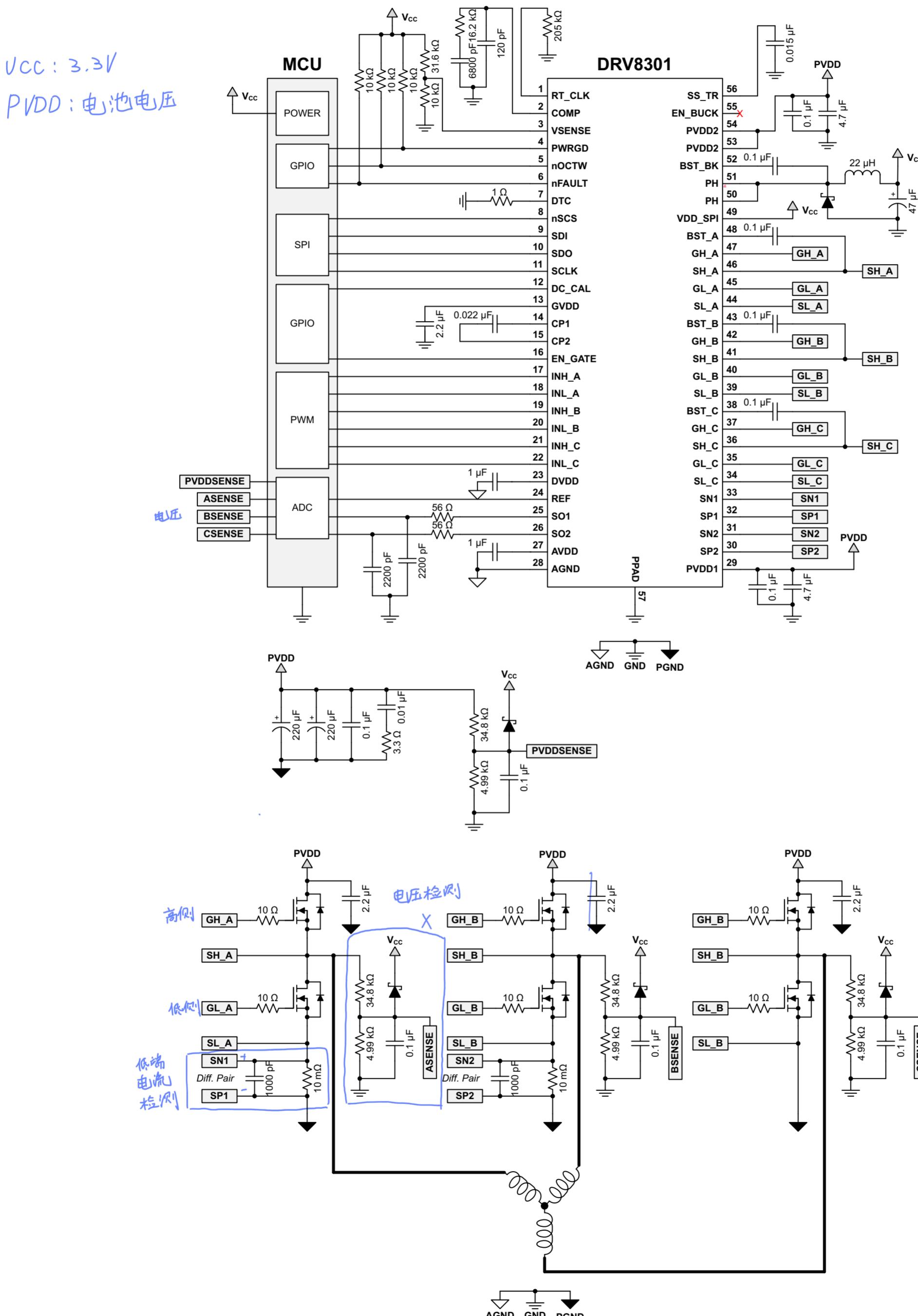


Figure 7. Typical Application Schematic