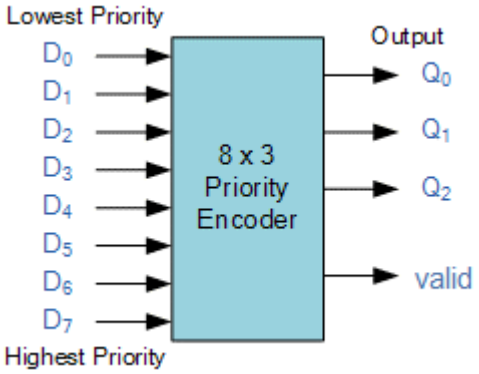
CMSC 132 2nd Semester, 2014-2015
Exercise 3: Combinational Circuit Design in VHDL

1. Create ***your own*** logic circuit design for a ***4:2 Priority Encoder***. Simplify your design by using Boolean Algebra or K-Map. *Write* your names, student numbers, lab section and solution on a sheet of yellow pad paper. Don't forget to include the truth table for the circuit as part of your solution.

2. Create VHDL program (Structural Design) and a test bench code for your solution. Then, simulate your work using GTKWave. Use *std_logic_vector* type for your input and encode output.

3. Create a VHDL program (Behavioral Design) and test bench for a 8:3 Priority Encoder. Simulate your work using GTKWave. Use *std_logic_vector* type for your input and encode output.



4. Don't forget to *document* (*comment*) your codes. Failure to do so will earn you some deductions.

5. This exercise is to be done in *pairs*. If you have any questions or clarifications, feel free to e-mail or consult your lab instructor.

6. Submission details:

   - Deadline for the submission of your written solution will be five *(5)* days after this exercise was given to your lab section.

   - Store your **VHDL codes** inside a ZIP file. Name your ZIP file as "surname1_surname2_labsection_exer3.zip". Example: *bautista_surname2_t-4l_e3.zip*

     Create separate folders for the 8:3 and 4:2 Priority Encoders.

   - Submit your .zip file via *schoology.com*. Note: All members must submit a copy of the exercise on their respective Schoology accounts.

   - You are required to present your VHDL codes.