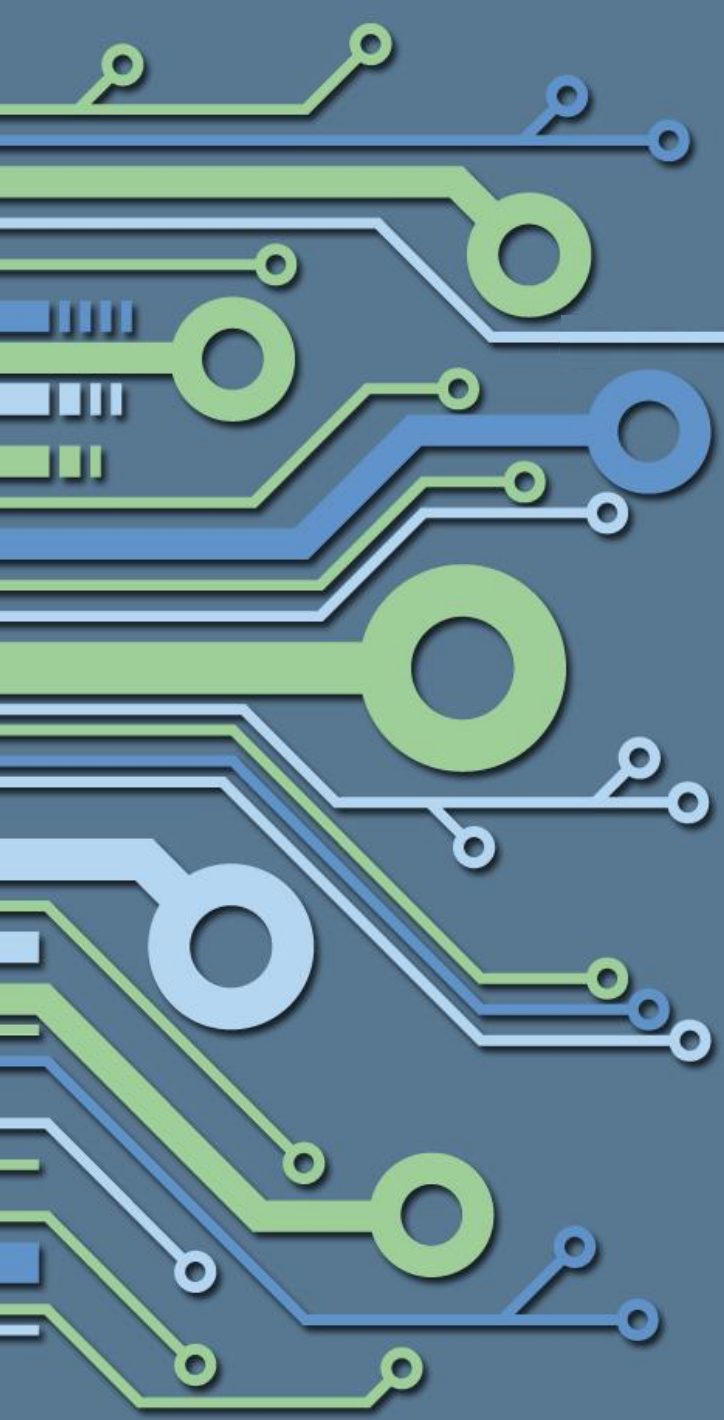


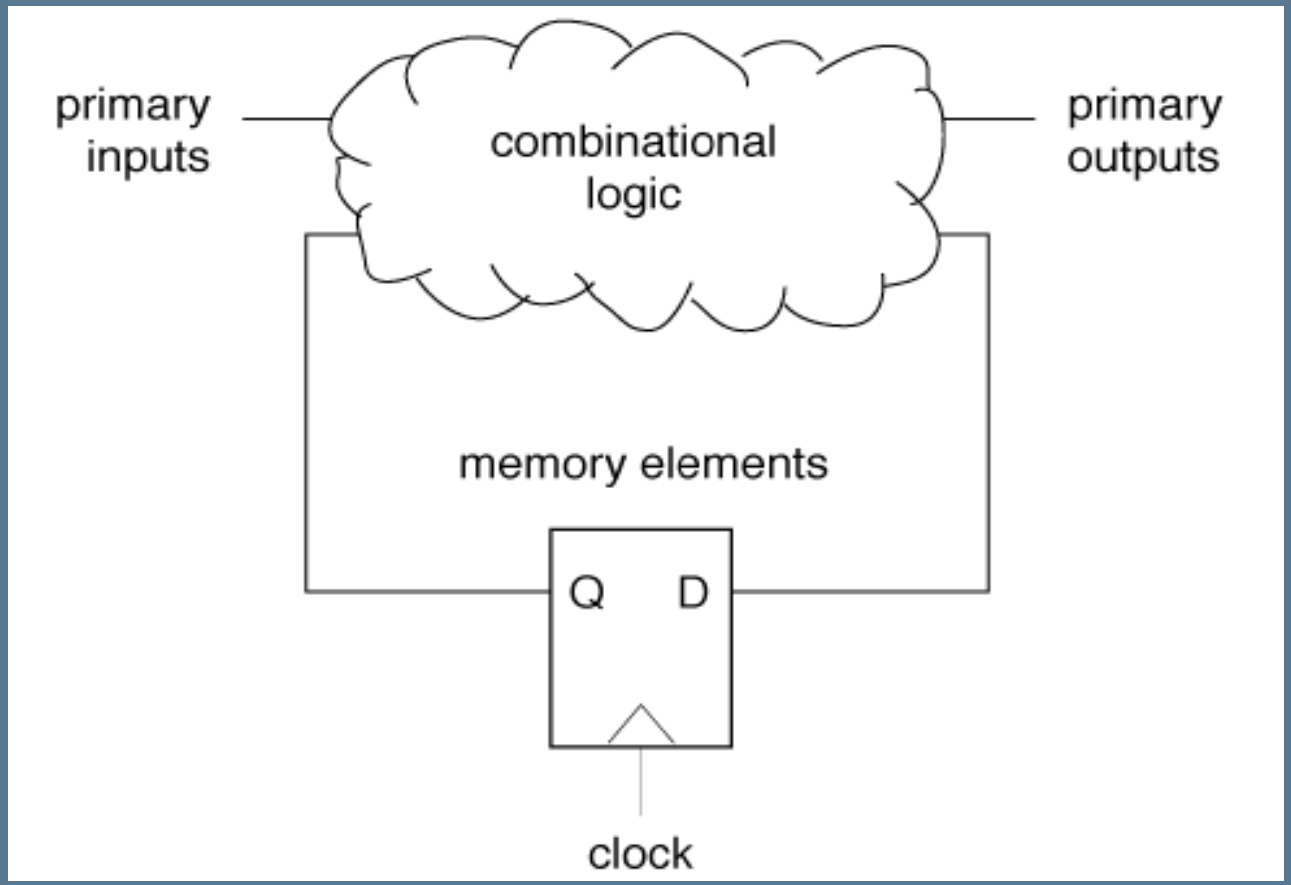
Chapter 8

SEQUENTIAL LOGIC

Sequential Logic

- Current output depends on past inputs as well as current inputs
- Can have different output response when the same input is reapplied to the circuit
- Example sequential circuits are latches, flip-flops, state machines, counters, and registers

Block Diagram of a Sequential Logic



Types of Sequential Circuits

- Synchronous
  - system whose behaviour can be defined from the knowledge of its signals at discrete times
  - use flip-flops (FF)
- Asynchronous
  - system whose behaviour can be defined from the order in which its input signals change
  - uses gates with feedback to form memory elements
  - uses time-delay devices

Latches and Flip-flops

- In the same way that gates are the building blocks of combinational circuits, latches and flip-flops are the building blocks of sequential circuits.
- Both are circuit elements whose output depends not only on the current inputs, but also on previous inputs and outputs.

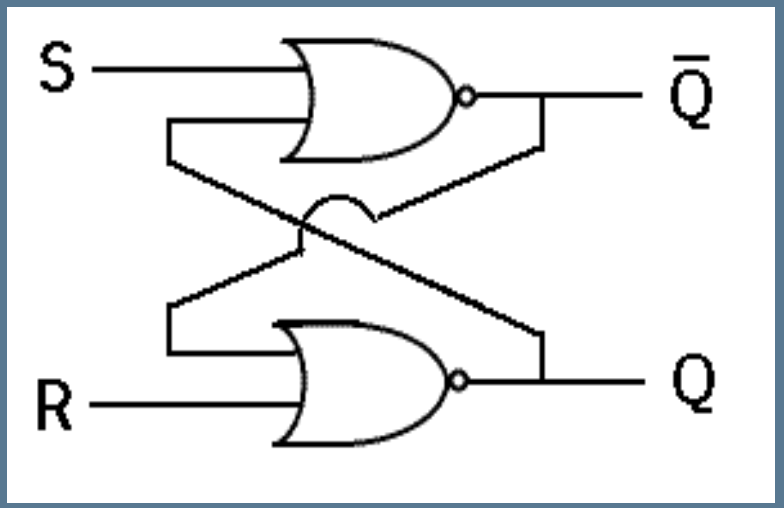
Latch vs. Flip-flop

- Latch (asynchronous)
  - Single-bit storage
  - It changes state at any time due to input change
  - Types
    - SR Latch
    - !S-!R Latch
- Flip-flop (synchronous)
  - Single-bit storage
  - It changes state ONLY when a clock edge or pulse is applied
  - Types
    - SR flip-flop
    - JK flip-flop
    - D flip-flop
    - T flip-flop

SR Latch

- SR Latch is the simplest latch, where S and R stand for SET and RESET.
- It is constructed from a pair of cross-coupled NOR gates.

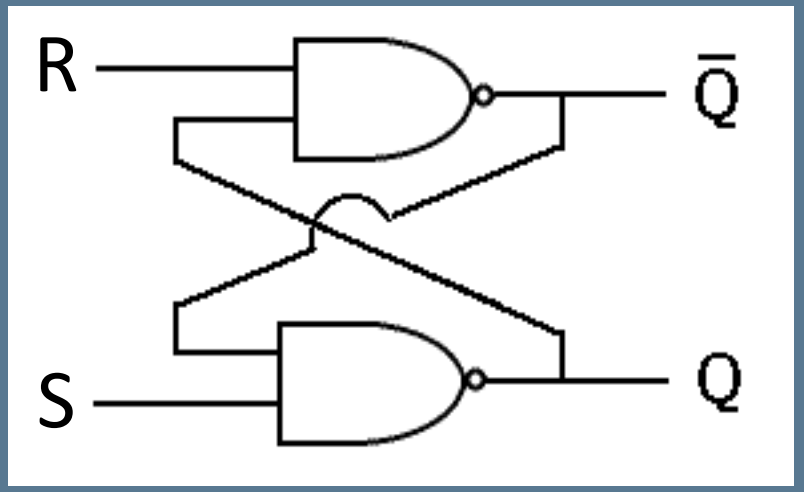
S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0



!S-!R Latch

- A latch that is constructed using two cross-coupled NAND gates

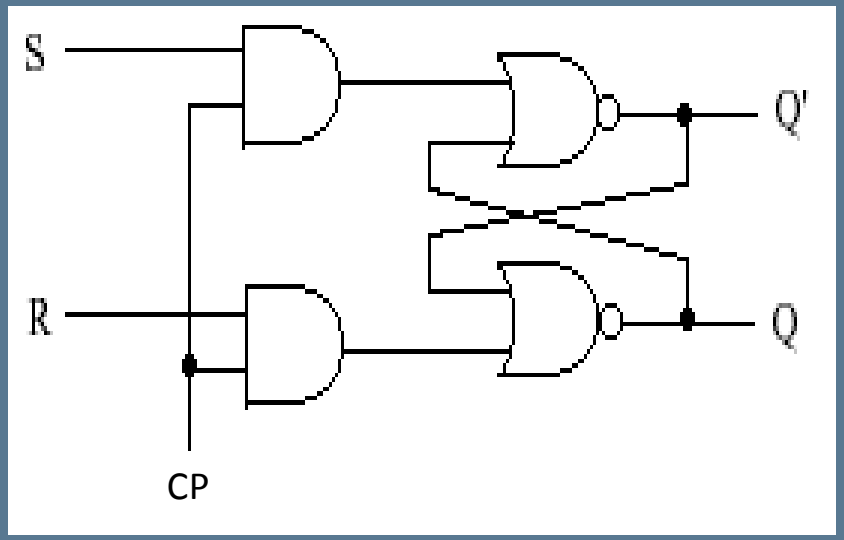
S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1



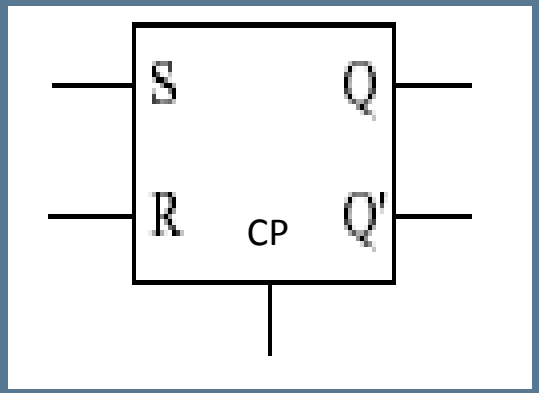
Flip-flops

- Four types:
  - SR Flip-flops
  - JK Flip-flops
  - D-type flip-flops
  - T-type flip-flops

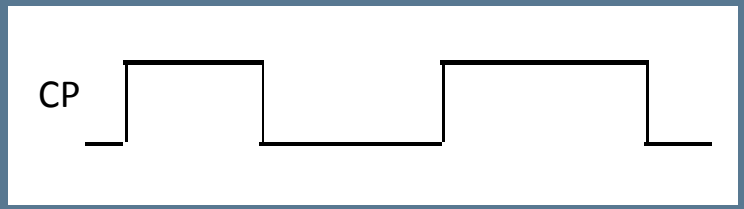
SR Flip-flop



Logic Diagram



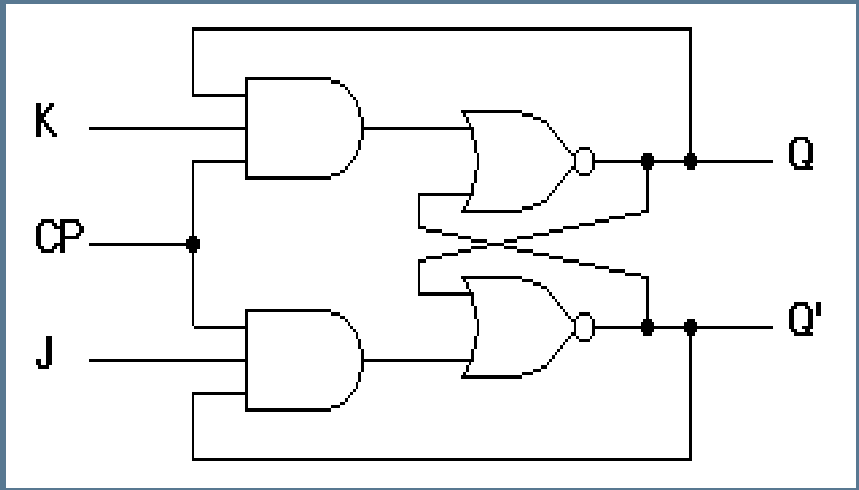
Block Diagram



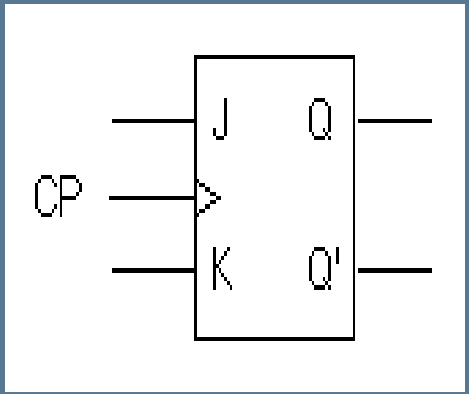
SR Flip-flop Characteristic Table

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

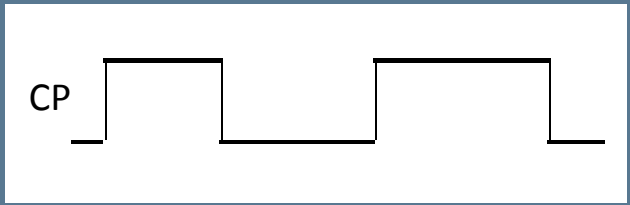
JK Flip-flop



Logic Diagram



Block Diagram



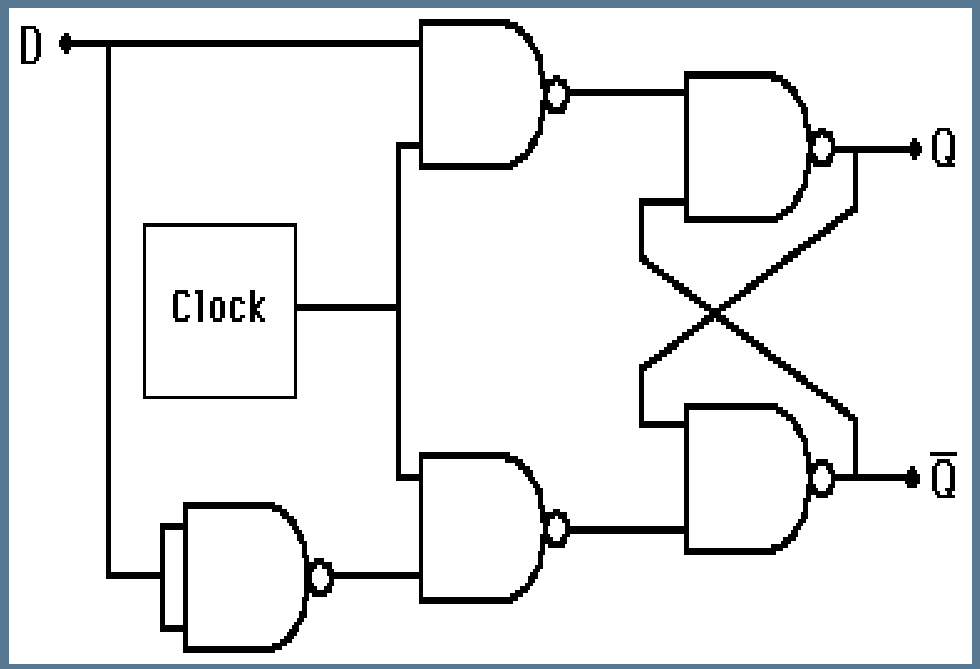
JK Flip-flop Characteristic Table

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

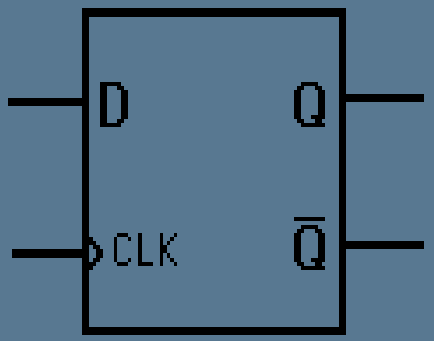
Golden Rule of JK Flip-flops

- If J and K are different, the Q(t+1) is always the same as the value of J.
- If J and K are both equal to zero, nothing happens.
- If J and K are both equal to one, the output toggles.

D-type Flip-flop

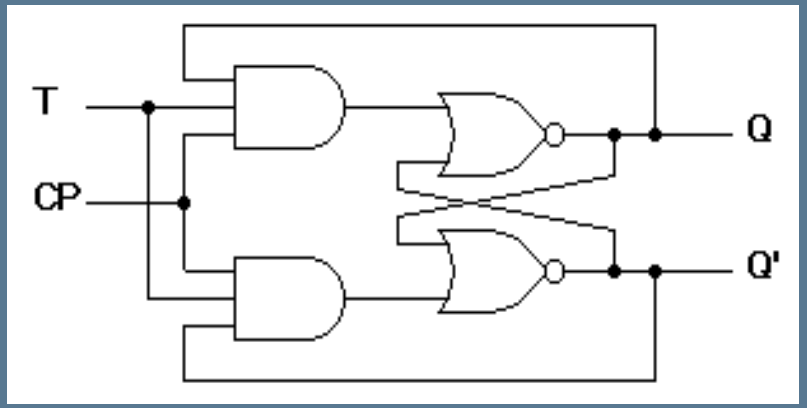


Logic Diagram



Block Diagram

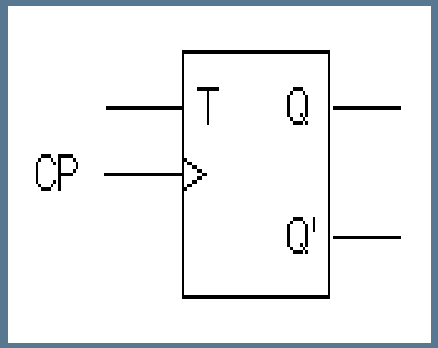
T-type Flip-flop



Logic Diagram

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Table



Block Diagram

Flip-flop Characteristic table

S	R	Q(t+1) NOR	Q(t+1) NAND
0	0		
0	1		
1	0		
1	1		

J	K	Q(t+1)
0	0	
0	1	
1	0	
1	1	

D	Q(t+1)
0	
1	

T	Q(t+1)
0	
1	

Flip-flop Characteristic table

S	R	Q(t+1) NOR	Q(t+1) NAND
0	0	Q(t)	
0	1	0	
1	0	1	
1	1	?	

J	K	Q(t+1)
0	0	
0	1	
1	0	
1	1	

D	Q(t+1)
0	
1	

T	Q(t+1)
0	
1	

Flip-flop Characteristic table

S	R	Q(t+1) NOR	Q(t+1) NAND
0	0	Q(t)	?
0	1	0	1
1	0	1	0
1	1	?	Q(t)

J	K	Q(t+1)
0	0	
0	1	
1	0	
1	1	

D	Q(t+1)
0	
1	

T	Q(t+1)
0	
1	

Flip-flop Characteristic table

S	R	Q(t+1) NOR	Q(t+1) NAND
0	0	Q(t)	?
0	1	0	1
1	0	1	0
1	1	?	Q(t)

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q‘(t)

D	Q(t+1)
0	
1	

T	Q(t+1)
0	
1	

Flip-flop Characteristic table

S	R	Q(t+1) NOR	Q(t+1) NAND
0	0	Q(t)	?
0	1	0	1
1	0	1	0
1	1	?	Q(t)

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q‘(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	
1	

Flip-flop Characteristic table

S	R	Q(t+1) NOR	Q(t+1) NAND
0	0	Q(t)	?
0	1	0	1
1	0	1	0
1	1	?	Q(t)

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q‘(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q’(t)

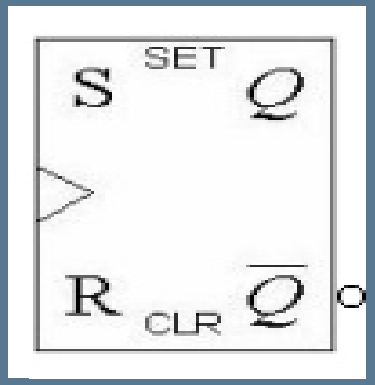
Triggering of Flip-flops

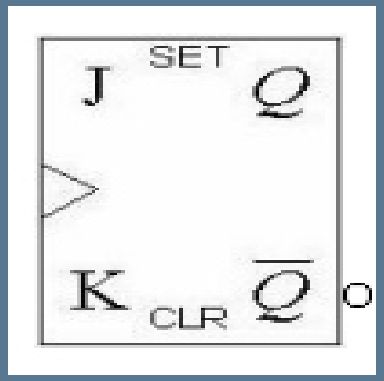
- Trigger
  - Momentary change in the input signal
  - Clocked flip-flops are triggered by pulses
  - Edge-triggered flip-flops
  - Pulse-triggered flip-flops

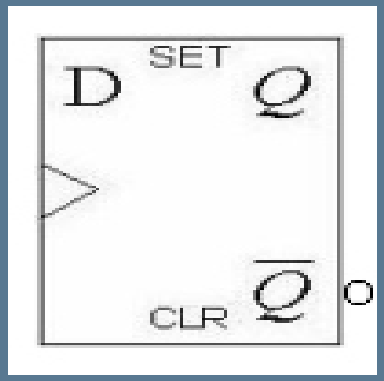
Edge-Triggered Flip-flops

- Positive edge-triggered
  - Leading edge or rising edge triggering
  - Indicated by a triangle placed inside the clock terminal
- Negative edge-triggered
  - Trailing edge triggered
  - Indicated by a bubble outside the clock terminal

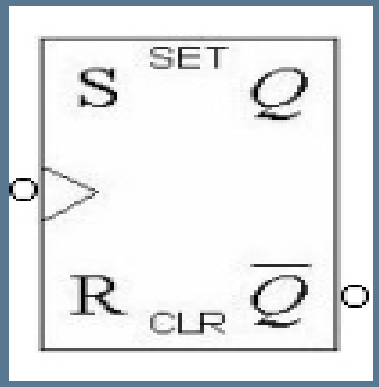
Edge-Triggered Flip-flops

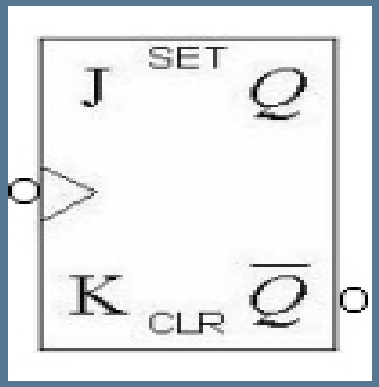


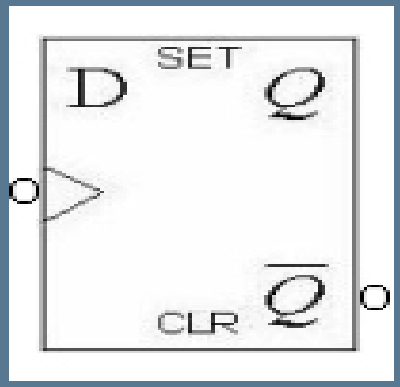




Positive Edge-triggered FF

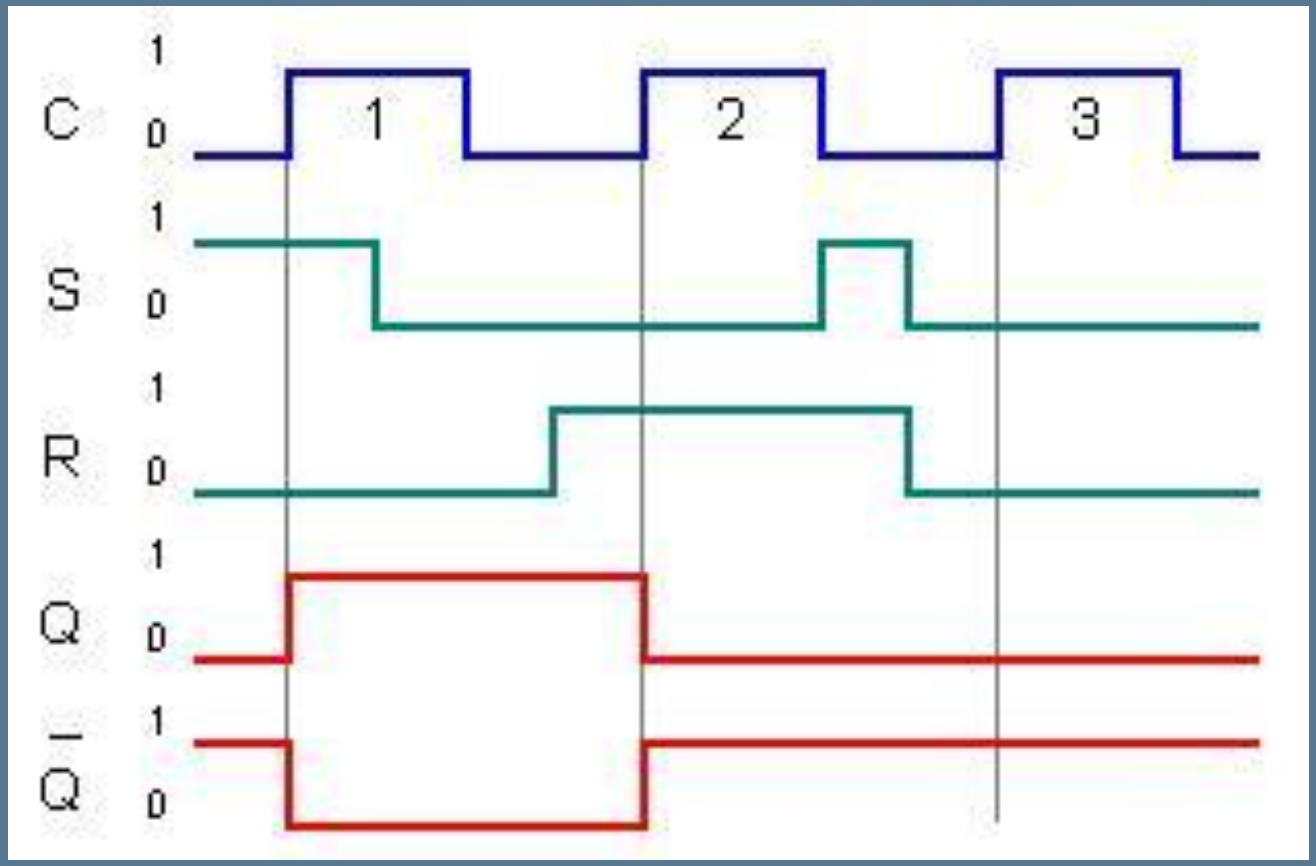




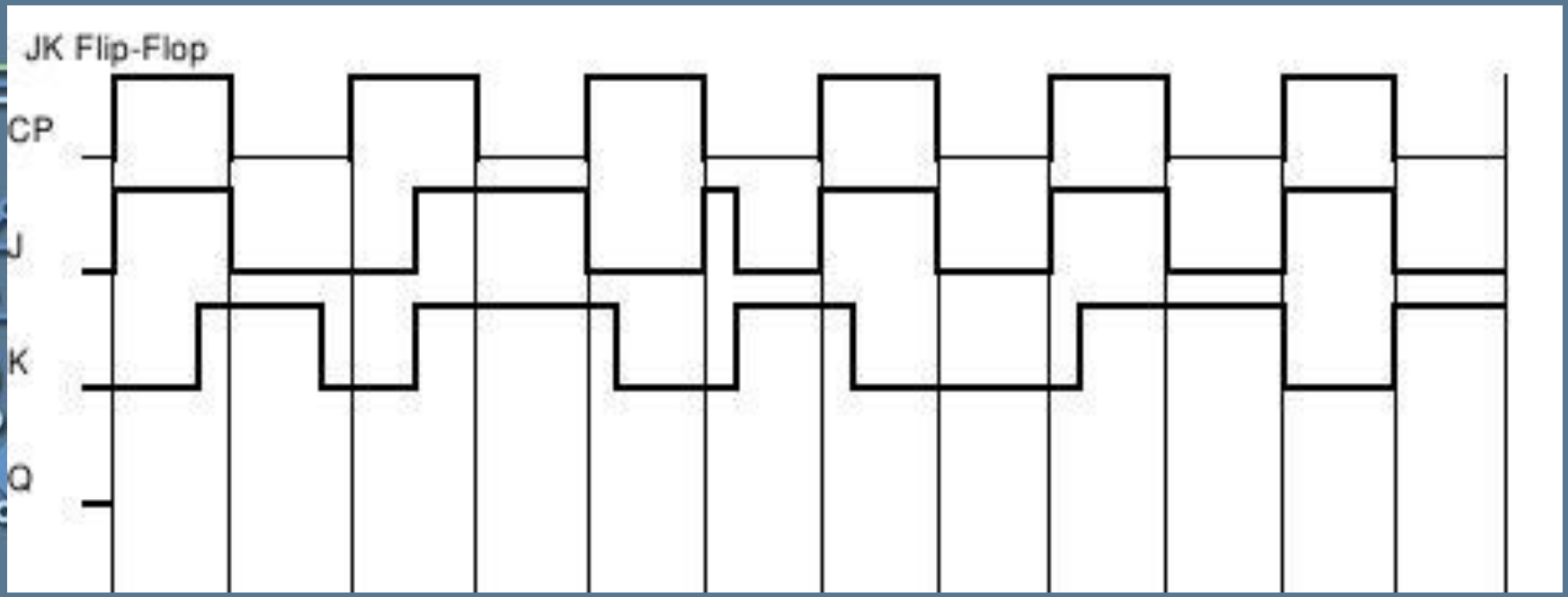


Negative Edge-triggered FF

Example: Edge-Triggered SR FF

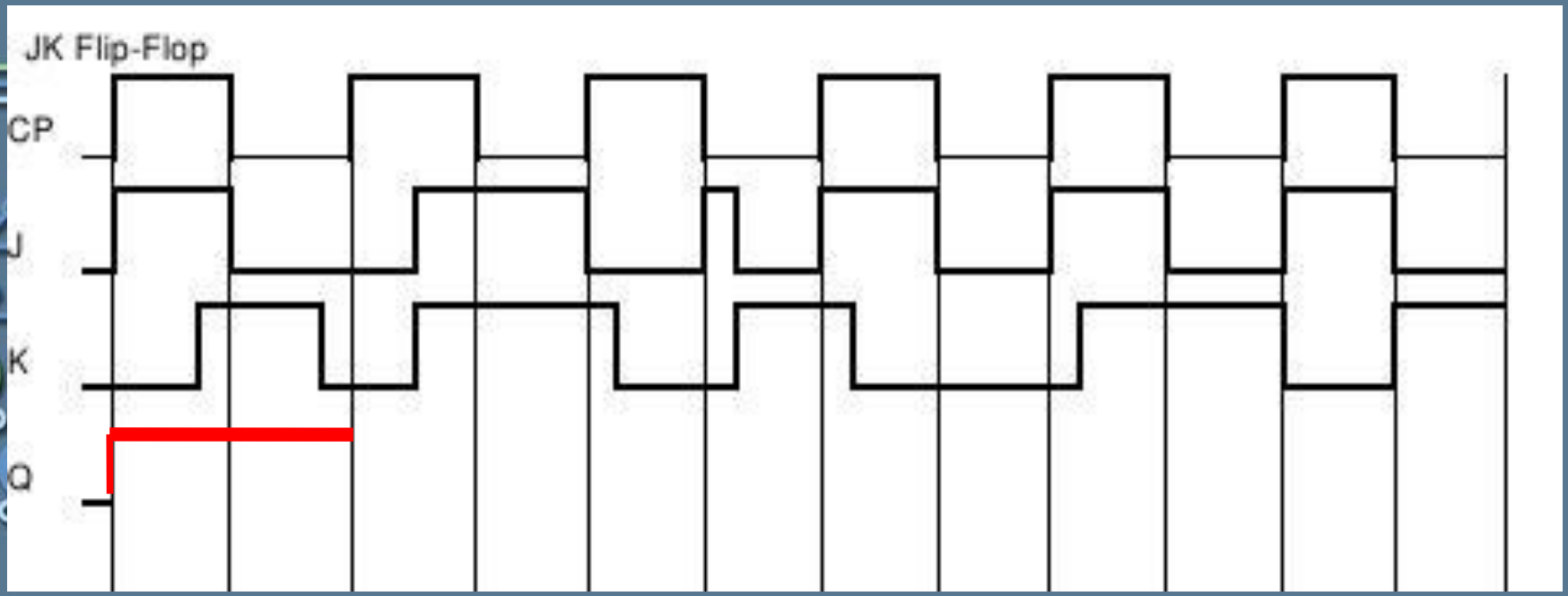


Examples



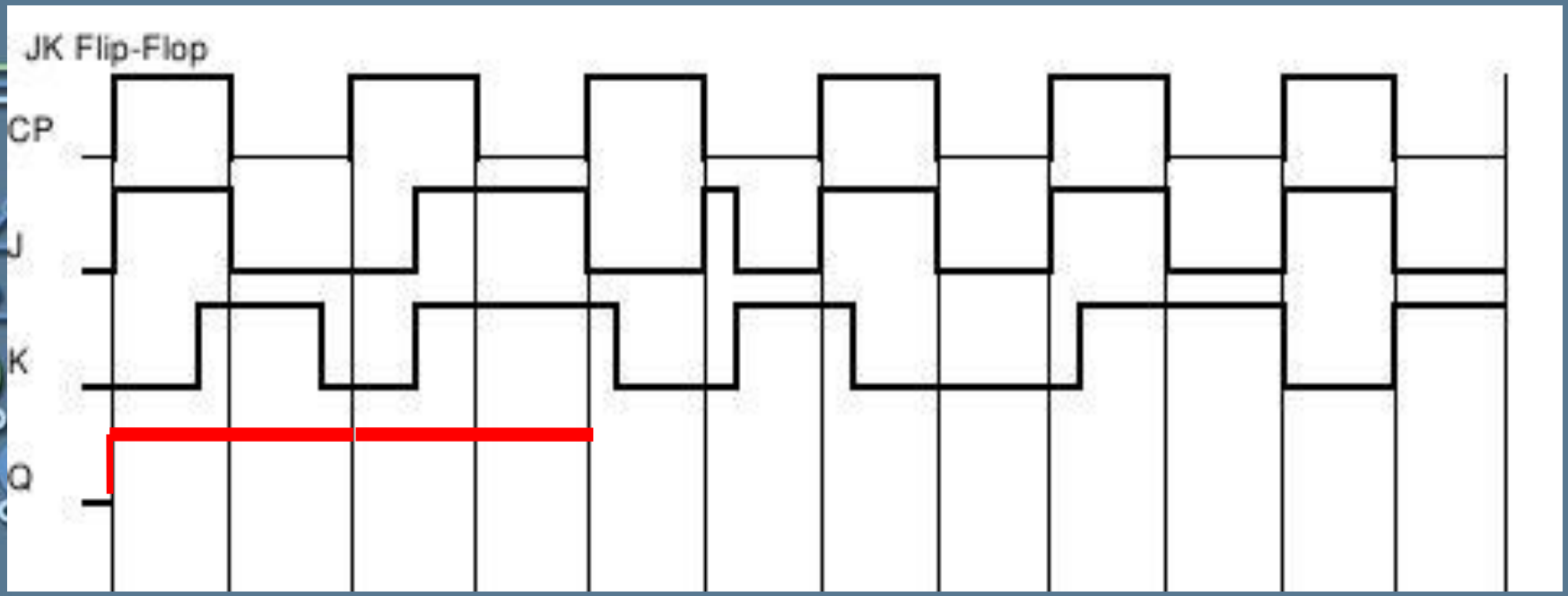
Positive edge-triggered

Examples



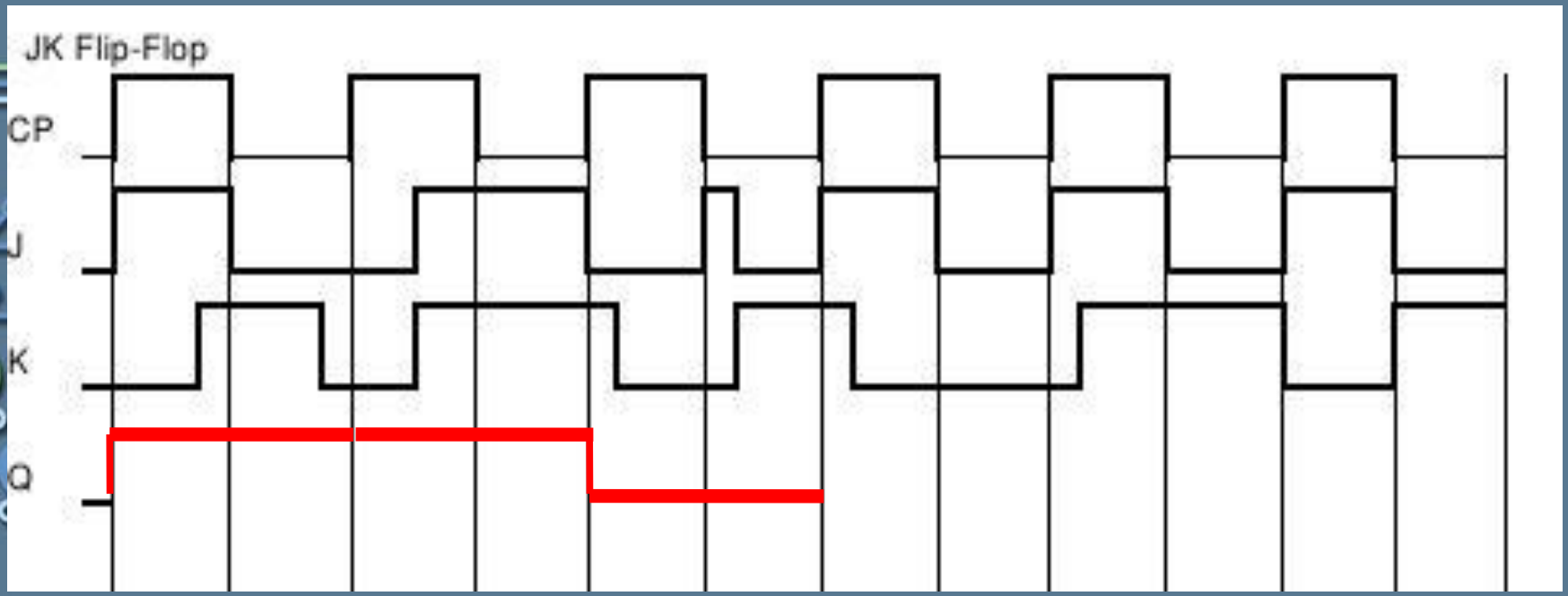
Positive edge-triggered

Examples



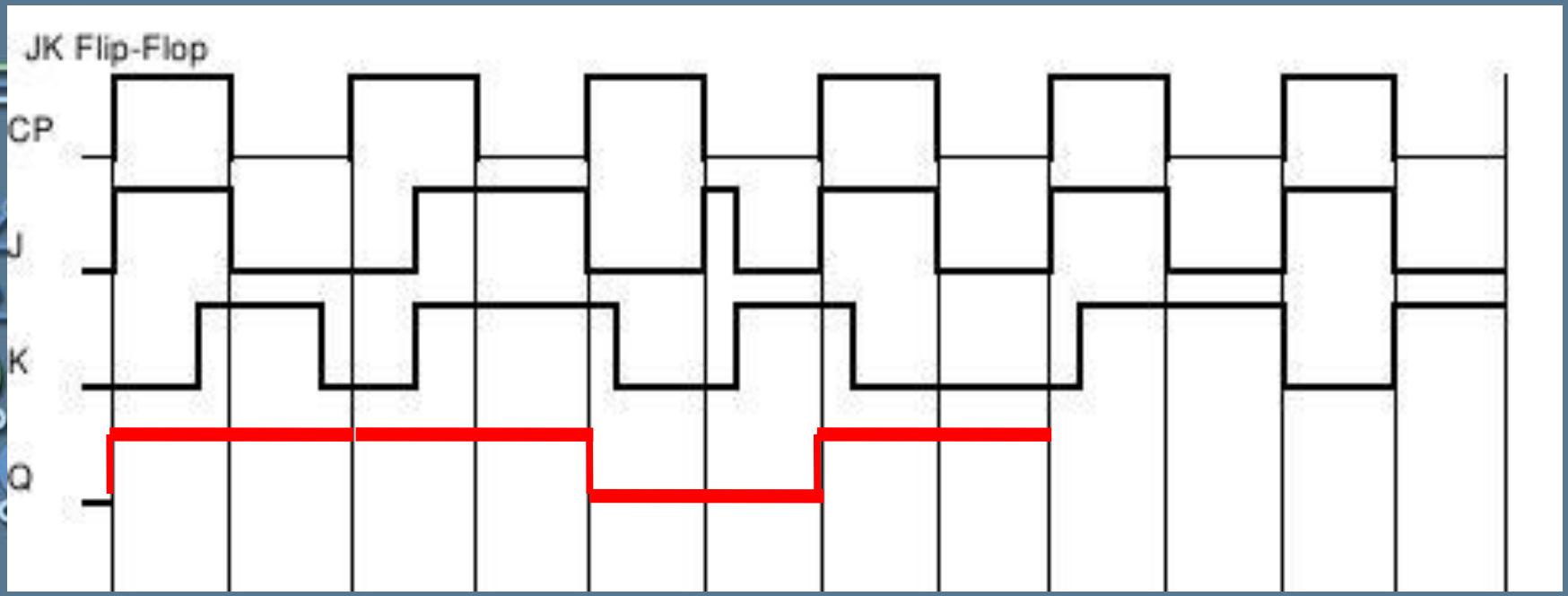
Positive edge-triggered

Examples



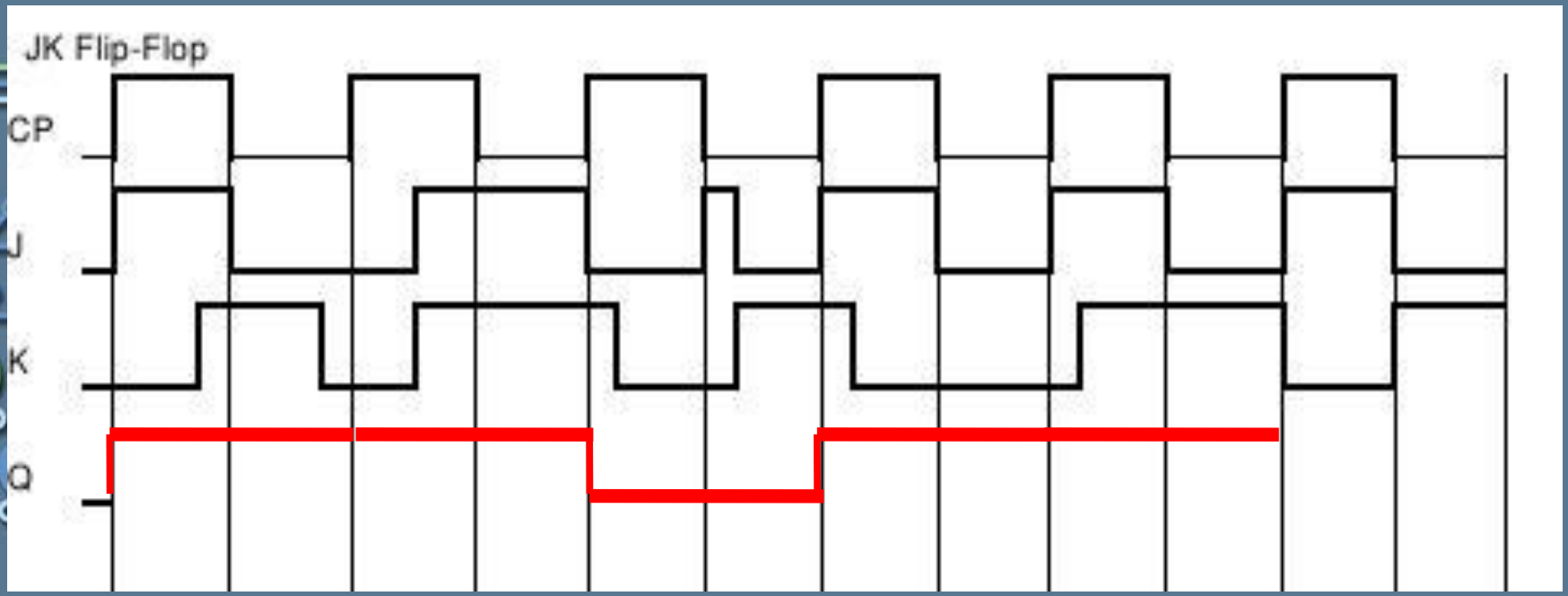
Positive edge-triggered

Examples



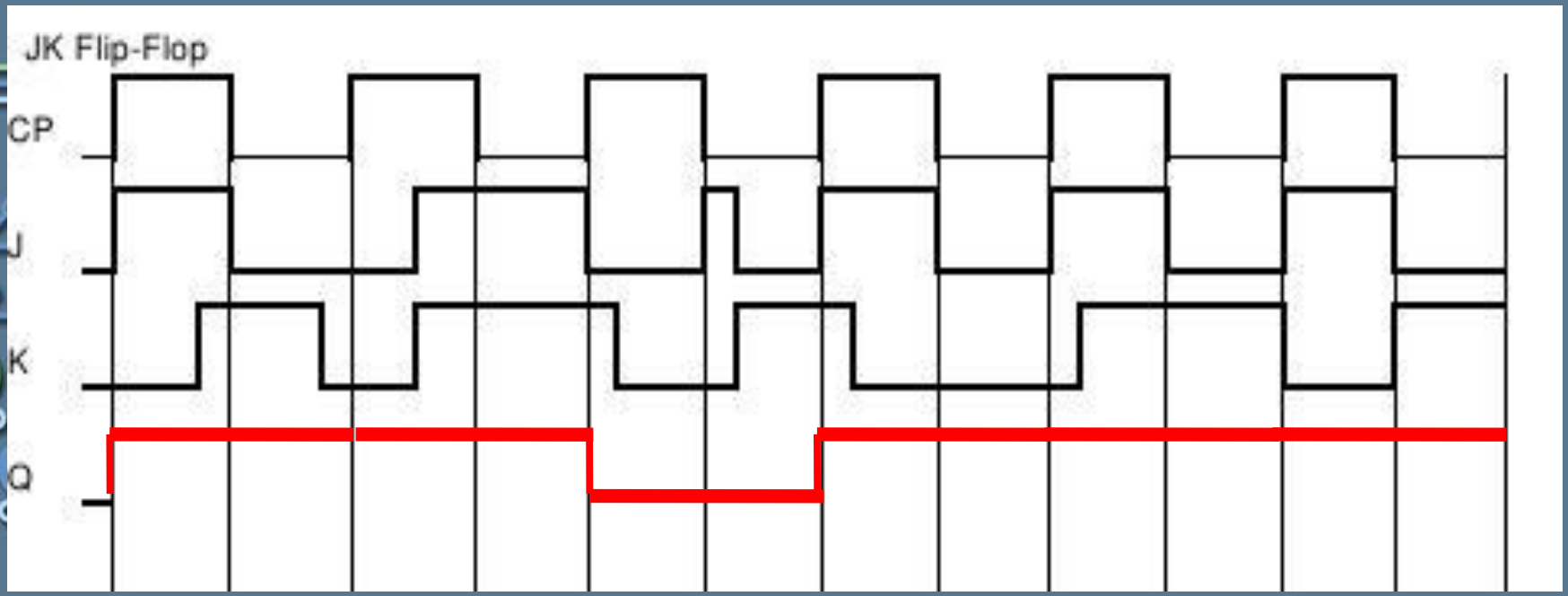
Positive edge-triggered

Examples



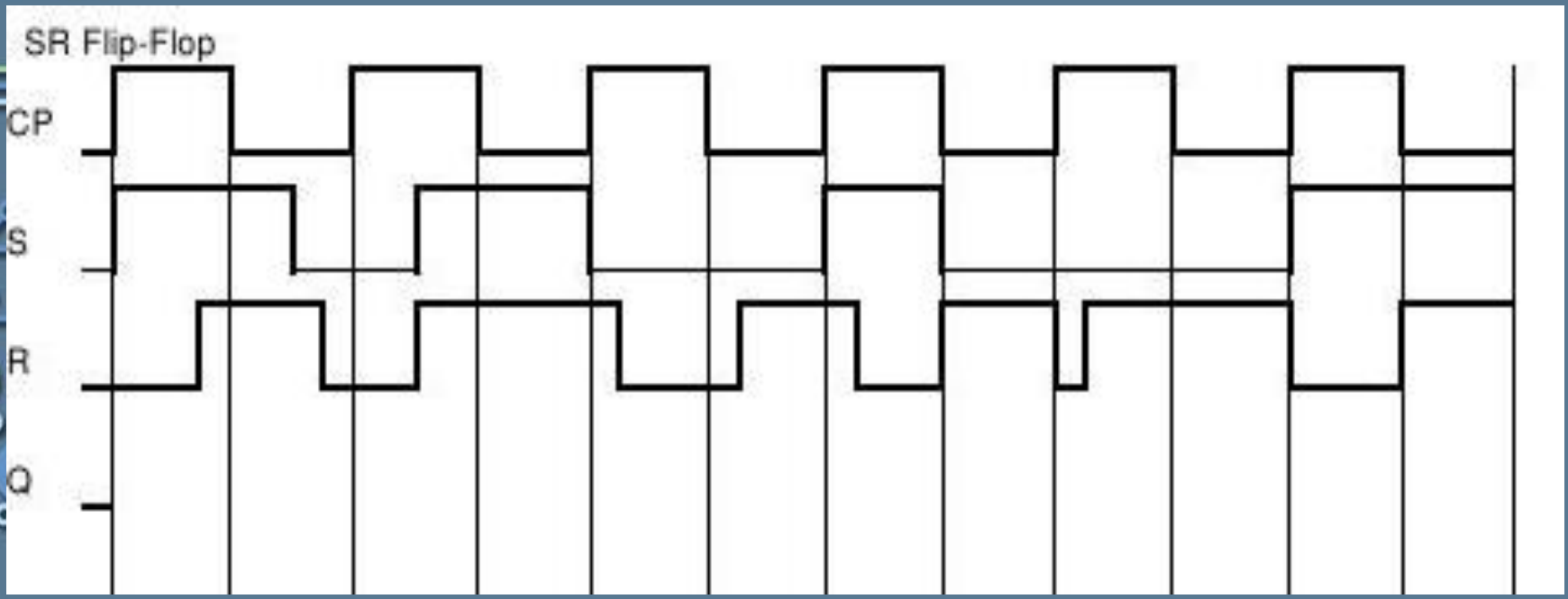
Positive edge-triggered

Examples



Positive edge-triggered

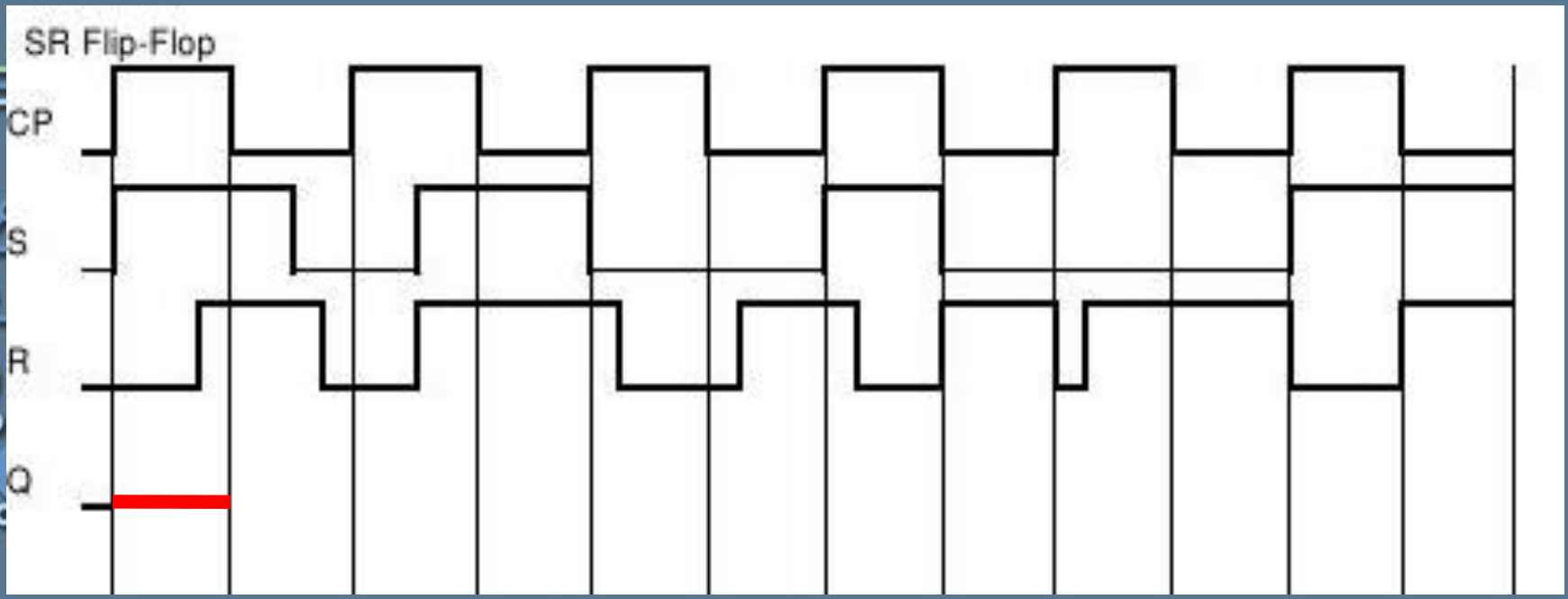
Examples



Negative edge-triggered

Indeterminate = 1

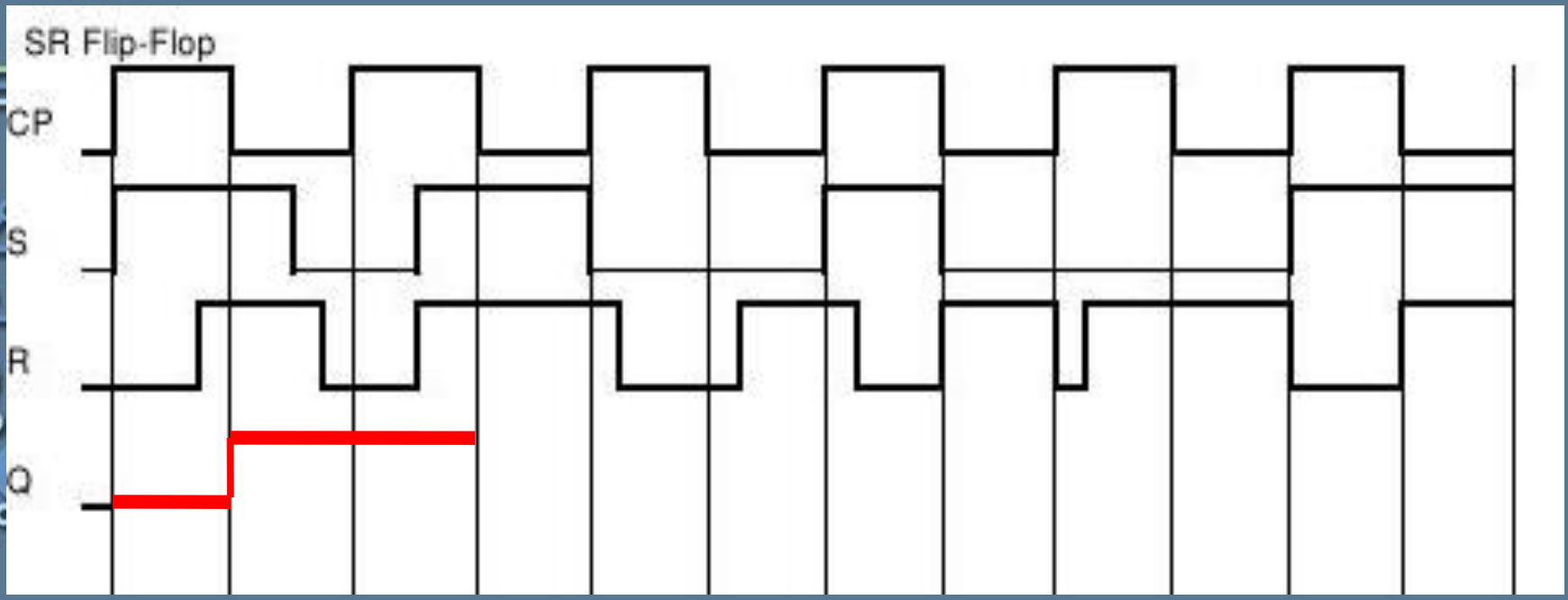
Examples



Negative edge-triggered

Indeterminate = 1

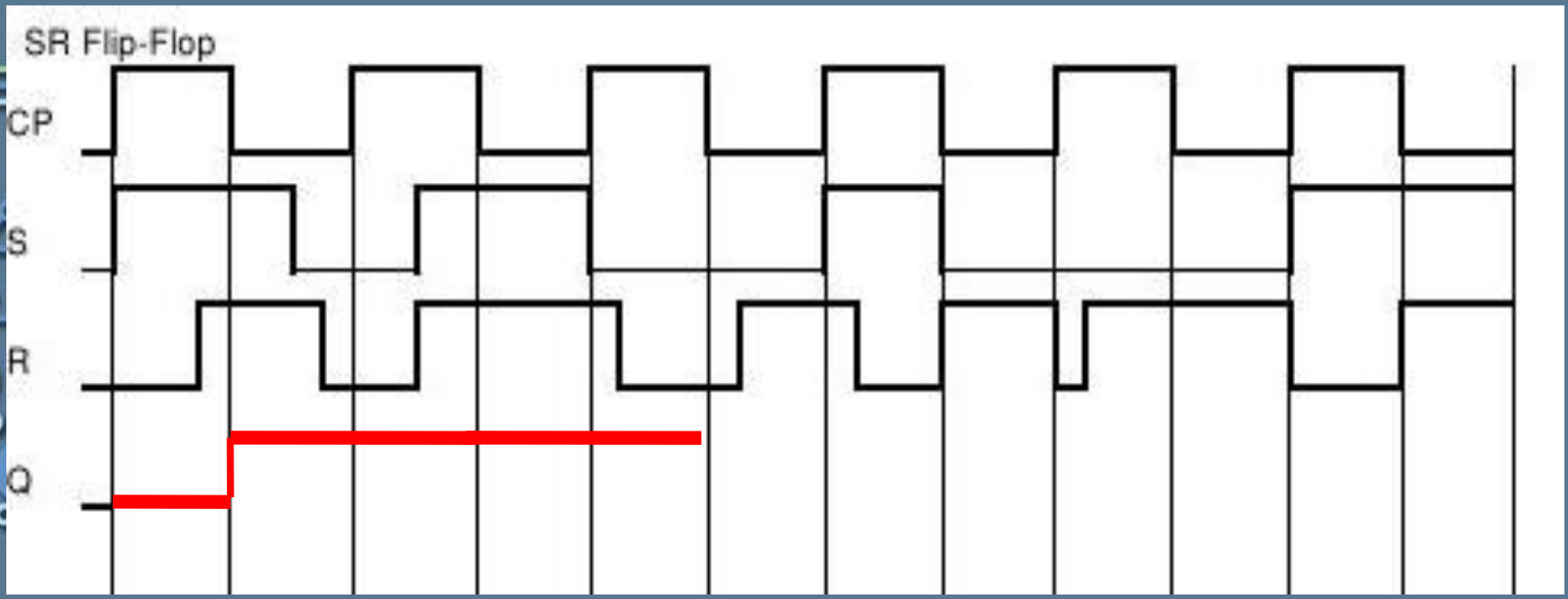
Examples



Negative edge-triggered

Indeterminate = 1

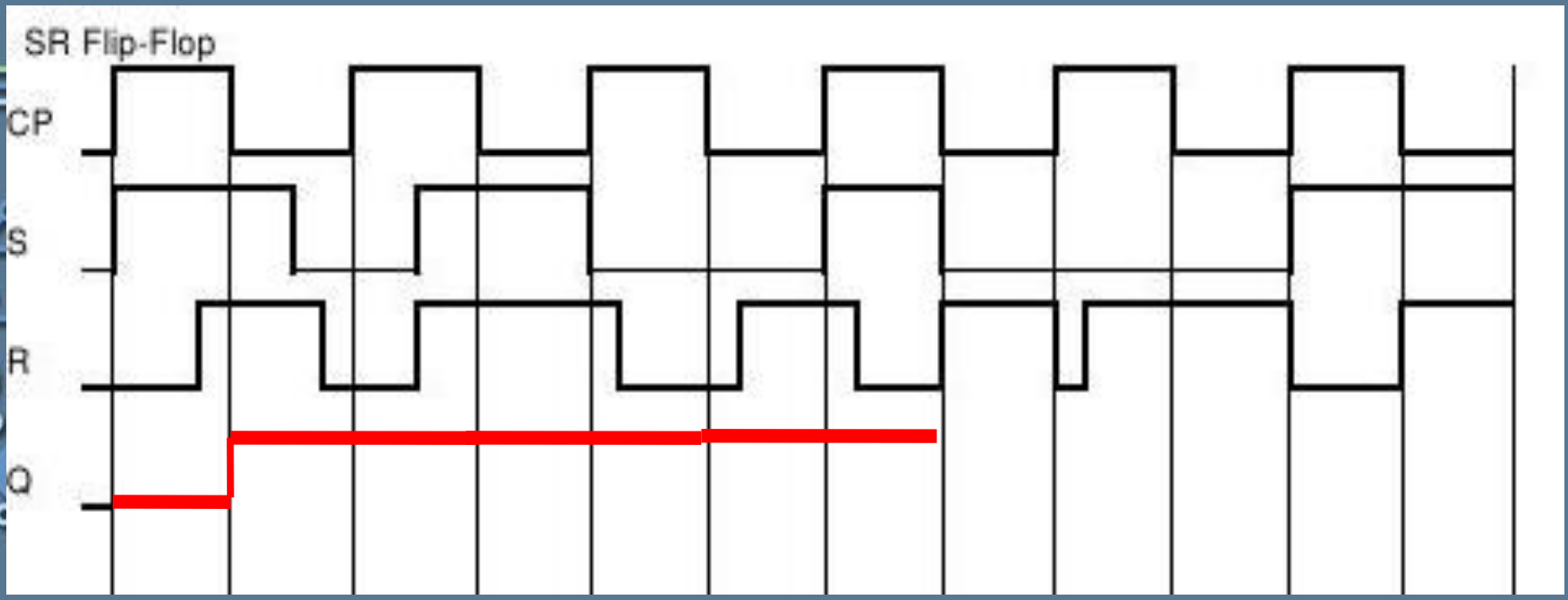
Examples



Negative edge-triggered

Indeterminate = 1

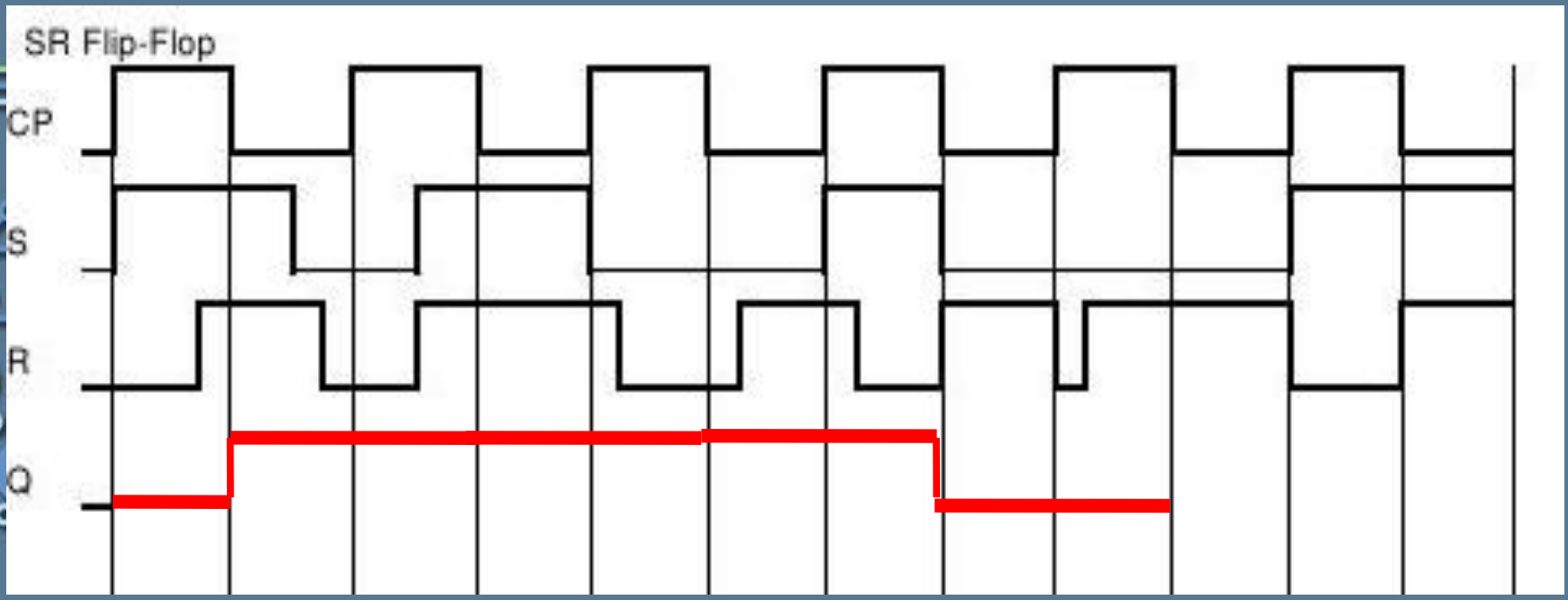
Examples



Negative edge-triggered

Indeterminate = 1

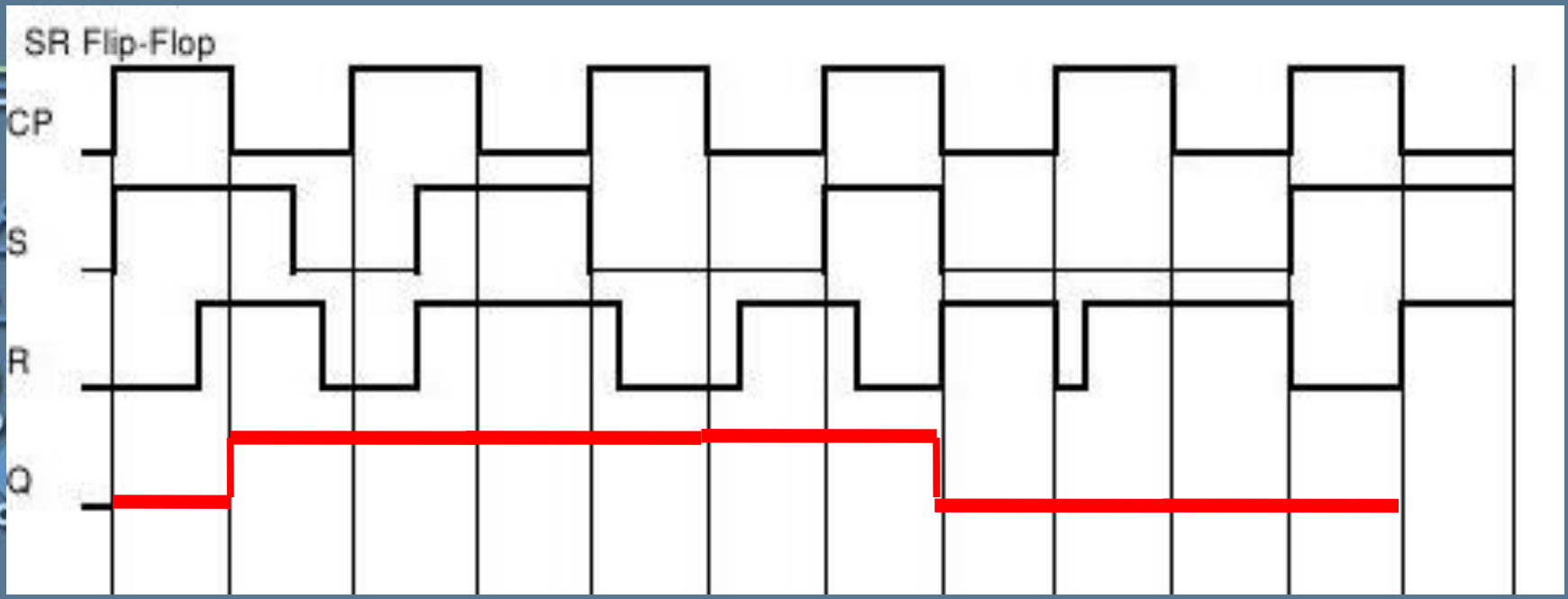
Examples



Negative edge-triggered

Indeterminate = 1

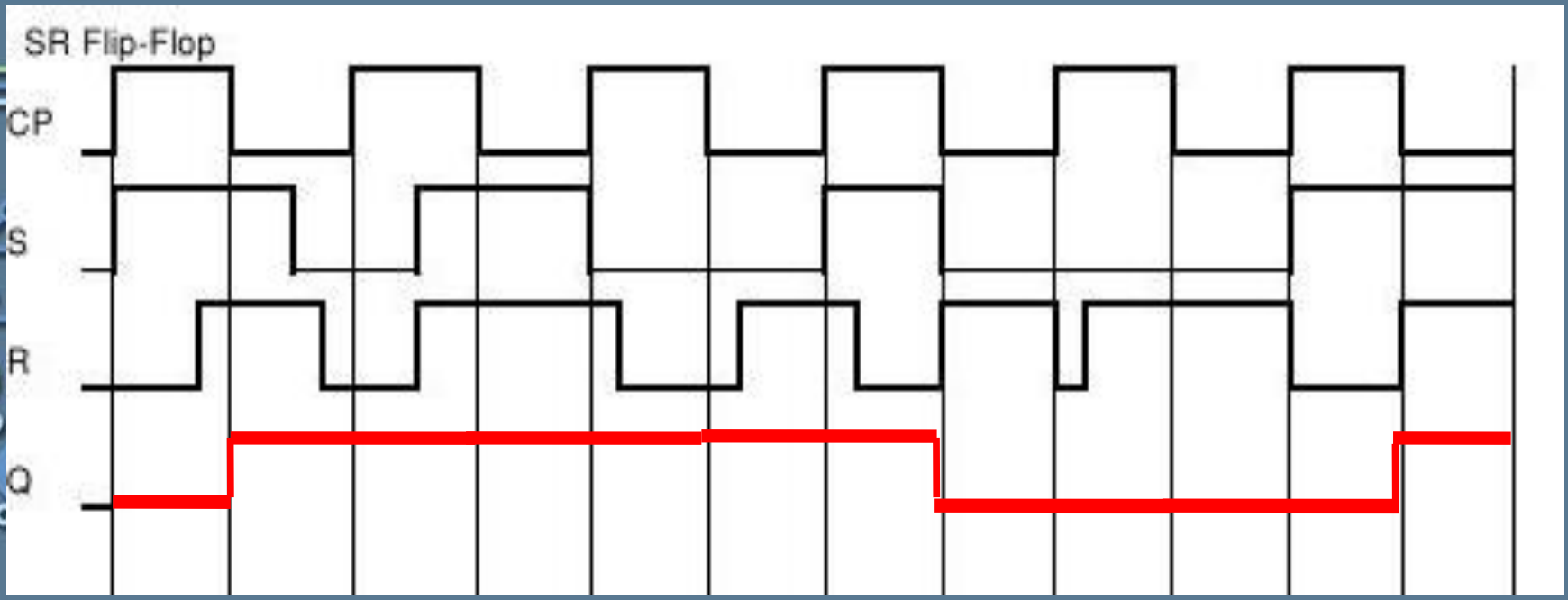
Examples



Negative edge-triggered

Indeterminate = 1

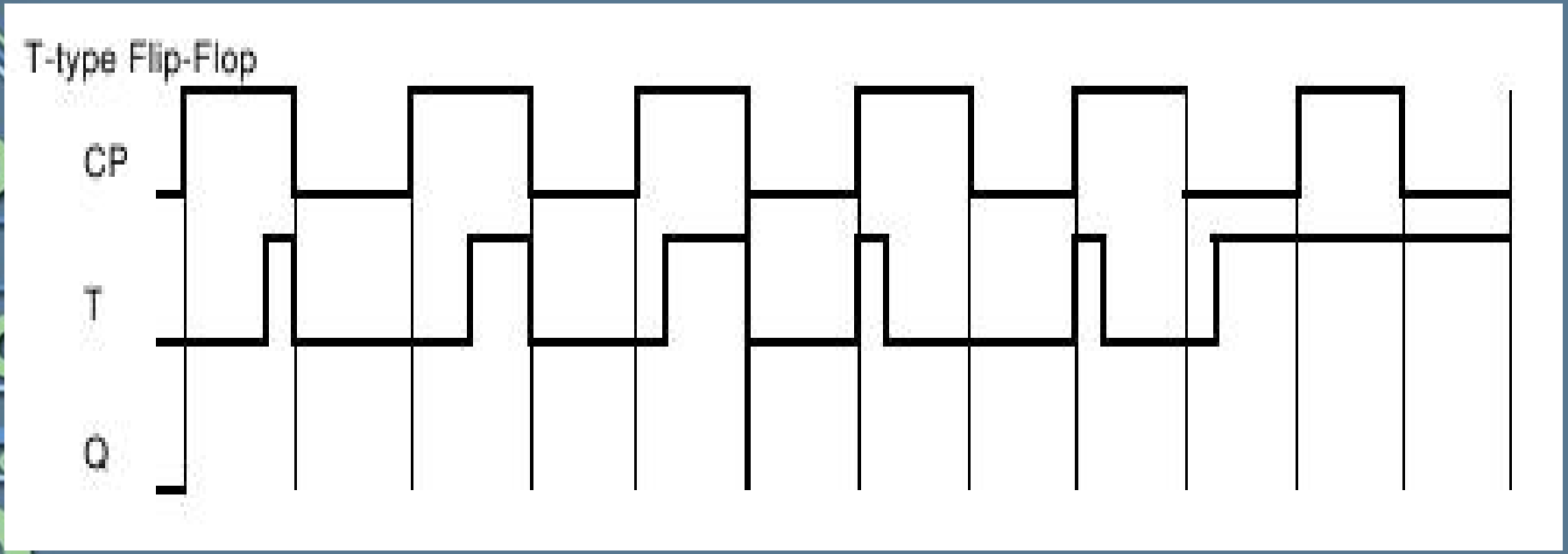
Examples



Negative edge-triggered

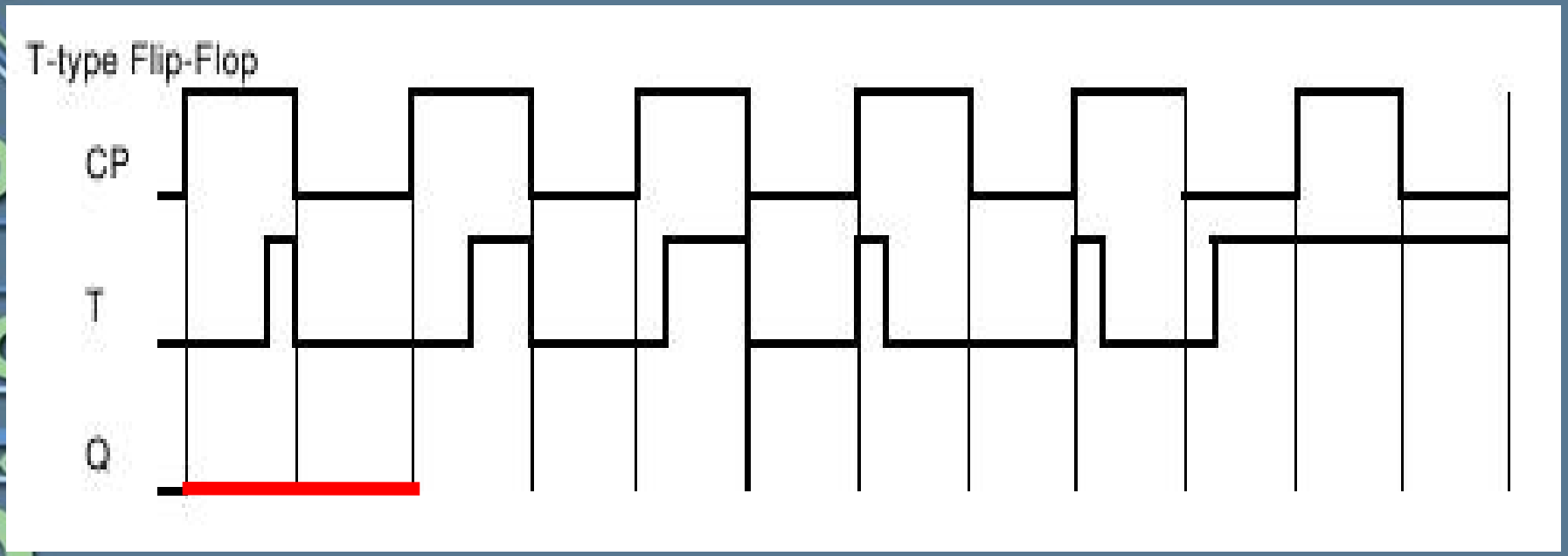
Indeterminate = 1

Examples



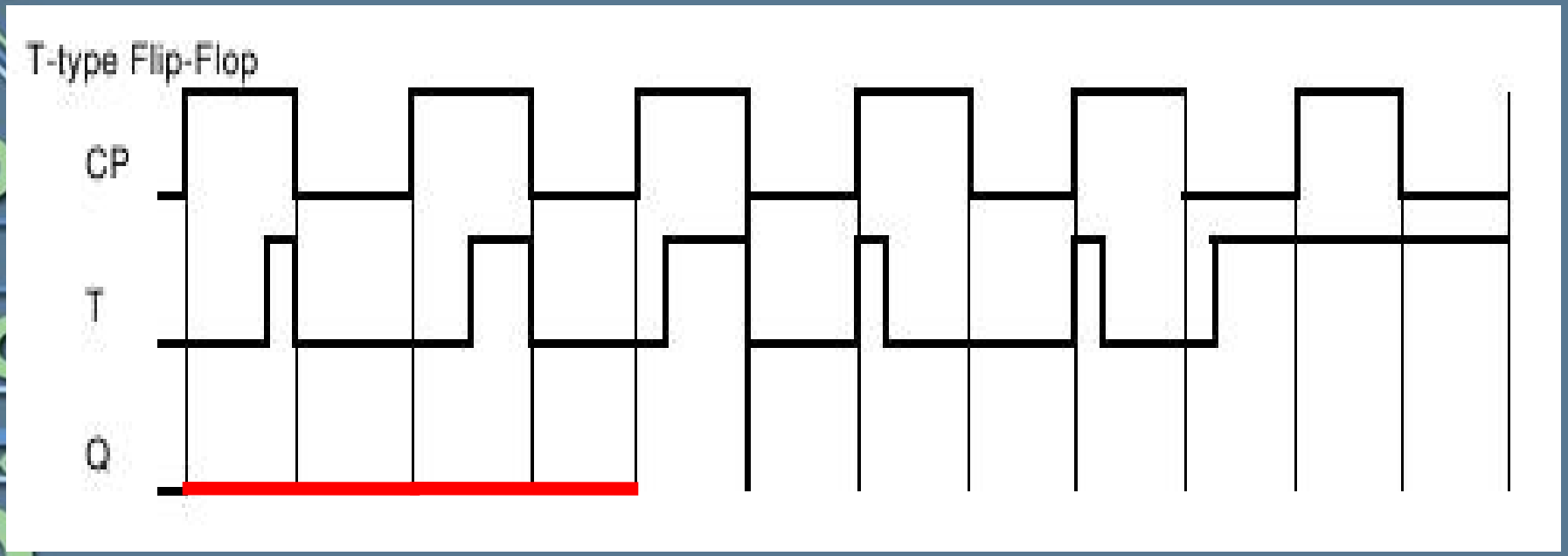
Positive edge-triggered

Examples



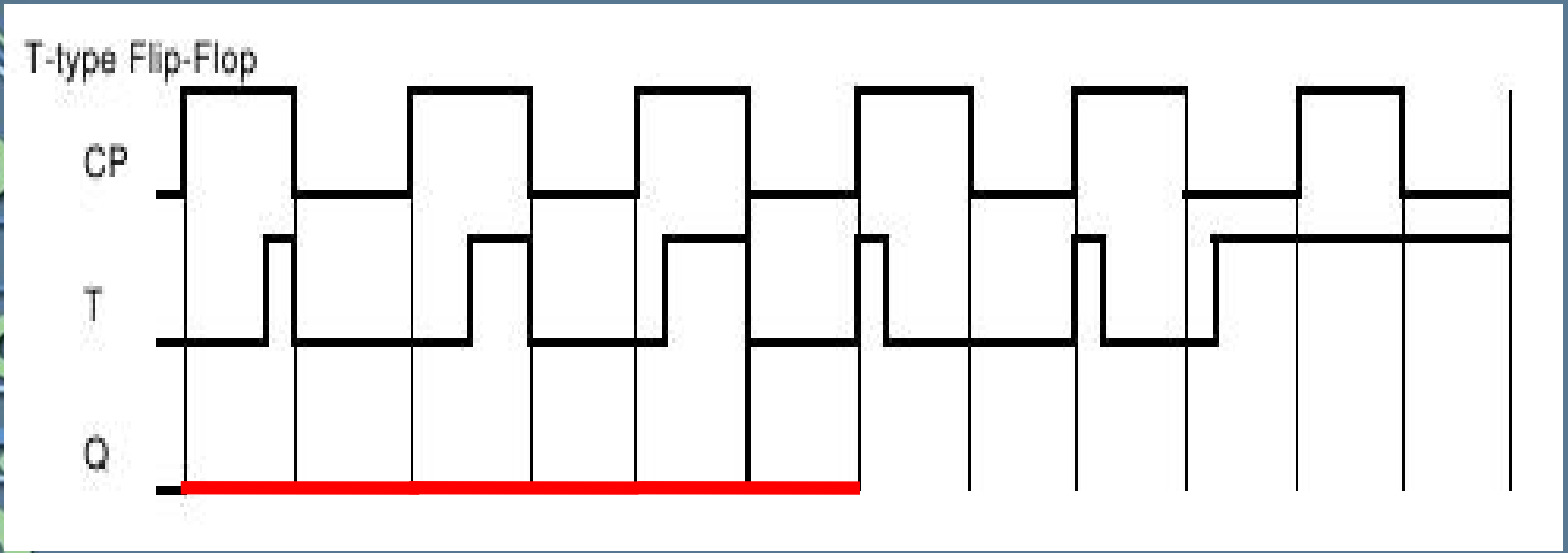
Positive edge-triggered

Examples



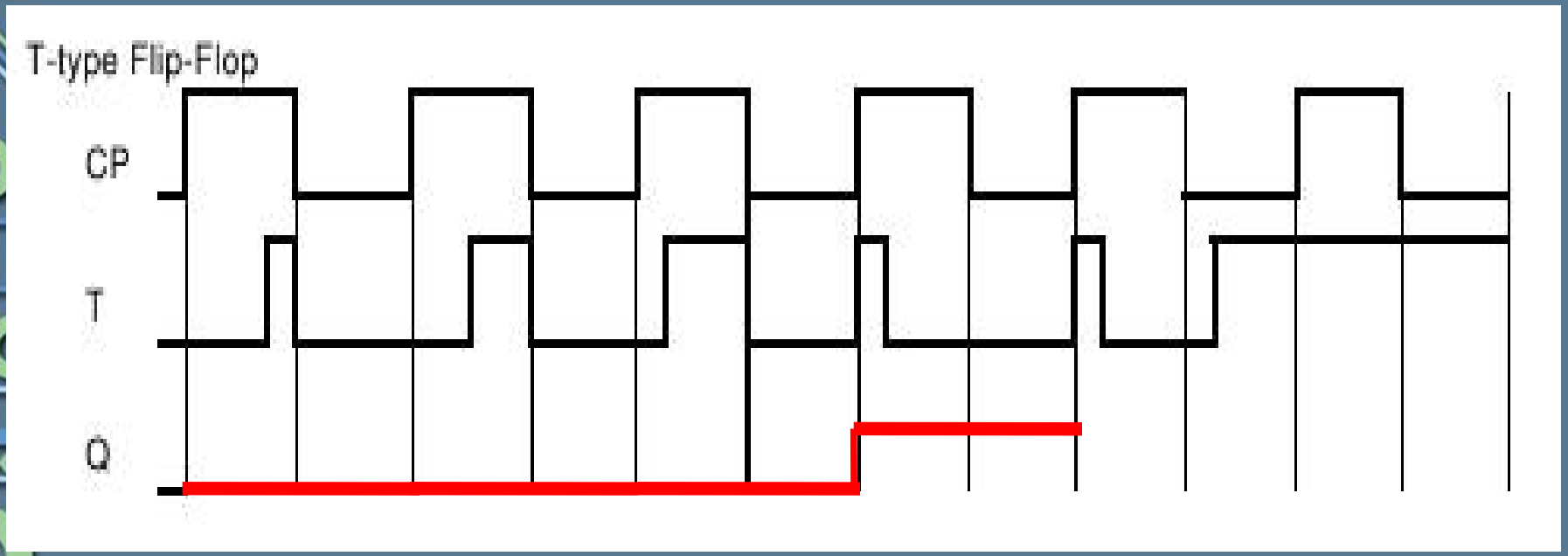
Positive edge-triggered

Examples



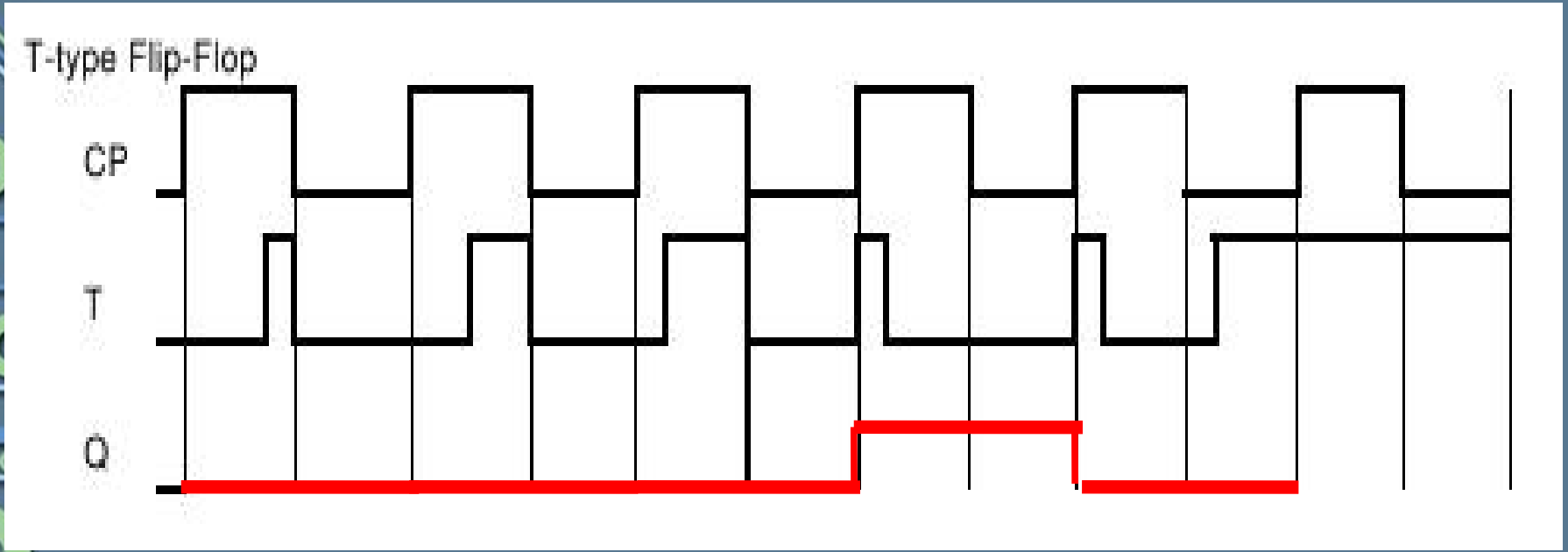
Positive edge-triggered

Examples



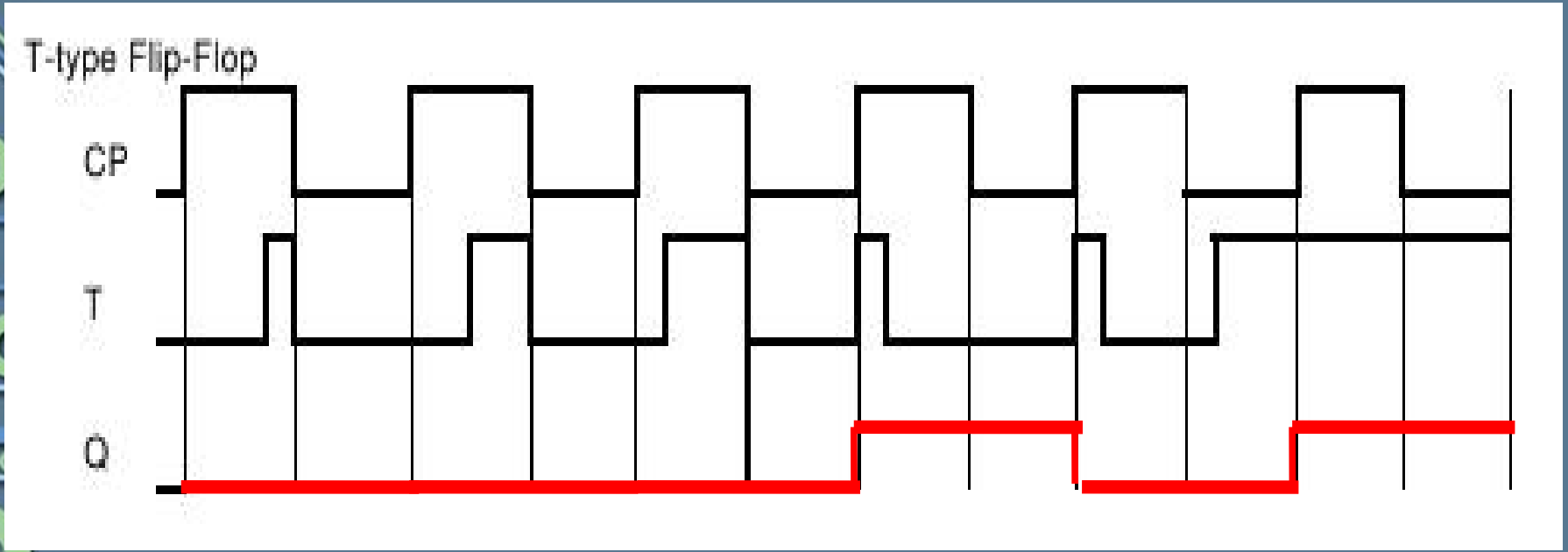
Positive edge-triggered

Examples



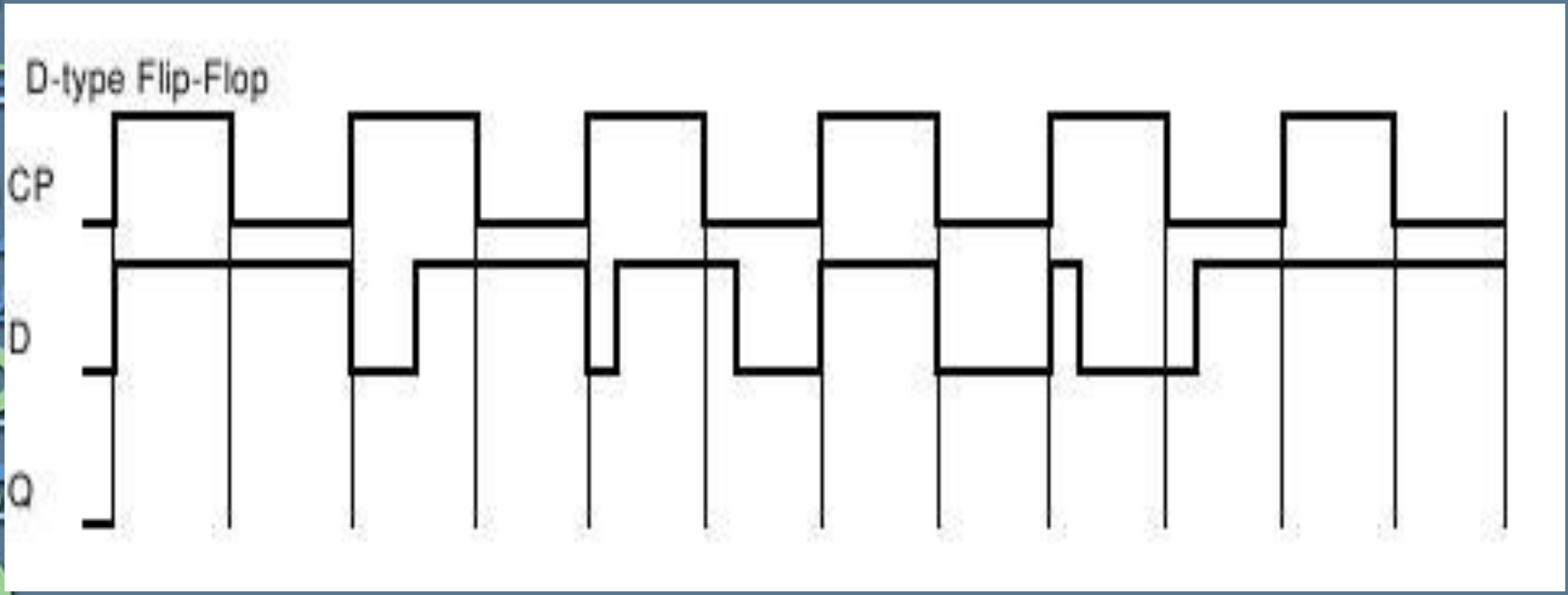
Positive edge-triggered

Examples



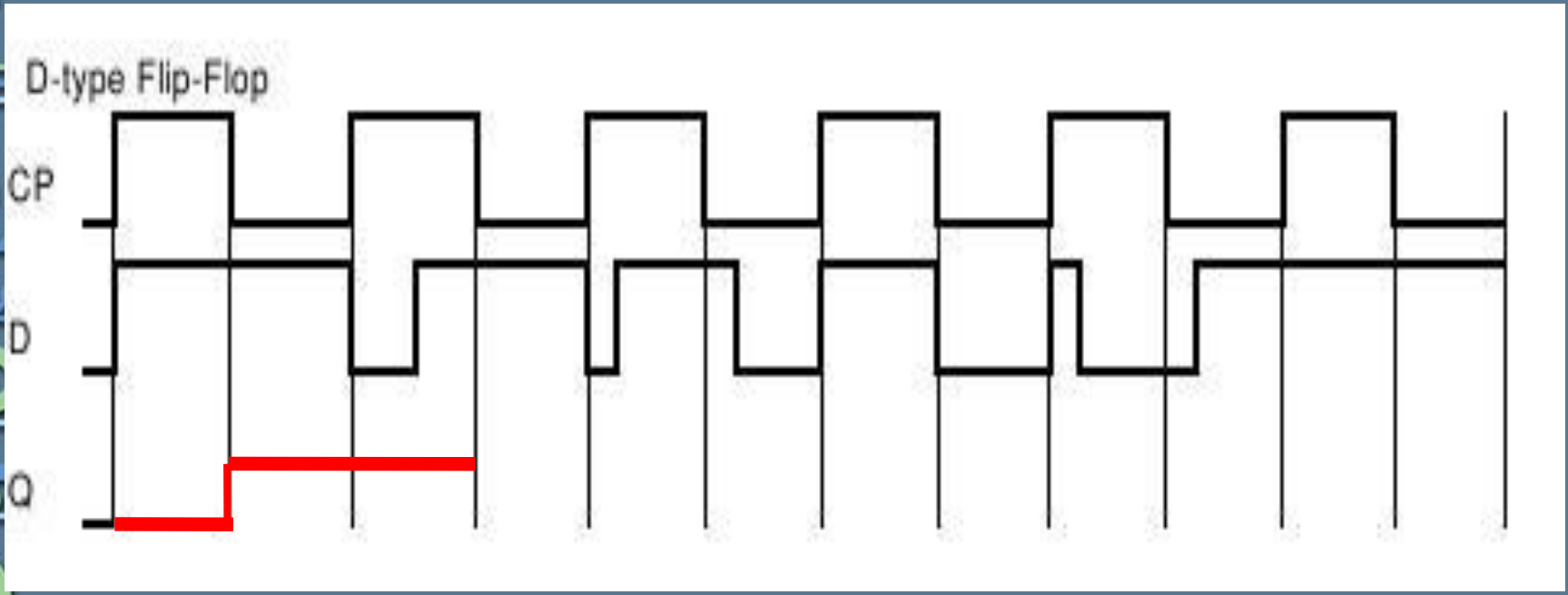
Positive edge-triggered

Examples



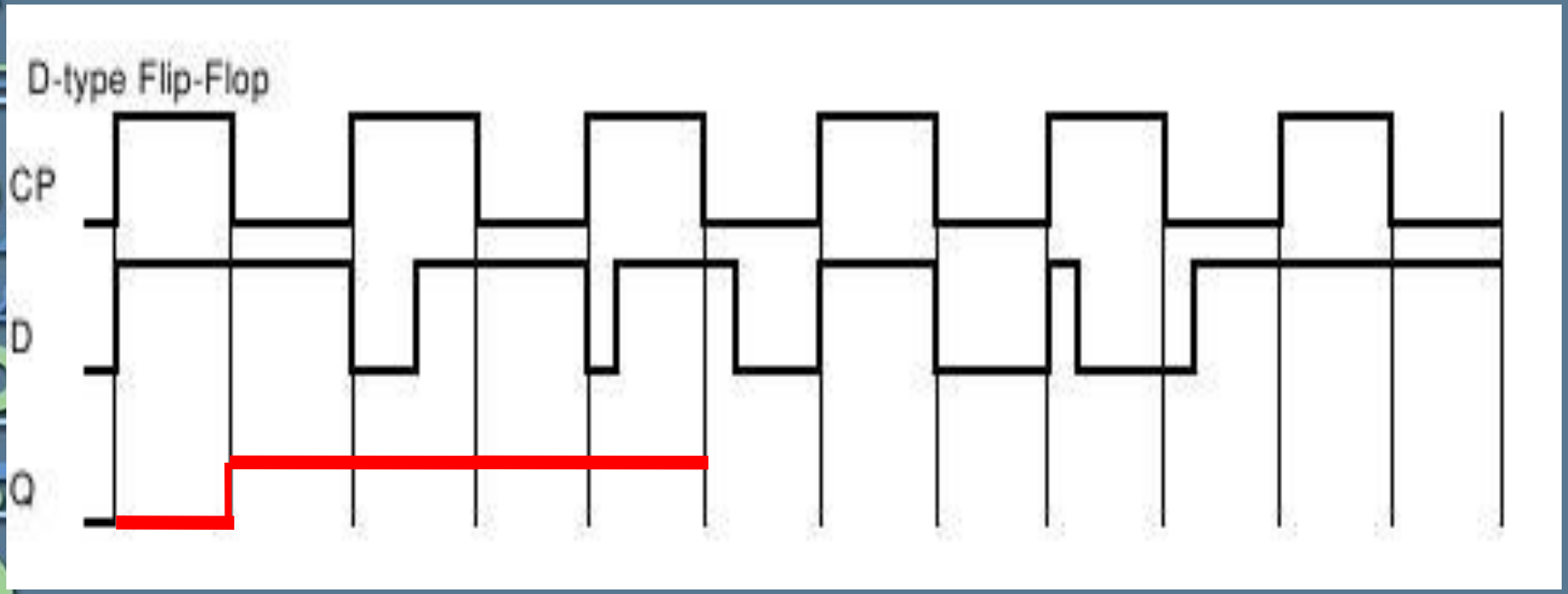
Negative edge-triggered

Examples



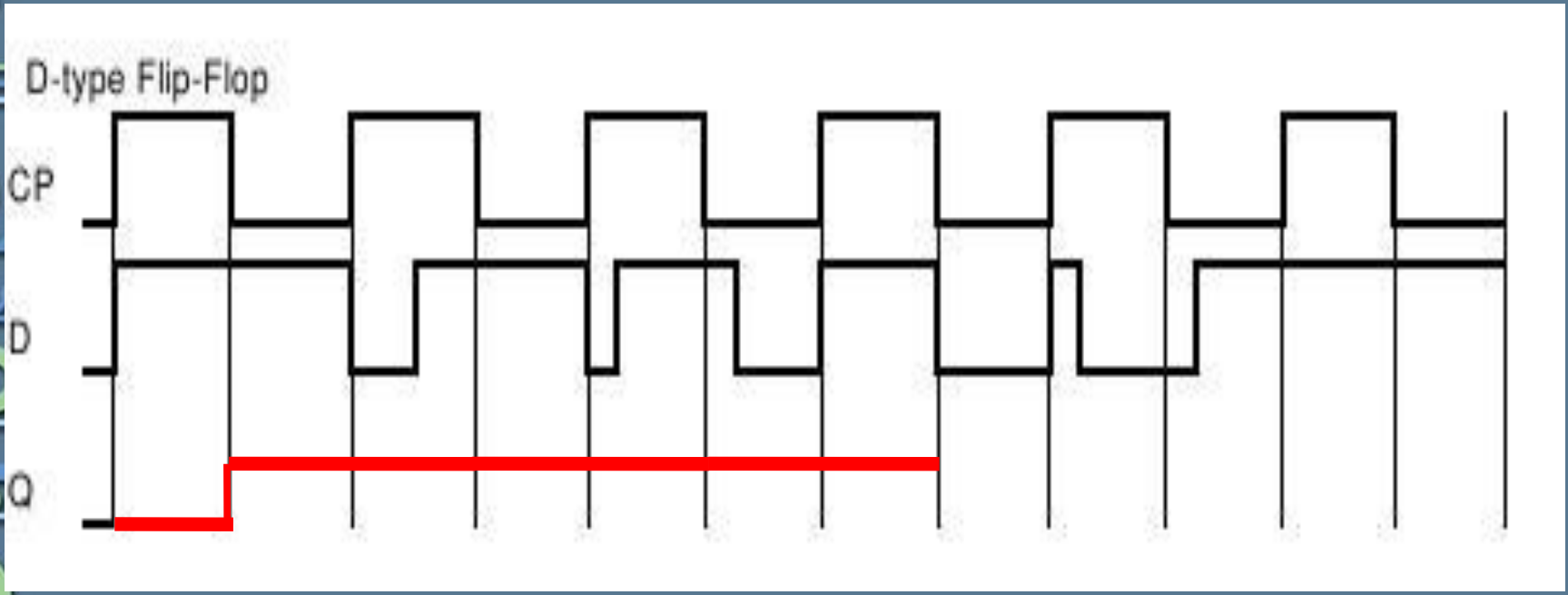
Negative edge-triggered

Examples



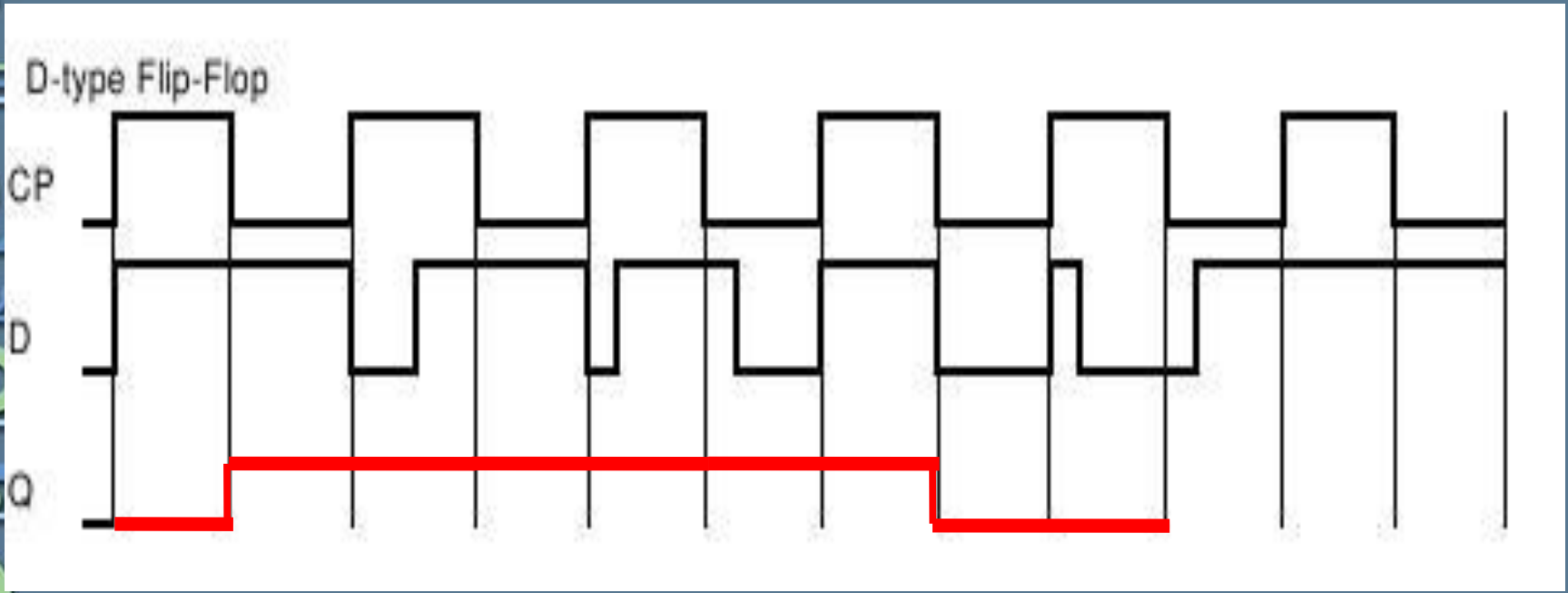
Negative edge-triggered

Examples



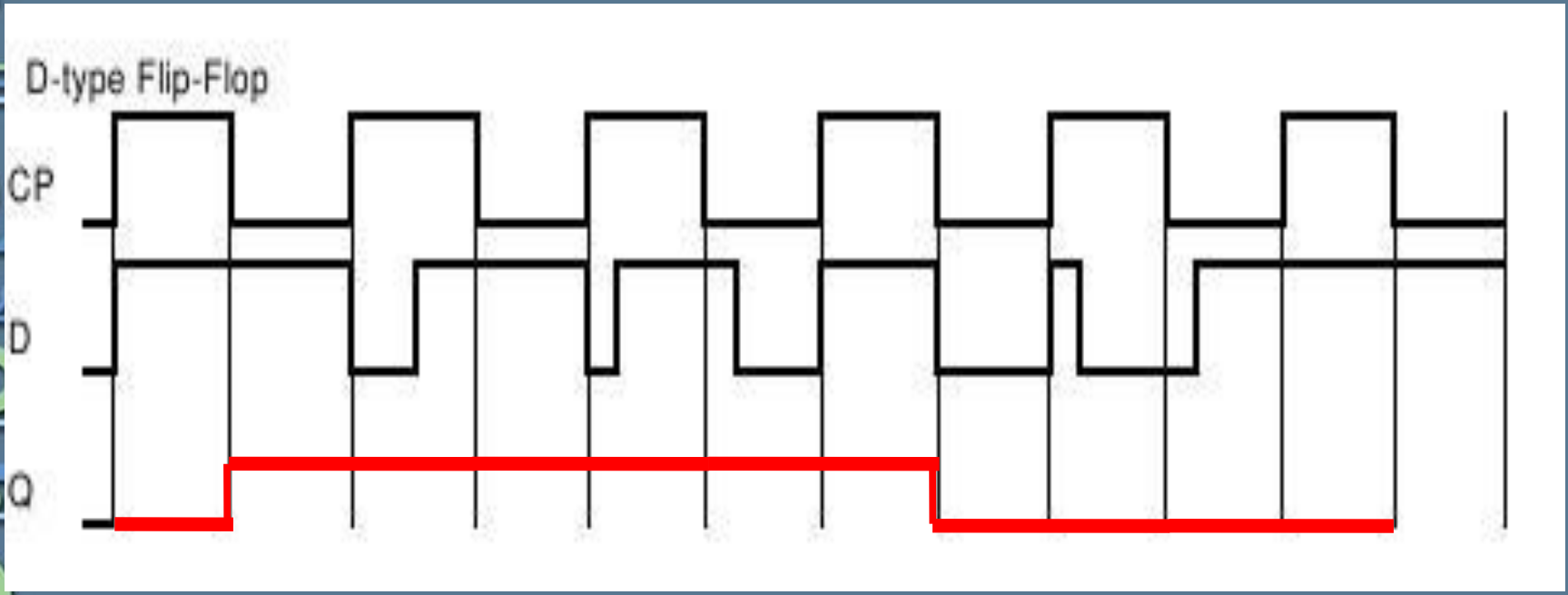
Negative edge-triggered

Examples



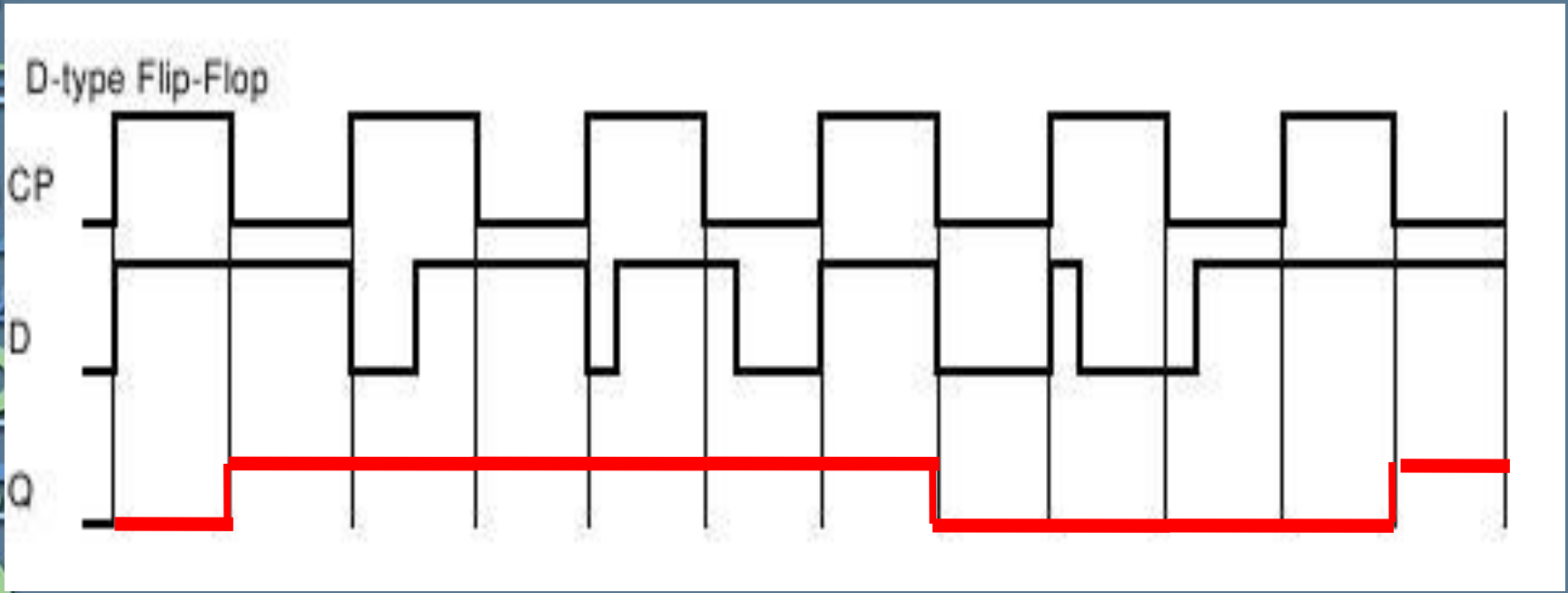
Negative edge-triggered

Examples



Negative edge-triggered

Examples

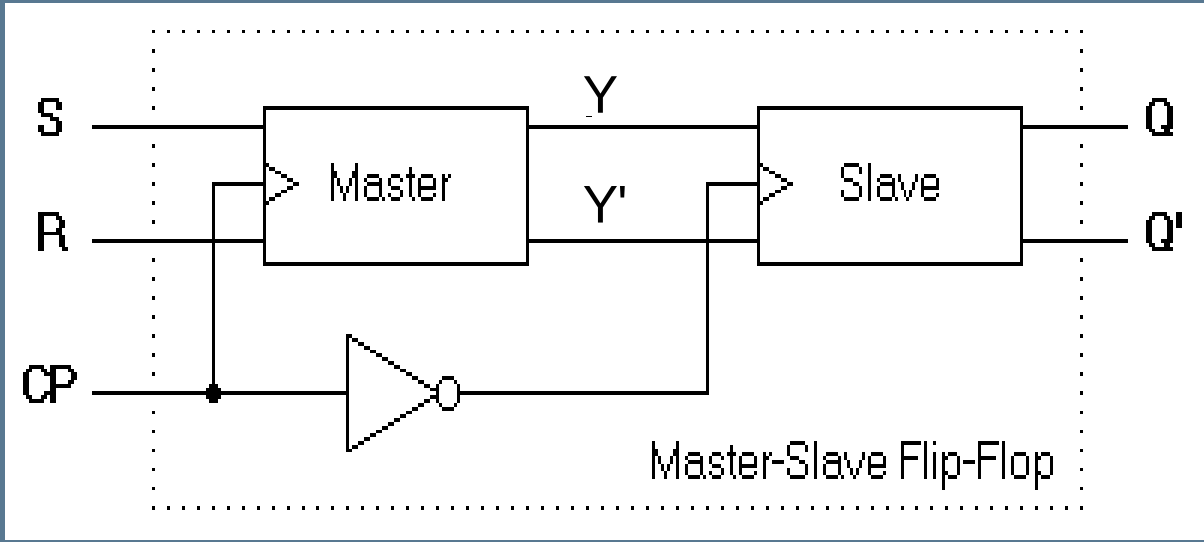


Negative edge-triggered

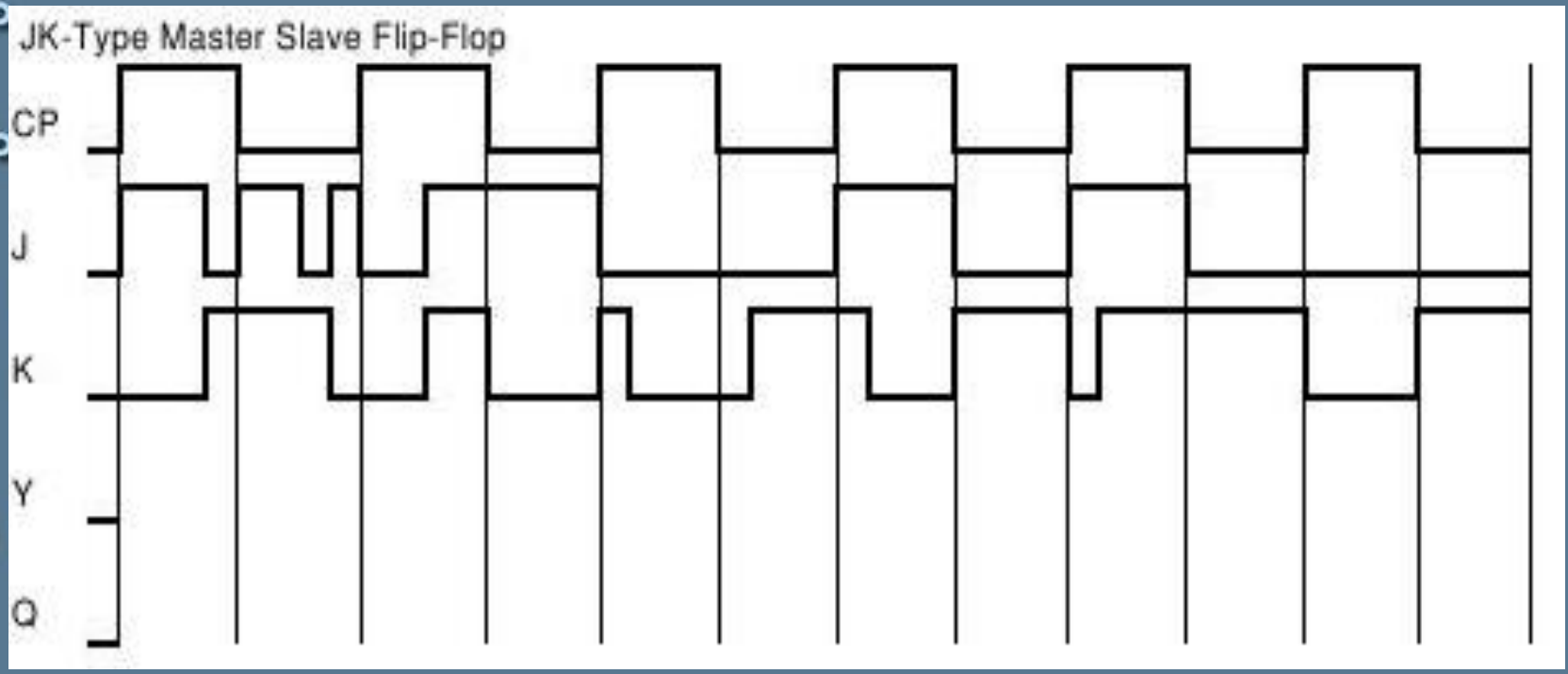
Pulse-Triggered Flip-flops

- Master-slave design
- Data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse

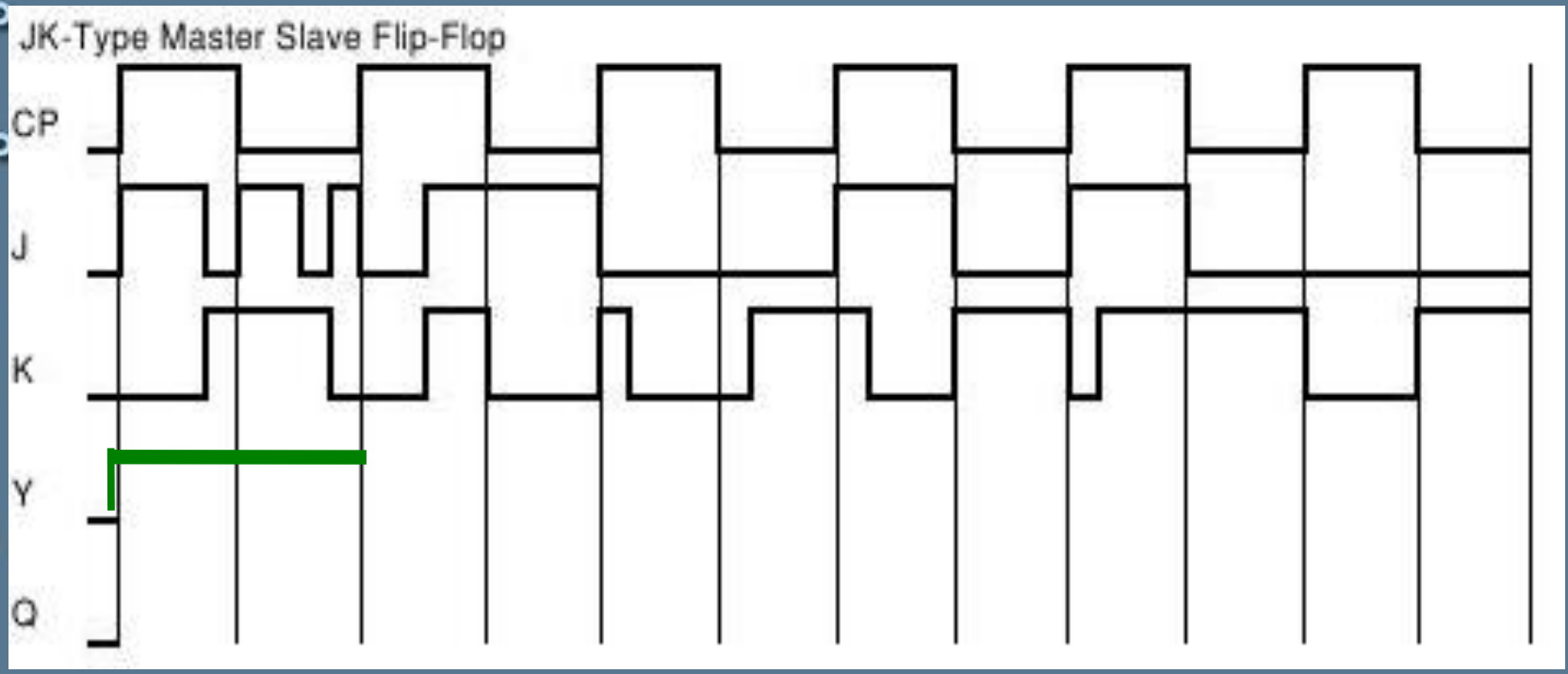
Example: Pulse-Triggered FF



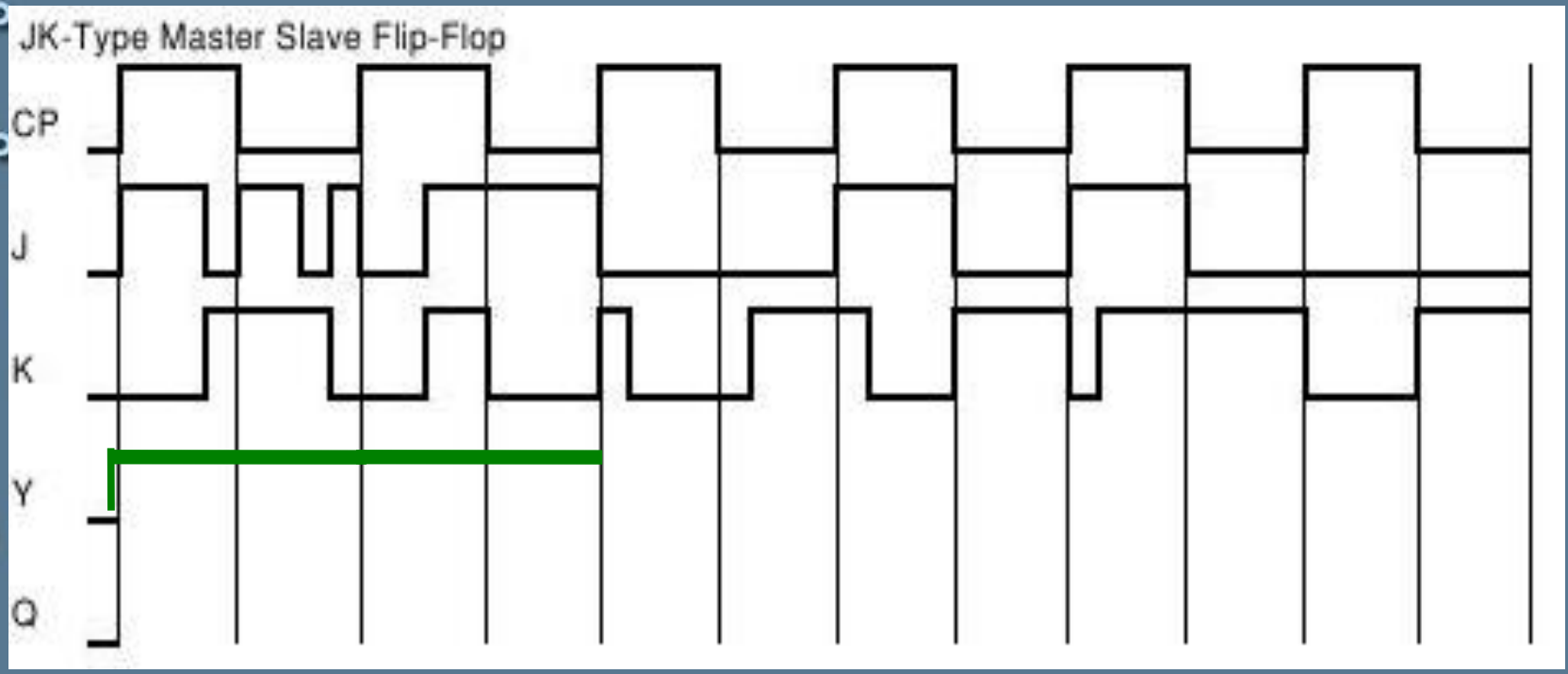
Examples



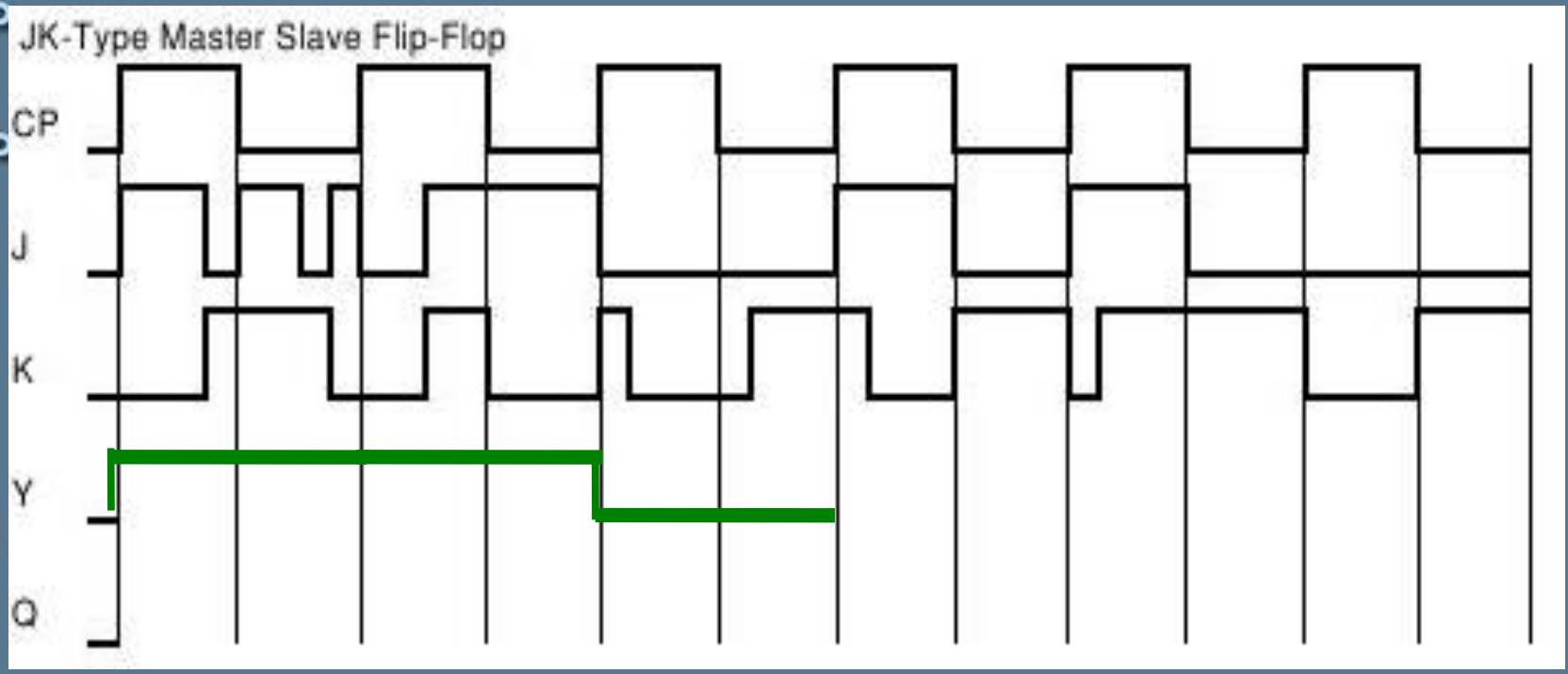
Examples



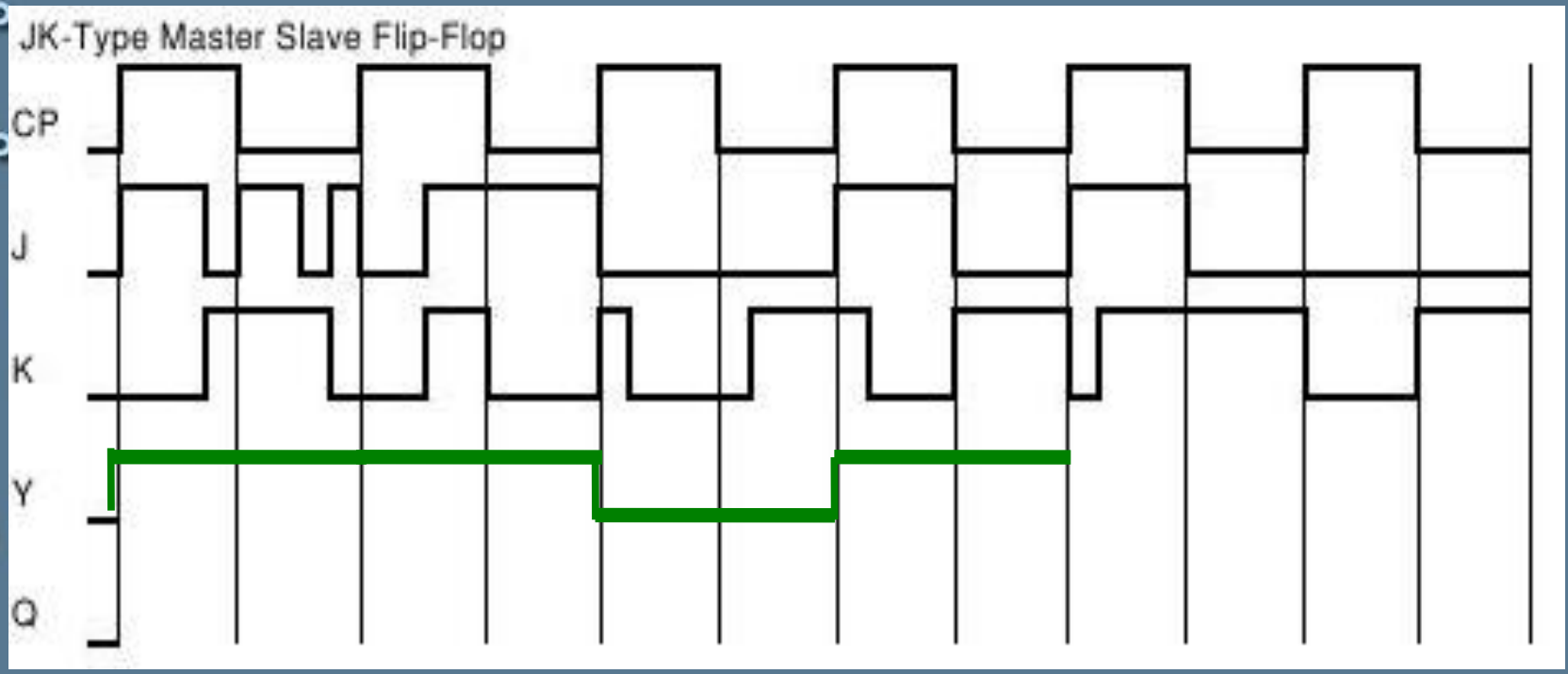
Examples



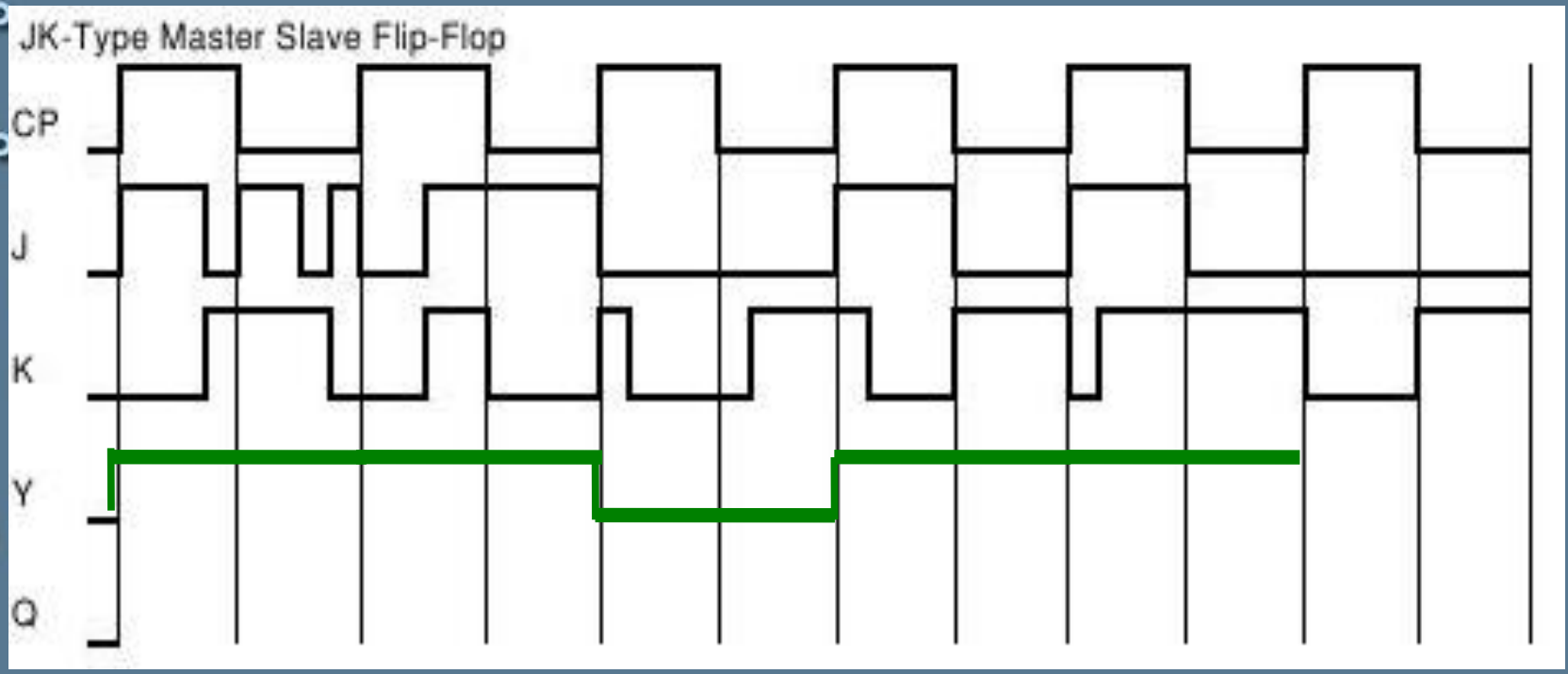
Examples



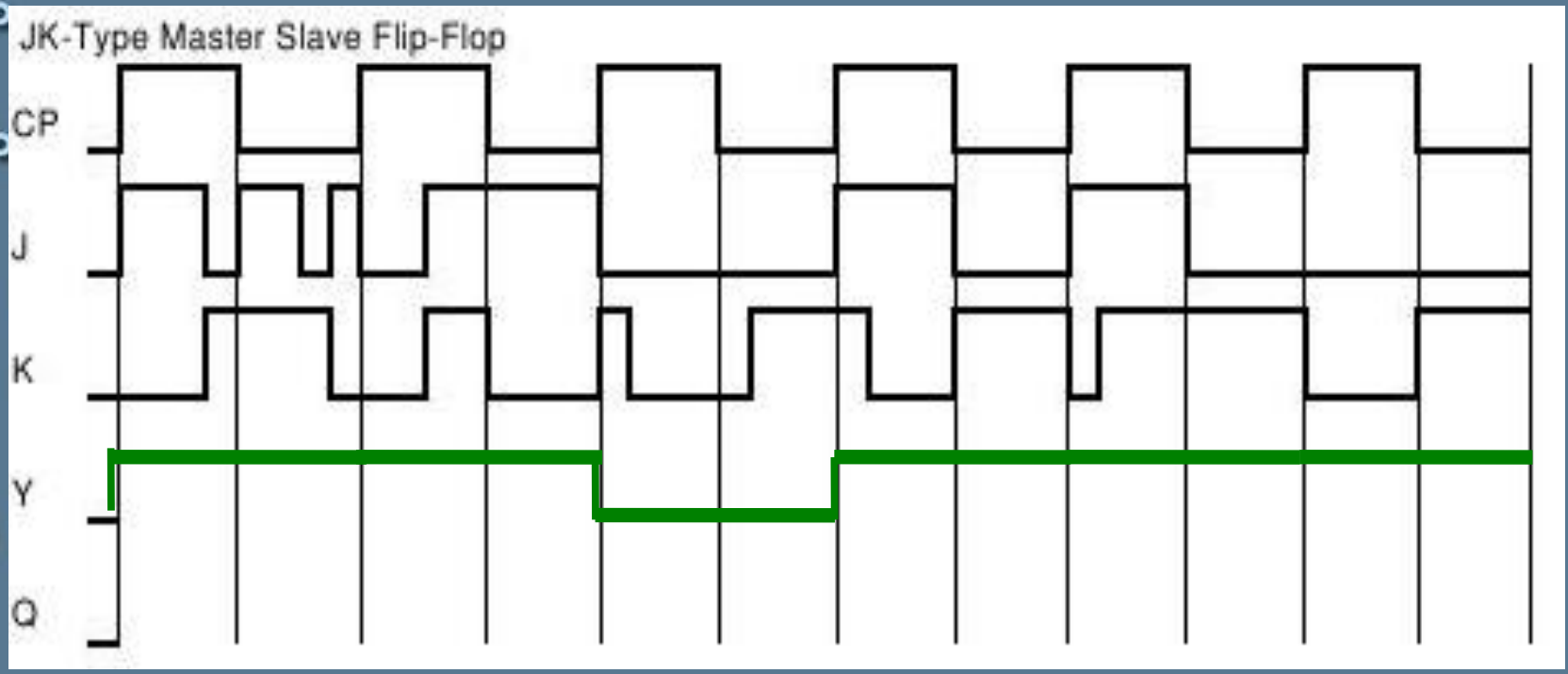
Examples



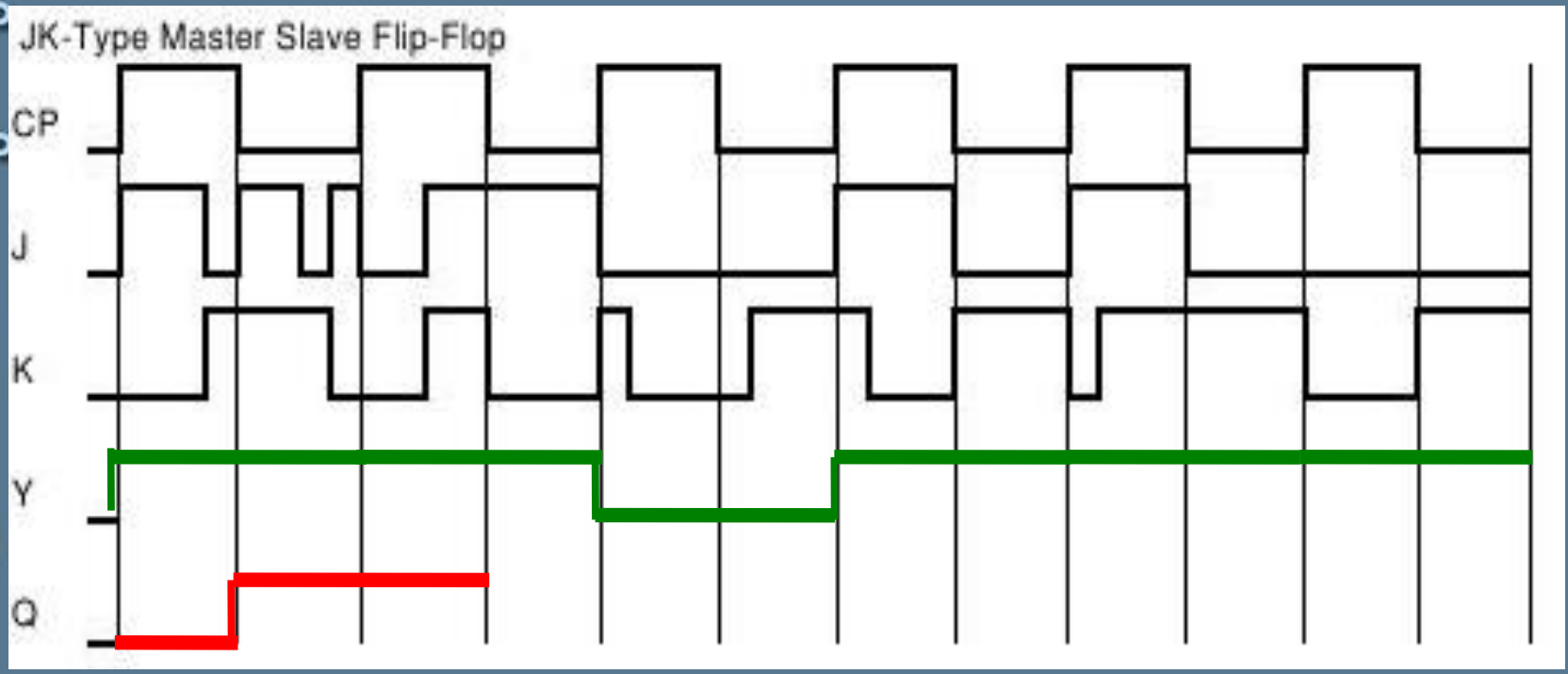
Examples



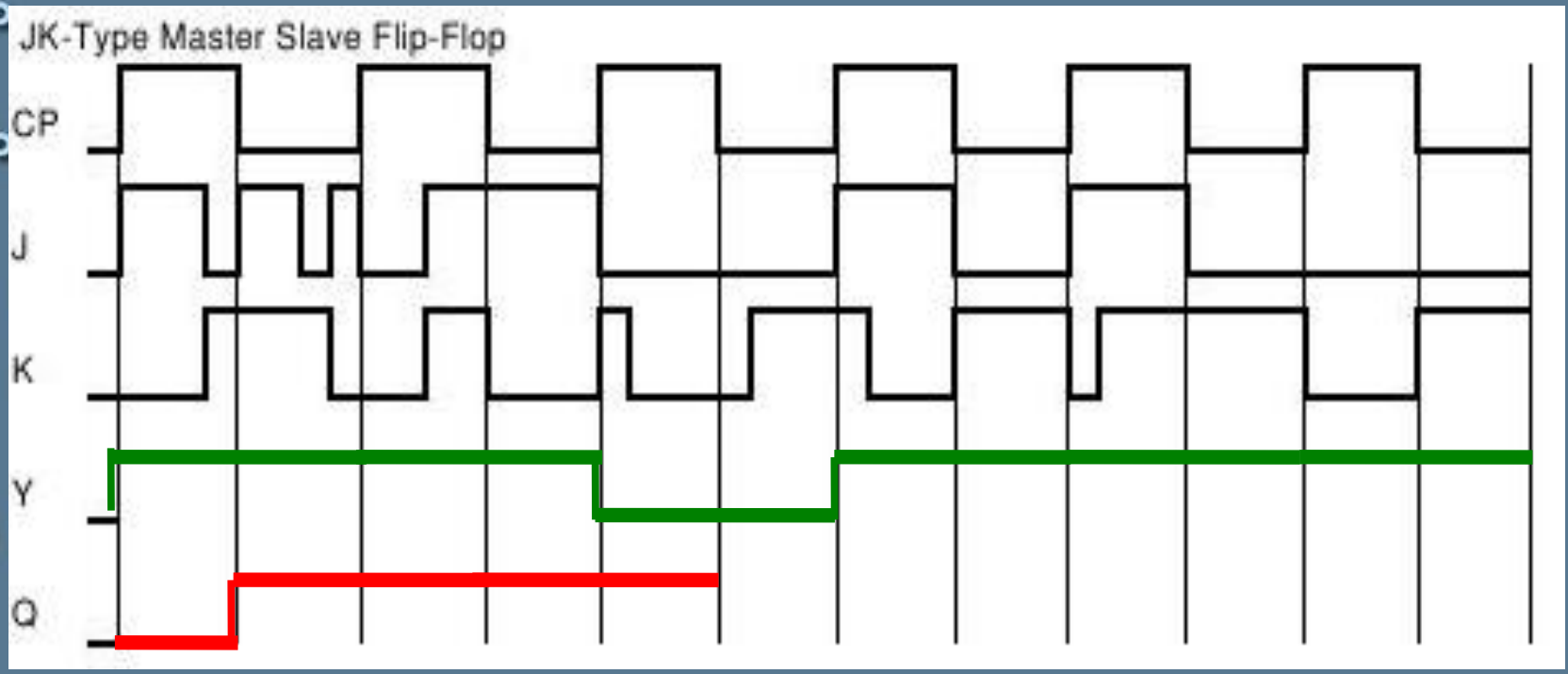
Examples



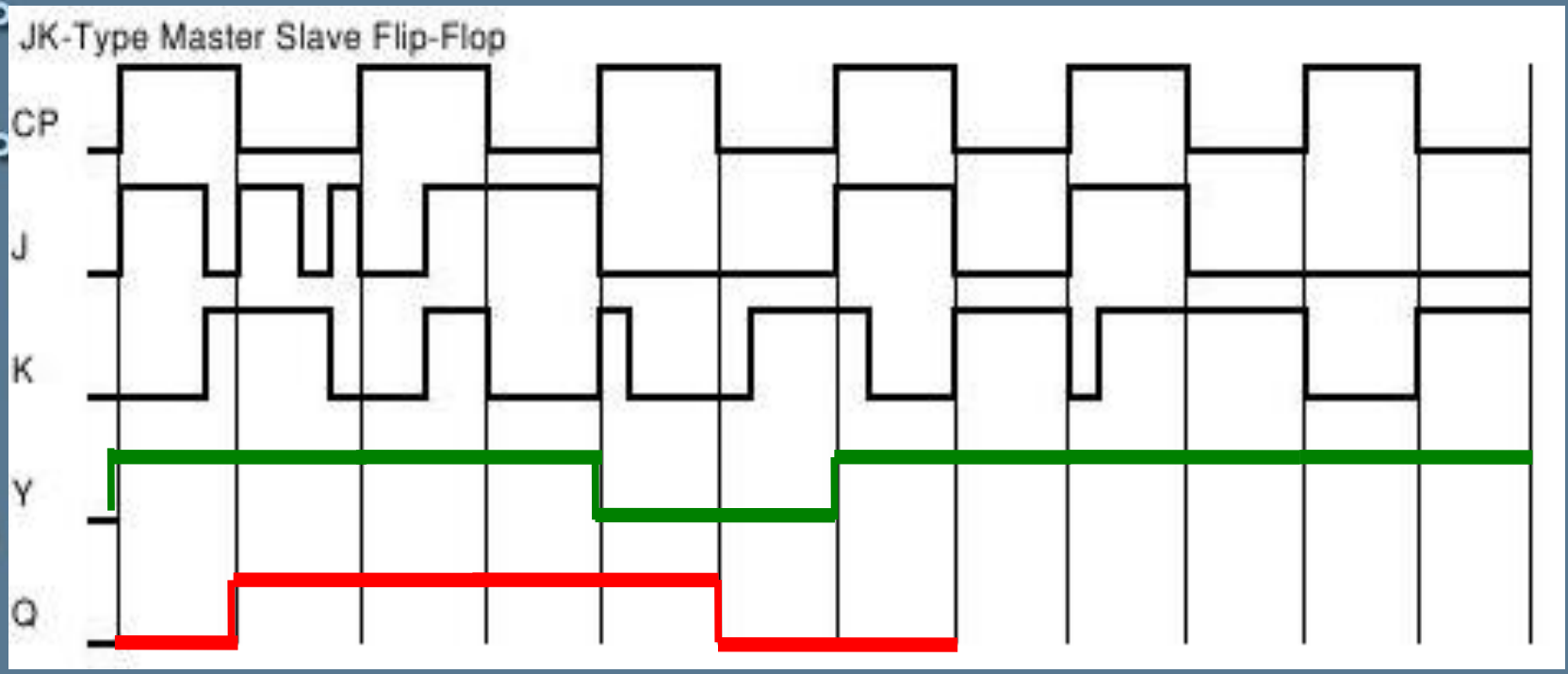
Examples



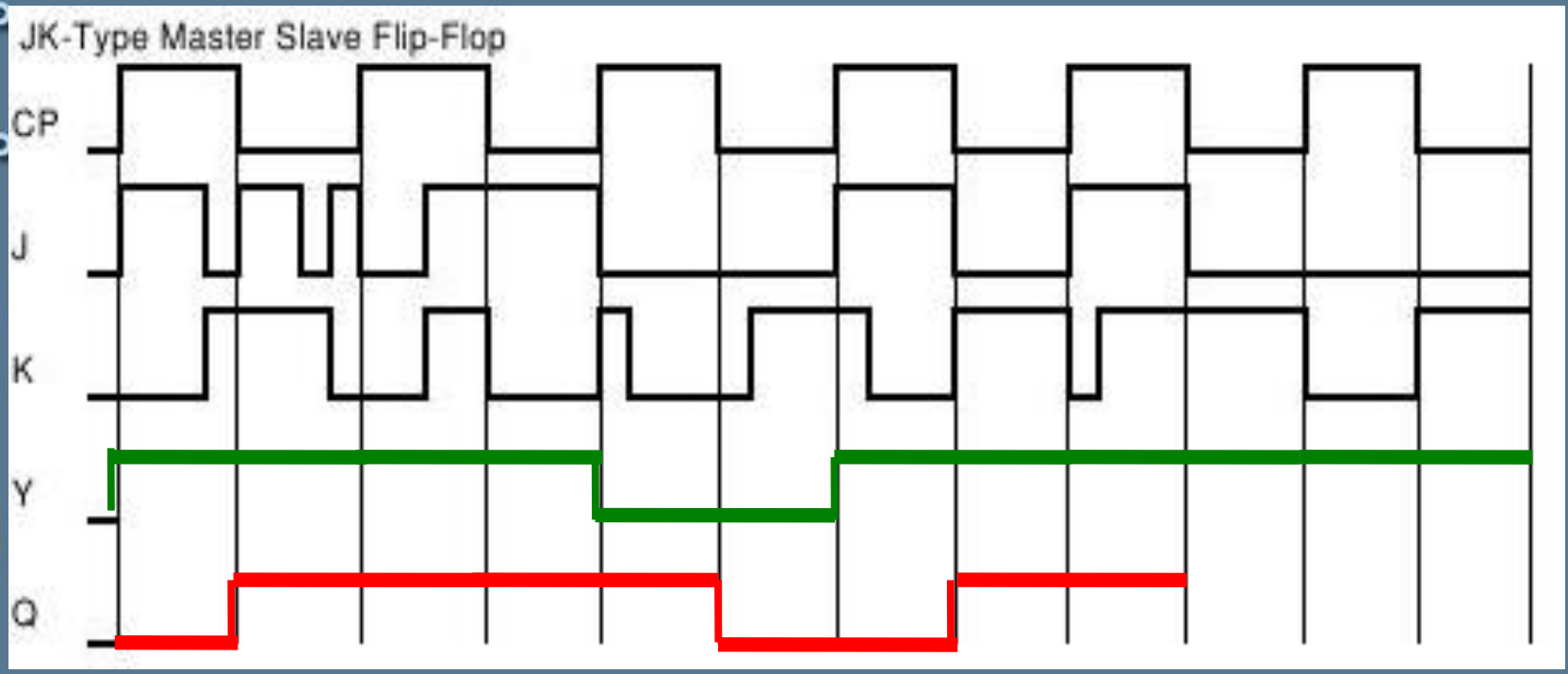
Examples



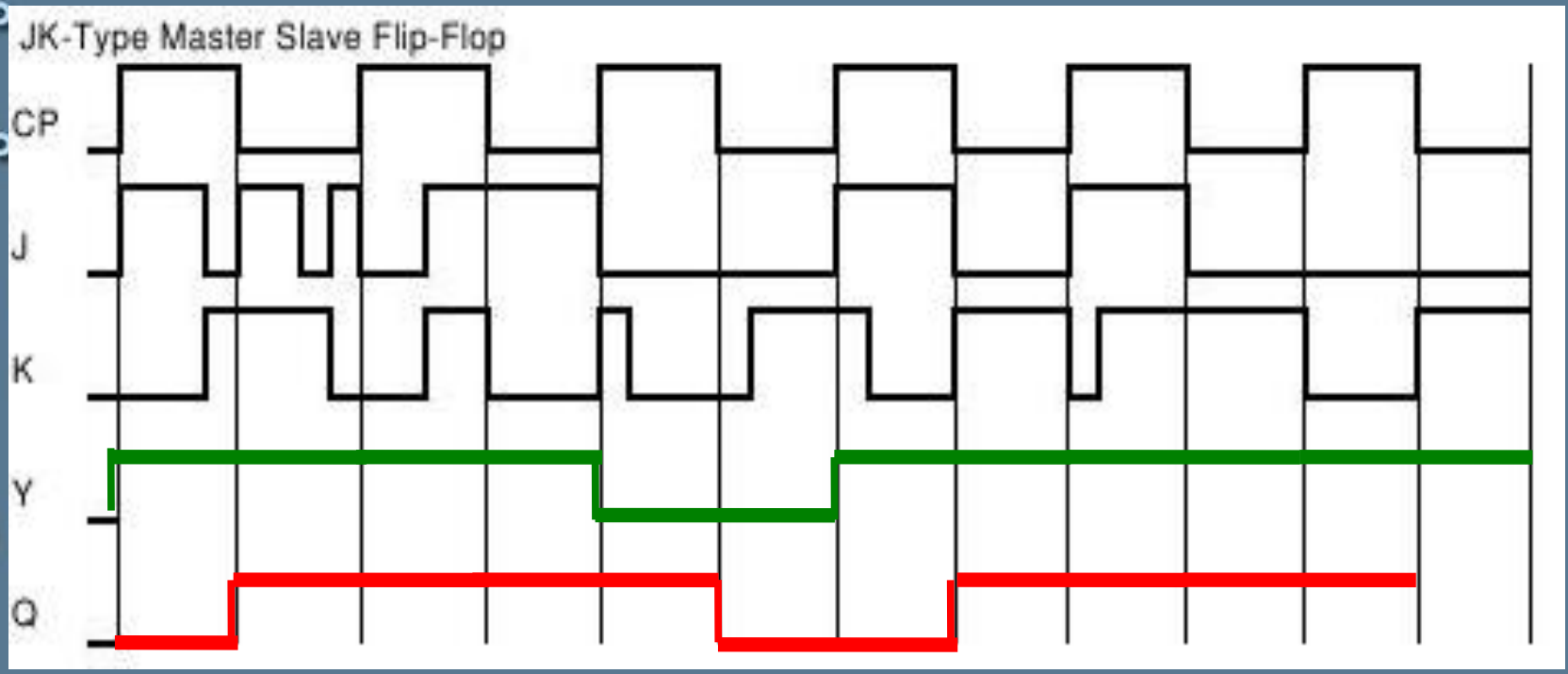
Examples



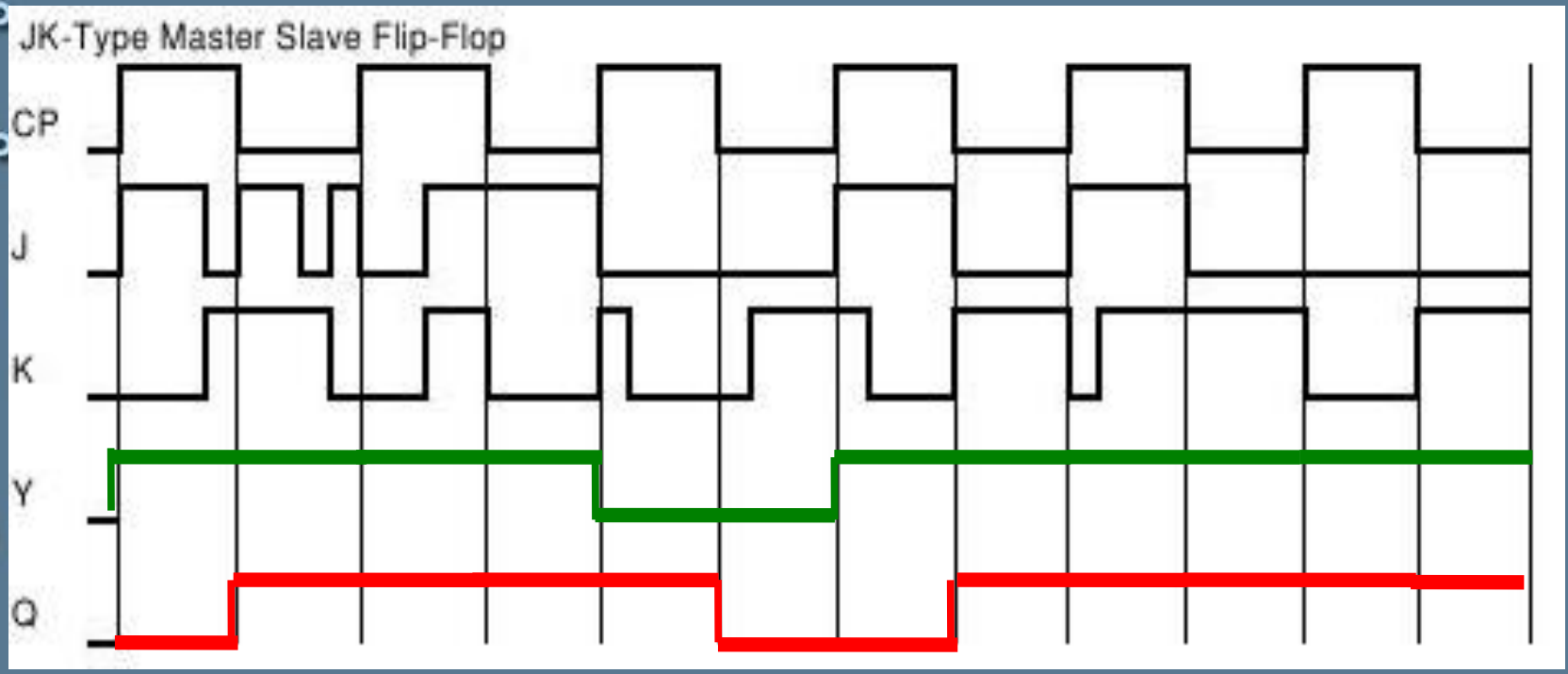
Examples



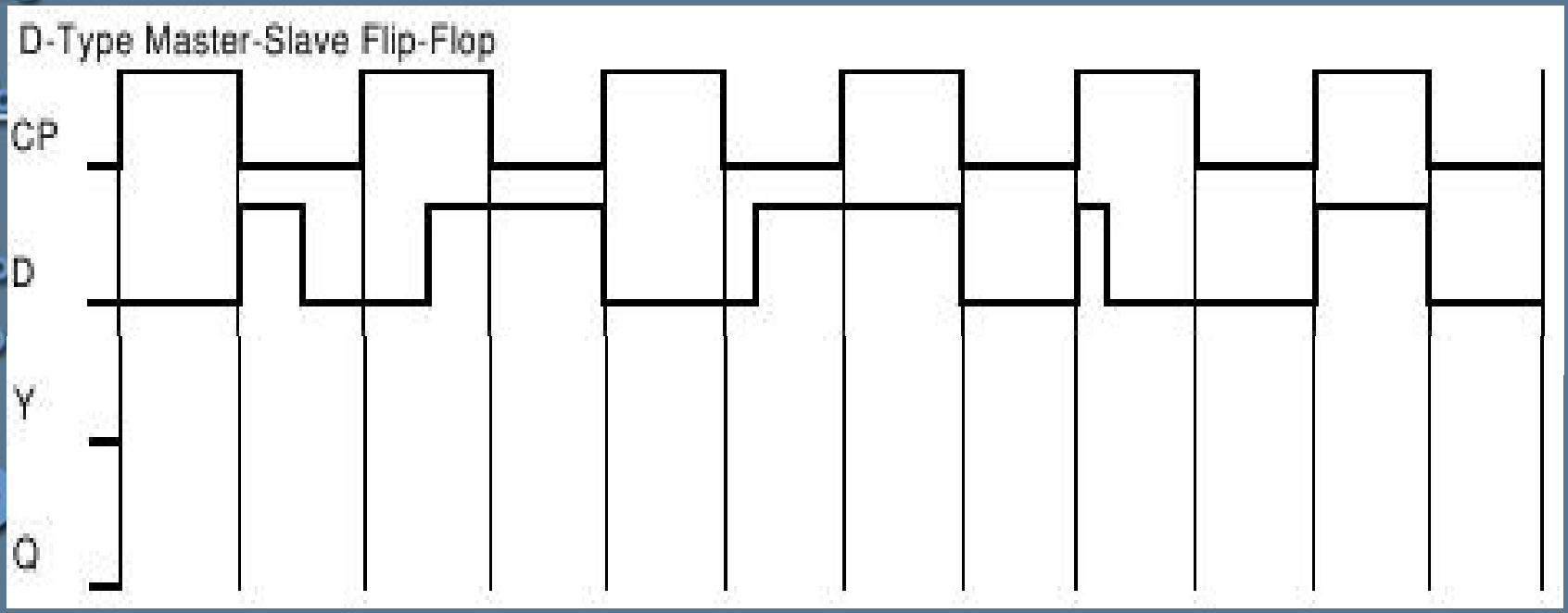
Examples



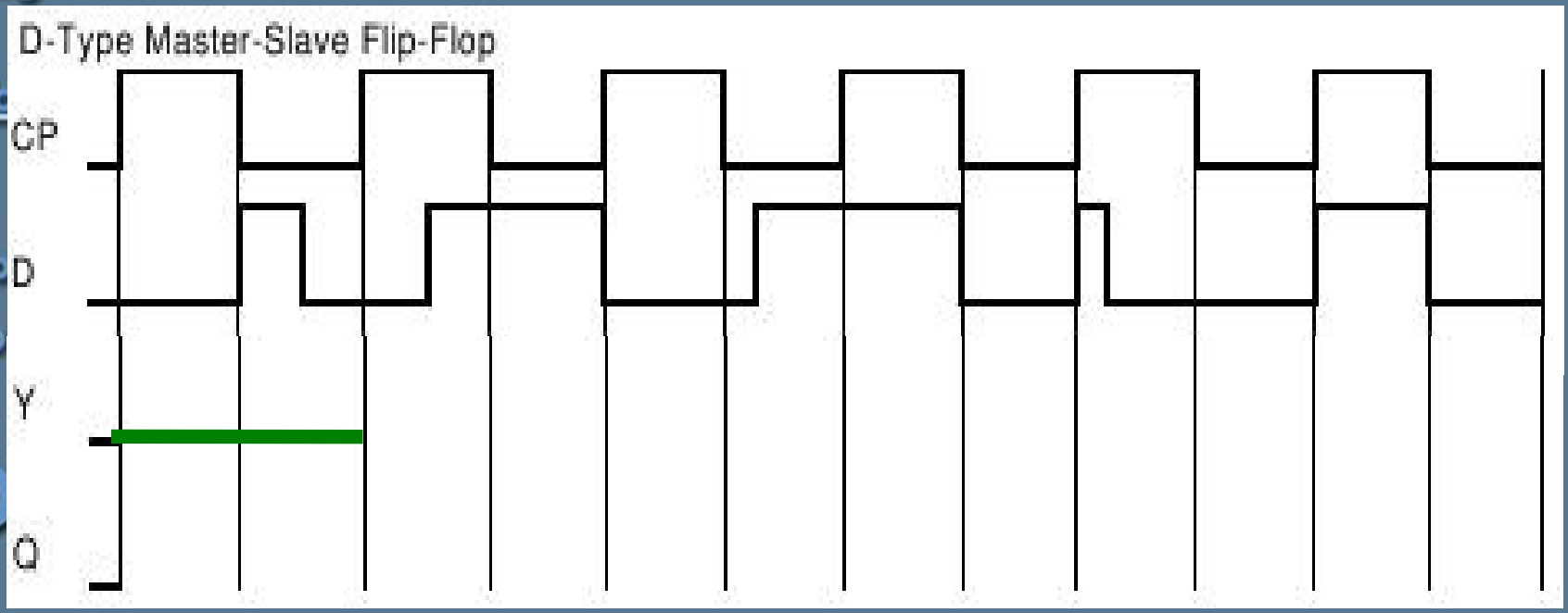
Examples



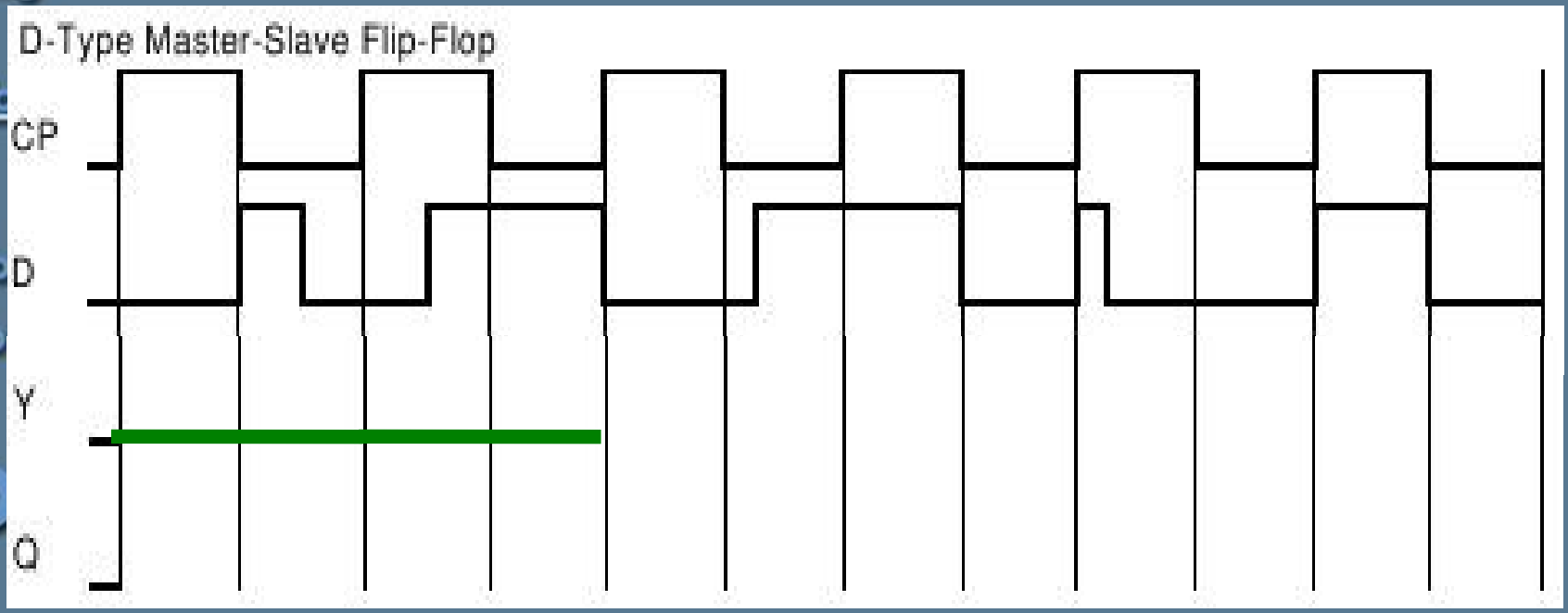
Examples



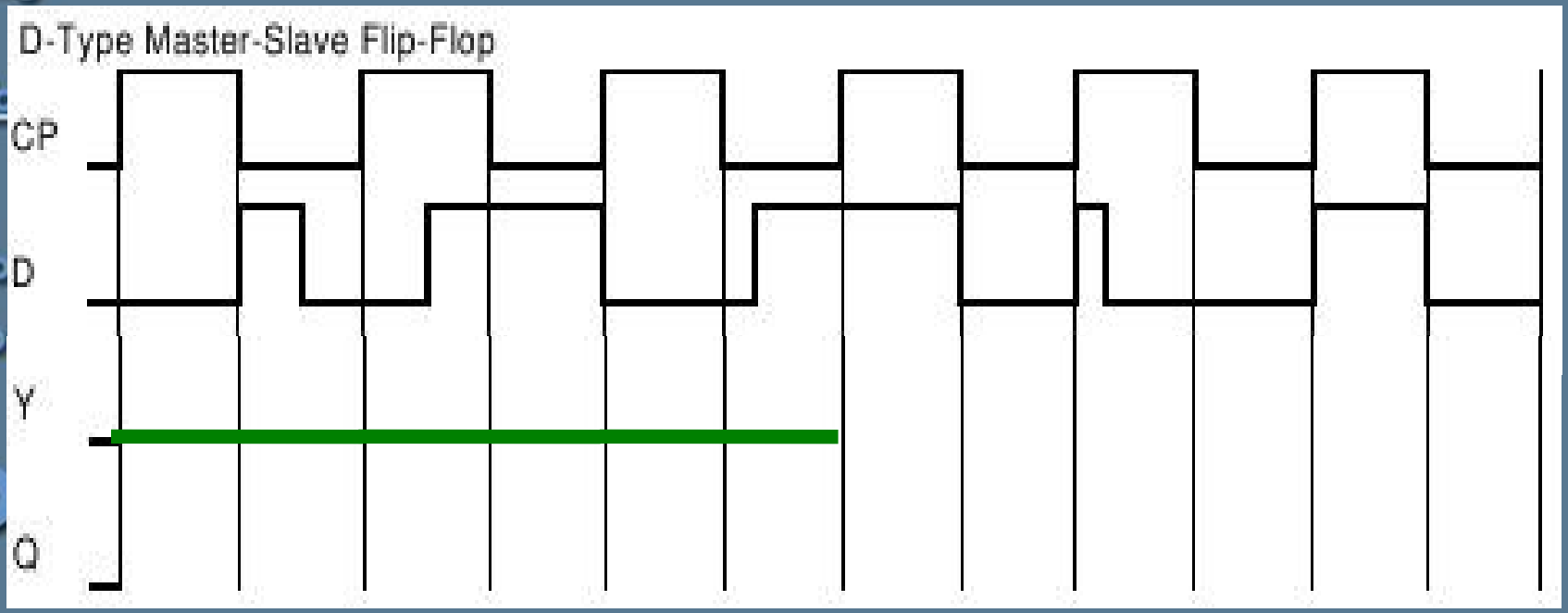
Examples



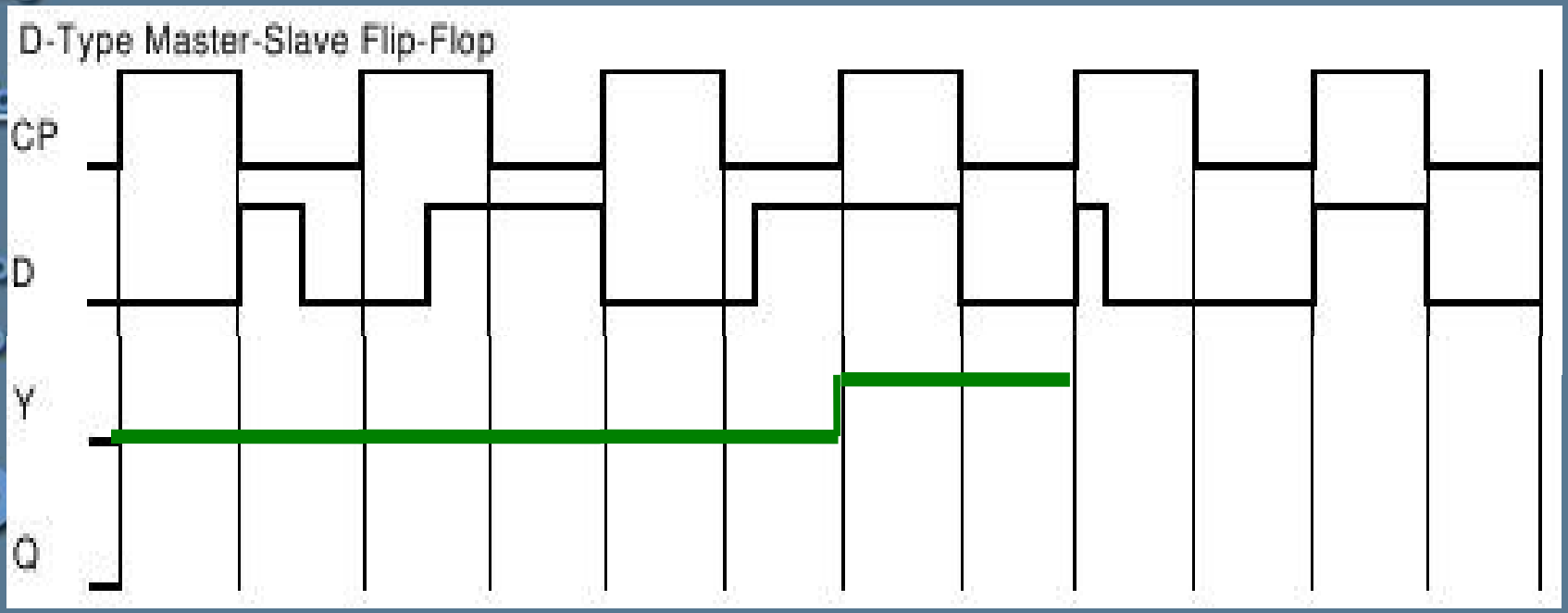
Examples



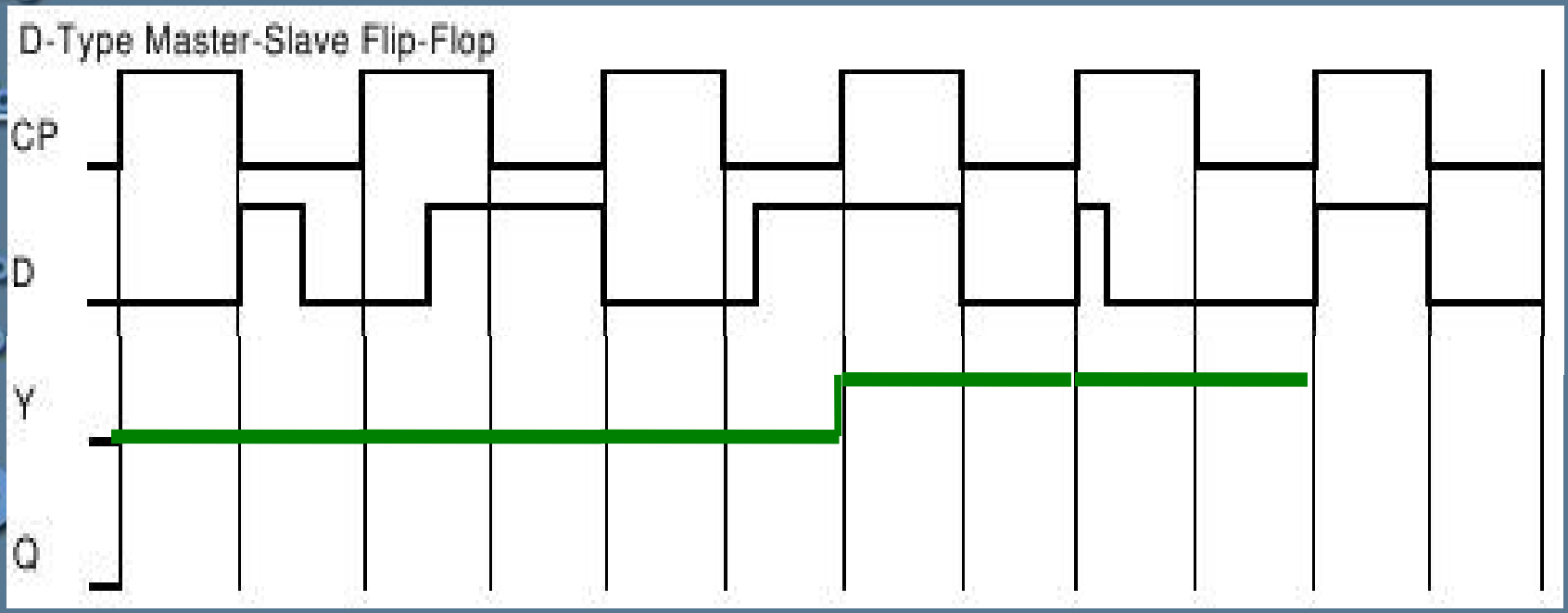
Examples



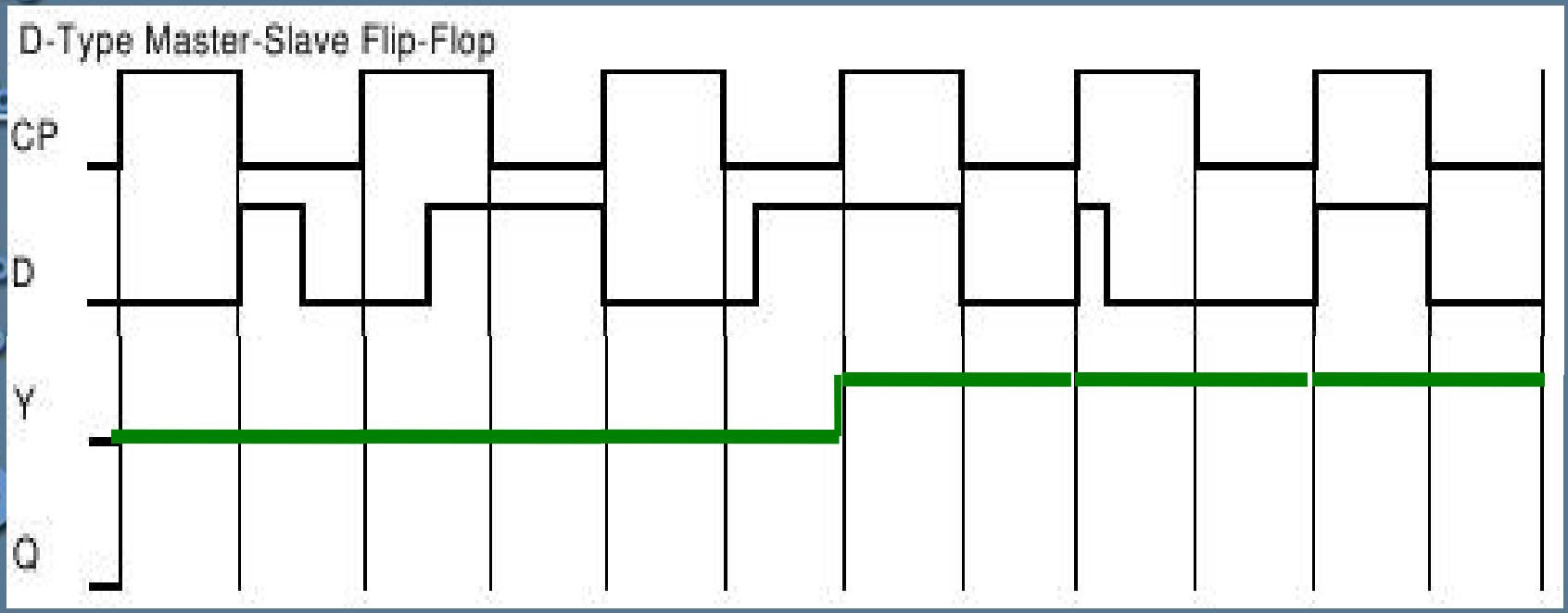
Examples



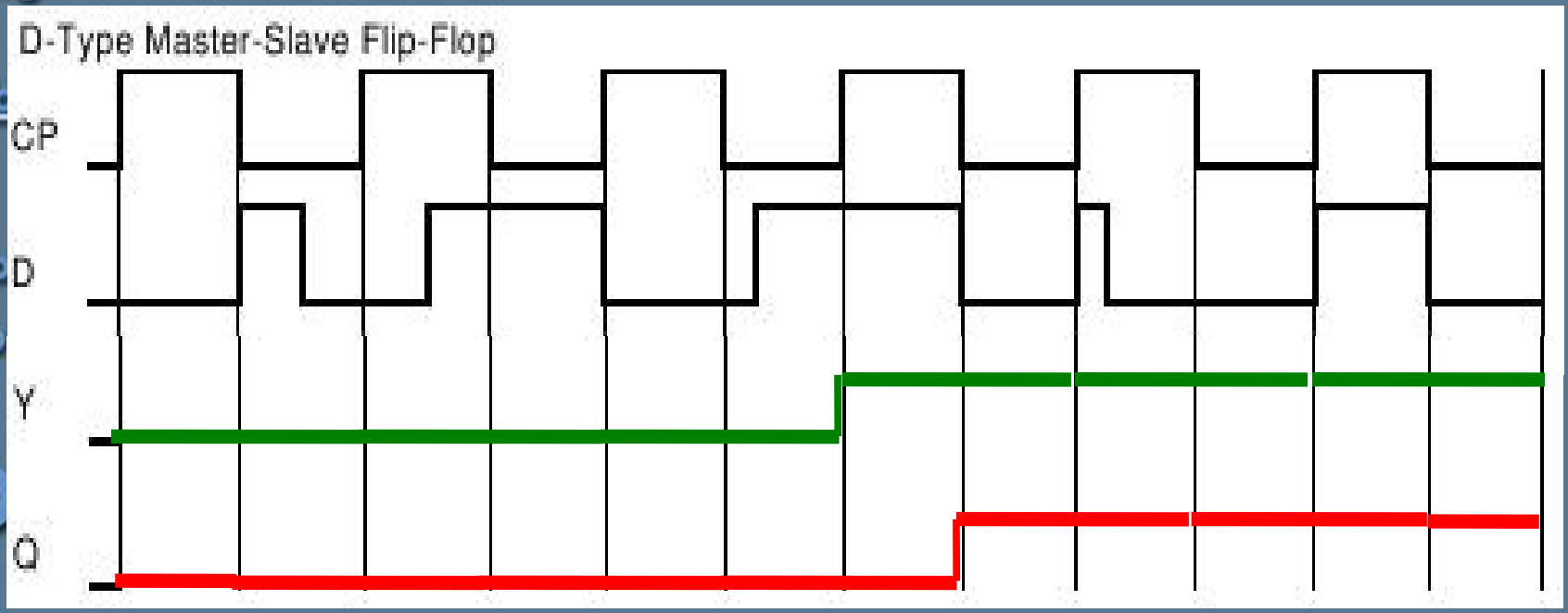
Examples



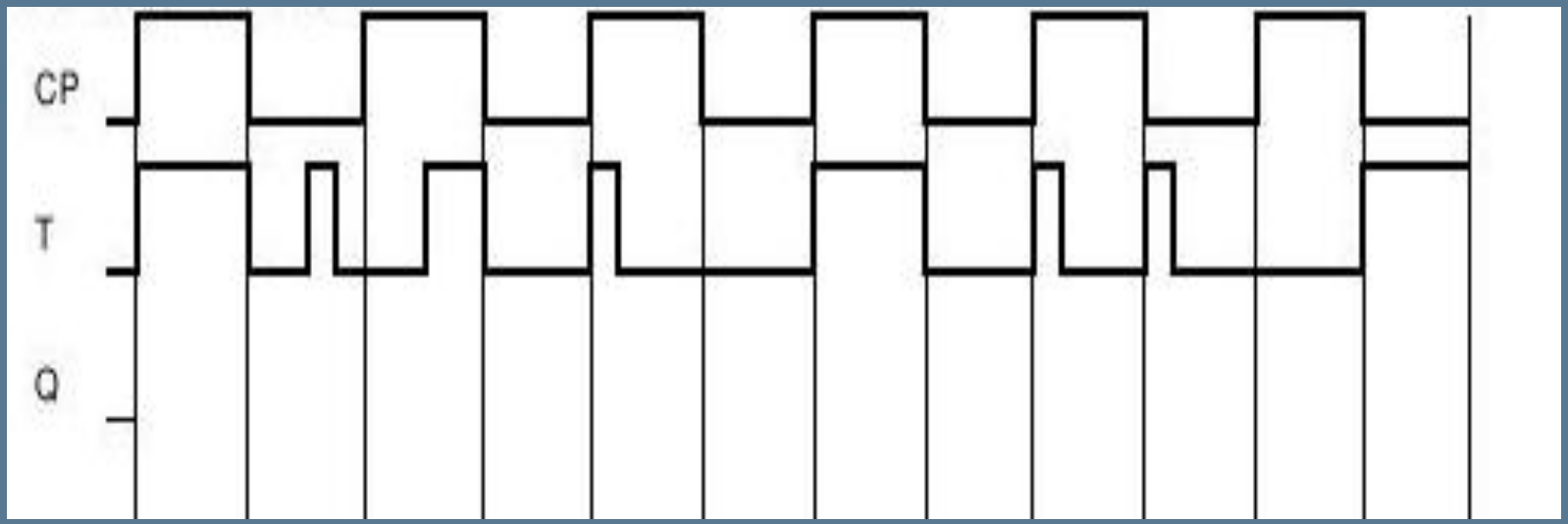
Examples



Examples



Quiz



How many times will the positive edge-triggered T flip flop change state from 0 to 1?