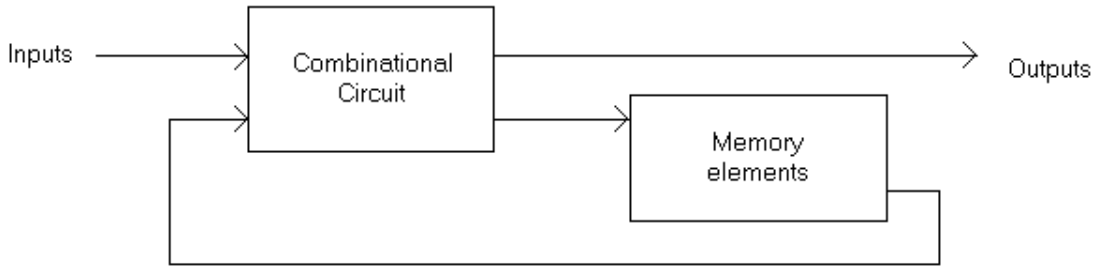
CMSC 130 – Logic Design and Digital Computer Circuits
Handout # 8: SYNCHRONOUS SEQUENTIAL LOGIC - FLIP-FLOPS



Block Diagram of a Sequential Circuit

Sequential circuit

- consists of a combinational circuit to which memory elements are connected to form a feedback path
- memory elements – store binary info which defines the *state* of the sequential circuit
- output – is determined by the external inputs and the present state
- next state of the memory elements – is a function of external inputs and the present state
- hence, a sequential circuit is a time sequence of inputs, outputs, and internal states
- *synchronous* – a system whose behavior can be defined from the knowledge of its signals at discrete instants of time
- *asynchronous* – depends upon the order in which its input signals change and can be affected at any instant of time

Synchronous Sequential Logic Systems

- *master-clock generator* – timing device used for synchronization; generates a periodic train of *clock pulses*
- memory elements are affected only upon the arrival of the synchronization pulse
- *clocked sequential circuits* – synchronous sequential circuits that use clock pulses in the inputs of memory elements

Flip-Flops

- memory elements used in clocked sequential circuits
- binary cells capable of storing one bit of info
- flip-flop circuits have two inputs, normal and complemented
- A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t+1)	Operation
0	0	Q(t)	no change
0	1	0	reset
1	0	1	set
1	1	Q'(t)	complement

SR Flip-Flop

S	R	Q(t+1)	Operation
0	0	Q(t)	no change
0	1	0	reset
1	0	1	set
1	1	?	indeterminate

D Flip-Flop (Data)

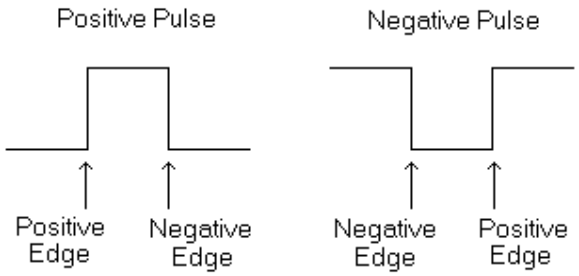
D	Q(t+1)	Operation
0	0	reset
1	1	set

T Flip-Flop (Toggle)

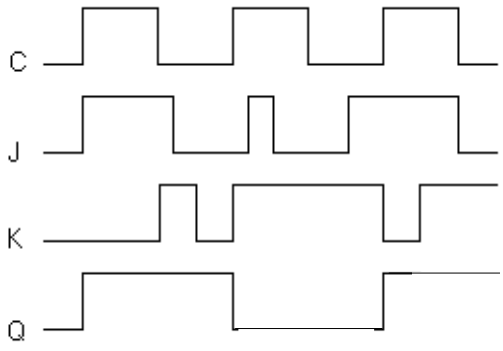
T	Q(t+1)	Operation
0	Q(t)	no change
1	Q'(t)	complement

Triggering of Flip-Flops

- *trigger* – a momentary change in the input signal which switches the state of a flip-flop
- *clock pulse* – triggers clocked flip-flops; starts from an initial value of 0, goes momentarily to 1, and after a short time, returns to its initial 0 value; may be positive or negative
- *positive clock pulse* – remains at 0 during the interval between pulses and goes to 1 during the occurrence of a pulse
- the clock pulse goes through two signal transitions: from 0 to 1 and the return from 1 to 0
- positive transition is defined as the *positive edge*, negative transition as the *negative edge*



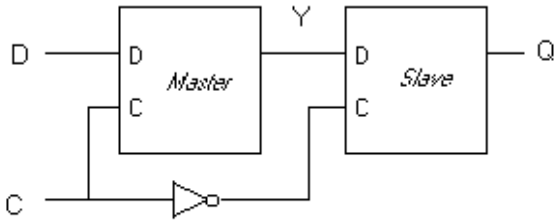
Definition of clock-pulse transition



Timing Diagram of a JK Flip-Flop

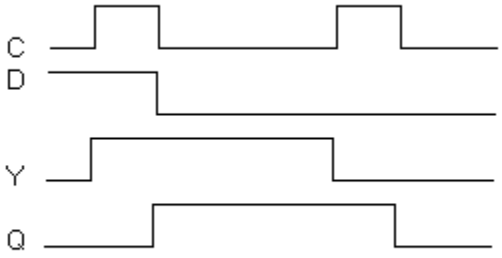
Master-Slave Flip-Flop

- consists of two latches (master and slave) and an inverter



Master-Slave D Flip-Flop

- when the clock pulse input C is 0, the output of the slave latch is enabled and its output Q is equal to the master output Y, master latch is disabled (its C input = 0)
- when the input pulse changes to the logic-1 level, the data in the external D input is transferred to the master
- the slave is disabled as long as the pulse remains in the 1 level (its C input = 1)
- any changes in the external D input changes the master output Y but cannot affect the slave output Q
- when the pulse returns to 0, the master is disabled and is isolated from the D input
- at the same time, the slave is enabled and the value of Y is transferred to the output of the flip-flop at Q



Timing Relationship with a Master-Slave Flip-Flop