Pulsed E-/D-Mode Switchable GaN HEMTs With a Ferroelectric AlScN Gate Dielectric

Jeong Yong Yang, Seung Yoon Oh, Min Jae Yeom, Seokgi Kim, Gyuhyung Lee, Kyusang Lee, Sungkyu Kim, and Geonwook Yoo

***Abstract*— In this study, we demonstrate ferroelectric GaN high-electron mobility transistors (HEMTs) with a sputtered AlScN gate dielectric, exhibiting a large memory window of ~ 14.6 V and a high on/off ratio of ~ 10^8. The strong polarization of AlScN layer contributes to the remarkably large threshold voltage (V_{th}) tuning range with counterclockwise hysteresis depending on voltage sweep ranges and pulsed parameters. Moreover, a recessed-gate structure enables the pulsed enhancement and depletion mode switching. The reconfigurable V_{th} via pulse modulation further allows feasibility of NOR logic gate with the single ferroelectric GaN HEMT.**

***Index Terms*— GaN-HEMT, AlScN, ferroelectric, reconfigurable.**

I. Introduction

GALLIUM-NITRIDE (GaN) high-electron-mobility transistors (HEMTs) have been extensively investigated for use in high-frequency and power applications owing to its high electron mobility and wide bandgap [1], [2], [3]. Recent GaN-based CMOS circuits are promising toward energy efficient and high-density integration toward all GaN-based integrated circuits and systems [4]. However, the thick GaN layer and short-channel effect of GaN HEMTs have restricted the possibility of GaN channel scaling [5], [6]. Thus, a reconfigurable GaN HEMT has emerged as an alternative device structure to impart high functionality [7], [8], [9], [10], [11]. In particular, ferroelectric GaN HEMTs using BTO, PZT, and HZO have been proposed toward normally off, dynamic threshold voltage (V_{th}) control, and negative-capacitance transistors to foster GaN-based reconfigurable and emerging devices [7], [10], [12], [13], [14].

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So far, the V_{th} modulation in both negative (depletion mode; D-mode) and positive (enhancement mode; E-mode) with a broad tunable range has not been demonstrated due to the strong polarization of AlGaN layer [7], [8], [10], [13]. Therefore, a proper HEMT structure with a suitable ferroelectric film is of significant interest. Recently, AlScN has attracted great attentions as a promising ferroelectric film with a large ferroelectric polarization and coercive field [15], [16]. Notably, GaN HEMTs with the ferroelectric AlScN gate stack are reported to exhibit tunable V_{th}, and the epitaxially grown AlScN on GaN can be a promising barrier layer to further enhance radio frequency performance [9], [17], [18], [19].

In this study, we report ferroelectric GaN HEMTs with an AlScN/Al_2O_3 gate stack on the recessed-gate structure. Thanks to the large remanent polarization and square-like voltage-polarization characteristics of AlScN, as well as the recessed-gate structure, we were able to achieve a large ΔV (~ 14.6 V) and a high on/off ratio (~ 10^8) by effectively suppressing the depolarization effect. An obvious counterclockwise hysteresis and normally off characteristic were observed. The dependency of ΔV was examined *via* variable gate voltage sweep ranges and pulse parameters in order to substantiate reconfigurable V_{th} behaviors. Finally, a NOR logic gate was demonstrated with the single ferroelectric GaN HEMT *via* a combination of two distinct input gate pulses and corresponding output currents.

II. Device Fabrication and Measurement

An epitaxial layer of AlGaN/GaN HEMTs consisting of 1 nm AlN, 25 nm $Al_{0.26}Ga_{0.74}N$, and a 3 nm GaN capping layer were grown through MOCVD. The fabrication was initiated with mesa isolation and gate recess etching using inductively coupled plasma (ICP) etching. Next, an ohmic contact source/drain metal stack of Ti/Al/Ni/Au (25/140/40/50 nm) was deposited via e-beam evaporation, followed by rapid thermal annealing at 870 °C for 30 s under N_2 atmosphere. The insulator Al_2O_3 (4 nm) was deposited *via* atomic layer deposition using trimethylaluminum and ozone precursors at a stage temperature of 450 °C. Subsequently, $Al_{0.72}Sc_{0.28}N$ (40 nm) was deposited *via* a reactive RF-magnetron sputtering system utilizing an $Al_{0.57}Sc_{0.43}$ single alloy target with Ar/N_2 mixed gas. Then, 30 W power was applied to the $Al_{0.57}Sc_{0.43}$ target at a working pressure of 2.5 mTorr and a stage temperature of 350 °C without post-annealing. Then contact vias were opened by ICP etching. Finally, a gate electrode of Ni/Au (50/100 nm) was formed. An additional metal-ferroelectric-metal (MFM) capacitor of Ti/Pt/AlScN/Ni (5/50/40/50 nm) was fabricated on the highly

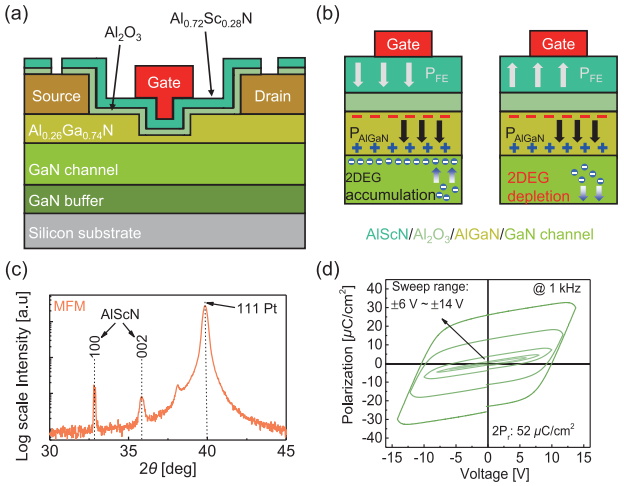

Fig. 1. Cross-sectional schematics of (a) fabricated device and (b) operation mechanism for elucidating accumulation and depletion states including P_{FE} and polarization of AlGaN (P_{AlGaN}). (c) XRD 2θ scan plot for peak value vs intensity measured on the AlScN film. (d) P-V hysteresis curves of an MFM capacitor measured for incremental bias sweep range at 1 kHz.

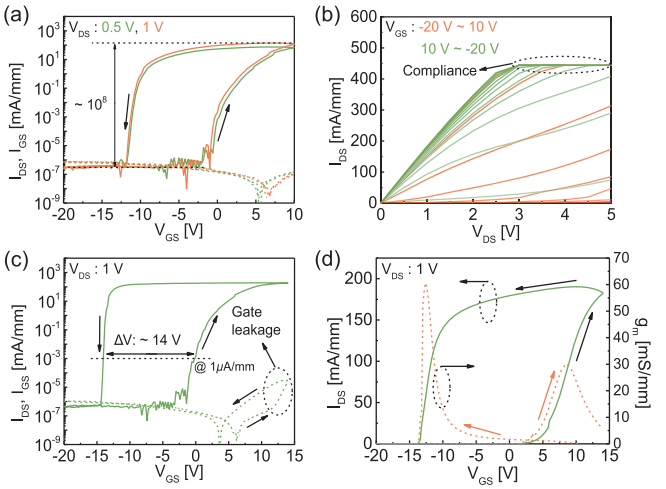

Fig. 2. (a) Bi-directional I_{DS}, I_{GS} vs V_{GS} curves at V_{DS} = 0.5, 1 V. (b) Output characteristics of forward and reverse sequential sweeps of V_{GS}. (c) The bi-directional I_{DS}, I_{GS} vs V_{GS} curve for an increased wide sweep range, and (d) its linear scale with transconductance (g_m).

doped silicon to characterize ferroelectricity of the AlScN film which was deposited on the same condition for the HEMTs.

The depth profile was verified using atomic force microscopy (NX-10/Park system). An XRD (SmartLab/ Rigaku) 2θ scan was utilized to certify the crystalline peaks of AlScN, Pt, and Si on the MFM. A ferroelectric tester (RT66C/Radiant) was used to examine the ferroelectricity of AlScN. All electrical measurements were conducted using a parameter analyzer with a preamp (Keithely-4200A-SCS), and a pulse measurement was pursued via PMU-4225 with an amplifier unit.

III. Results And Discussion

Fig. 1(a) illustrates a cross-section of the AlScN/GaN HEMT. The channel width and length are 225 and 6 μm, respectively. The recess depth was measured to be about 13 nm. The P_{FE} was examined *via* polarization-voltage (P-V) hysteresis loop measurements by applying a triangular pulse to the MFM capacitor. The origin of ferroelectricity in AlScN is predominantly tied to the crystallization of AlScN along the c-axis (002 peaks in XRD) [15]. Thus, an XRD 2θ scan was employed to confirm the 002 peak in the MFM, as shown in Fig. 1(c), and both (100) and (002) peaks were confirmed.

Fig. 1(d) shows the measured P-V curves by applying a triangular pulse with a pre-set pulse. The square-like P-V curve shows that the polarization increases according to the sweep range [20]. In particular, the P-V curves exhibited a large remanent polarization (P_r) of 26 μC/cm^2 measured under 1 kHz with a sweeping range of -14 V to 14 V.

Fig. 2(a) shows the bi-directional drain current (I_{DS}), gate leakage current (I_{GS}) vs. applied gate voltage (V_{GS}) at drain voltages (V_{DS}) of = 0.5, 1 V. Furthermore, low and stable I_{GS} are maintained within the sweep range because the Al_2O_3 layer prevents carrier flow between the AlScN and AlGaN layers [17]. Therefore, a high on/off ratio ($\sim 10^8$) was achieved. The subthreshold slopes (SS) were extracted using the equation $SS = \partial\partial V_{GS}/\partial\partial \log(I_{DS})$. To provide an accurate comparison of the SS characteristics, we calculated the average SS values of 318 and 216 mV/dec for forward and reverse sweeps, respectively. These values were obtained for two orders magnitude of a drain current range from 2×10^{-5} mA/mm to 2×10^{-3} mA/mm. Broad SS during forward sweep can be attributed to capacitance mismatching stemming from the thick polycrystalline AlScN film ($\sim$ 40 nm) [21], [22], [23], [24]. And the broad SS induces large subthreshold leakage current and requires large on/off switching voltage range. One approach to address this problem is to decrease the thickness of the AlScN film for reducing the coercive voltage of AlScN; another approach is to engineer a fully recessed structure for manipulating the operating gate voltage range of the device. The output curves were measured for forward (V_{GS} from -20 V to 10 V) and reverse (V_{GS} from 10 V to -20 V) sweep sequences, as shown in Fig. 2(b). The output currents of the device exhibit a discrepancy between the forward sweep (V_{GS} ranging from -20 V to 10 V) and the reverse sweep (V_{GS} ranging from 10 V to -20 V) because the large remanent polarization in AlScN maintained the accumulation/depletion of two-dimensional electron gas (2DEG) until a sufficient gate voltage is applied.

Fig. 2(c) shows the bi-directional I_{DS} vs. V_{GS} curve with the sweep range up to 14 V, and ΔV of 14.6 V is observed attributed to the large P_r of AlScN dielectric. As V_{GS} exceeds 10 V, meanwhile, I_{GS} significantly increases due to the tunneling of carriers from the 2DEG to the gate electrode through AlScN/Al_2O_3 [25]. Fig. 2(d) presents transfer curves in a linear scale with the transconductance (g_m) curves. A large tunable V_{th} for the forward and reverse sweeps is clearly observed with two distinct peaks for g_m. Moreover, a positive V_{th} of 5.6 V was extracted at the forward sweep due to the preeminent ferroelectricity of AlScN.

The dependency of ΔV on V_{GS} sweep ranges is studied by modulating the start (V_{start}) and end (V_{end}) of V_{GS}. Fig. 3(a) shows the observed negative V_{th} shift which are attributed to the increment of downward polled P_{FE} sustaining more accumulation of 2DEG. Likewise, Fig. 3(b) presents positive V_{th} shifts from the forward sweep for decreasing V_{start} which are induced by the increasing of upward polled

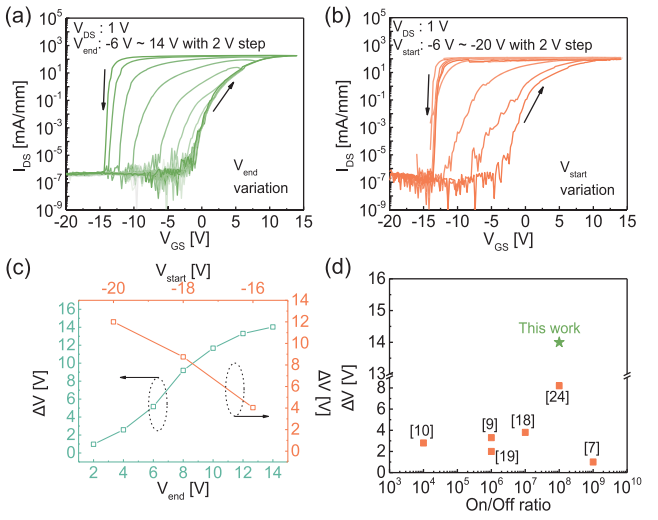

Fig. 3. Bi-directional I_{DS} vs V_{GS} curves for variable (a) V_{end} and (b) V_{start}. (c) Calculated ΔV for V_{end} and V_{start} show similar dependency on the V_{end} and V_{start} ranges, respectively. (d) Benchmarking of ferroelectric GaN HEMTs by comparing ΔV and an on/off ratio.

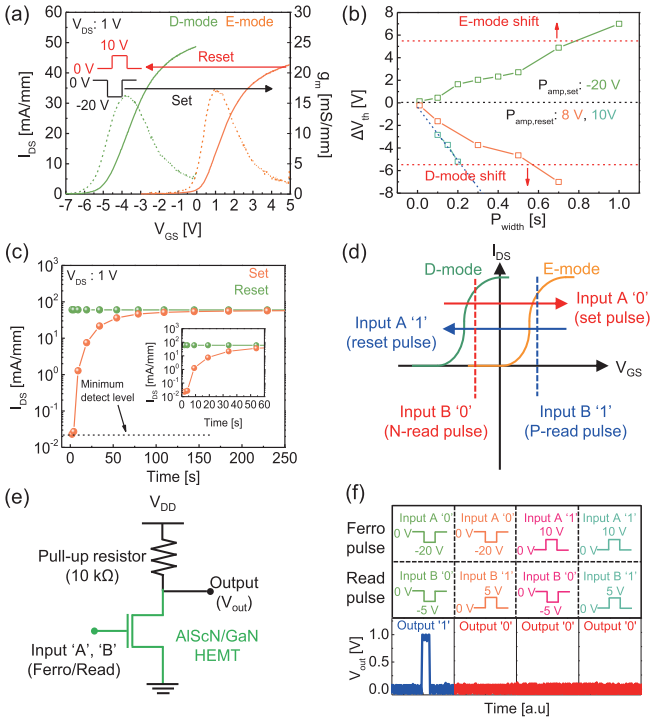

Fig. 4. (a) Pulse modulation of D-mode and E-mode operation after applying set and reset pulses. (b) V_{th} modulation (ΔV_{th}) vs. P_{width} plots for various $P_{amp,set}$ and $P_{amp,reset}$. (c) Retention time plot. (d) Pulse schemes illustrating NOR logic gate operation with input and read pulses. (e) The circuit diagram of AlScN/GaN HEMT connected with a pull-up resistor. (f) A truth table for NOR Boolean algebra. The input pulse schemes are also represented.

P_{FE} maintaining the depletion of 2DEG. The dependencies of ΔV on V_{end} and V_{start} are summarized in Fig. 3(c). It is to be noted that each V_{th} is extracted using the constant current method at $I_{DS} = 1$ μA/mm for simplicity. Then ΔV is determined to be the difference between the forward and reverse sweeps. A significant large ΔV of $\sim$ 14.6 V with an on/off ratio of $\sim 10^8$ is achieved in the proposed GaN HEMT as benchmarked in Fig. 3(d) [24].

The depletion and accumulation of 2DEG in the fabricated device can be directly controlled by programming P_{FE}, and thus reconfigurable V_{th} characteristics can be achieved as shown in Fig. 4(a). After being applied by an initialization pulse, a D-mode transfer curve was measured. Subsequently, a set pulse with an amplitude (P_{amp}) of -20 V and a width (P_{width}) of 1 s was applied to switch the operation mode. After measuring an E-mode transfer curve, restoration of V_{th} to the D-mode by applying a reset pulse ($P_{amp} = 10$ V, $P_{width} = 200$ ms) was verified. To select the appropriate P_{with} and P_{amp} for V_{th} modulation, the pulse amplitudes for the set ($P_{amp,set}$) and reset ($P_{amp,reset}$) were examined for various P_{width}, as shown in Fig. 4(b). Each red line indicates the minimum ΔV_{th} for the operation mode switch, and ΔV_{th} of 5.5 V is found to be sufficient. Although $P_{amp,reset} = 8$ V with $P_{width,reset} = 500$ ms can induces a mode switching, $P_{amp,reset} = 10$ V with $P_{width} = 200$ ms is chosen for the faster reset operation. $P_{amp,reset}$ of higher than 10 V is not considered to suppress gate leakage and prevent device degradation [26]. Fig. 4(c) shows the retention behavior of the AlScN/GaN HEMT measured at $V_{GS} = -5$ V. The set operation ($P_{amp} = -20$ V, $P_{width} = 1$ s) and reset operation ($P_{amp} = 10$ V, $P_{width} = 1$ s) indicate that the retention time for the set operation cannot exceed 60 s due to the depolarization field generated by the residual AlGaN barrier layer ($\sim$ 13 nm). However, a retention behavior of 60 s is feasible for reconfigurable logic operation as the previous input state only needs to be maintained during computation with the subsequent sequential input pulse within the latency. Based on the pulsed V_{th} reconfiguration, the NOR logic gate operation with a single ferroelectric GaN HEMT was examined. Fig. 4(d) depicts the scheme of the NOR gate operation, where the two independent inputs are ferro (set and reset for E-/D- mode shift) and read (N-read and P-read) pulse signals. The input pulse for ferroelectric switching and read voltage is defined as input A and B, respectively [27]. Moreover, the pull-up resistor (10 kΩ) is connected with AlScN/GaN HEMT to obtain an output voltage signal for NOR gate logic operation as shown in Fig. 4(e). Owing to the pulsed E-/D-mode switching, the combination of two input signals and the corresponding output voltage (V_{out}) shows a NOR gate Boolean algebra. Fig. 4(f) shows the truth table of the NOR gate representing two input signals with an illustration of each state pulse scheme and the measured output signal.

IV. Conclusion

To summarize, the AlScN/GaN HEMT exhibited a large ΔV ($\sim$ 14.6 V) and high on/off ratio ($\sim 10^8$) after implementing an AlScN ferroelectric dielectric on the gate recessed structure. The strong polarization of AlScN and the recess etching process of the AlGaN barrier layer could successfully suppress the depolarization effect as well as confirm the normally off behavior. The evident dependency of ΔV on V_{end} and V_{start} is verified, proving that the P_{FE} of AlScN amply induces the accumulation and depletion of 2DEG. The switching of the operation modes (D-mode and E-mode) is substantiated by applying a pulse, and adequate pulse parameters are determined. Finally, NOR gate Boolean algebra is successfully demonstrated with two distinct input pulses and a corresponding output current.

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