Ferroelectric Transistor Model based on Self-Consistent Solution of 2D Poisson's, Non-Equilibrium Green's Function and Multi-Domain Landau Khalatnikov Equations

A. K. Saha[1], P. Sharma[2], I. Dabo[1], S. Datta[2] and S. K. Gupta[1]
[1]Penn State University, University Park PA, USA, [2]University of Notre Dame, South Bend, IN, USA, email: aks54@psu.edu

***Abstract*—**We present a physics-based model for ferroelectric/negative capacitance transistors (FEFETs/ NCFETs) without an inter-layer metal between ferroelectric and dielectric in the gate stack. The model self-consistently solves 2D Poisson's equation, non-equilibrium Green's function (NEGF) based charge and transport equations, and multi-domain Landau Khalatnikov (LK) equations with the domain interaction term. The proposed simulation framework captures the variation of ferroelectric (FE) polarization (*P*) along the gate length due to non-uniform electric field (*E*) along the channel. To calibrate the LK equations, we fabricate and characterize 10nm HZO films. Based on the calibrated model, we analyze the gate/drain voltage dependence of *P* distribution in the FE and its effect on the channel potential and current-voltage characteristics. Our results highlight the importance of larger domain interaction to boost the benefits of FEFETs with subthreshold swing (SS) as small as ~50mV/decade achieved at room temperature. As domain interaction increases, the characteristics of FEFETs without inter-layer metal (SS, negative drain induced barrier lowering (DIBL), negative output conductance) approach those of FEFETs with inter-layer metal.

I. Introduction

FEFETs have garnered an immense interest in the recent past due to the possibilities of achieving sub-60mV/decade sub-threshold swing at room temperature [1]. Negative capacitance of the FE integrated in the gate stack of an FEFET interacts with the capacitance of the underlying transistor to yield steep switching. However, if the FE is fabricated directly on a dielectric layer (i.e. without an inter-layer metal [2]), the non-uniform electric field (*E*) in the channel makes the polarization (*P*) in FE variable along the gate length. Many models of FEFETs [3-5] assume uniform *P* and therefore, are mostly valid for FEFETs with an inter-layer metal which screens the effect of non-uniform channel potential from FE. However, for FEFETs without the metal, it is essential to capture the interactions of the multi-domain FE with the non-uniform *E* in the underlying channel. *To that effect, we present a model based on 2D Poisson's, NEGF and multi-domain LK equations, all of which are solved self-consistently with each other. We describe important effects of P variation in FE along the gate length on the characteristics of FEFETs.*

II. FEFET Model

The proposed model numerically and self-consistently solves 2D Poisson's equation with multi-domain LK equation in the FE layers and 2D NEGF equations in silicon following the mode space approach [6]. The simulation flow and the double gate FEFET device structure used for the simulation are shown in Fig. 1. We have considered the ferroelectric thickness (T_{FE}) of 1 nm (unless otherwise stated) on top of 0.5nm SiO_2. Following the discussion in [7], the LK equation is solved along T_{FE} (*y*-direction) i.e. the *y*-component of *P* (P_y) is related to E_y through the LK equation; whereas in the *x*-direction, P_x component is dependent on E_x through $P_x = \epsilon_0 \chi_x E_x$ (where χ_x=21). In our further discussion, the use of 'polarization' term represents the *y*-component of *P*. We have made a reasonable assumption that P_y in FE does not vary significantly along its thickness (*y* direction) as T_{FE} is small. However, along the gate length (*x* direction), proper multi-domain behavior is captured through the domain interaction term in the LK equation (see Fig. 1). It is important to note that, same Landau coefficients (α, β, γ) are used for each grid point of FE layer. Therefore, variation in P_y along the gate length is due to the electric field distribution along the channel coupled with the polarization interactions between different grid points in FE captured by setting domain interaction coefficient (K_P) > 0. The multi-domain LK equation is solved iteratively with the 2D Poisson's equation to capture the non-linear dependence of P_y in the FE region on E_y as well as variation of polarization along the gate length ($P_y(x)$) self-consistently with the potential profile (ϕ) of the entire device. At the same time, self-consistent solution between Poisson's equation and NEGF equation ensures the consistency between charge distribution (ρ) and potential profile (ϕ). After achieving three-fold self-consistency for ρ, ϕ and *P*, ballistic NEGF transport equations are used to obtain the current. It is important to note that the assumption of ballistic transport does not significantly change the interaction of the multi-domain FE with the underlying channel. Therefore, the trends presented subsequently are not limited to ballistic NEGF model, but are generally valid.

III. Experimental Characterization of HZO and Model Calibration

To extract the Landau coefficient (α, β and γ) of HZO we fabricate metal-ferroelectric-insulator (SiO_2)-Si (MFIS) capacitor, where Si is highly doped. The MFIS capacitors are fabricated on highly doped p-type Si substrate (~10^{20} cm^{-3}). First, a 10 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film is grown by atomic layer deposition (ALD). A capping layer of 5 nm TiN is subsequently deposited by ALD. Next, the crystallization of HZO film is performed with rapid thermal process (RTP) in N_2 ambient at 500 ^{0}C for 30 s. Finally, the top electrode is patterned using lithography and subsequent etch. The TEM image of MFIS capacitor is shown in Fig.2 and the measured P-E curve and corresponding Landau coefficients are shown in Fig. 3.

IV. Device Analysis

A. FE Polarization Variation along the Gate Length

To analyze the effect of multi-domain FE behavior on FEFET characteristics, we show the variation of P_y along the

gate length for different gate/drain biases (V_{GS} and V_{DS} - Fig. 5) At V_{GS}=0, all FE domains exhibit negative P_y due to the negative E emanating from the source/drain (S/D) depletion regions. At V_{DS}=0.6V, P_y is more negative at the drain-end due to larger drain E-fields. As V_{GS} is increased, FE domains start to flip (negative-P to positive-P) from source-end of FE and create a domain wall. With further increase in V_{GS}, the domain wall shifts towards drain (Fig. 5(a)). If V_{DS} is decreased (Fig. 5(b)), the drain E-fields decrease and P_y on the drain end becomes less negative. At low V_{DS} (0-0.25V) and V_{GS} = 0.6V, all domains flip to positive P_y. In Fig. 6, we show the variation in P_y-E_y of FE with respect to the S-shaped L-K path (K_P=0). Increase in V_{GS} tends to pull the FE polarization towards more positive values. On the other hand, an increase in V_{DS} tends to increase the variability of P_y and E_y along the gate length. It is important to note that the difference between simulated P-E and the LK path is due to the domain interaction term ($0.5\times K_P\times d^2P_y/dx^2$). It is also interesting to observe that at V_{GS} = 0.6V and V_{DS} = 0.1V, the distribution of P_y significantly reduces (under the influence of high gate E-field). This reduces the contribution of $0.5\times K_P\times d^2P_y/dx^2$ and the simulated P-E points lie on the L-K path.

Next, we analyze the conduction band (CB) along the S/D (Fig. 7(a)). As discuss previously, at low V_{GS}, P_y is negative (Fig. 5(a)), which pulls up the CB compared to the standard FET. At high V_{DS}, P_y is larger than at low V_{DS}. Thus, CB is pulled further up as V_{DS} increases, leading to negative DIBL (Fig. 7(a)). At high V_{GS}, and low V_{DS} (=0.1V), all the FE domains have P_y >0 (Fig. 5(b)). This leads to negative E_y in the FE layer, which lowers the CB compared to standard. With small increase in V_{DS} (<0.2V), P_y still remains positive, and the top of the source barrier is lowered as in a standard FET. However, further increase in V_{DS} (>0.2V), P_y at the drain end becomes negative. Due to domain interaction, P_y on the source end becomes less positive, which pulls up the CB (Fig. 7(b)). This non-monotonic behavior of CB with respect to V_{DS} leads to interesting FEFET characteristics, as discussed subsequently.

The gate to gate potential profile of the FEFET and baseline FET are shown in Fig.8. At V_{GS}=0V, the voltage drop across FE is positive due to negative P_y, which lowers the channel potential compared to the baseline. On the other hand at V_{GS}=0.6V, the voltage drop across FE is negative (due to positive P_y), which increases the channel potential, showing voltage step-up due to the negative capacitance (NC) effect.

These effects are manifested in the transfer and output characteristics of FEFET (Fig.9). Decrease in OFF current (I_{OFF}) due to lowering of channel potential at V_{GS} = 0 can be observed. Lower SS (due to NC effect) as well negative DIBL (due to the impact of drain E-fields on P_y) can also be seen. The non-monotonic behavior of CB with respect to V_{DS} (Fig. 7(b)) yields non-monotonic trends of I_{DS} with respect to V_{DS} (Fig. 10), which results in negative output conductance (NOC). To complete the analysis, we show the effect of T_{FE} on I_{DS}-V_{GS} characteristics in Fig. 11. Increasing T_{FE} leads to lower SS and I_{OFF} due to increase in the NC effect.

B. Effect of K_P on FEFET characteristics

Next, we analyze the effect of domain interaction on FEFET characteristics. Decreasing K_P lowers the interactions between FE domains, allowing more variation along the gate length (Fig. 12(a)). As a result, the effect of drain-side P_y on the source-side P_y decreases. Thus, the increase in the source barrier caused by drain E-fields (see Fig.7(a)) is lower for lower K_P. This translates to increase in I_{OFF} as K_P is decreased (Fig. 13). For the same reason, negative output conductance effect also decreases for low K_P (Fig. 14). To explain the increase in SS with decrease in K_P, let us consider Fig. 12(b), which shows lower $|E|$ in the FE as K_P is lowered. This can be easily understood from the LK equation (Fig. 1), which shows that the domain interaction term adds an additional component to E, since $d^2P_y/dx^2 < 0$ (Fig. 5). Thus, as K_P decreases, E in FE also decreases leading to lower NC effect. To further analyze the effect of P_y variation along x, we simulate an FEFET with a metal layer between FE and SiO_2. This inter-layer metal maximizes the effect of drain E-fields by distributing the potential uniformly along the gate. Further, the NC effect uniformly affects the potential along the channel. Thus, reduction in SS is larger for FEFET with inter-layer metal compared to FEFET without the metal (Fig. 15). Fig. 16 compares SS, ON-OFF current ratio, DIBL and output conductance of FEFETs with and without metal. It can be observed that as K_P increases, the behavior of FEFET without metal approaches the one with the inter-layer metal.

V. CONCLUSIONS

In this paper we presented a numerical model of FEFETs which solves Poisson's equation, multi-domain LK equation and NEGF equations self-consistently. Using our model, we discussed the effect of polarization variation in FE along the gate length and showed that with increase in the domain interaction, the signatures of NC effect (negative DIBL, negative output conductance and lower SS) become more prominent.

ACKNOWLEDGMENT

This work was supported in part by DARPA Young Faculty Award, SRC-GRC and NSF under grant 1717999.

REFERENCES

[1] S. Salahuddin and and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," *Nano Letters* 2008 8 (2), 405-410.

[2] P Sharma, *et. al.*"Impact of Total and Partial Dipole Switching on the Switching Slope of Gate-Last Negative Capacitance FETs with Ferroelectric HZO Gate Stack," *VLSI Technology*, 2017.

[3] H. Ota, T. Ikegami, J. Hattori, K. Fukuda, S. Migita and A. Toriumi, "Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration," *IEDM*, 2016, pp. 12.4.1-12.4.4.

[4] A. Aziz, S. Ghosh, S. Datta and S. K. Gupta, "Physics-Based Circuit-Compatible SPICE Model for Ferroelectric Transistors," in *IEEE Electron Device Letters*, vol. 37, no. 6, pp. 805-808, June 2016.

[5] A. I. Khan, C. W. Yeung, Chenming Hu and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," *IEDM*, 2011, pp. 11.3.1-11.3.4.

[6] S. Datta, "Quantum Transport: Atom to Transistor".

[7] A. Cano and D. Jiménez, "Multidomain ferroelectricity as a limiting factor for voltage amplification in ferroelectric field-effect transistors," *Applied Physics Letters* 2010 97:13.

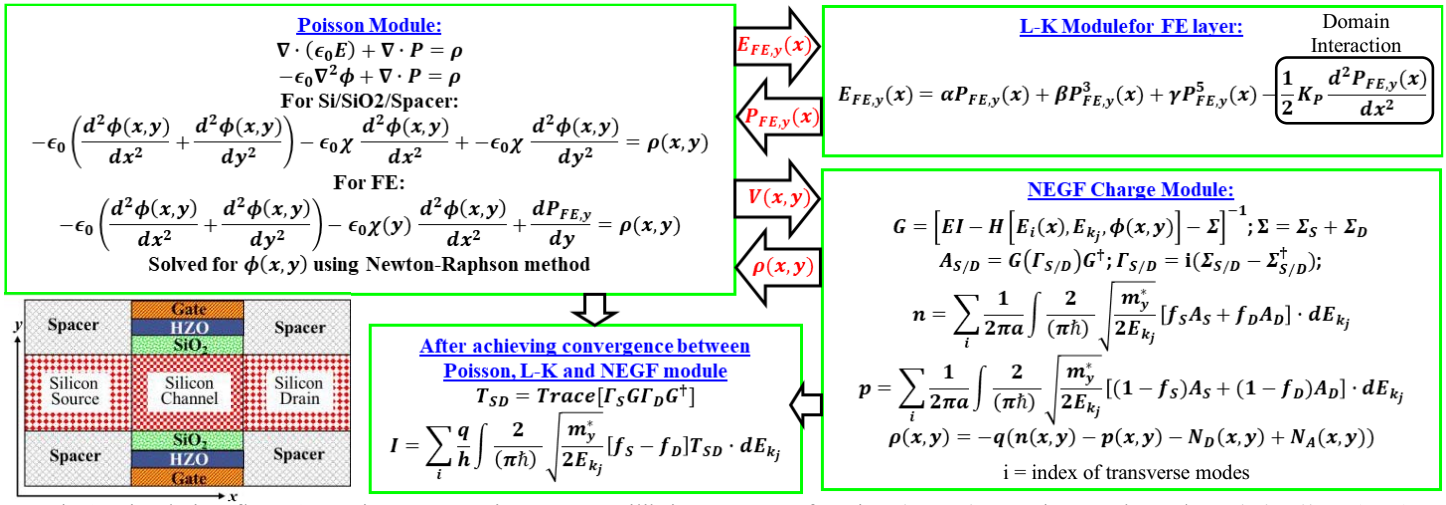

Fig.1: Simulation flow: 2D Poisson's equation, Non-equilibrium Green's function (NEGF) equations and Landau-Khalatnikov (L-K) equation with domain interaction term have been solved self-consistently. The device schematic used for simulation shown on bottom left. Baseline standard FET (Std.) is without HZO (effective oxide thickness = 0.5nm)

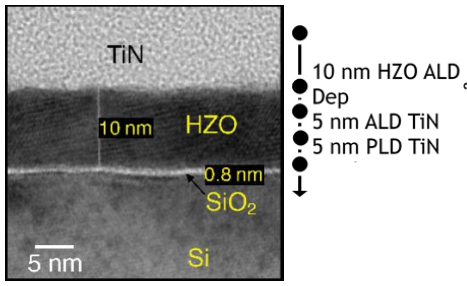

Fig.2: TEM image of fabricated 10nm HZO + 0.8nm SiO_2. Process flow is shown alongside.

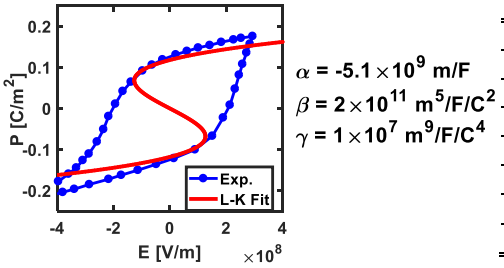

Fig.3: Measured polarization (P) – electric field (E) curve for HZO and the L-K fit used to extract α, β, γ for model calibration.

Gate Length	12 nm
Gate Underlap	1 nm
Silicon Thickness	4 nm
SiO_2 Thickness	0.5 nm
FE Thickness	1 nm
K_P	$5 \times 10^{-7}\ m^3/F$
Channel Doping	$10^{15} cm^{-3}$
S/D Doping	$10^{20} cm^{-3}$

Fig. 4: Simulation Parameters.

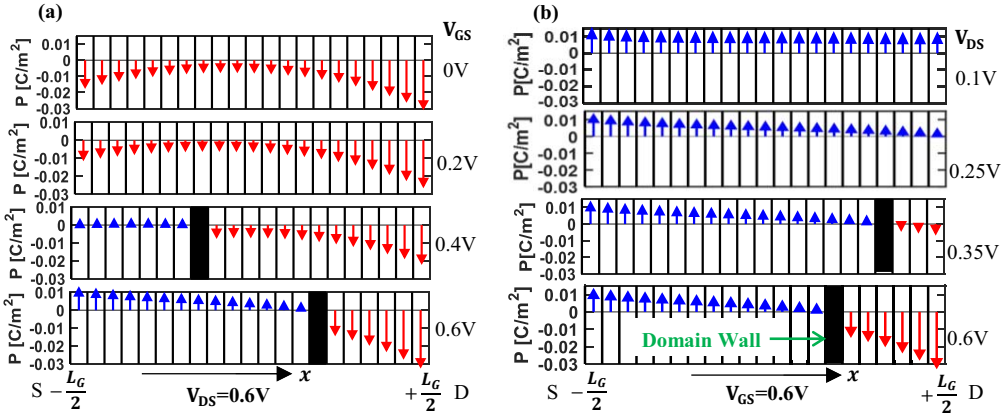

Fig. 5: Polarization of FE along the gate (from source to drain) for (a) $V_{DS} = 0.6V$ and different V_{GS}, (b) $V_{GS} = 0.6V$ and different V_{DS}. The variation in polarization is caused by non-uniform electric-field along the channel due to built-in potential and high V_{DS}.

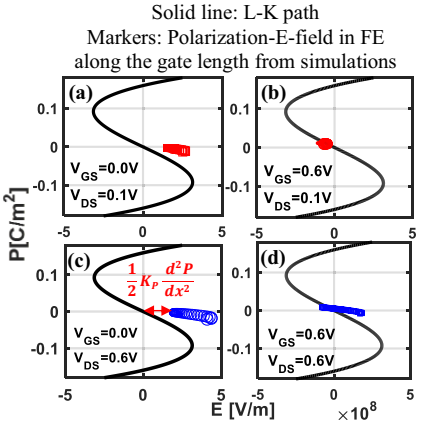

Fig. 6: Polarization of FE for different biases showing that high V_{GS} pulls the polarization in positive direction and high V_{DS} increases its variability along the gate length.

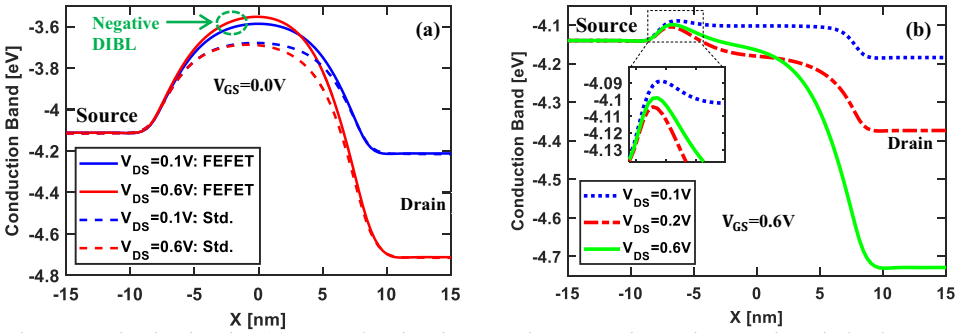

Fig. 7: Conduction band at (a) $V_{GS} = 0V$ showing negative DIBL due to decrease in polarization caused by drain electric fields, and (b) $V_{GS} = 0.6V$ showing non-monotonic effect of V_{DS} on the top of the source barrier, which is caused by the impact of drain electric fields on the channel potential which tends to lower the barrier and polarization reduction in FE with increasing V_{DS} which tends to increase the barrier.

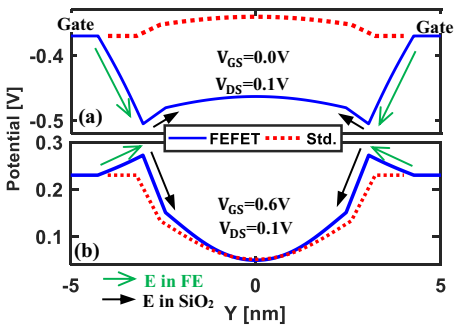

Fig. 8: Potential (ϕ) along the gate-to-gate direction at (a) $V_{GS} = 0V$ and (b) $V_{GS} = 0.6V$ showing opposite electric fields in FE and SiO_2 due to negative dP/dV of FE.

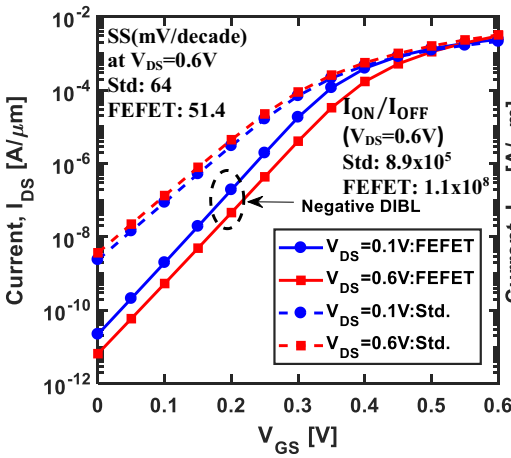

Fig.9: $I_{DS} - V_{GS}$ characteristics of FEFET showing negative DIBL and steep-slope characteristics.

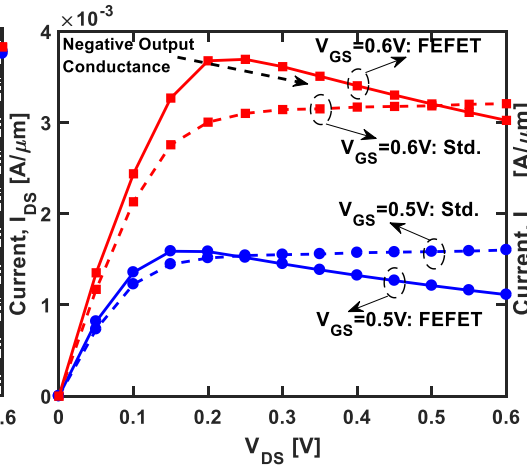

Fig.10: $I_{DS} - V_{DS}$ characteristics of FEFET showing negative output conductance due to non-monotonic dependence of source barrier on V_{DS}.

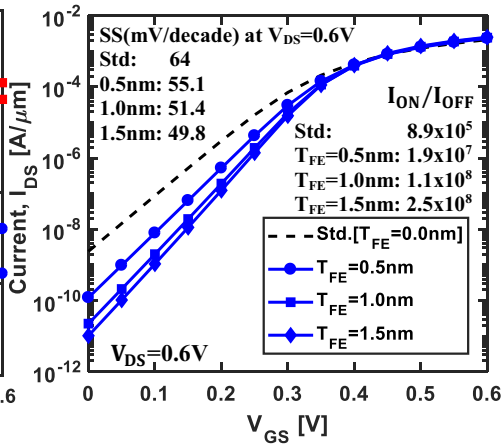

Fig.11: $I_{DS} - V_{GS}$ characteristics of FEFET for different T_{FE} showing that increasing T_{FE}, increases the steep-slope characteristics.

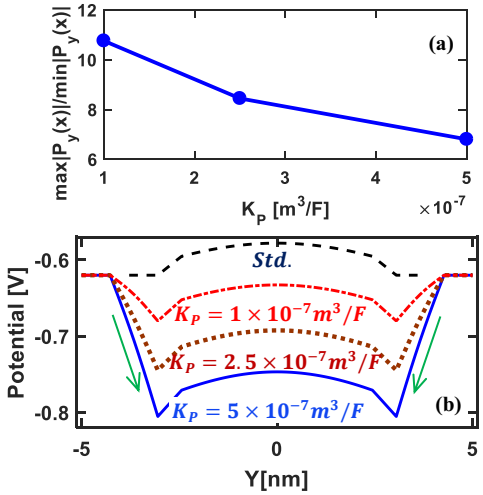

Fig.12: (a) Ratio of maximum to minimum |P_y| of FE along the gate for different K_P showing decrease in P_y variation with higher K_P, (b) gate to gate potential profile for different K_P showing larger |E_y| in FE for larger K_P.

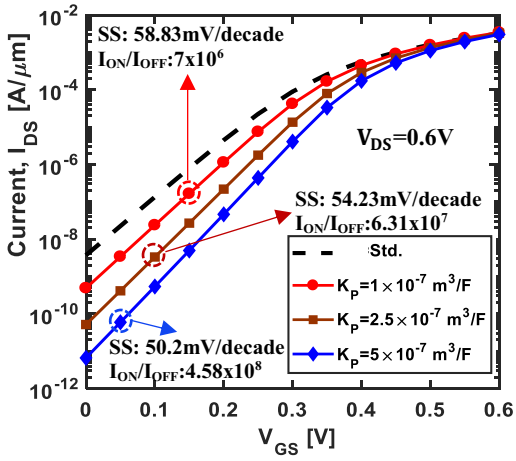

Fig.13: $I_{DS} - V_{GS}$ characteristics of FEFET for different K_P showing that increase in K_P reduces subthreshold-swing (SS) and increases the ratio of ON and OFF current.

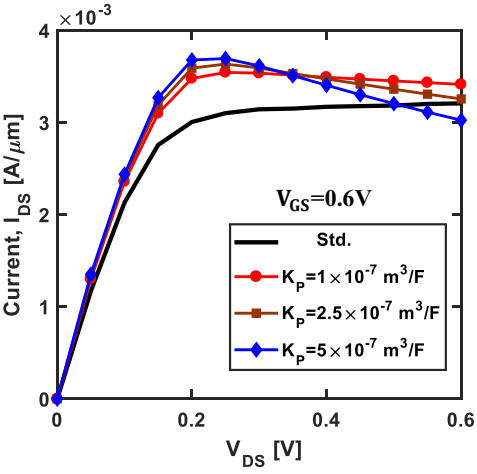

Fig.14: $I_{DS} - V_{DS}$ characteristics of FEFET for different K_P showing that increase in K_P boosts the negative output conductance (NOC).

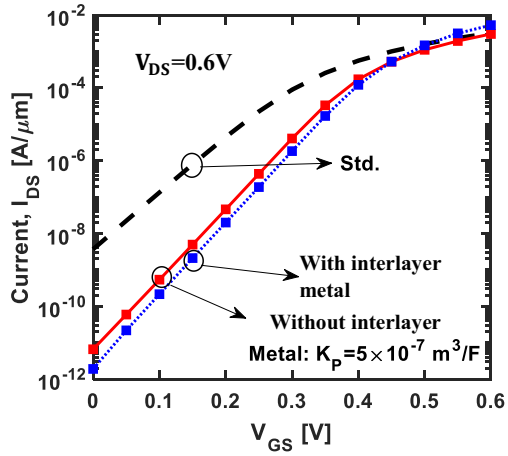

Fig.15: $I_{DS} - V_{GS}$ characteristics of FEFET with and without interlayer metal between FE and SiO_2, showing that an interlayer metal yields steeper slope as it makes the polarization uniform along the gate.

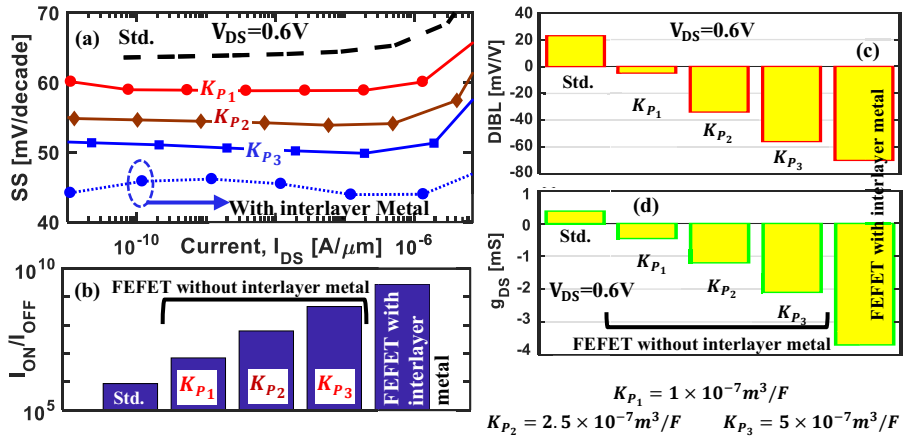

Fig.16: Comparison of (a) subthreshold-swing (SS), (b) I_{ON}/I_{OFF} (c) DIBL and (d) output conductance (g_{DS}) of FEFETs without interlayer metal (for different K_P), with interlayer metal and baseline (Std.) FET, showing the metrics of FEFET without metal approach those of FEFET with metal as K_P increases.