A Physics-Based Model for Oxide–Semiconductor-Based Ferroelectric Field-Effect Transistors

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***Abstract*— This article presents a comprehensive physics-based model for back-end-of-line (BEOL)-compatible oxide–semiconductor-based ferroelectric field-effect transistors (FeFETs). The proposed model describes the polarization switching behavior and enables bidirectional bias sweeps for the hysteretic I_DV_G curve. The model has been validated against a TCAD model as well as experimental results. Simulations using the proposed model show that polarization switching during the erase operation is primarily influenced by the fringing field in the absence of holes in the amorphous channel. Furthermore, the memory window (MW) increases as the channel length decreases, which is attributed to the enhanced influence of the fringing field in shorter channel devices, resulting in a larger portion of negative polarization being switched during the erase operation. Simulations using this model suggest an MW of 1.2 V, which shows excellent agreement with experimental data.**

***Index Terms*— Back-end-of-line (BEOL) ferroelectric field-effect transistor (FeFET), device modeling, ferroelectric (FE) memory, monolithic 3-D (M3D), oxide–semiconductor.**

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I. Introduction

When studying compute-in-memory (CIM) architectures [1], [2], [3], monolithic 3-D (M3D) integration techniques can provide significant advantages in terms of latency, area, and power consumption [4]. In M3D CIM architectures, nonvolatile memory (NVM) arrays are fabricated in the back-end-of-line (BEOL), while the peripheral circuitry resides in the front-end-of-line (FEOL). Consequently, the development of BEOL NVM is of great importance for the success of the M3D CIM architecture solutions. The BEOL-compatible ferroelectric field-effect transistor (FeFET) that adopts ferroelectric (FE) HfO_2 and an oxide–semiconductor channel is of great interest as it enables M3D integration and offers excellent performance and reliability [4], [5], [6]. Nevertheless, a physics-based model specifically tailored for such BEOL FeFETs is currently unavailable. Any FeFET model must model the following: 1) the FE module and 2) the semiconductor channel. Different FE models are available, ranging from the single-domain Landau–Khalatnikov (L–K) model, the multidomain L–K model [7], the multidomain nucleation-limited-switching (NLS) model [8], [9], [10], the infinite-domain Preisach model [11], [12], and the Jiles–Atherton model [13]. These FE models can be leveraged for BEOL FeFET modeling; this work adopts the multidomain L–K model.

Most existing FeFET models cannot be directly applied for BEOL FeFETs due to their fundamentally different working mechanisms. In a conventional FeFET [14], [15], the silicon channel can supply both electrons and holes to facilitate program-erase operations [Fig. 1(a)]. However, in BEOL n-type FeFETs, the amorphous metal oxide thin-film channel lacks holes needed for effective erase operations due to its n-type doping and wide-bandgap [Fig. 1(b)]. This has profound implications on device operations and, hence, model development as it requires 2-D treatment of electrostatics during the erase operation, rather than the simple 1-D analysis. During erase, compensation charge mainly arises from the following: 1) the channel depletion charge and 2) the source/drain electrodes and their fringe fields; capturing these effects is critical.

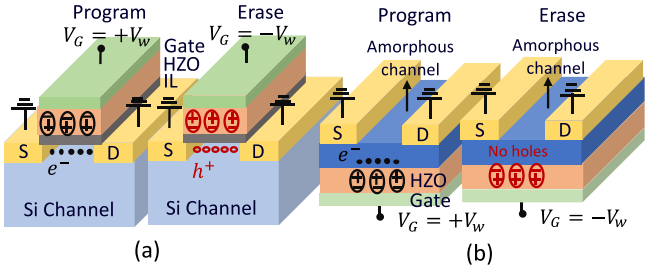


Fig. 1. Memory operation of the conventional FeFET and the BEOL FeFET. (a) Program-erase operation of the conventional FeFET. (b) Program-erase operation of the BEOL FeFET.

A compact model based on amorphous indium–gallium–zinc–oxide (IGZO) for BEOL FeFETs has recently been reported [16]. However, in that structure, HZO is sandwiched between the top and bottom metal layers, and thus, the polarization does not directly modulate the channel; instead, the polarization of the whole film is averaged out by the intermediate electrode for channel modulation. In such a case, treatment of 2-D electrostatics is not necessary, since the structure bears similarities with the model for conventional FeFETs. To the best of our knowledge, no physical model has been developed based on the device structure in Fig. 1(b).

In this article, we introduce a novel physics-based model for BEOL FeFETs. This model employs a combination of the surface potential-based junctionless FET (JLFET) model [17], [18] and the L–K model [7] to comprehensively describe the polarization switching phenomenon in BEOL FeFETs. Moreover, we integrate the JLFET-LK modeling framework with the indium tungsten oxide (IWO) transistor model [19], which governs the current transport behavior, resulting in a cohesive BEOL FeFET physical model. The IWO transistor model, relying on the virtual source model, can effectively capture the characteristics of current transport [19], [20], [21]. The proposed physical model for BEOL FeFET shows excellent agreement with TCAD simulation results and also suggests that the polarization switching observed during the erase operation is primarily influenced by the inner-fringing field near the source and drain regions. Furthermore, simulation results from our proposed model demonstrate a memory window (MW) of 1.2 V, exhibiting excellent agreement with experimental data [5]. In addition, our simulations reveal that the MW increases as the channel length is scaled down. This behavior can be attributed to the amplified effect of the inner-fringing field in shorter devices, leading to a larger portion of negative polarization and ultimately resulting in a larger MW. Though the developed model is still computationally expensive, it will serve as a stepping stone for future compact model development.

II. Modeling Framework of the Physical Model

Fig. 2 illustrates the modeling framework for the BEOL FeFET physics-based model. The FE polarization (P) is obtained from the JLFET-LK model, while the IWO transistor model governs the current transport behavior. Ultimately, P is integrated with the IWO transistor model, resulting in the realization of a comprehensive physics-based model for BEOL FeFETs.

Initially, we solve a 2-D Poisson's equation, which enables us to determine the surface potential distribution $[\varphi_s(x)]$ along the channel. We consider the presence of only electrons (n) and ionized donor atoms (N_D) as no holes can be generated at a reasonable time scale of the memory operation. The 2-D Poisson's solver utilized is based on the JLFET model [17], [18]. Equations (1) and (2) are solved simultaneously to obtain the surface potential (φ_s). Instead of the original JLFET modeling approach, we incorporate the influence of P, which directly affects the channel charge (Q_{ch}), as expressed in (2). Here, C_{FE} represents the linear capacitance of the FE, excluding the nonlinear polarization. V_G denotes the gate voltage, and V_{FB} signifies the flat band voltage. Upon acquiring $\varphi_s(x)$, we calculate the electric field (E_y) across the FE layer, where T_{FE} corresponds to the thickness of the FE layer. E_y is used to solve for the polarization distribution $[P(x)]$ along the channel by employing the L–K model. Furthermore, to obtain the updated polarization value (P_{new}) based on the L–K model, we perform an analytical integration of $P(x)$ along the length of the channel, and it is imperative to ensure that P_{new} is eventually congruent to the P value considered in the 2-D Poisson's solver. In the first iteration of our framework, we set P to zero, which serves as the initial value. In subsequent iterations, P is updated to P_{new}. The iterative calculations continue until P equals P_{new}, when the polarization across the FE layer converges. At this point, P is not only balanced with the channel charge, but also aligns with the polarization obtained from the L–K model.

To obtain the $I_D V_G$ hysteresis curve, we incorporate P with the IWO transistor model to perform bidirectional dc sweeps. In the IWO transistor model, the Schottky diodes located at the source and drain regions serve to represent the gate-voltage modulated contact resistance. Thus, the current flowing through the source and drain regions is proportional to the exponential of the voltage across the gate and source/drain. The Schottky diode models at the source/drain are in series with an intrinsic FET based on the virtual source model to ensure the consistency of the drain current. This model has shown excellent agreement with experimental data [19], [20], [21].

It is noteworthy that the proposed physics-based model has not yet accounted for time-dependent dynamic operations and the influence of interfacial traps. The numerical computations involved in the 2-D Poisson's solver are computationally intensive, demanding a considerable amount of time for static operation simulations. Consequently, the incorporation of time-dependent dynamic operations into the proposed model would markedly extend the simulation duration. Furthermore, considering the impact of interfacial traps would not only amplify the time requirements of the simulations but also deviate from the intended scope of this article.

III. Results and Discussion

Fig. 3 illustrates the device structure and simulation parameters. The double-gate structure is employed to validate the 2-D

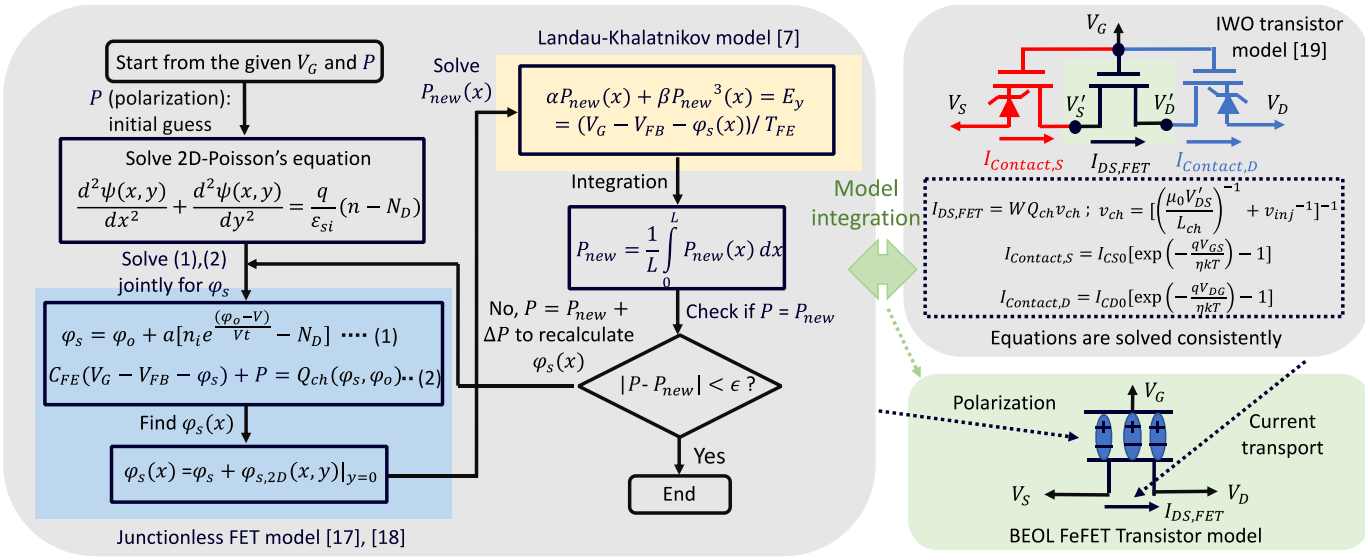
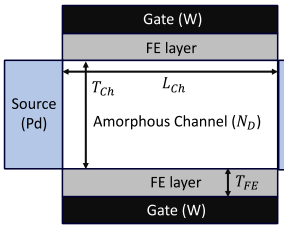


Fig. 2. Modeling framework for the BEOL FeFET physics-based model.



Parameter	Value
Channel Length (L_{Ch})	15, 28, 80nm
Channel Thickness (T_{Ch})	5, 10nm
FE Thickness (T_{FE})	5, 10nm
Channel Doping (N_D)	5.2x10^{19} (cm^{-3})
Mobility (μ_0)	20 (cm^2/V-s)
Injection Velocity (v_{inj})	2x10^6 (cm/s)

Fig. 3. Device structure and parameters for the simulations.

Poisson's model. In our model, we adopt the double-gate structure instead of the bottom-gated structure [see Fig. 1(b)], since the boundary condition from the top side of the bottom-gated structure is challenged to be defined, resulting in the 2-D Poisson's equation unsolvable. Therefore, as a first attempt, we used the double-gate structure as a proxy, since it allows solving the 2-D Poisson's equation. A more accurate model will be studied in future work.

We provide the V_{GS} values of 4, 0, and -4 V, with the channel lengths of 28 and 80 nm as case studies. We configured the thickness of the FE layer and the IWO channel (T_{Ch}) to both 5 and 10 nm. We first validate the 2-D Poisson's model for obtaining the electric field across the FE layer by comparing the FE layer voltage V_{FE} obtained from the model with TCAD numerical results (see Fig. 4). Specifically, V_{FE} represents the voltage across the FE layer when $P = 0$. Model results suggest an excellent match with TCAD results with respect to the distribution of V_{FE} along the channel. Notably, at $V_{GS} = -4$ V, there are negative fringing fields in the vicinity of the source and drain regions [see Fig. 4(a) and (b)]. Furthermore, the portion of the inner-fringing field is larger in shorter devices compared with the longer ones, which effectively facilitates polarization switching during the erase operation.

The model results demonstrate a strong agreement with TCAD results for various values of T_{FE} and T_{Ch} [see Fig. 4(c)]. It is noteworthy that at $V_{GS} = -4$ V, the value of V_{FE} decreases (i.e., the absolute value of V_{FE} increases) as either T_{FE} or T_{Ch} increases. To understand this phenomenon, we can begin by expressing the charge equality equation: $C_{FE}V_{FE} = -Q_{Ch}$. Under $V_{GS} = -4$ V, the channel is fully depleted, leaving only fixed charge in the channel, which can be expressed as $Q_{Ch} = qN_DT_{Ch}$. When T_{FE} increases, C_{FE} decreases, leading to a reduction in the value of V_{FE}, while the channel charge remains unchanged. We also consider the impact of T_{Ch} on V_{FE}. First, V_{FE} can be expressed as $V_{FE} = V_G - V_{FB} - \varphi_s$. The value of φ_s is increased when T_{Ch} increases, and this observation aligns with the findings in the literature [22] concerning the correlation between T_{Ch} and φ_s. Consequently, the increased value of φ_s contributes to a reduction in the value of V_{FE}. Moreover, based on the results in Fig. 4(c), this model can be utilized for optimizing device performance.

We further investigate the behavior of the electric field (E_{FE}) across the FE layer under varying T_{FE} and T_{Ch}, when $P = 0$ and $V_{GS} = -4$ V [see Fig. 4(d) and (e)]. In Fig. 4(d), it is evident that E_{FE} remains nearly identical with a slightly amplified negative inner-fringing field when T_{FE} is decreased, and T_{Ch} is fixed. Furthermore, Fig. 4(e) illustrates that the negative E_{FE} is enhanced when T_{Ch} is increased, and T_{FE} is fixed. These observations reveal the potential for optimizing the device performance by changing T_{Ch} and T_{FE}, particularly for the efficiency of the erase operation.

Next, we use our model to examine the polarization–voltage (P–V) hysteresis curve and the polarization distribution along the channel. Fig. 5(a) displays the P–V hysteresis curve for the channel lengths of 15, 28, and 80 nm, respectively, with $V_{DS} = 0.2$ V. We can observe that more polarization is switched back at $V_{GS} = -4$ V for shorter channel devices. This can be attributed to the larger portion of the negative fringing field in proximity to the source and drain regions [see Fig. 4(a) and (b)]. Consequently, the average polarization across the FE layer becomes smaller. In addition, Fig. 5(b) shows the P–V hysteresis curve for different values of V_{DS} at a channel length of 28 nm. At higher values of V_{DS}, due to the increase of an opposing electric field, one observes a

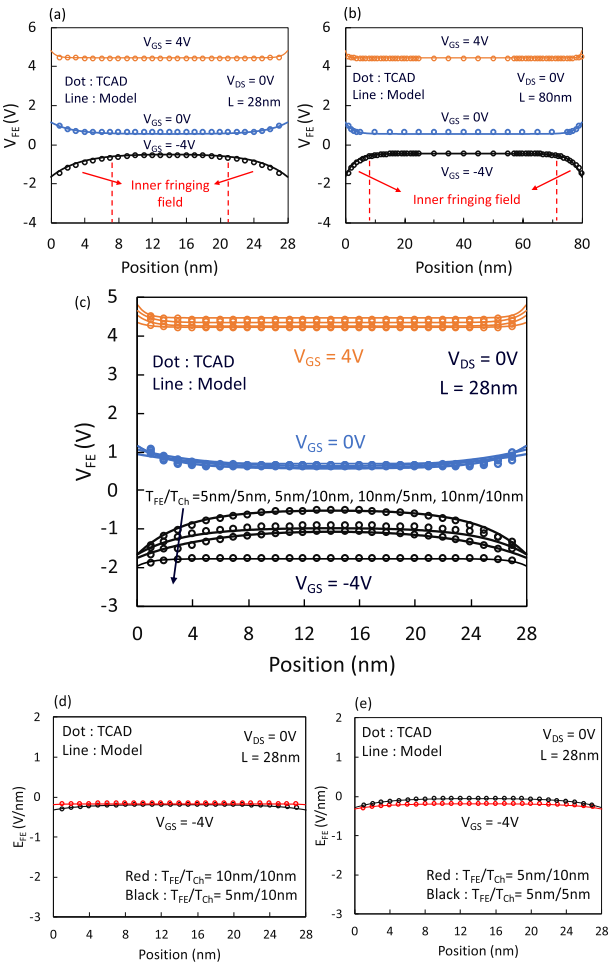


Fig. 4. Validation results of the 2-D Poisson's model. (a) Comparisons between the 2-D Poisson's model and the TCAD simulation results at a channel length of 28 nm. (b) Comparisons between the 2-D Poisson's model and the TCAD simulation results at a channel length of 80 nm. (c) Comparisons between the 2-D Poisson's model and the TCAD simulation results for different thicknesses at a channel length of 28 nm. (d) Electric-field values across FE layer when T_{FE} is 5/10 nm, and T_{Ch} is fixed at 10 nm. (e) Electric-field values across FE layer when T_{Ch} is 5/10 nm, and T_{FE} is fixed at 5 nm.

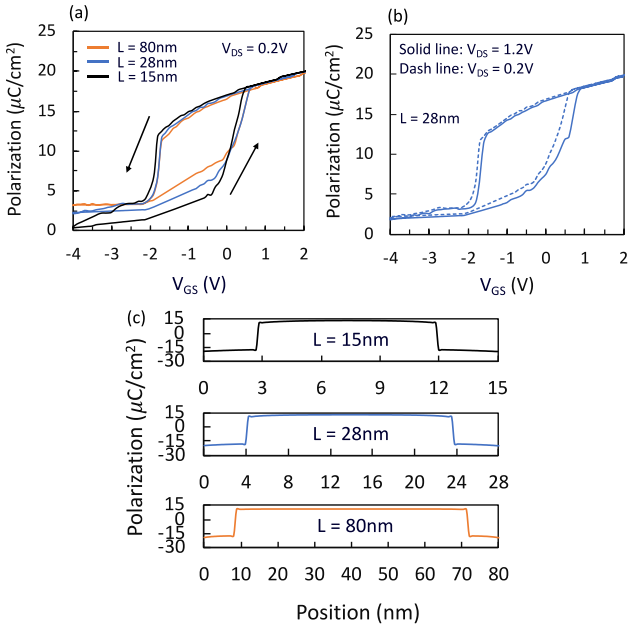


Fig. 5. Polarization–voltage (P–V) hysteresis curve and the polarization distribution along the channel. (a) P–V hysteresis curve for various channel lengths. (b) P–V hysteresis curve for different values of V_{DS} at L = 28 nm. (c) Polarization distribution along the channel at V_{GS} = −4 V for different channel lengths.

delay in switching to the higher polarization value, as well as faster switching back to the lower polarization value. This demonstrates the impact of 2-D electrostatics on the polarization switching behavior. Fig. 5(c) illustrates the polarization distribution along the channel at $V_{GS} = -4$ V for different channel lengths. It is evident that negative polarization switching occurs exclusively near the source and drain region. Due to the absence of holes in the IWO channel, FE domains that are not in close proximity to the source and drain region remain unaltered. Furthermore, for varying channel lengths, we observe that the proportion of negative polarization, relative to the channel length, is larger in shorter devices compared with longer channel devices. This occurrence may increase the MW when the channel length is scaled down.

We further examine the $I_D V_G$hysteresis curve generated by our proposed model. We set the HZO and IWO channel thickness to 5 nm, consistent with the experimental device [5]. Furthermore, we determined the values of FE parameters (i.e., α and β) in the L–K model by calibrating the simulated MW at $L = 28$ nm with the experimental data [5]. These parameters, α and β, play a crucial role in obtaining remnant polarization and coercive voltage for the FE capacitor. In our model, we employed $\alpha = -4.1 \times 10^{11}$ (cm/F) and $\beta = 1.7 \times 10^{21}$ (cm^5/F/μC^5) throughout all simulations. In Fig. 6(a), experimental data [5] suggest an MW of 1.2 V for a channel length of 28 nm. As shown in Fig. 6(b), our model's results for the same channel length suggest the same MW as the experimental data. The disparity observed in the $I_D V_G$ hysteresis path between the experimental data and simulation results can be attributed to the presence of channel percolation and multidomain effects [23], which have not been incorporated into the proposed model. We also performed dc sweep simulations for different channel lengths, as illustrated in Fig. 6(c). We observe that a shorter channel length results in a larger MW. This can be attributed to the enhanced influence of the fringing field in shorter devices, as discussed earlier.

While prior work [6], [24] has demonstrated that the following hold: 1) the inner-fringing field near the source and drain regions can facilitate polarization switching during the erase operation and 2) the MW increases as channel length scales down, and these observations have primarily relied on experimental and TCAD simulations. For the first time, this article presents a physics-based compact model for BEOL FeFETs, which not only suggests the same MW as experimental data, but also provides quantitative explanation for polarization switching.

In summary, this study has yielded a comprehensive physics-based model for BEOL FeFETs. The primary aim was to delve into the underlying physics of BEOL FeFET operations using this model, with a specific focus on capturing

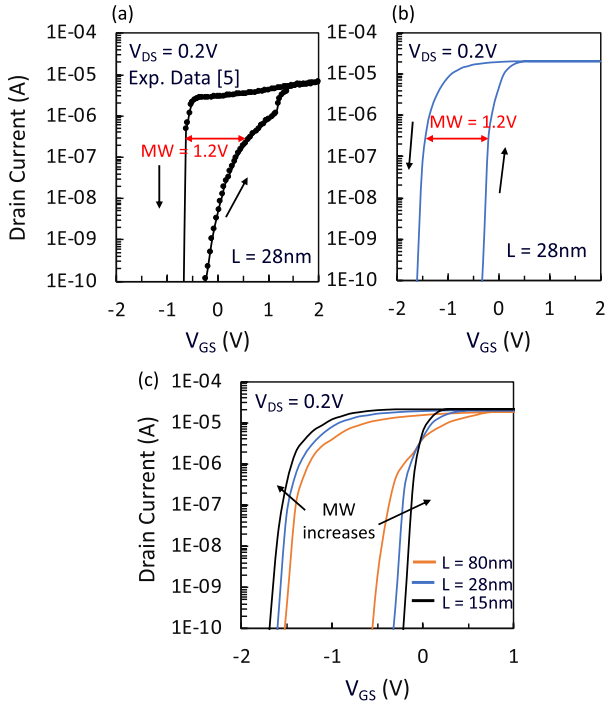


Fig. 6. Bidirectional dc sweep for the $I_D V_G$ curve. (a) Experimental result shows an MW of 1.2 V for a channel length of 28 nm [5]. (b) Simulation result shows the same MW of 1.2 V as experimental data for a channel length of 28 nm. (c) I_D V_G curve for different channel lengths, indicating an increase in the MW as the channel length is scaled down.

the critical role of the inner-fringing field in aiding challenging erase operations. Moreover, the model's results not only demonstrate a strong agreement with TCAD results but also closely align with experimental data, including MW and the observed reduction in channel length in relation to MW. Furthermore, due to the utilization of the general 2-D Poisson's solver, our proposed physics-based model is capable of assessing the performance of diverse BEOL FeFET devices (e.g., [25], [26], [27], [28]), particularly in evaluating the efficiency of the erase operation.

It is noteworthy that our assumption of neglecting holes in the 2-D Poisson's solver is more applicable to amorphous oxide–semiconductor n-type channels with a wide-bandgap. The proposed model may not universally apply to all BEOL-compatible devices, such as poly-silicon-based devices. Silicon channel possesses a smaller bandgap compared with the oxide–semiconductor channel, which may lead to hole generation. Furthermore, it is important to acknowledge that the intensive numerical calculations within the 2-D Poisson's solver make it less suitable for implementation in a compact form, such as a Verilog-A model. In addition, dynamic operations are not presently considered in the proposed model due to the substantial computational overhead involved. Consequently, in future work, our objective is to simplify the existing model and adapt it into the Verilog-A framework. Furthermore, the dynamic operations will be easier to incorporate with the Verilog-A compact model. Ultimately, the compact model could be utilized in large-scale circuit simulations aimed at assessing the performance of M3D CIM architectures.

IV. Conclusion

This physical model, validated through TCAD comparisons and agreement with experimental data, provides a comprehensive understanding of BEOL FeFET behavior. This model offers valuable insights into the design and optimization of BEOL FeFET-based memory devices for M3D integration.

In our future work, we will develop a compact model, derived from the proposed physics-based model. The compact model will aim to not only eliminate the necessity for intricate numerical computations inherent in the 2-D Poisson's solver, but also facilitate the evaluation of performance for M3D CIM architectures.

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