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Compact model of ferroelectric-gate field-effect transistor for circuit simulation based on multidomain Landau–Kalathnikov theory

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We report a new compact model for a ferroelectric-gate field-effect transistor (FeFET) considering multiple ferroelectric domain structures that can be thermally activated. The dynamics of the electric polarization and the thermal activation rate are calculated on the basis of the Landau–Khalatnikov (LK) theory. We implement this compact model in a circuit simulator, SmartSPICE, using Verilog-A language for analog circuit simulations. The device characteristics of FeFETs reported in experiments are well fitted by our compact model. We also perform the circuit simulation for the inverter utilizing FeFETs by using this compact model. Unlike normal inverters composed of MOSFETs, the switching speed of the inverter changes with the voltage pulse before the operation. © 2017 The Japan Society of Applied Physics

1. Introduction

In recent years, nonvolatile memory, which requires no refresh operation, has attracted considerable attention as a novel storage device with low power consumption. Various types of nonvolatile memories have been extensively studied aiming at their commercialization; exmaples of such memories are resistive random-access memory (RRAM),[1,2] magnetoresistive random-access memory (MRAM),[3,4] phase-change random-access memory,[5,6] and interfacial phase change memory (iPCM).[7,8] The one-transistor (1T)-type nonvolatile memory based on a ferroelectric-gate field-effect transistor (FeFET) is one of the promising candidates for commercial memories.[9–15] The FeFET has a high scalability with a high endurance, and a 100 nm gate length with 10^8 cycle endurance has been achieved.[15] Moreover, owing to the low power dissipation in write/erase operation, the NAND flash memory using 1T-FeFETs is expected to show better performance in power consumption than the conventional NAND flash memory based on floating-gate MOSFETs.[16] In addition, the FeFETs show an analog-like response to the applied gate voltage.[14] Polycrystalline ferroelectric layers used in FeFETs such as $SrBi_2Ta_2O_9$ (SBT) have multiple ferroelectric domains. The partial polarization of a large number of domains for the applied voltage results in the analog-like response of the FeFETs. Such an analog response is expected to be a fundamental component of neuromorphic computers,[17,18] and their characteristics have also been investigated from the viewpoint of nm-scale neuromorphic circuits.[19,20] Therefore, the FeFETs are key devices for novel large scale integrated (LSI) circuits.

The development of compact models that describe device characteristics is crucial for designing the LSI circuits, and the compact models for various types of MOSFETs have been developed so far. The latest standard compact models[21,22] enable us to treat novel devices such as silicon on thin buried oxide (SOTB)-MOSFETs and Fin-FETs. On the other hand, no standard compact models for FeFETs have yet been established. To develop reliable compact models, studies on the device modeling of FeFETs and ferroelectric capacitors have been vigorously conducted using semi-empirical mathematical models[23–25] and the Landau–Khalatnikov (LK) theory.[26,27] However, these models did not take into account the thermal activation of multiple ferroelectric domains. The thermal activation strongly affects the polarization hysteresis and the response to the sequence write/erase pules,[28] and thus, a compact model considering the thermal effects are required for reliable circuit simulations.

In this work, we develop a compact model of FeFETs based on the multi domain LK theory taking into account thermal activation. Our compact model reproduces well both the drain current versus gate voltage (I_d–V_g) characteristic and the dynamical response to the voltage pulse reported in an experimental study.[14] We perform a simulation for a simple inverter circuit composed of FeFETs, and confirm that this compact model runs well on the circuit simulator SmartSpice.[29]

2. Modeling

We focused on the most successful FeFET at this stage, composed of a metal–ferroelectric–insulator–semiconductor (MFIS) stack.[14,15] Figure 1(a) shows a schematic figure of the FeFET. In this device, a bias voltage applied to the gate induces electric polarization in the ferroelectric layer. The residual polarization changes the effective voltage applied to the oxide layer, and thus changes the threshold voltage V_{th}. Since the value of residual polarization depends on the record of the applied voltage before the operation, the shift of V_{th} can be used as nonvolatile memory. To describe the above situation, we considered an equivalent circuit model for a gate-to-channel region consisting of three capacitors connected in series. Figure 1(b) shows an equivalent circuit model of the FeFET, and the gate-to-channel region composed of a ferroelectric capacitor, an oxide capacitor, and a depletion capacitor is indicated by the dotted square. The circuit equation for this region is given by

$$V_{GB} - V_{FB} = d_F\left(\frac{\sigma_Q}{\epsilon_0} - \frac{\bar{P}}{\epsilon_0}\right) + \frac{\sigma_Q}{C_{od}},$$
$$C_{od} = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}}, \quad (1)$$

where ϵ_0 is the dielectric constant of the free space, d_F is the thickness of the ferroelectric layer. Moreover, C_{ox} and C_{dep} are the capacitances of the oxide and depletion layers, C_{od} is the combined capacitance of the oxide and depletion layers, $\bar{P}$ is the average polarization in the ferroelectric layer, σ_Q is the charge density of the capacitors, V_{FB} is the flat-band

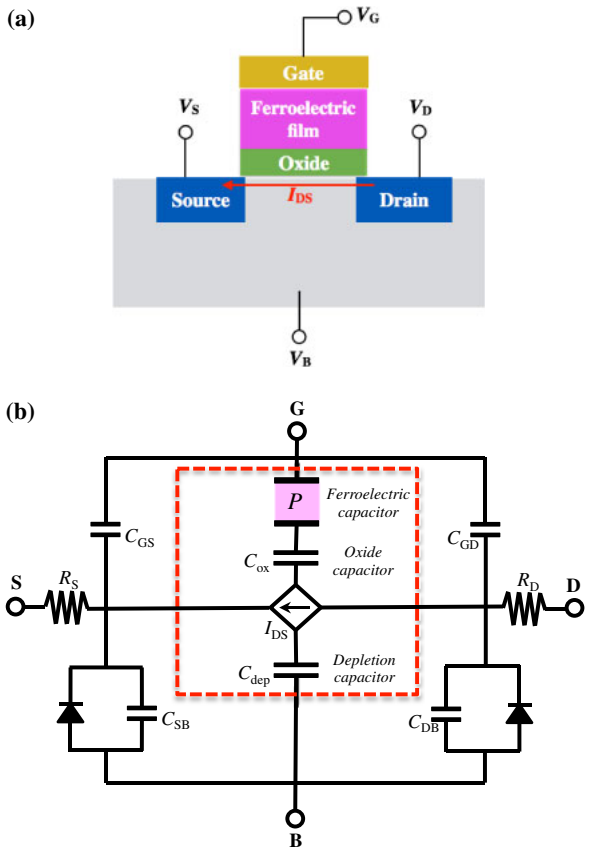

Fig. 1. (Color online) (a) Schematic figure of the FeFET with MIFS stack. (b) Equivalent circuit model for the FeFET. The dotted square indicates the gate-to-channel region of the FeFET.

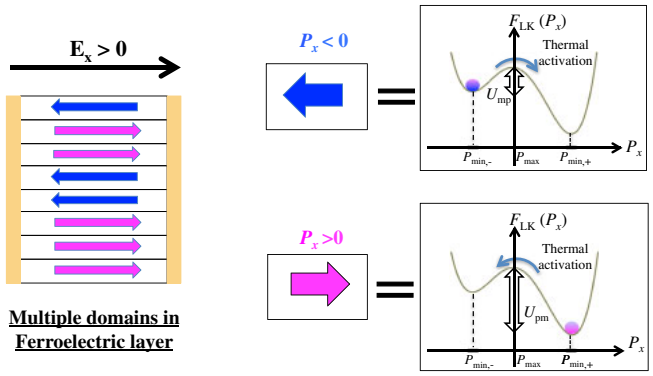

Fig. 2. (Color online) Schematic figure of multidomain model for the ferroelectric layer taking into account the thermal activation.

voltage, and V_{GB} is the bias voltage between the gate and the base. For comparison with the experiment, we set $d_f = 200\,\text{nm}$ and $C_{ox} = 8.63 \times 10^{-3}\,\text{F/m}^2$, which are comparable to the experimental conditions.[14,15] As described in Eq. (1), the residual polarization effectively changes the voltage applied to the oxide layer V_{ox}, and this results in the change of the source–drain current, I_{DS}. We calculated I_{DS} based on the well-known formula derived by Sah[30] for MOS transistors. For the subthreshold regime, we assumed a simple exponential dependence of I_{DS} on V_{ox}.

Regarding the dynamics of the polarization, we focused on the component of the polarization parallel to the electric field applied to the ferroelectric layer, P_x. The time evolution of P_x based on the LK theory is described as[31]

$$\frac{1}{D}\frac{dP_x}{dt} = -\frac{dF_{LK}(P_x)}{dP_x} = -2\alpha P_x - 4\beta P_x^3 + E_x, \qquad (2)$$

where F_{LK} is the free energy density of the ferroelectric domain, D is the diffusion constant, α and β are the parameters specifying the properties of the ferroelectric polarization, and $E_x = (\sigma_Q - \bar{P})/\epsilon_0$ is the electric field applied to the ferroelectric layer and is given by the summation of the electric field originating from the charge of the capacitor and the polarization. In this study, we considered $\alpha = 5.65 \times 10^7\,\text{V·m/C}$, $\beta = 1.09 \times 10^9\,\text{V·m}^5/\text{C}^3$, and $D = 8.85 \times 10^{-2}\,\text{F/(m·s)}$. For describing the properties originating from the multiple-ferroelectric domain structure, we considered multiple P_x's corresponding to the number of domains, N_D. We assumed that the dynamics of these P_x's are described by equations similar to Eq. (2); however, they can flip their polarity independently by thermal activation. Figure 2 shows the schematic figure of our multidomain model for the ferroelectric layer. To implement this model in circuit simulators by using Verilog-A language,[32] we simply treated the two equations representing domains with the positive polarity P_x^+ and the negative polarity P_x^-, and described the average polarization by $\bar{P} = (N_D^+ P_x^+ + N_D^- P_x^-)/N_D$, where N_D^+ and N_D^- are the numbers of positive and negative polarities, respectively. N_D^+ and N_D^- change with time and the electric field E_x in accordance with the activation rate, and their variations are given by

$$\delta N_D^+ = -\delta N_D^- = \delta t \omega_0 \left[\exp\left(\frac{-\Omega_D U_{mp}}{k_B T}\right) - \exp\left(\frac{-\Omega_D U_{pm}}{k_B T}\right)\right], \qquad (3)$$

where δt is the calculation time step, ω_0 is the trial frequency for the activation, Ω_D is the average volume of the domains, k_B is the Boltzmann constant, T is the temperature, and U_{mp} and U_{pm} are the activation energies from the negative-to-positive and positive-to-negative polarities, respectively. To obtain the activation energies, firstly, we calculate stationary points of the free energy, P_{max}, $P_{min,+} > 0$ and $P_{min,-} < 0$, by solving $dF_{LK}(P_x)/dP_x = 0$. Here, P_{max} corresponds to a relative maximum, and $P_{min,+}$ and $P_{min,-}$ correspond to relative minima. Then, we calculate $U_{mp} = F_{LK}(P_{max}) - F_{LK}(P_{min,-})$ and $U_{pm} = F_{LK}(P_{max}) - F_{LK}(P_{min,+})$ (see the double-headed arrows in Fig. 2). Since the free energy F_{LK} changes with the electric field E_x, as shown in Eq. (2), U_{mp} and U_{pm} depend on E_x. In this study, we consider $\omega_0 = 8 \times 10^{-2}\,\text{s}^{-1}$ and $\Omega_D = 0.9 \times 10^{-24}\,\text{m}^{-3}$.

3. Results and discussion

3.1 Basic properties of n-type FeFET

We calculated the device characteristics of the FeFET using the circuit simulator SmartSpice and compared them with the experimental results.[14] First, we investigated P_x–V_{GS} and I_{DS}–V_{GS} curves. In the experiments, the gate voltage was swept from −4 to 6 V because the flat-band voltage shifted the applied voltage to the ferroelectric layer at around −1 V. In this calculation, we set the threshold voltage without the polarization as $V_{th0} = 1.4\,\text{V}$ and the flat-band voltage as $V_{FB} = 0.9\,\text{V}$, and swept the gate voltage between −4 and 6 V. Figures 3(a) and 3(b) show P_x and I_{DS} as functions of V_{GS} and those of the experiment, respectively. These figures indicate that V_{th} shifts with the direction of the voltage sweep

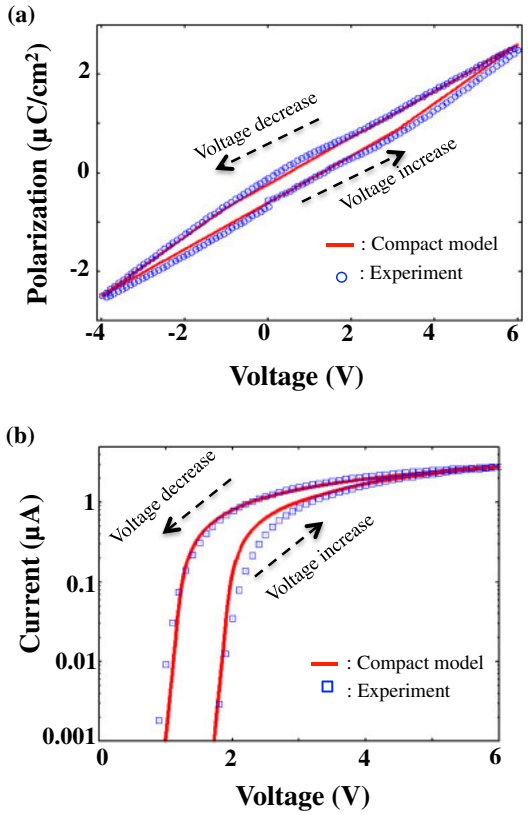

Fig. 3. (Color online) (a) P_x–V_{GS} and (b) I_{DS}–V_{GS} curves calculated using our compact model and those of the experiment.[14)]

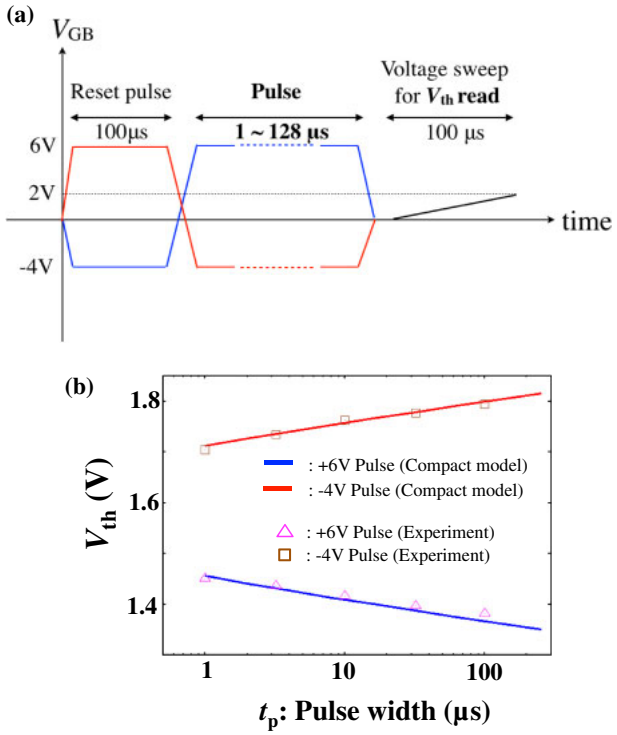

Fig. 4. (Color online) (a) Schematic of the pulse voltages. (b) V_{th} as a function of the pulse width t_p calculated using our compact model and those of the experiment.

owing to the change in residual polarization, and our results show good agreement with experimental results. The positive (negative) residual polarization effectively increases (decreases) the gate voltages, and this leads to the decrease (increase) in V_{th}. Next, we applied voltage pulses and investigated the dependence of V_{th} on the pulse width. In this calculation, we set $V_{th0} = 1.48\,V$ and $U_{FB} = 0.98\,V$. Figure 4(a) shows the schematic of the pulse voltages. We swept the voltage from 0 to 2 V after the input pulse for determining V_{th}, where I_{DS} reached 10^{-8} A/μm. Figure 4(b) shows V_{th} as a function of the pulse width t_p and those of the experiment. In this figure, we can see that V_{th} linearly increases (decreases) with respect to the "logarithm" of the width of the negative (positive) pulse. These results indicate that the absolute value of the residual polarization linearly increases with the logarithm of t_p, and that our compact model reproduces this property well. This peculiar property can be attributed to the negative feedback of the thermal activation along the pulse polarity. The voltage pulses promote the flip of the polarization along the pulse polarity. However, the flip of the polarization by thermal activation reduces the electric field E_x along the polarity, and this results in the decrease in the thermal activation rate itself. The delay of the polarization flip owing to this negative feedback leads to the logarithmic change in the polarization.

3.2 Inverter composed of n- and p-type FeFETs

Finally, we performed circuit simulation of the inverter composed of n- and p-type FeFETs. Here, we considered same parameters for both FeFETs except for their polarity. Figure 5(a) indicates the circuit diagram of the inverter. The operation voltage V_{DD} is 3 V. We calculated the time evolution of the output of the inverter with and without the

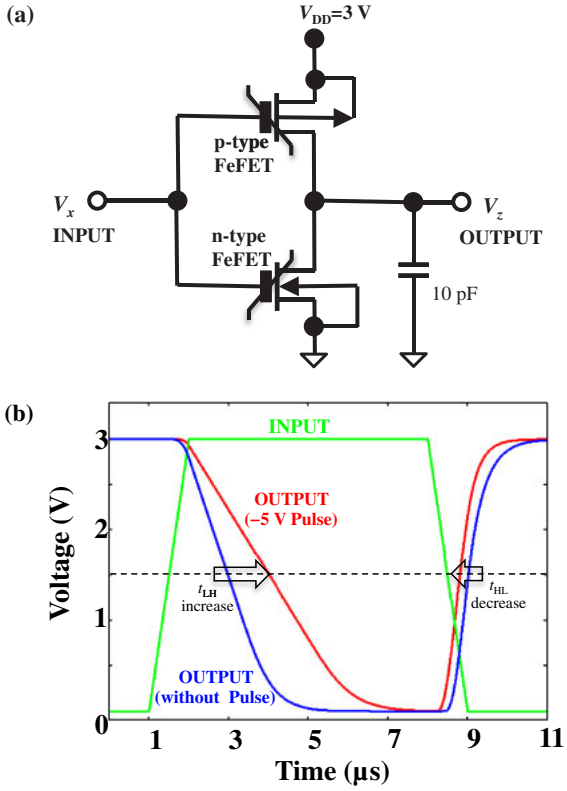

Fig. 5. (Color online) (a) Circuit diagram of the inverter composed of n- and p-type FeFETs. (b) Operation of the inverter composed of FeFETs with and without −5 V voltage pulse.

pre-voltage pulse $V_x = -5\,V$ with 5 μs width. Note that the $|V_{th}|$ shifts of the n- and the p-type FeFETs caused by the voltage pulse are opposite because of the difference in their

polarity. Figure 5 shows the characteristics of the output for a trapezoidal input. By applying a negative pulse, the high-to-low propagation delay time (t_{HL}) is increased owing to the increase in the $|V_{th}|$ of the n-type FeFET. On the other hand, the low-to-high delay time (t_{LH}) decreases owing to the reduction in the $|V_{th}|$ of the p-type FeFET. Such tunability by the pulse intensity will be helpful for the design of a high-speed and low-power-consumption circuit.

4. Conclusions

We have developed a compact model of the FeFET multidomain ferroelectricity. In this model, multiple ferroelectric domain structures and their thermal activations are taken into account, and the dynamics of the electric polarization and the thermal activation rate are calculated in the framework of the Landau–Khalatnikov (LK) theory. Our compact model implemented in Verilog-A language reproduces both the I_d–V_g characteristic and the dynamical response to the voltage pulse reported in the experimental study. Of particular note is that the logarithmic dependence of V_{th} on the pulse width is reproduced well. This peculiar property can be explained by the change in the thermal activation rate, which is naturally incorporated into our compact model. Moreover, by using this compact model, we have performed the simulation of the inverter circuits composed of FeFETs and shown that the delay time of the inverter is controlled by the voltage pulse. As presented in this paper, our compact model can be implemented in circuit simulators and will be useful for various types of novel circuits utilizing FeFETs.

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