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Design space exploration of hysteretic negative capacitance ferroelectric FETs based on static solutions of Landau–Khalatnikov model for nonvolatile memory applications

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Systematic design space exploration of negative capacitance ferroelectric field-effect transistors (FeFETs) for nonvolatile memory operations was performed, combining load line analyses and circuit simulations. Unlike those FeFETs aiming at a steep subthreshold slope, the key design target here is to achieve bi-stable current versus voltage FET characteristics with appropriate hysteresis width (i.e. memory window). Remanent polarization, coercive voltage, and interfacial layer thickness were selected as design parameters. The results show that, if a ferroelectric gate dielectric film obeying ideal single-domain Landau–Khalatnikov model dynamics with reduced remanent polarization is available, ultralow voltage nonvolatile memories operating with sub-one volt voltage swing would become possible. An interesting feature of the negative capacitance FeFETs is that, unlike conventional multiple domain FeFETs, the memory window can be adjusted to a much smaller value than twice the coercive voltage. The lowered remanent polarization is required to suppress the depolarization field to an acceptable level for reliability. It is proposed that considering the abrupt polarization switching, three-transistor and two-transistor memory cells would be suitable for working and code storage memories, respectively. © 2021 The Japan Society of Applied Physics

1. Introduction

Today, the ferroelectric field-effect transistor (FeFET) is attracting research interest from multiple aspects. FeFET is a metal–insulator–metal FET (MISFET) whose gate insulator is, at least partly, composed of a ferroelectric film. It was first proposed as a nonvolatile memory device, which memorizes states "0" and "1" by the direction of polarization of the gate dielectric.[1,2] Later, the possibility of realizing a steep subthreshold slope lower than the thermal limit (i.e. 60 mV/decade at room temperature) using FeFETs (often called negative capacitance FETs, or NCFETs, in this context) was proposed.[3,4] Research activities in these two directions were accelerated by the discovery of hafnium oxide-based ferroelectric materials,[5,6] which are friendly to existing CMOS technology platforms.[7–11] For modeling FeFETs and ferroelectric capacitors, two different ferroelectricity models are typically used in the literature. One is a single domain Landau–Khalatnikov (LK) model,[3] and the other is the Preisach model of hysteresis.[12–14] In the LK model, ferroelectric dynamics is described using free energy U which is a simple polynomial function of electric polarization P having two minima. Using this model, P can be stable at only two values at most, given a fixed applied electric field. Negative capacitance ($dP/dV < 0$) is also predicted, which could be exploited to realize a steep subthreshold slope. On the other hand, the Preisach model assumes that a ferroelectric material is a collection of an infinite number of ideal hysteresis switches, whose positive and negative switching fields $E+$ and $E-$ ($E+ > E-$) are statistically distributed. As a result of this distributed nature, the material can retain some memory of the past history of the applied field. Depending on the history, for a given constant applied field, polarization P can be stable at any value between the fully polarized upper (positive) and lower (negative) limits. To summarize, the LK model is bi-stable, and the Preisach model is continuously stable. The former and latter correspond to two extreme cases of the single-polarization domain, and continuously distributed domains, respectively. Preisach model has been successfully used for modeling ferroelectric capacitors including those for commercial memory products,[15] which are relatively large in size, and therefore, believed to be containing multiple domains. On the other hand, abrupt polarization switching was reported for miniaturized 28 nm technology FeFETs.[16–18] This suggests that, by shrinking the area of FeFET gates, single-domain behavior would become possible, which would be necessary for achieving steep slope NCFETs.

Recently, the lower limit of operation voltage for one transistor (1T) cross point FeFET nonvolatile memory was analyzed by circuit simulations assuming Preisach type hysteresis.[19] Bit-wise programming and reading without using dedicated selector transistors was assumed, which is possible by using the cell transistors also as selector devices, exploiting the continuous nature of Preisach hysteresis. As a result, it was found that at least around ±2 V swing would be necessary, not including any variability and reliability margin, even after tailoring the ferroelectric characteristics of a reference $Hf_{0.5}Zr_{0.5}O_2$ capacitor. The necessity of relatively high voltage is also suggested based on experimental results.[18] On the other hand, simulation studies on nonvolatile FeFET memories based on the LK model are also reported.[20–24] Interestingly, it is reported that very low voltage (less than one volt) nonvolatile operation is possible. This suggests that LK-type hysteresis is attractive, not only for steep slope devices but also for realizing ultralow-power nonvolatile memories.

In this work, design space exploration was performed for LK-type FeFET nonvolatile memories using analytical and circuit simulation models. Remanent polarization, coercive voltage, and interfacial layer (IL) thickness were chosen as parameters. Device design considerations for realizing sub-1 V operating nonvolatile FeFET memories, as well as preferred memory cell structures, will be discussed. It should be pointed out here that there is still debate on the validity of the LK type FeFET model predicting steep subthreshold slope.[11] It is considered that the LK model, which is based on simple free energy considerations, would be a reasonable model

for describing the basic physics of ferroelectricity. However, as for real devices, very different behavior from LK model prediction is usually observed, such as nucleation-limited slow switching of FeFETs.[16,17] A possible reason for this discrepancy would be that, while the LK model may be valid for perfect bulk crystals, non-ideal effects originating in crystal boundaries, defects, etc. are dominating in real devices. Assuming the above explanation, it is considered that realization of LK-type FeFETs may be very difficult. By scaling down, it would be possible to achieve single crystal, single domain devices. However, crystal boundaries at the surfaces (top, bottom, and perimeter) still remain. The area over volume ratio even increases. The boundaries may hinder dipole switching, forming an additional barrier that must be overcome to switch the device, resulting in the non-LK model behavior. Therefore, to realize practical LK type operation of scaled devices, it would be required to develop a special material system at the surfaces that allows free motion of ferroelectric dipole as if there is no boundary. Nevertheless, the authors think that examining the outcome of the LK model is still of value since the LK model captures a fundamental microscopic aspect of ferroelectricity and that it is too early to deny the possibility of devices exploiting the ideal ferroelectric properties.

2. Modeling

A FeFET is modeled as a simple series connection of an LK type ferroelectric (FE) capacitor and a normal silicon n-channel MISFET [Fig. 1(a)], where the channel area and capacitor area are set to be equal. Capacitor voltage V_{FE} is assumed to be expressed as

$$V_{FE} = \left(\alpha P + \beta P^3 + \gamma \frac{dP}{dt}\right) T_{FE}, \quad (1)$$

where P is polarization and T_{FE} is ferroelectric film thickness. Electric displacement D is given by

$$D = \epsilon E + P, \quad (2)$$

where $E = V_{FE}/T_{FE}$ is capacitor electric field and ϵ is permittivity. Figure 1(b) shows the modeled D versus V_{FE} characteristics fitted to measured 10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ data (remanent polarization = 15.6 μC cm^{-2}, coercive field = 0.86 MV cm^{-1}).[19,25] Here, in addition to α and β, ϵ was treated as a fitting parameter to better reproduce the measured data, instead of setting ϵ equal to vacuum permittivity ϵ_0 ($\epsilon = 11.5\epsilon_0$). This is equivalent to slightly deforming the model Eq. (1). Only stationary states are considered here, and hence, the third term of the right-hand side of (1) is set to zero. Then, the effects of varying FE characteristics on FeFET behavior is examined by simply scaling the reference D versus V_{FE} curve in Fig. 1(b) both vertically and horizontally. The vertical and horizontal scaling factors will be denoted k_{PR} and k_{VC}, which change the remanent polarization P_R and coercive voltage V_C, respectively. Practically, P_R and V_C are governed by material properties, and therefore, may not be freely tunable. Nevertheless, to explore the theoretical possibility of FeFET memories, in this work, k_{PR} and k_{VC} are treated as adjustable parameters. As for the MISFET part, both analytical and circuit simulation models were used for convenience. The former was used for systematic mapping of hysteresis behavior, and the latter for confirming transistor hysteresis characteristics by circuit simulations. The lines labeled 1E15 and 1E18 in Fig. 1(c) show Si channel surface potential versus displacement D relationships by the analytical MIS diode model for two different substrate doping concentrations N_{SUB}. The curves are obtained by using the classical model,[26] and further taking into account quantum confinement effects by adding an extra surface insulating layer. The SiO_2-equivalent thickness of the layer is set to $\Delta T_{INV} = 0.4$ nm for inversion and $\Delta T_{ACC} = 0.6$ nm for accumulation. These values were selected such that quantum mechanical simulation results[27] can be approximately reproduced. For circuit simulations, 16 nm LSTP (low standby power) PTM-MG NMOS model for

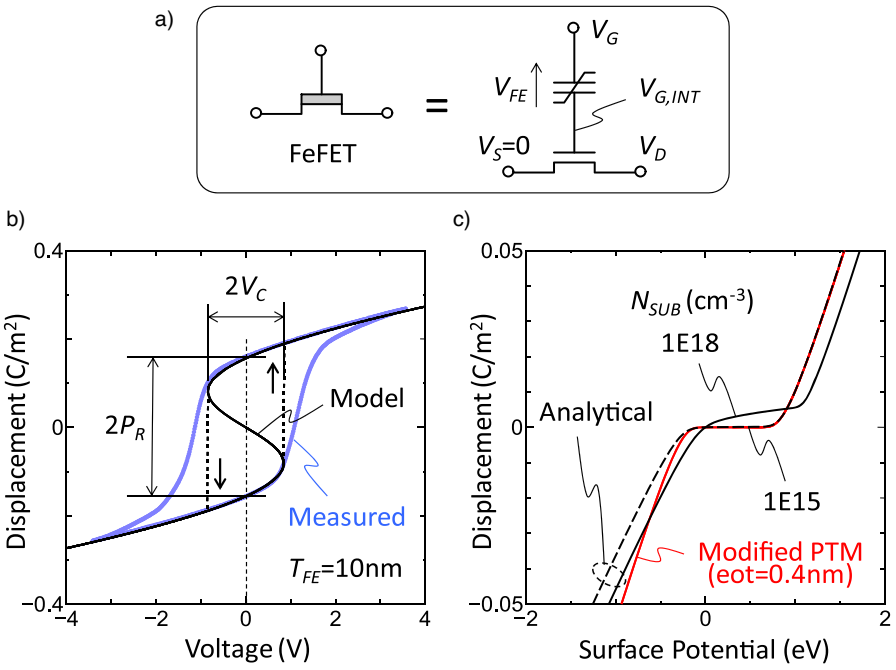

Fig. 1. (Color online) FeFET modeling method and model characteristics: (a) equivalent circuit model of a FeFET, (b) base FE capacitor model characteristics, and (c) MISFET model characteristics.

FinFETs,[28] which is based on BSIM-CMG,[29] was modified and used for the MISFET, and was combined with a Verilog-A code of the LK model. Similar to the previous work,[19] the following modifications of the PTM model were made. Firstly, gate leakage was disabled to ensure charge conservation at the floating node. Secondly, all gate-to-source and gate-to-drain fringe capacitances were set to zero. These modifications were made intending to eliminate side effects introduced by the floating electrode assumed in the model, which does not actually exist in a FeFET. In particular, the inclusion of the fringe capacitances will result in erroneously enlarged MIS capacitance and result in miscalculation of the capacitance matching effects. Thirdly, an equivalent oxide thickness parameter eot (originally 1 nm) was set equal to assumed IL thickness plus $\Delta T_{INV} = 0.4$ nm. Finally, originally disabled accumulation charge calculation was enabled by setting a switch parameter capmod = 1, since the MISFET may be used both in inversion and accumulation modes. The line labeled "Modified PTM" in Fig. 1(c) shows the resulting voltage versus displacement relationship for zero IL thickness (i.e. eot = 0.4 nm). Good agreement with the analytical model in the depletion and inversion conditions was confirmed, though there is disagreement in the accumulation condition since the BSIM model does not allow independent control of inversion and accumulation capacitances. Fortunately, this discrepancy will not be a problem for later discussions.

It should be pointed out here that the speed of the formation of an accumulation layer depends on the MISFET architecture; It will be fast in the bulk planer and bulk FinFETs (holes are supplied from the substrate), but very slow in floating body SOI FETs (holes are supplied only via carrier generation). Therefore, if only the use of SOI FETs is assumed, it could be possible to ignore the hole accumulation. However, in this work, it was decided to always take into account the accumulation mode, considering the wider usage of bulk FETs, including bulk FinFETs, today.

3. Hysteresis design

3.1. Dependence of hysteresis on design parameters

First, the dependence of the FeFET hysteresis behavior on P_R and V_C (or k_{PR} and k_{VC}), as well as the IL thickness T_{IL}, is examined using the analytical model. Referring to the FeFET model (Fig. 1), the following conditions must be satisfied:

$$D_{FE} = D_{MIS}, \tag{3a}$$

$$V_G = V_{FE} + V_{G,INT}, \tag{3b}$$

where D_{FE} and D_{MIS} are the electric displacements of the FE capacitor and MISFET, respectively. V_G and $V_{G,INT}$ are defined in Fig. 1(a). Based on these equations, load line analyses can be used, as shown in Fig. 2(a). The colored D_{FE} versus V_{FE} ferroelectric curve here was obtained by setting $k_{PR} = 0.5$ and $k_{VC} = 1.2$. Note that, compared with Fig. 1(b), the horizontal and vertical axes are swapped. V_G–$V_{G,INT}$ versus D_{MIS} load line curves by the MISFET analytical model for two constant V_G values of 0.12 V and 0.65 V are also shown; $N_{SUB} = 1 \times 10^{18}$cm^{-3}, $T_{IL} = 0$ [i.e. $V_{G,INT}$ equals surface potential in Fig. 1(c)] and flat band voltage $V_{FB} = 0$. It is well known that, by shifting the load lines up and down by changing V_G, and finding intersections with the D_{FE} versus V_{FE} curve (e.g. the squares and circles), FeFET D versus V_G relationships can be graphically obtained. Figure 2(a) can be easily converted into Fig. 2(b), by subtracting the load line curve for $V_G = 0$ from the FE curve, which further simplifies this process. Using figures as Fig. 2(b), displacement D (i.e. charge density) induced by a certain applied $V_G = V_{FE} + V_{G,INT}$ can be determined from the intersection(s) of a D versus V_G curve and a horizontal straight line. D thus obtained can then be translated, using Fig. 1(c), into MISFET surface potential, which is directly related to the FeFET channel conductance. In some cases, there are more than two intersections for one V_G value, which indicates the presence of hysteresis. As for this particular example of Fig. 2(b), it can be seen that, due to the complex D versus V_G curvature, there are two separate bi-stable ranges around $V_G = 0.12$ V (accumulation side) and $V_G = 0.65$ V (inversion side). Squares and circles show stable stationary points for $V_G = 0.12$ V and $V_G = 0.65$ V, respectively. Note that the other intermediate intersections are unstable. FeFET hysteresis behavior for various FE characteristics is shown in Fig. 3. Referring to Figs. 3(a) and 3(b), while there is no

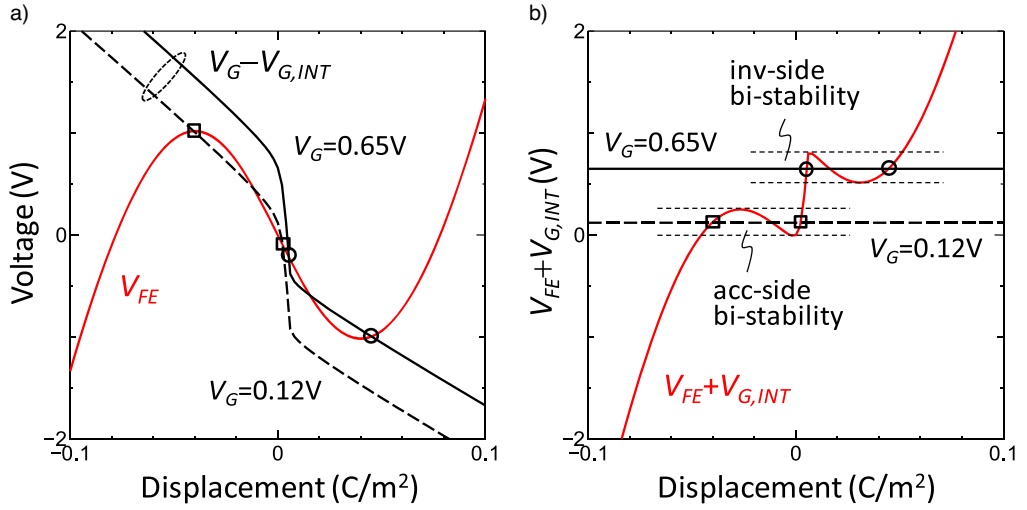

Fig. 2. (Color online) Method of analyzing hysteresis: (a) load line analysis example, and (b) D versus V_G (= V_{FE} + $V_{G,INT}$) characteristics obtained from (a).

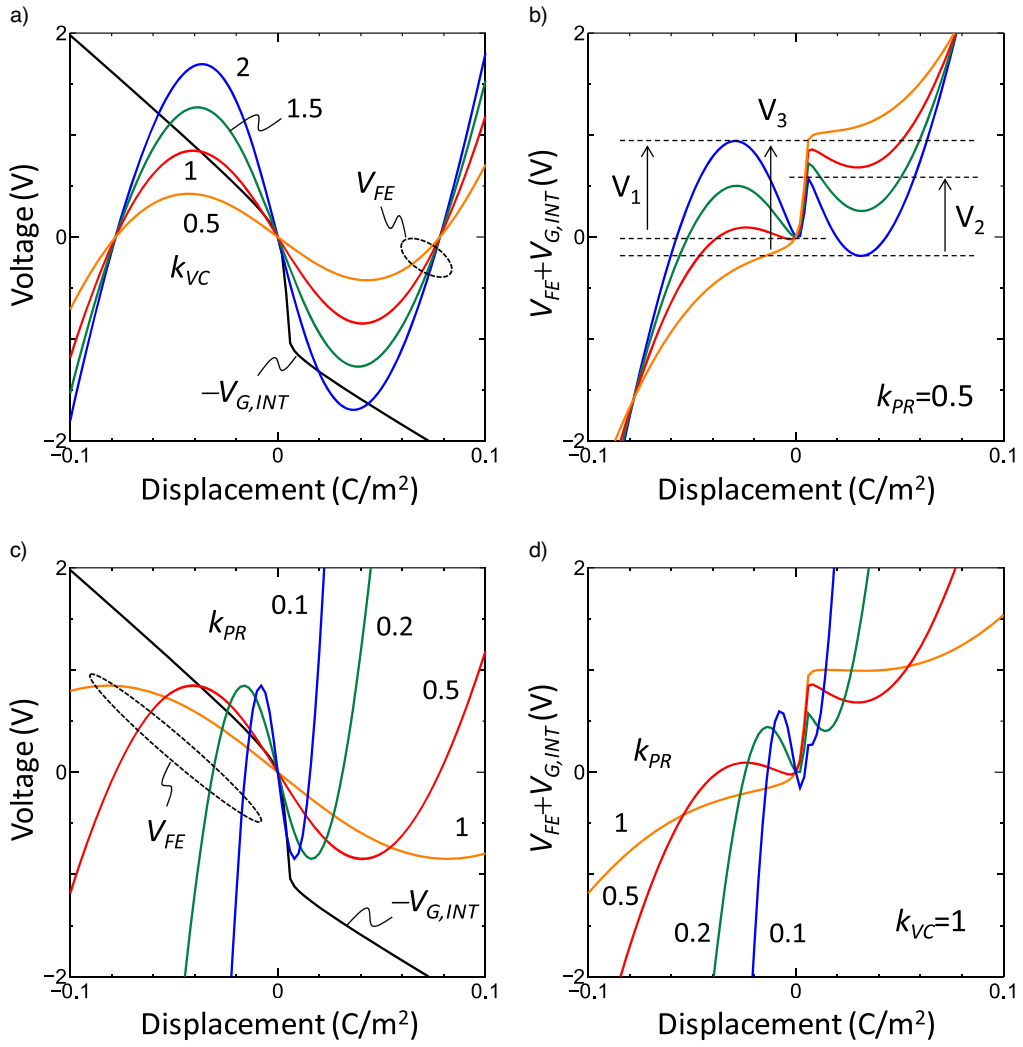

Fig. 3. (Color online) Hysteresis behavior examples for various combinations of k_{VC} and k_{PR}, $T_{IL} = 0$: (a) load line analyses for varied k_{VC}, (b) D versus V_G characteristics obtained from (a), (c) load line analyses for varied k_{PR}, and (d) D versus V_G characteristics obtained from (c). In (b), V_1, V_2, and V_3 for $k_{PR} = 0.5$ and $k_{VC} = 1$ (blue curve) are also shown.

hysteresis for $k_{VC} = 0.5$, two separate bi-stable voltage ranges coexist for $k_{VC} = 1$, one in inversion and the other in accumulation ranges. For increased k_{VC} of 1.5 and 2, two bi-stable voltage ranges are overlapped, resulting in the formation of tri-stability, though the intermediate stable point near $D = 0$ for $k_{VC} = 2$ cannot be reached by simply sweeping V_G up and down. Figures 3(c) and 3(d) show similar graphs for varied k_{PR}. Note that, though the curves in Figs. 2(b), 3(b), and 3(d) are complex, the origin of such behavior, including the tri-stability, can be readily understood graphically by turning back to the original load line charts [Figs. 2(a), 3(a) and 3(b)]. It should be also noted that the FeFET voltage hysteresis width in Figs. 2 and 3 is much smaller than twice the coercive voltage $2V_C$ of the FE capacitors. This is a distinctive feature of LK-type FeFETs caused by the negative capacitance characteristics.

Figure 3 shows that, depending on the ferroelectric and MISFET design parameters, FeFET D versus V_G characteristics will change in a complex manner. Figure 4 shows hysteresis types mapped on a k_{PR} versus k_{VC} plane for three combinations of N_{SUB} and T_{IL}. To obtain Fig. 4, the load line analyses were performed repeatedly by changing k_{PR} from 0.1 to 1.6, and k_{VC} from 0.1 to 2.0, respectively, both at an interval of 0.1. Then, hysteresis behaviors were classified into the following eight types:

(0) no hysteresis,
(1) accumulation only,
(2) inversion only,
(3) both, separated, $V_1 > V_2$,
(4) both, separated, $V_1 \leqslant V_2$,
(5) both, overlapped, $V_1 > V_2$,
(6) both, overlapped, $V_1 \leqslant V_2$,
(7) both, overlapped and extended, $V_3 > V_1$ and $V_3 > V_2$.

Here, V_1 and V_2 are hysteresis voltage swings in accumulation and inversion, respectively, and V_3 is a voltage swing between accumulation side maxima and inversion side minima (a swing of extended hysteresis). For example, V_1, V_2, and V_3 for $k_{PR} = 0.5$ and $k_{VC} = 2$ exhibiting type 7 behavior are shown in Fig. 3(b). All the eight types were found for $N_{SUB} = 1 \times 10^{18}$ cm^{-3} [Fig. 4(a)], while only five types for $N_{SUB} = 1 \times 10^{15}$ cm^{-3} [Fig. 4(b)]. These results can be explained as follows. Since D_{MIS} versus V_G slope is slightly steeper in inversion mode than accumulation ($\Delta T_{INV} < \Delta T_{ACC}$), V_2 tends to be larger than V_1. Hence, types (2), (4), and (6) hysteresis generally occurs. As for the higher N_{SUB} case, the bulk charge effect in depletion mode

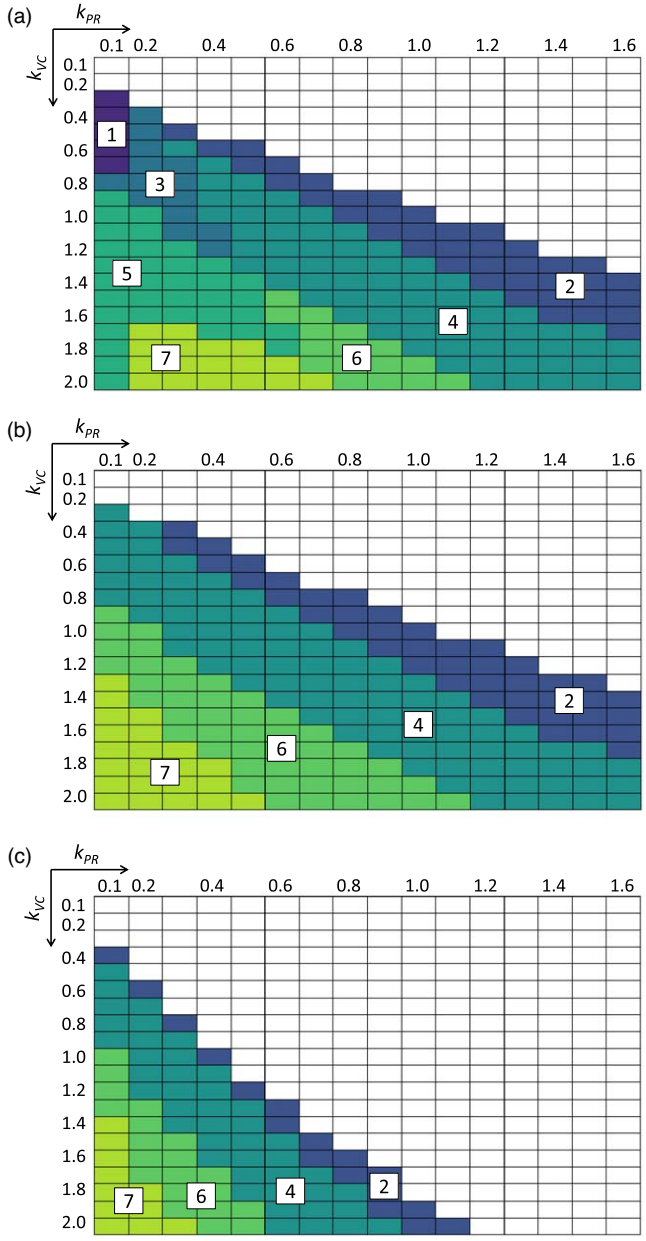

Fig. 4. (Color online) Hysteresis type maps for (a) $T_{IL} = 0$ and $N_{SUB} = 1 \times 10^{18}$ cm^{-3}, (b) $T_{IL} = 0$ and $N_{SUB} = 1 \times 10^{15}$ cm^{-3}, and (c) $T_{IL} = 0.6$ nm and $N_{SUB} = 1 \times 10^{15}$ cm^{-3}.

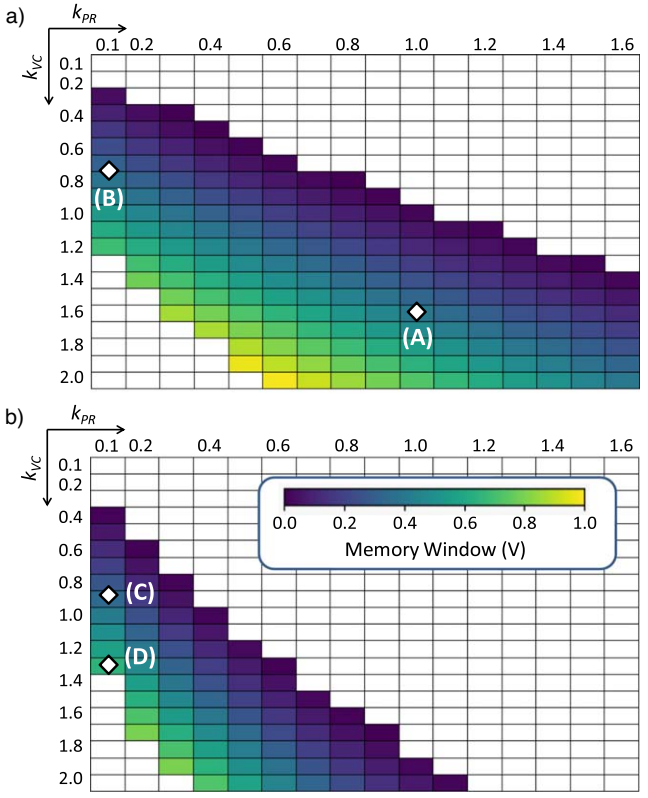

Fig. 5. (Color online) Maps of inversion-side memory window V_2 for (a) $T_{IL} = 0$ and (b) $T_{IL} = 0.6$ nm. $N_{SUB} = 1 \times 10^{15}$ cm^{-3}.

becomes important for low k_{PR} cases, resulting in hysteresis of types (1), (3), and (5). Insertion of a 0.6 nm IL decreased the k_{PR} range where hysteresis can be obtained [Fig. 4(c)], due to reduced steepness of D_{MIS} versus V_G slope. Figure 5 shows maps of hysteresis voltage swing of inversion side V_2. This corresponds to the so-called memory window, assuming that the inversion side hysteresis is utilized for memory operations. Only $N_{SUB} = 1 \times 10^{15}$ cm^{-3} results, where body charge is negligible, is considered hereafter, assuming FinFETs or fully depleted SOI FeFETs. Note that the memory window will be forced to be equal to V_3 for type 7 hysteresis characteristics. Therefore, the type 7 bins in Fig. 5 were left blank to avoid misinterpretation. It can be seen that the memory window can be flexibly controlled, and the desired value (e.g. 0.35 V for sub-1 V operation) can be obtained for a wide range of PR if V_C is appropriately selected (possibly by thickness tuning).

3.2. FeFET characteristics

Next, FeFET characteristics for specific choices of device parameters will be examined using the circuit simulation model, to make clear other design constraints and guidelines. Designs marked (A)–(D) in Fig. 5 will be focused on. Starting from design (A), Fig. 6 shows single fin FeFET current versus voltage characteristics and corresponding load line chart for $k_{PR} = 1$, $k_{VC} = 1.5$ and $T_{IL} = 0$ (eot = 0.4 nm). In Fig. 6(a), black curves show drain current I_D versus external gate voltage V_G characteristics of the FeFET, obtained by sweeping V_G from -0.5 to 0.5 V, and back to -0.5 V using transient simulation. Drain voltage V_D is fixed to 50 mV. To align the hysteresis center to $V_G = 0$, the threshold voltage of the MISFET was adjusted by -0.24 V ($V_{FB} = -0.54$ V), assuming the availability of work function engineering of the gate stack. The corresponding I_D versus internal gate voltage $V_{G,INT}$ trace is also shown in Fig. 6(a) by purple marks, which lies on the static I_D versus $V_{G,INT}$ curve of the base MISFET shown by gray marks. The corresponding trace of D_{FE} versus V_{FE} on the load line chart during the sweep is shown by blue marks in Fig. 6(b), together with four load lines for $V_G = \pm 0.5$ V and the two positive and negative switching gate voltages V_{G+} and V_{G-}. For the above three traces, arrows show discontinuous off-to-on (solid) and on-to-off (dotted) transitions due to hysteresis. Referring to Fig. 6(b), the off-to-on transition occurs when V_G increases to $V_{G+} = +0.18$ V, and the intersection near the origin disappears. Similarly, the on-to-off transition occurs when V_G decreases to $V_{G-} = -0.18$ V, and the intersection in the upper-left portion of the S-shaped FE curve disappears. It can be confirmed that a 0.35 V memory window can be obtained with $k_{PR} = 1$, in agreement with Fig. 5(a) [marked

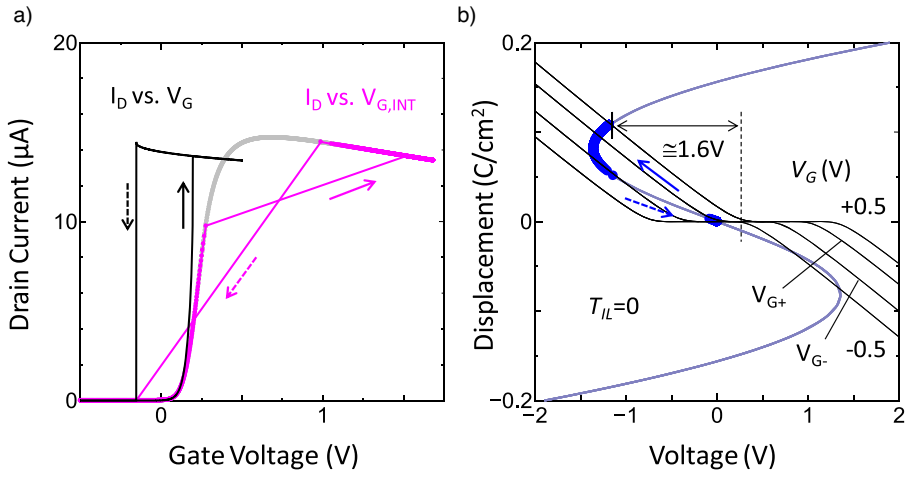

Fig. 6. (Color online) FeFET characteristics for $k_{PR} = 1$, $k_{VC} = 1.6$, $T_{IL} = 0$, and $V_{FB} = -0.60$ V: (a) current versus voltage curves and (b) load line chart. Corresponds to point (A) in Fig. 5. Off-state stable point in (b) stays close to the origin.

as design (A)]. It can be also confirmed that the accumulation side hysteresis does not interfere with this operation. However, there is a serious concern about this design; a high internal gate voltage of around 1.6 V is applied to the MISFET inversion layer of only 0.4 nm equivalent thickness at $V_G = +0.5$ V, as indicated in Fig. 6(b). The negative transconductance (i.e. abnormal mobility degradation) seen in Fig. 6(a) is a result of this unusually high gate electric field that lies outside the validity range of the compact MISFET model.

To reduce the electric field stress on the MISFET gate, it is required to lower the remanent polarization P_R, or k_{PR}. Figure 7 shows inversion side displacement at $V_G = 0.35$ V versus k_{PR} for those designs satisfying $V_2 = 0.35$ V calculated using the analytical model. V_G was set to 0.35 V, since, from variability margin considerations, ±0.35 V would be a reasonable choice of positive and negative write voltages for the 0.35 V memory window centered at $V_G = 0$. Figure 7 shows that the displacement D monotonically increases with k_{PR}. Roughly assuming that D must be kept lower than [SiO_2 dielectric constant] × 0.7 V/1 nm = 0.024 C m^{-2}, which is typical for state-of-the-art high-k/metal gate CMOS technologies, Fig. 7 shows that k_{PR} should be reduced to around 0.2 or less. Figures 8 and 9 show FeFET characteristics for designs (B) and (C) in Fig. 6, where k_{PR} is set to 0.1. It is confirmed that the target memory window can be obtained for both $T_{IL} = 0$ (eot = 0.4 nm) and 0.6 nm (eot = 1 nm) while keeping the gate field stress to sufficiently low levels. Another benefit of reducing k_{PR} would be that it makes the use of an IL possible, which will be beneficial for obtaining good interface quality.

Figure 10 shows FeFET characteristics for design (D), which has an enlarged memory window of 0.65 V and 0.6 nm IL. This is achieved by increasing k_{VC} from Fig. 9 and would be useful for realizing high-density memory cells as discussed later. Since this design is close to the type 7 range, accumulation side hysteresis now interferes with its operation. When V_G decreases to V_{G-}, the stable point in the upper-left portion of the S-shape disappears, and the FeFET will switch to the stable point near the origin, similarly to Figs. 6–8. In addition, when V_G further decreases to −0.5 V, the stable point near the origin also disappears, and the

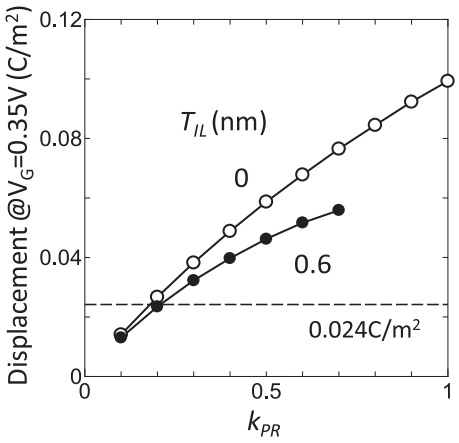

Fig. 7. Displacement at $V_G = 0.35$ V versus k_{PR} for designs satisfying $V_2 = 0.35$ V.

FeFET now switches to an accumulation side stable point located in the lower-right portion of the S-shape. Fortunately, it is considered that this is not a serious problem in this particular case, since the FeFET can be safely driven back to the inversion side stable point by applying $V_G = +0.5$ V If an SOI FET is used, this accumulation side switching would be avoided.

4. Discussion

In this section, based on the results described above, possible cell structures for the LK type FeFET memories are discussed to illustrate the practical value that the devices could provide. For Preisach type FeFETs, it is possible to choose a high-density 1T type cell as shown in Fig. 11(a). To read the cells in a selected row, a higher voltage is applied to the selected word line, whereas, a lower voltage is applied to the unselected word lines. This suppresses the current flow through unselected cells and makes it possible to distinguish the FeFET conductance of the selected cells without being interfered with by the unselected cells.[19] In this operation, the cell transistors function not only as a memory device but also as a selector device. This is possible since the FeFET conductance can be modulated by several orders without losing its memory content, though the memory may be weakened, thanks to the continuous nature of the Preisach

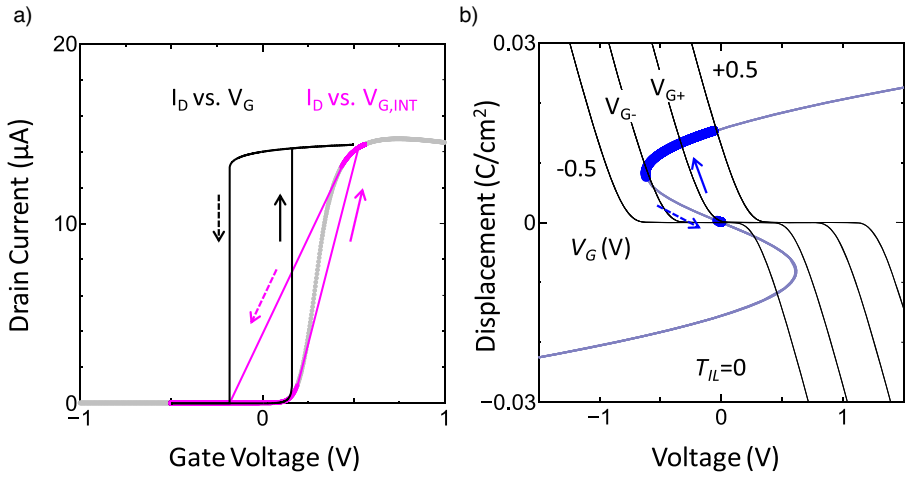

Fig. 8. (Color online) FeFET characteristics for $k_{PR} = 0.1$, $k_{VC} = 0.73$, $T_{IL} = 0$, and $V_{FB} = -0.54$ V: (a) current versus voltage curves and (b) load line chart. Corresponds to point (B) in Fig. 5.

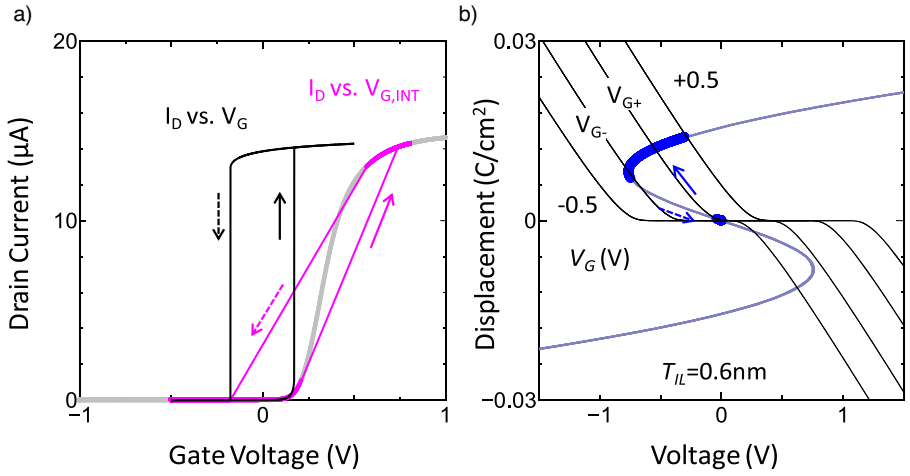

Fig. 9. (Color online) FeFET characteristics for $k_{PR} = 0.1$, $k_{VC} = 0.90$, $T_{IL} = 0.6$ nm, and $V_{FB} = -0.52$ V: (a) current versus voltage curves and (b) load line chart. Corresponds to point (C) in Fig. 5. Almost the same current–voltage characteristics as Fig. 8 in spite of insertion of IL.

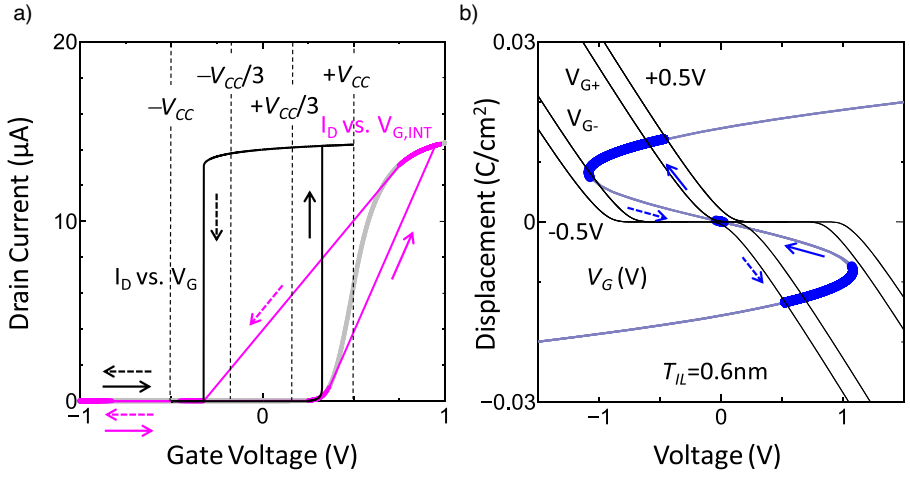

Fig. 10. (Color online) FeFET characteristics for $k_{PR} = 0.1$, $k_{VC} = 1.28$, $T_{IL} = 0.6$ nm, and $V_{FB} = -0.35$ V: (a) current versus voltage curves and (b) load line chart. Corresponds to point (D) in Fig. 5. Fast formation of accumulation layer is assumed.

type hysteresis. However, as for the LK type FeFETs, using a memory FeFET also as a selector device is not possible due to the abrupt switching between the stable states. Sufficient conductance change cannot be realized without destroying the memory content. Therefore, for the LK type FeFET memories, a three-transistor (3T) type memory cell[30] [Fig. 11(b)] would be appropriate. FeFET characteristics as shown in Figs. 8 and 9 will be suited to be used here. By using this cell, voltage mode read and write operations similar to standard six-transistor (6T) SRAMs are possible.

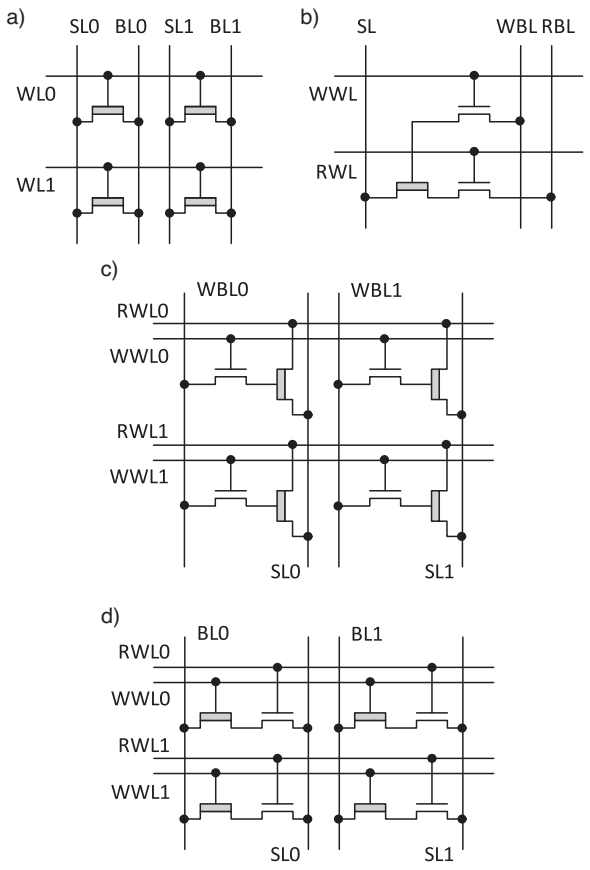

Fig. 11. FeFET memory cell structures: (a) 1T, (b) 3T, (c) 2T with write selector, and (d) 2T with read selector.

Table I. Voltage control sequence of 1/3–2/3 V_{CC} scheme.

Time	0	1	2	3	4	5	6
BL0/SL0	0	0	0	0	0	0	0
BL1/SL1	0	0	2/3	2/3	2/3	0	0
WWL0	0	1/3	1/3	1	1/3	1/3	0
WWL1	0	1/3	1/3	1/3	1/3	1/3	0

Note. Numbers show voltage normalized by $\pm V_{CC}$ defined in Fig. 10(a). This sequence will selectively write top-left cell of Fig. 11(d).

Therefore, the 3T LK type FeFET memories will be suitable for replacing 6T-SRAMs.

For achieving higher density, a two-transistor (2T) cell was also proposed [Fig. 11(c)] assuming LK type hysteresis.[20] Here, the read selector transistor in Fig. 11(b) is removed, and a current mode sensing scheme is adopted for reading. By applying a voltage only to a selected read word line (e.g. RWL0), grounding all other RWLs, the current flowing into a sense line (e.g. SL0) is detected using a current sense amplifier, whose input terminal is virtually grounded. A drawback of this reading method would be that the input offset voltage of the sense amplifier caused by variability must be suppressed to an extremely low level. Only a small offset voltage (e.g. between RWL1 and SL0) will cause significant stray current via unselected cells belonging to the same sense line since a few hundred or more cells are usually connected to one sense line. Therefore, an alternative type of 2T cell,[31] as shown in Fig. 11(d) would be more appropriate. In this cell, instead of the read selector, the write selector in the 3T cell is removed. This is possible by adopting a 1/3–2/3 V_{CC} writing scheme,[8] combined with wide hysteresis characteristics as in Fig. 10. By manipulating the source lines and write word lines as shown in Table I, a specific target bit can be driven to either high or low states without changing states of the other bits, by keeping the non-target bit gate-to-source/drain voltage within the range of $\pm V_{CC}/3$. This type of memory cell would be typically suited for use in code storage memories, where frequent writing is not necessary.

5. Conclusion

If LK-type FeFETs with appropriate characteristics become available, it is anticipated that nearly ideal nonvolatile working memories, which are low power, high speed, and randomly accessible would become possible. Negative capacitance ferroelectricity is attractive not only for steep slope logic applications, but also for memory applications.

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