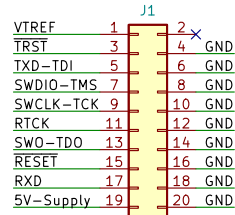
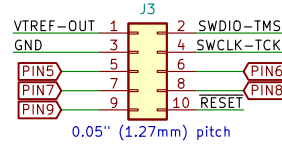
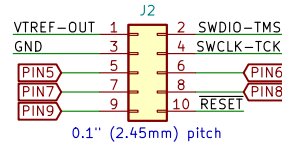


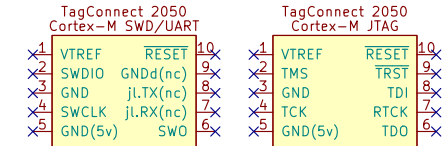
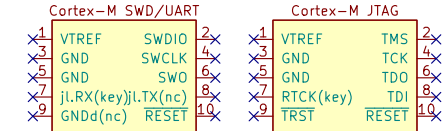
J-LINK INPUT HEADER



SWD/JTAG OUTPUT HEADERS

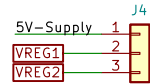


HEADER REFERENCES FOR TARGET BOARD



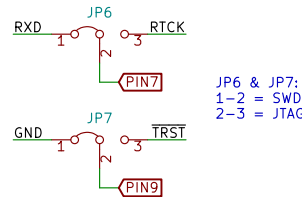
The connectors above slightly differ from the pinout of the default J-Link connectors. The original pinout is put in brackets: (key) (this is normally not populated), (nc) and (5v). SEE JUMPERS JP3-4-6-7 TO RECONFIGURE THESE PINS IF NECESSARY.

DC-DC CONVERTER HEADER



(not plugged in = disabled)

SWD/JTAG MODE SELECTION

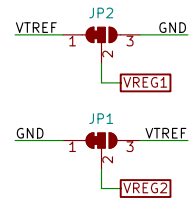


INLINE CURRENT MEASURING JUMPER

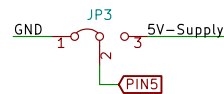


The target gets power from the adapter through VTREF(-OUT) if the DC-DC converter is plugged in.

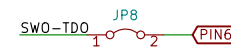
DC-DC CONVERTER PINOUT SELECTION



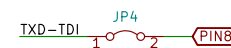
PIN 5 MODE SELECTION



PIN 6 DISCONNECT



PIN 8 DISCONNECT



BEST PRACTICES

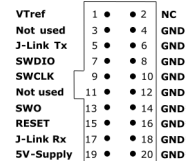
Use the 0.05" pinheader for 'regular' development and the TagConnect cable for fast, on-location reprogramming.

GNDdetect (GNDd) can be used by the target board to detect if a debugger is present. (pin 9 is in SWD mode connected to GND)

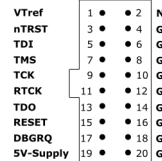
Put a 100 kΩ pullup resistor on the SWDIO line and a 10 kΩ pullup resistor on the RXD line of the target board.

If RTCK is not available on the target board it should be connected to GND.

J-Link 20-pin SWD + VCOM



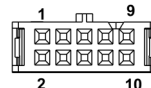
J-Link 20-pin JTAG



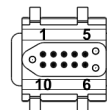
DBGRQ = NC inside J-Link

TagConnect 2050

END VIEW
2x5 0.1" PITCH
IDC CONNECTOR



END VIEW
10 PIN
TAG-CONNECT



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adapter.brechtve.be

Brecht Van Eeckhoudt

Sheet: /

File: [jlink-tagConnect-adapter-v3.sch](#)

Title: Universal J-Link Adapter

Size: A4

Date: 2020-11-26

KiCad E.D.A. kicad 5.1.5-52549c586ubuntu19.04.1

Rev: v3.0

Id: 1/1

