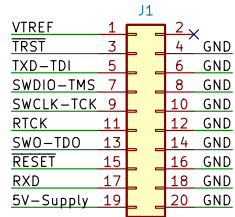
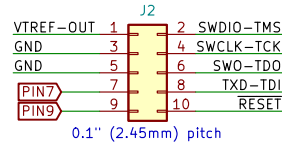


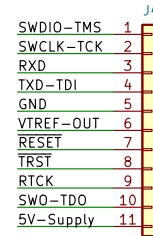
# J-LINK INPUT HEADER



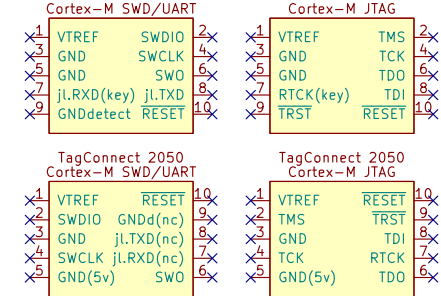
# SWD/JTAG OUTPUT HEADERS



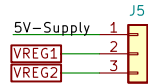
# SWD/JTAG BREAKOUT HEADER



# HEADER REFERENCES FOR TARGET BOARD

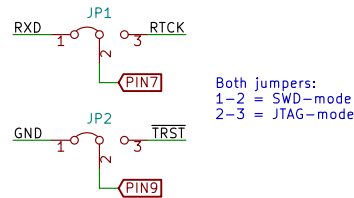


# DC-DC CONVERTER HEADER

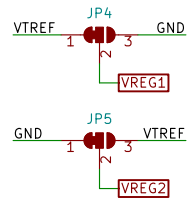


(not plugged in = disabled)

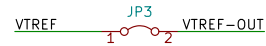
# SWD/JTAG MODE SELECTION



# DC-DC CONVERTER PINOUT SELECTION



# INLINE CURRENT MEASURING JUMPER



# BEST PRACTICES

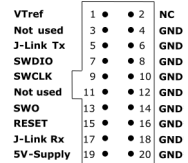
Use the 0.05" pinheader for 'regular' development and the TagConnect header for fast on-location reprogramming.

GNDdetect can be used by the target board to detect if a debugger is present. (pin 9 in SWD mode connected to GND)

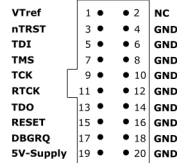
Put a 100 kΩ pullup resistor on the SWDIO line and a 10 kΩ pullup resistor on the RXD line on the target board.

If RTCK is not available on the target board it should be connected to GND.

# J-Link 20-pin SWD + VCOM

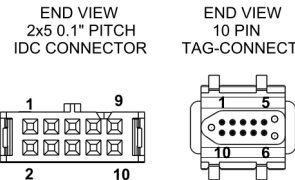


# J-Link 20-pin JTAG



DBGRQ = NC inside J-Link

# TagConnect 2050



# Copyright © Brecht Van Eeckhoudt 2019

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2.

You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (<http://ohwr.org/cernohl>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions.

If you choose to manufacture products based on this design, please notify me (see licence section 4.2) via [mail@brechtve.be](mailto:mail@brechtve.be)

[adapter.brechtve.be](mailto:adapter.brechtve.be)

**Brecht Van Eeckhoudt**



Sheet: /

File: jlink-tagConnect-adapter-v2.sch

**Title: J-Link / Tag-Connect adapter board**

Size: A4

Date: 2019-11-25

Rev: v2.0

KiCad E.D.A. kicad 5.1.5-52549c584ubuntu19.04.1

Id: 1/1

