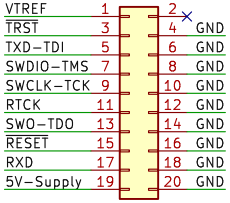
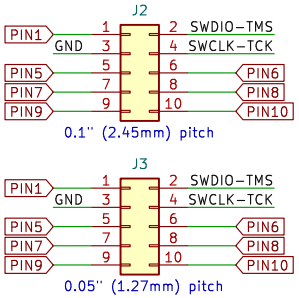
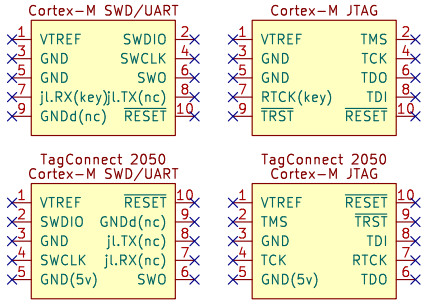
J-LINK INPUT HEADER



SWD/JTAG OUTPUT HEADERS

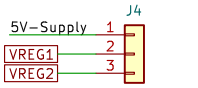


HEADER REFERENCES FOR TARGET BOARD



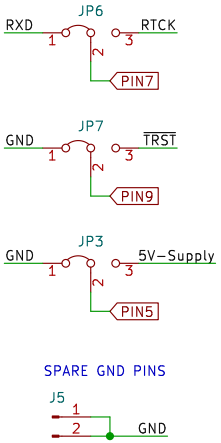
The connectors above slightly differ from the pinout of the default J-Link connectors. The original pinout is put in brackers: (key) (this is normally not populated), (nc) and (5v). SEE JUMPERS JP3-4-6-7 TO RECONFIGURE THESE PINS IF NECESSARY.

VOLTAGE CONVERTER HEADER

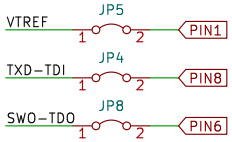


(not plugged in = disabled)

PIN MODE SELECTION



PIN DISCONNECTS



BEST PRACTICES

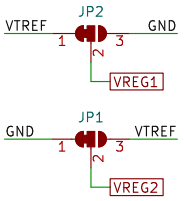
Use the 0.05" pinheader for 'regular' development and the TagConnect cable for fast, on-location reprogramming.

GNDdetect (GNDd) can be used by the target board to detect if a debugger is present. (pin 9 is in SWD mode connected to GND)

Target board resistors:
- 10 kΩ pullup: SWDIO|TMS, RXD TDO, TDI
- 10 kΩ pulldown: SWCLK|TCK

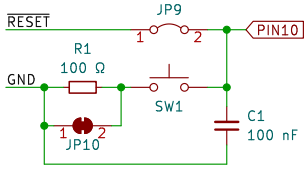
If RTCK is not available on the target board it should be connected to GND.

VOLTAGE CONVERTER PINOUT SELECTION

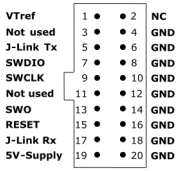


SPARE GND PINS

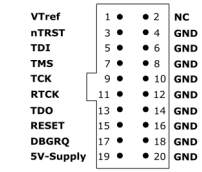
RESET DISCONNECT / BUTTON



J-Link 20-pin SWD + VCOM

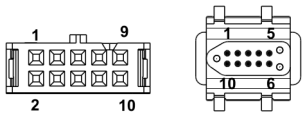


J-Link 20-pin JTAG



DBGRQ = NC inside J-Link

TagConnect 2050



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Sheet: /
File: jlink-tagConnect-adapter-v4.kicad_sch

Title: Universal J-Link Adapter

Size: A4	Date: 2024-07-20	**Rev: v4.0**
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1		Id: 1/1