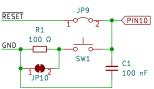
J-LINK INPUT HEADER SWD/JTAG OUTPUT HEADERS HEADER REFERENCES FOR TARGET BOARD 2 SWDIO-TMS TRST 4 SWCLK-TCK TXD-TDI 6 GND SWDIO-TMS 7 PIN7 SWCLK-TCK 9 10 GND RTCK 12 GND 0.1" (2.45mm) pitch SWO-TDO 14 GND RESET 16 GND 18 GND 2 SWDIO-TMS 4 SWCLK-TCK RXD 20 GND 5V-Supply 19 0.05" (1.27mm) pitch The connectors above slightly differ from the pinout of the default J-Link connectors. The original pinout is put in brackers: (key) (this is normally not populated), (nc) and (by). SEE JUMPERS JP3-4-6-7 TO RECONFIGURE THESE PINS IF NECESSARY. VOLTAGE CONVERTER HEADER PIN MODE SELECTION PIN DISCONNECTS 5V-Supply (not plugged in = disabled) BEST PRACTICES Use the 0.05" pinheader for 'regular' development and the TagConnect cable for fast, on-location reprogramming. VOLTAGE CONVERTER PINOUT SELECTION GNDdetect (GNDd) can be used by the target board to detect if a debugger is present. (pin 9 is in SWD mode connected to GND) RESET DISCONNECT / BUTTON PIN10 Target board resistors: R1 - 10 kΩ pullup: SWDIO|TMS, RXD TDO, TDI 100 Ω GND - 10 kΩ pulldown: SWCLK|TCK SPARE GND PINS SW1







	Cortex-M SWD/UAR	Cortex-M JIAG			
×1 ×3 ×5 ×7 ×9	VTREF SWDIO GND SWCLK GND SWO jl.RX(key)jl.TX(nc) GNDd(nc) RESET	2 × 1 4 × 3 6 × 5 8 × 7 10 × 9	VTREF GND GND RTCK(key)	TMS TCK TDO TDI RESET	2× 4× 6× 8× 10×
TagConnect 2050 Cortex-M SWD/UART			TagConnec Cortex-M	t 2050 I JTAG	
×1 ×2 ×3 ×4 ×5	VTREF RESET SWDIO GNDd(nc) GND jl.TX(nc) SWCLK jl.RX(nc)	10 ×1 9 × ×2 8 × ×3 7 × ×4	VTREF TMS GND TCK	RESET TRST TDI RTCK	10× 9× 8× 7

If RTCK is not available on the target board it should be connected to GND.

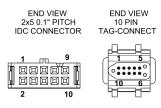
J-Link 20-pin SWD + VCOM

	F		
VTref	1 •	• 2	NC
Not used	3 ●	• 4	GND
J-Link Tx	5 •	• 6	GND
SWDIO	7 •	• 8	GND
SWCLK	ິ 9 ●	• 10	GND
Not used	11 •	• 12	GND
swo	13 ●	• 14	GND
RESET	15 ●	• 16	GND
J-Link Rx	17 •	• 18	GND
5V-Supply	19 •	• 20	GND
			J

J-Link 20-pin JTAG

TMS TCK 9 • 10 GND RTCK _11 • • 12 GND 13 ● 14 GND RESET 15 ● 16 GND 17 ● 18 GND DBGRO 5V-Supply 19 ● 20 GND DBGRQ = NC inside J-Link

TagConnect 2050



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Brecht Van Eeckhoudt

Sheet: /

File: jlink-tagConnect-adapter-v4.kicad_sch

Title: Universal J-Link Adapter

S	ize: A4	Date: 20	24-07-20	Rev: v4.0		
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