|  |  |  |
| --- | --- | --- |
| 0000 | ADD REG A, REG B | R[A] 🡨 R[A] + R[B] set status flags NZVC |
| 0001 | SUB REG A, REG B | R[A] 🡨 R[A] – R[B] set status flags NZVC |
| 0010 | AND REG A, REG B | R[A] 🡨 R[A] & R[B] set status flags NVZC |
| 0011 | OR REG A, REG B | R[A] 🡨 R[A] or R[B] set status flags NZVC |
| 0100 | MOV REG A, REG B | R[A] 🡨 R[B] |
| 0101 | ADDI REG A, IMMED | R[A] 🡨 R[A] + IMMED] set status flags NZVC |
| 0110 | ANDI REG A, IMMED | R[A] 🡨 R[A] & IMMED] set status flags NZVC |
| 0111 | SL REG A, IMMED[3..0] | R[A] 🡨 R[A<<IMMED] zero fill LSB C and V affected |
| 1000 | SR REG A, IMMED[3..0] | R[A] 🡨 R[A>>IMMED] zero fill MSB |
| 1001 | LW REG A, IMMED[7..0] | R[A] 🡨 MEM[IMMED] |
| 1010 | SW REG A, IMMED[7..0] | MEM[IMMED] 🡨 R[A] |
| 1011 | LWV REG A, REG S, IMMED[3..0] | R[A] 🡨 ExMEM[R[S] + IMMED] when ID=**00** |
| 1100 | SWV REG A, REG S, IMMED[3..0] | ExMEM[R[S] + IMMED] 🡨 R[A] when ID=**00** |
| 1101 | JAL IMMED[11..0] | STK[SP+] 🡨 [PC], PC 🡨 IMMED[15..0] |
| 1110 | RTL IMMED | PC 🡨 STK[SP], SP 🡨 SP-1 |
| 1111 | BRA MASK, IMMED[7..0] | PC🡨 [PC]+IMMED, if MASK & NVZC true |
|  | **SPECIAL INSTRUCTIONS** |  |
| 1011 | LWVI REG A, REGS, ID=**10**, IMMED[3..0] | INSTMEM[REGA] 🡨 ExMEM[S[R] + IMMED] |
| 1011 | LWVD REG A, REGS, ID=**01**, IMMED[3..0] | DATAMEM[REGA]🡨ExMEM[S[R] + IMMED] |
| 1011 | LWVS REG A, REGS, ID=**11**, IMMED[3..0] | S[R] 🡨 R[A] + IMMED |
| 1100 | INT REG A, REGS=**11** enable, REGS=00 disable, ID=**11**, IMMED[3..0] | Interrupt Enabled/Disabled  Bit [3..0] interrupt lines |
| 1100 | SWED REG A, REGS, ID=**01**, IMMED[3..0] | ExMEM[S[R] + IMMED] 🡨 DataMem[REGA] |
| 1100 | SWEI REG A, REGS, ID=**10**, IMMED[3..0] | ExMEM[S[R] + IMMED] 🡨 InstructionMem[REGA] |