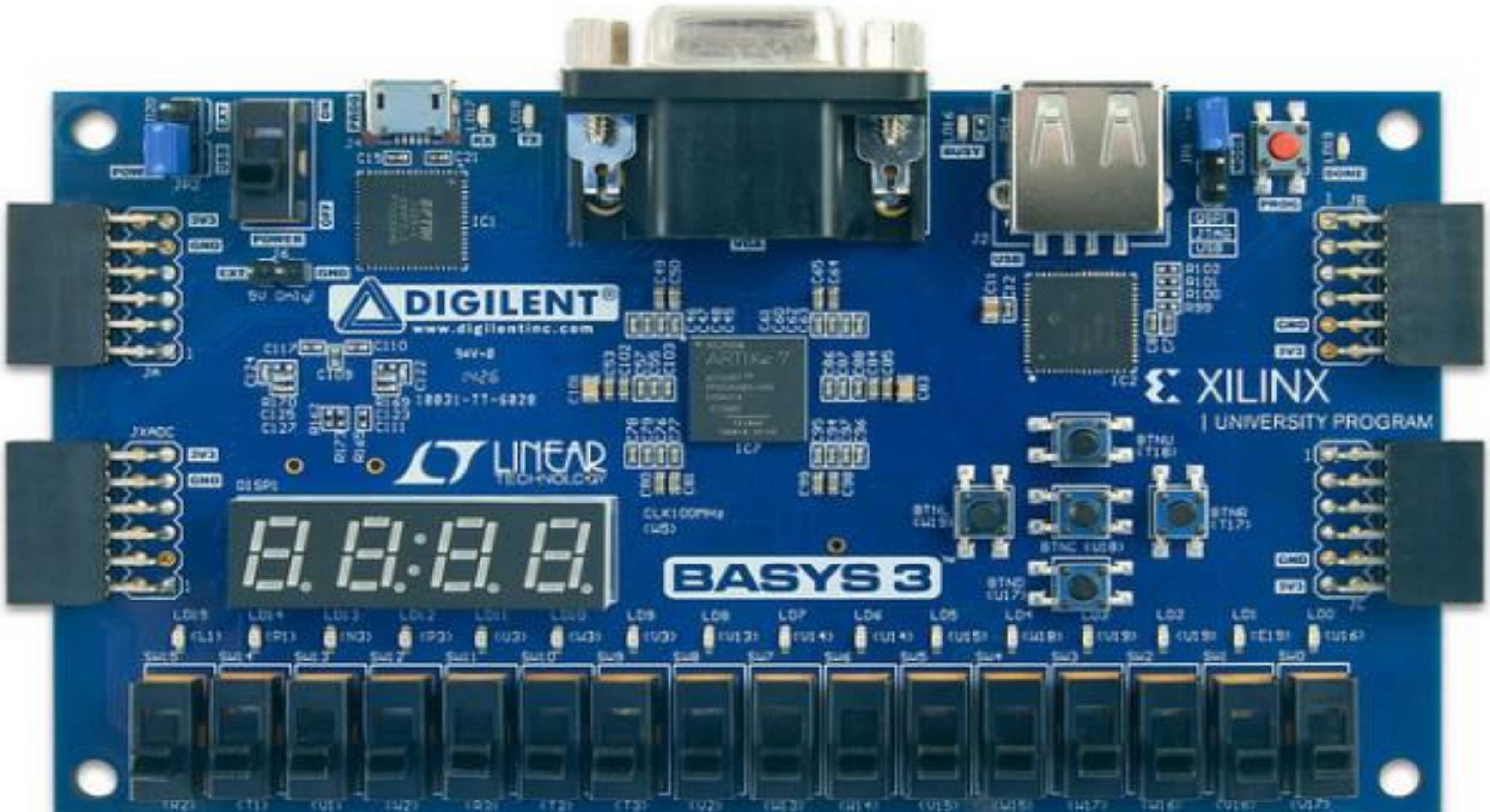
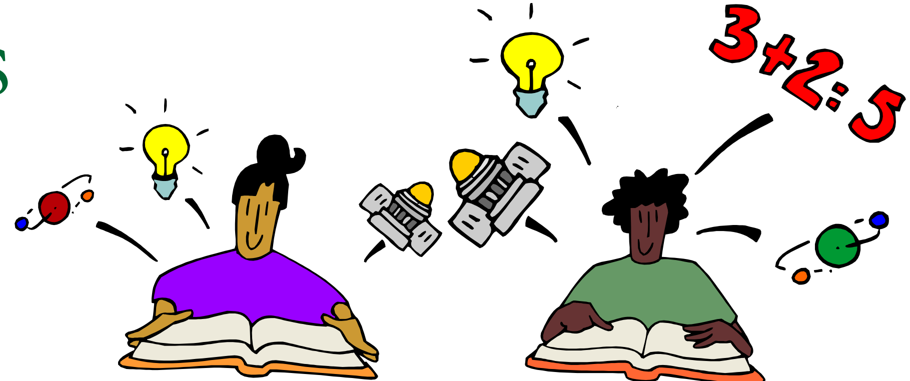


ECEG-2131 Applied Electronics I

Addis Ababa Institute of Technology (AAIT) School of Electrical and Computer Engineering

Addis Ababa University (Since 1950)

Learning Outcomes



- At the end of the lecture, students should be able to know about:
  - Operating Point.
  - Fixed-Bias Circuit.
  - Load-Line Analysis.
  - Emitter Bias Configuration.
  - Voltage-Divider Bias.

DC Biasing - BJTs

- Too often it is assumed that the transistor is a magical device that can raise the level of applied AC input without the assistance of external energy source.
- In actuality, any increase in voltage, current, or power is the result of a transfer of energy from applied DC supplies.
- **Biasing** is the application of DC voltages to establish a fixed level of current and voltage.
- The following relationships are basic in most analysis.

$$\boxed{V_{BE} \cong 0.7\text{ V}}$$

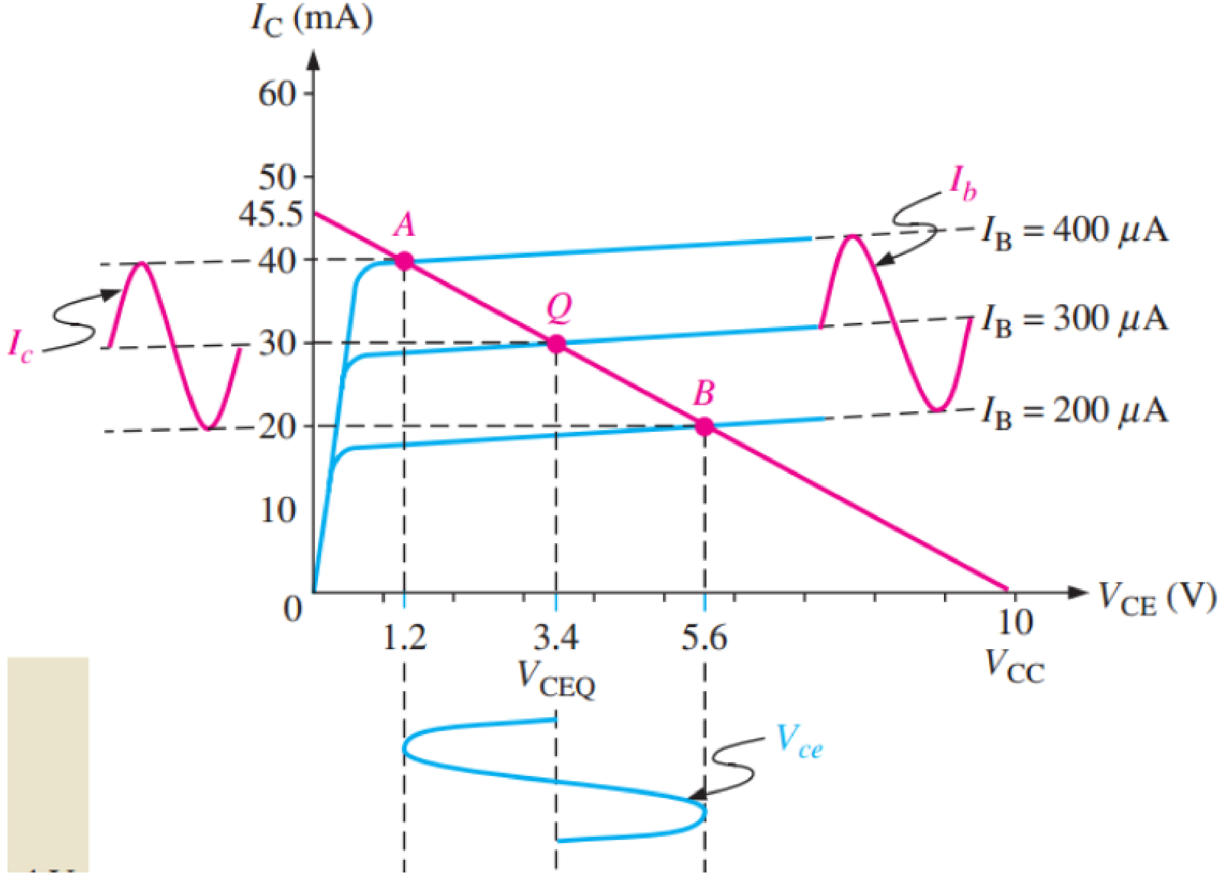
$$\boxed{I_E = (\beta + 1)I_B \cong I_C}$$

$$\boxed{I_C = \beta I_B}$$

- Once I_B is known, these relationships can be applied

DC Biasing - BJTs

- Bias establishes the operating point (Q-point) of a transistor amplifier; the ac signal moves above and below this point.



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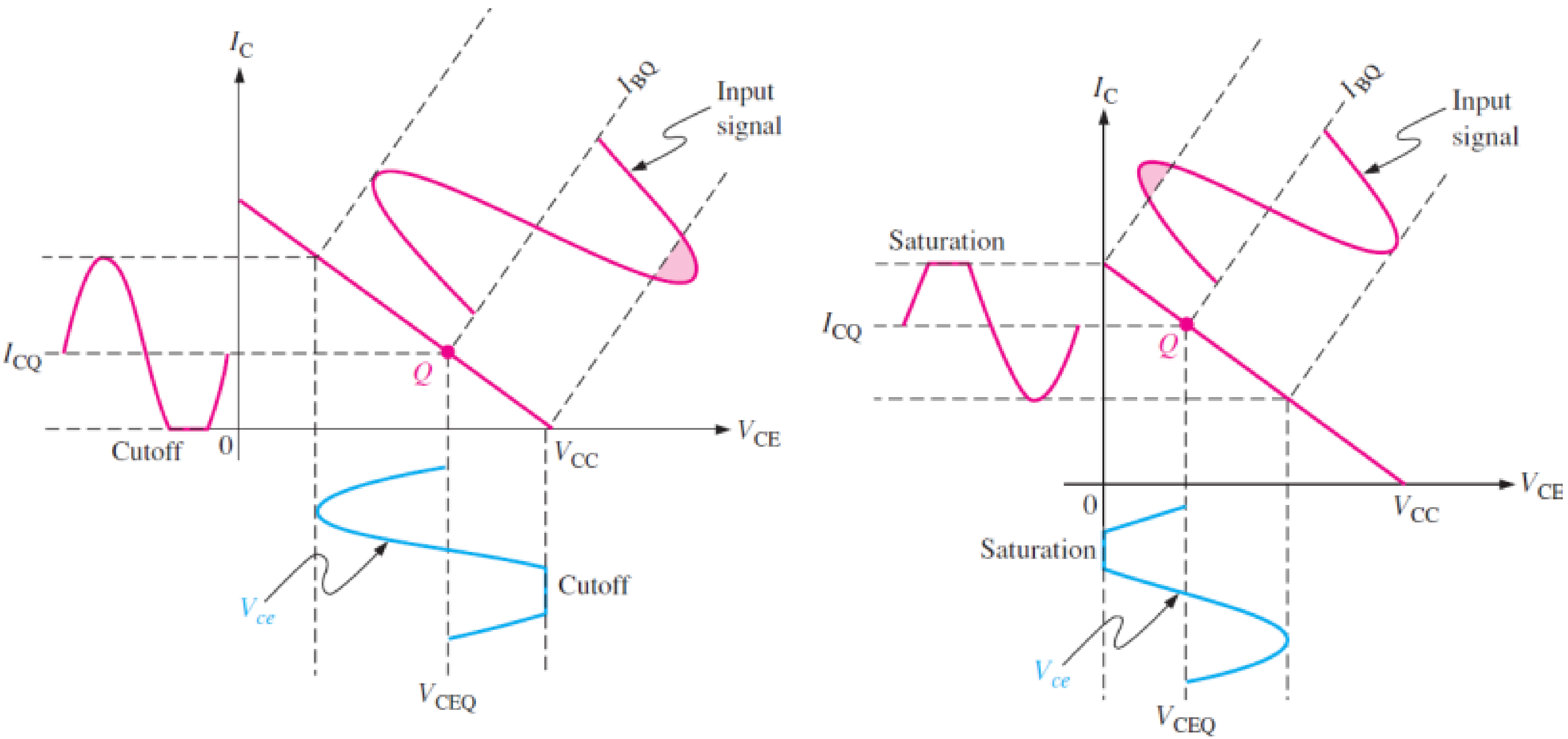
DC Biasing - BJTs

- A signal that swings outside the active region will be clipped.

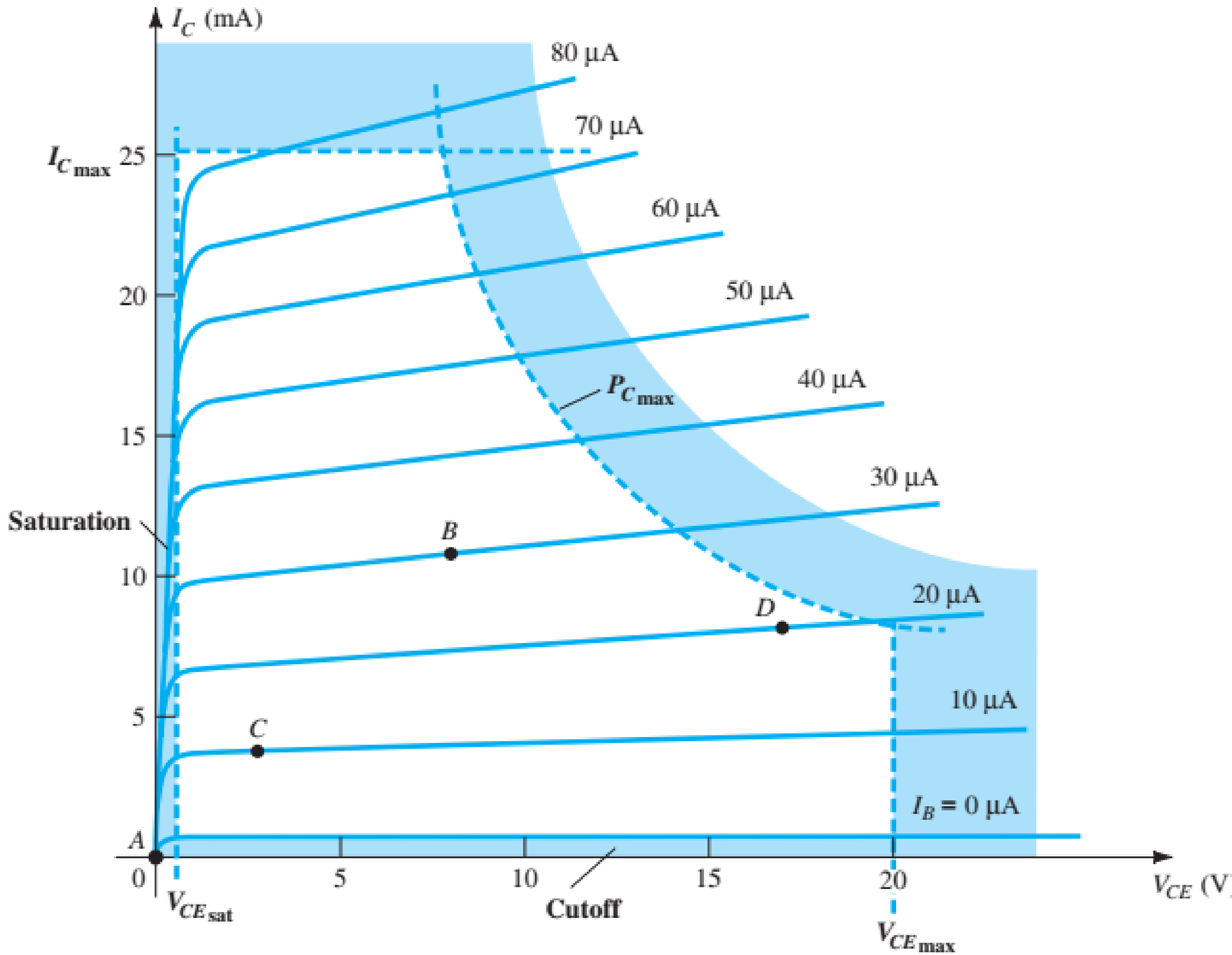


DC Biasing - BJTs

OPERATING POINT

BIASING

Application of dc voltages to establish a fixed level of current and voltage. (Q-point)



Operating Point

- Must NOT exceed the Maximum Rating of the transistor

$$I_{C\max} \qquad P_{C\max} \qquad V_{CE\max}$$

At point A:

Transistor “OFF”, zero current and voltage (not applicable)

At point B:

Center Point Biasing (applicable). Signal will swing in both Positive and Negative without entering into Cutoff or Saturation region.

At point C:

Applicable but not a good region since this will raise Nonlinearities to the output signal. Limitation of peak-to-Peak value of V_{CE}=0 Vand I_C=0 A.

Operating Point

At point D:

Applicable but not a good region also since this will sets the Device operating region near the maximum power.

Summary of the Biasing operation

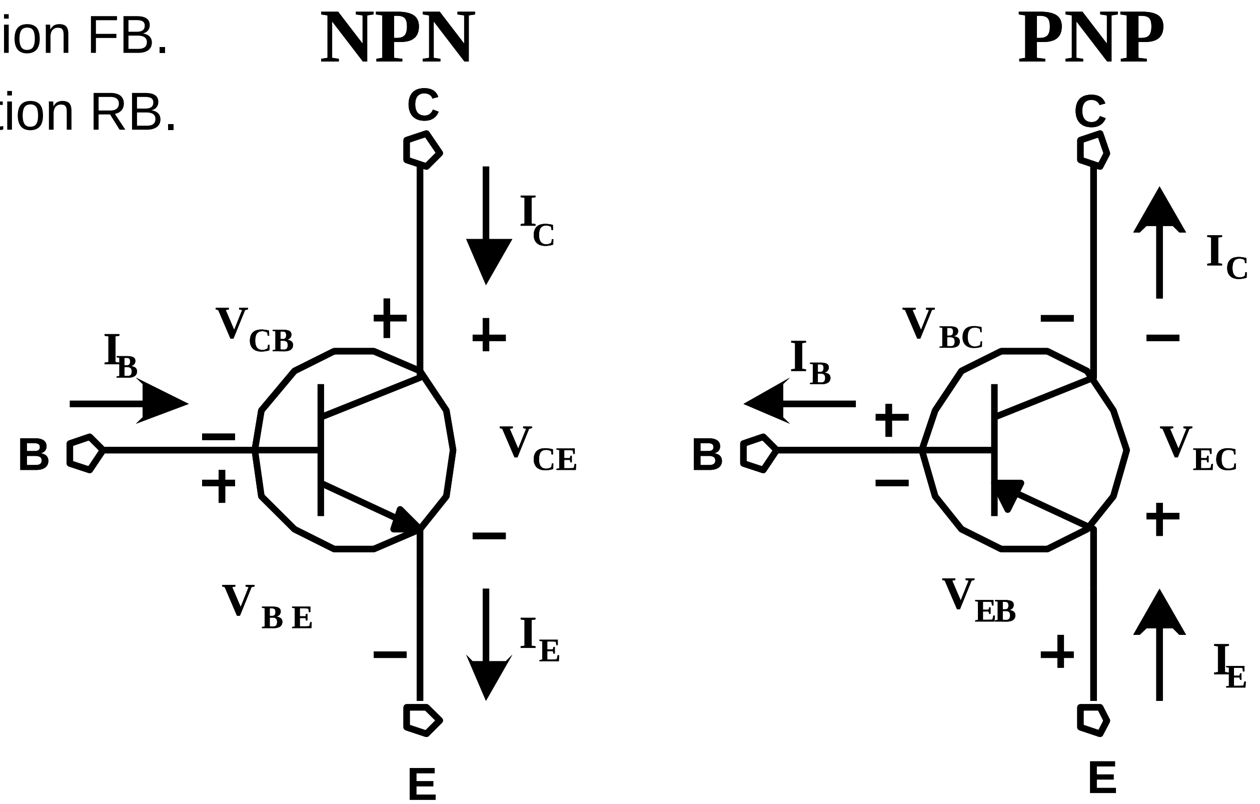
Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active (forward)	Forward	Reverse
Saturation	Forward	Forward

Standard Notation for Current and Voltage

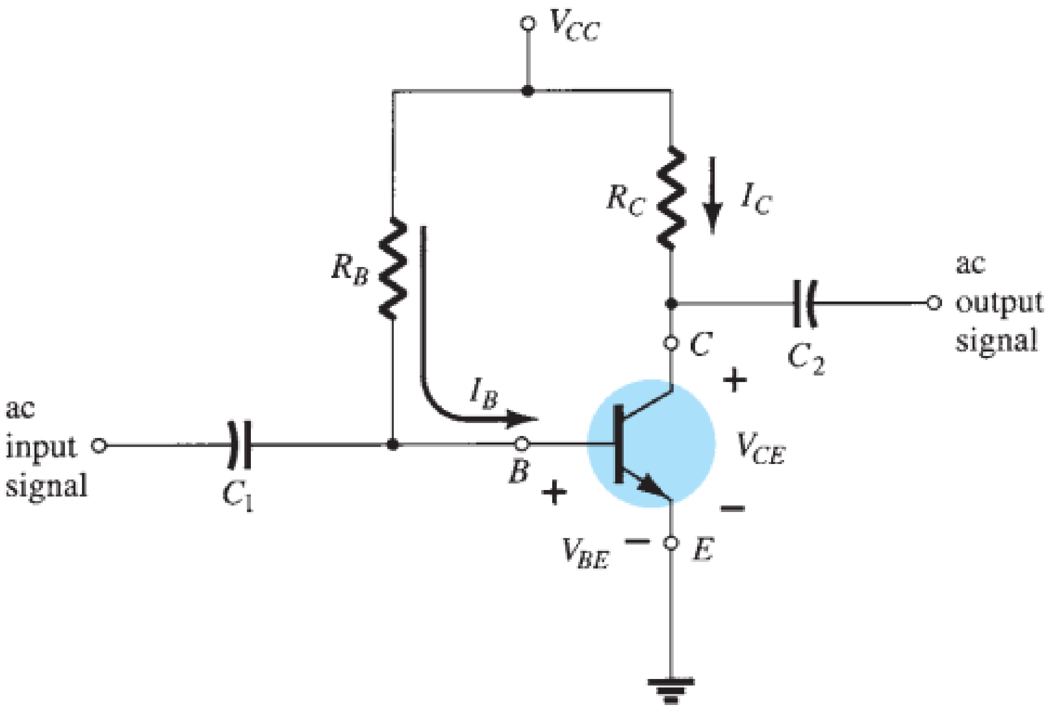
- For Linear (active) operation

    BE junction FB.

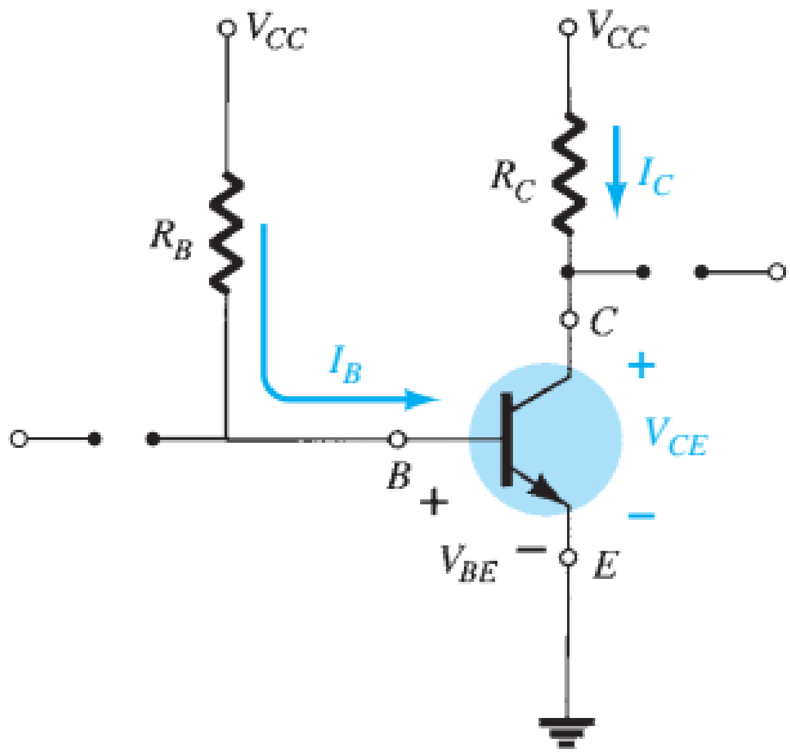
    BC junction RB.



Fixed-Bias Circuit Configuration



Fixed-Bias Circuit



DC Equivalent of Fixed-Bias

Fixed-Bias Circuit Configuration

Base-Emitter Loop:

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Collector-Emitter Loop:

$$I_C = \beta I_B$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

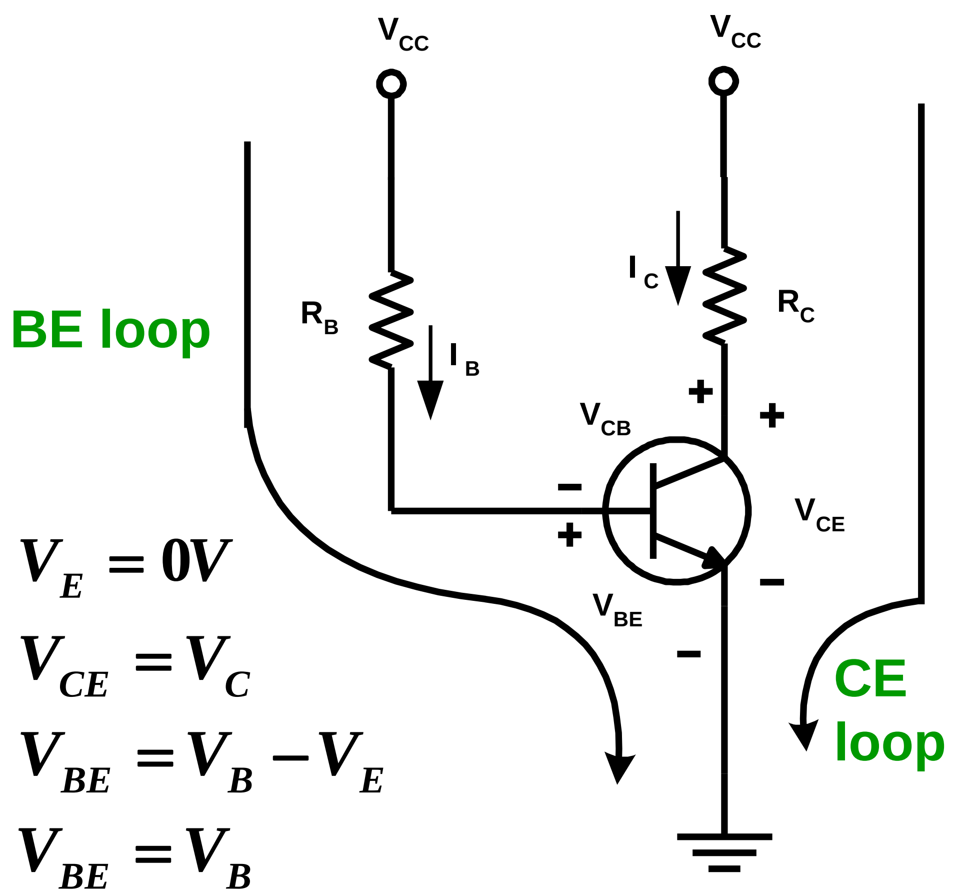
$$V_{CE} = V_C - V_E$$

$$V_E = 0V$$

$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$



Fixed-Bias Circuit Configuration

Example 4.1

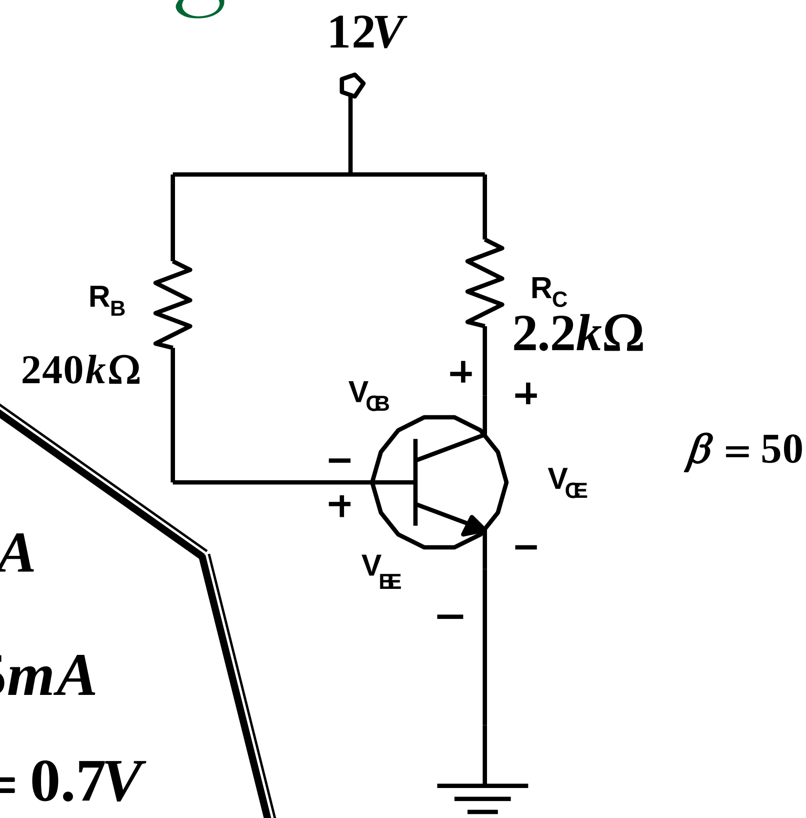
Find

(a) I_{BQ} and I_{CQ}

(b) V_{CEQ}

(c) V_B and V_C

(d) V_{BC}



$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240k} = 47.08\mu A$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08\mu) = 2.35mA$$

$$V_{CEQ} = V_{CC} - I_{CQ}R_C$$

$$= 12 - (2.35m)(2.2k)$$

$$= 6.83V$$

$$V_B = V_{BE} = 0.7V$$

$$V_C = V_{CE} = 6.83V$$

$$V_{BC} = V_B - V_C$$

$$= 0.7V - 6.83V = -6.13V$$

Fixed-Bias Circuit Configuration

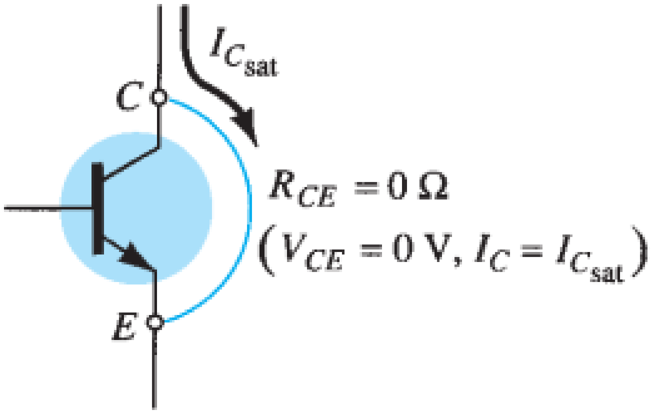
Transistor Saturation:

- For a transistor operating in the saturation region, the current is a maximum value for the particular design.
- I_{Csat} designed should be less than the maximum collector current provided by the data sheet.
- Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted.
- Resistor, R_{CE} between collector and emitter,

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{V_{CEsat}}{I_{Csat}}$$

- Assume V_{CEsat} = 0 V then, short-circuit.

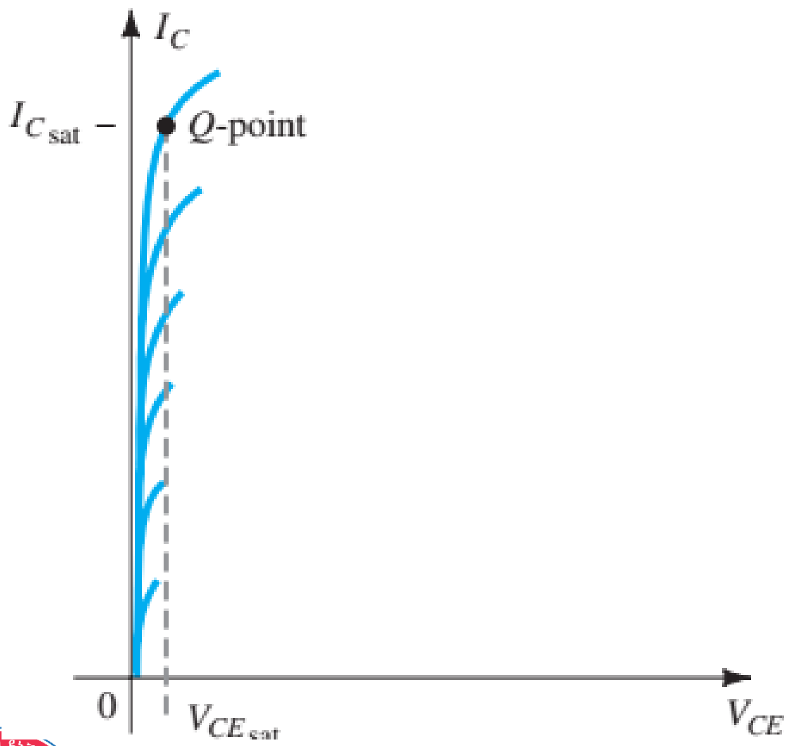
$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{V_{CEsat}}{I_{Csat}} = \frac{0}{I_{Csat}} = 0\Omega$$



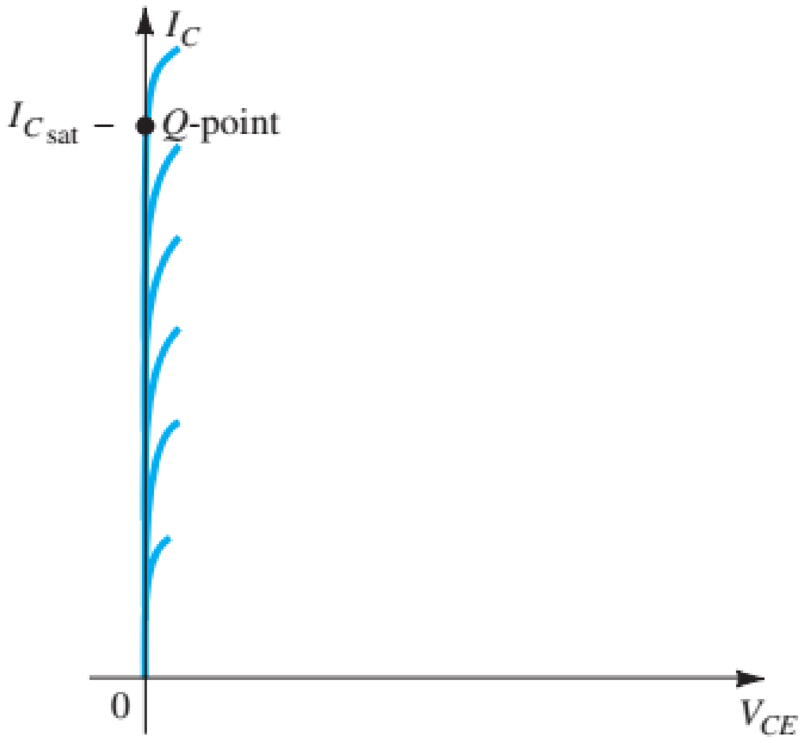
Fixed-Bias Circuit Configuration

Transistor Saturation

Actual saturation region



Approx. saturation region



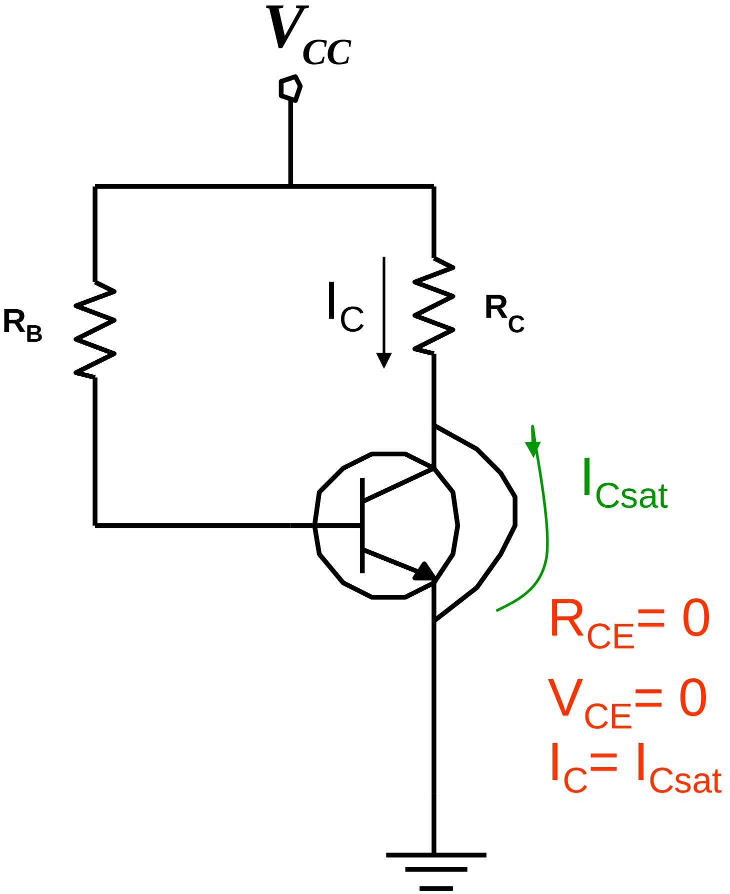
Fixed-Bias Circuit Configuration

Transistor Saturation

Saturation current for fixed-bias

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

I_{csat} = maximum possible I_C



Fixed-Bias Circuit Configuration

Load-Line Analysis for Fixed-Bias Circuit:

- To investigate the possible range of the Q-points.
- We Can obtain the load-line from the output characteristics.

$$V_{CE} = V_{CC} - I_C R_C \quad \text{---- (1)}$$

From eqn.1, we can obtain two possible points. When I_C = 0A,

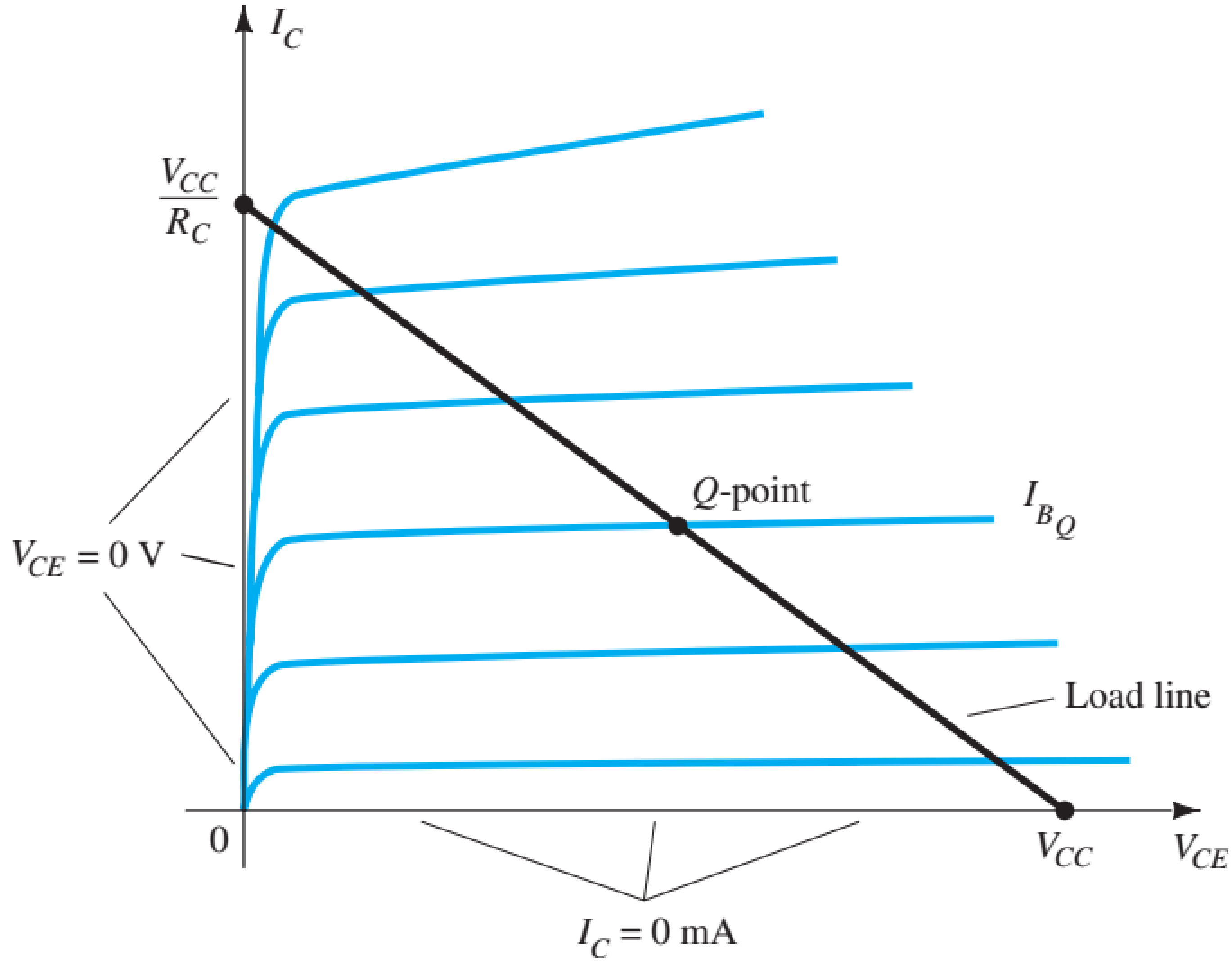
$$V_{CE} = V_{CC} - (0) R_C \qquad V_{CE} = V_{CC}\Big|_{I_C = 0A}$$

When V_{CE} = 0V,

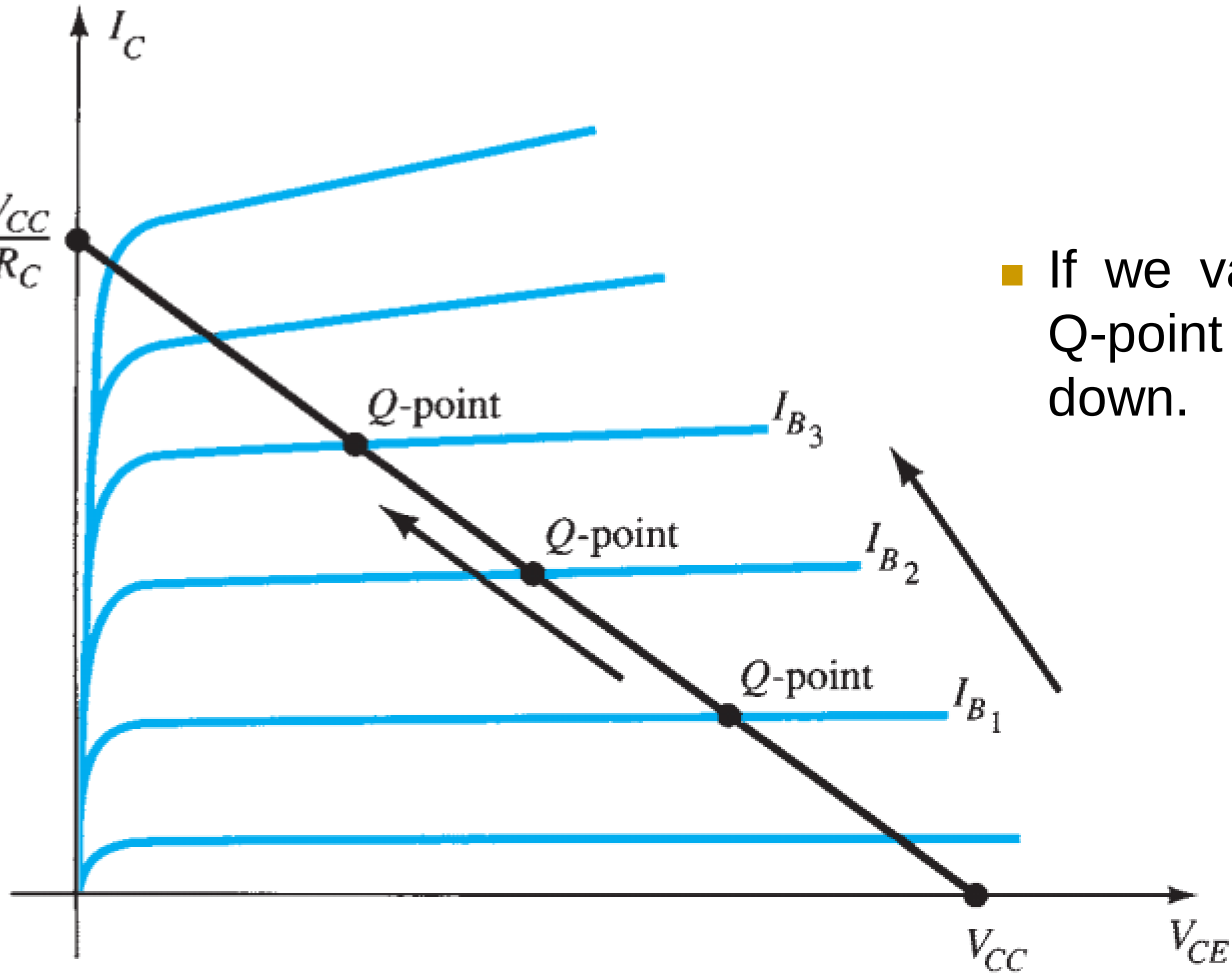
$$I_C = \frac{V_{CC}}{R_C}\Bigg|_{V_{CE} = 0V}$$

Insert this two points into the output characteristic curve.

Fixed-Bias Circuit Configuration

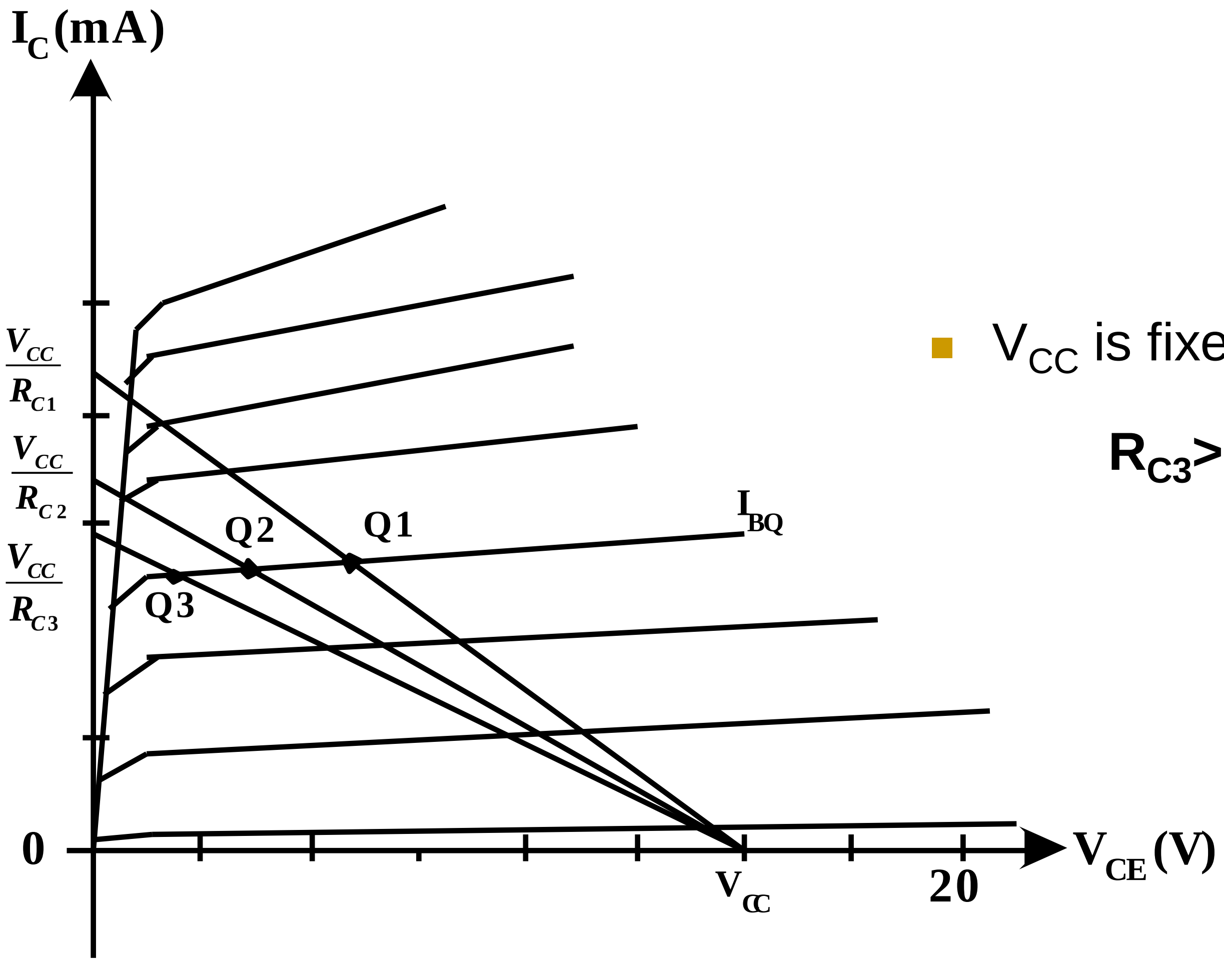


Fixed-Bias Circuit Configuration



- If we vary I_B by varying R_B, Q-point will move up and down.

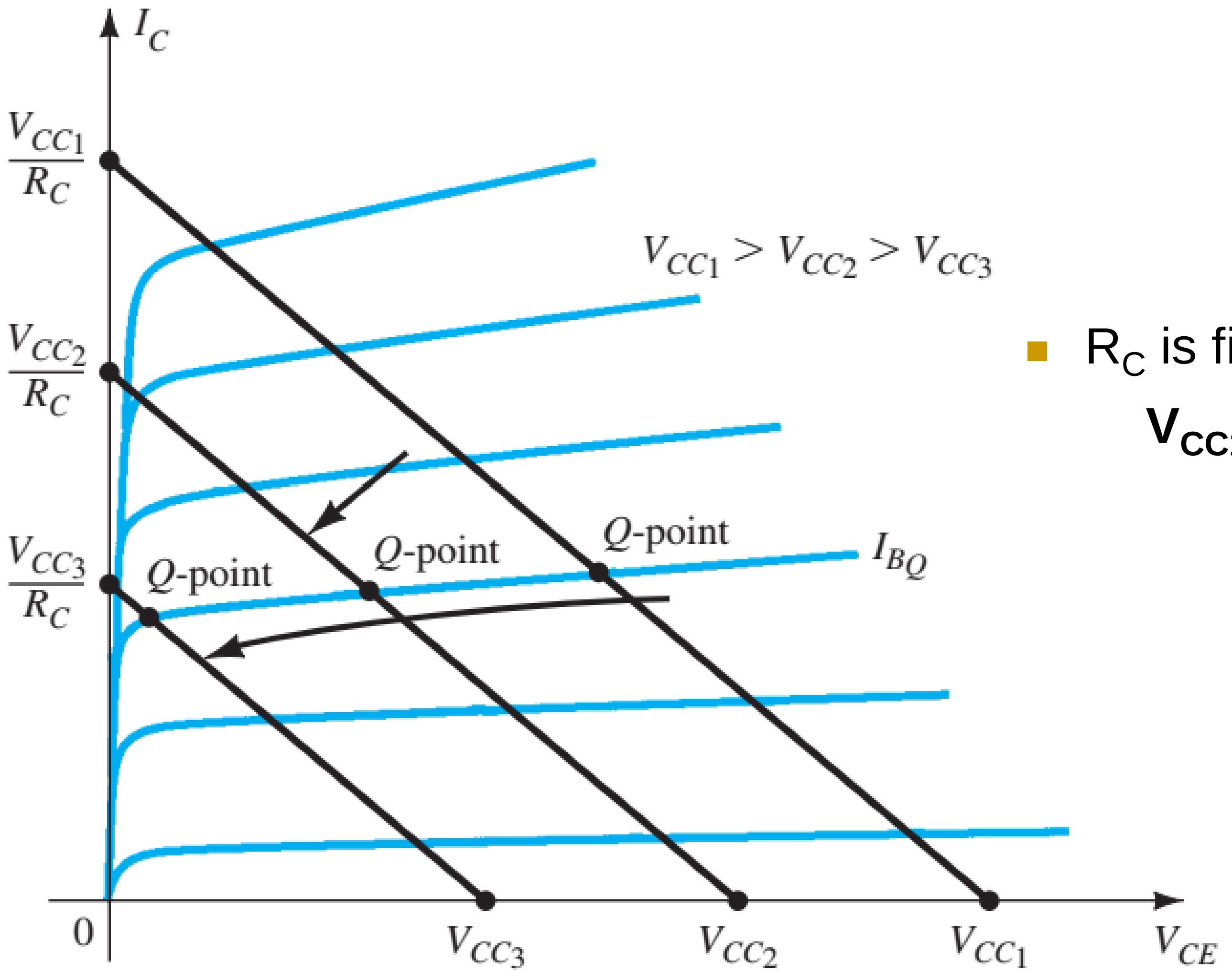
Fixed-Bias Circuit Configuration



- V_{CC} is fixed, R_C varies.

  $R_{C3} > R_{C2} > R_{C1}$

Fixed-Bias Circuit Configuration

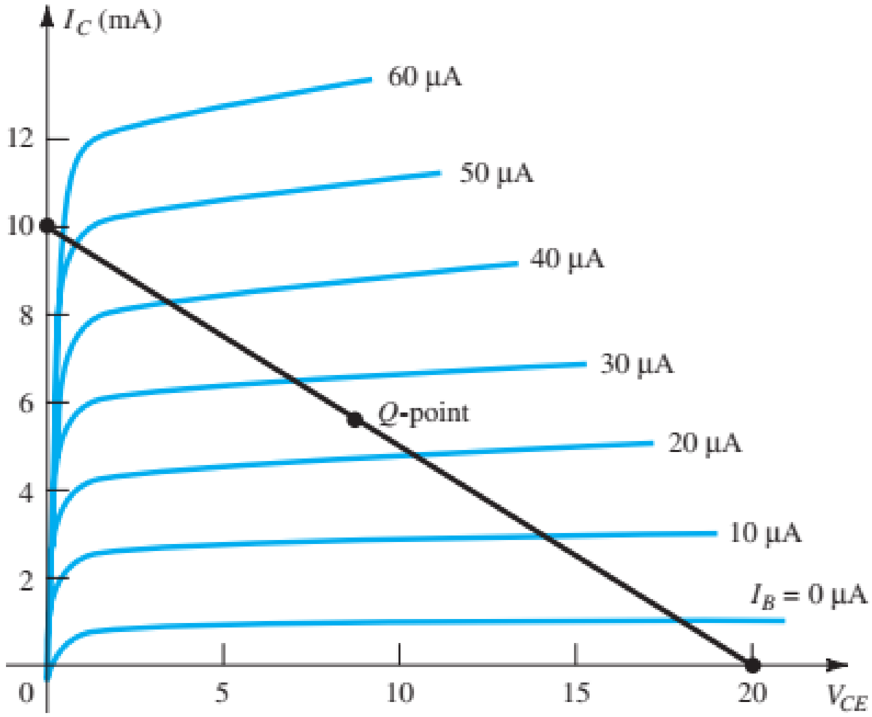


- R_C is fixed, V_{CC} varies.

  $V_{CC1}>V_{CC2}>V_{CC3}$

Fixed-Bias Circuit Configuration

- Example 4.3: Given the load line, Determine V_{CC}, R_C and R_B.



$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

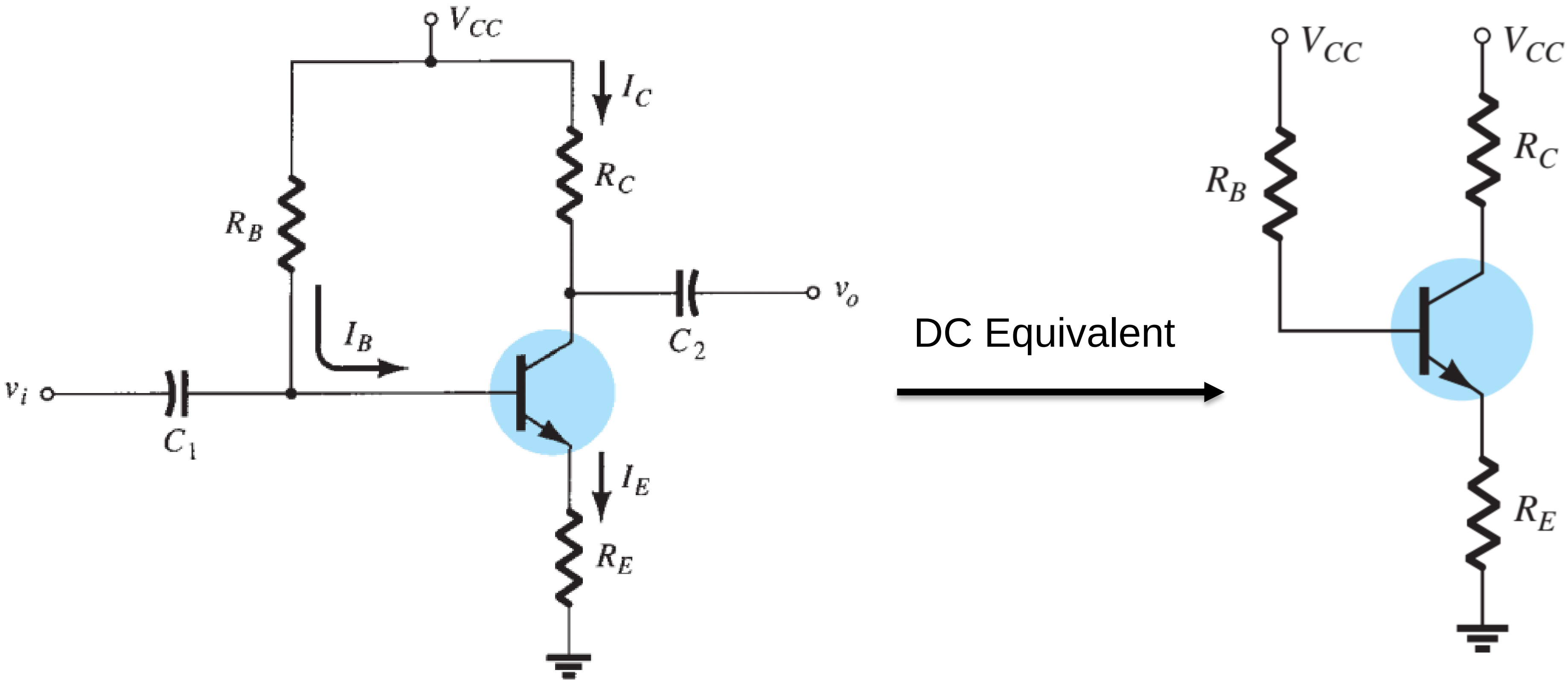
$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

Emitter Bias Circuit Configuration

- An emitter resistor is used to improve the stability level of the fixed-bias circuit.
- It results in Emitter Bias Circuit Configuration.



Emitter Bias Circuit Configuration

Base-Emitter Loop:

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Collector-Emitter Loop:

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \text{ and } I_E \cong I_C$$

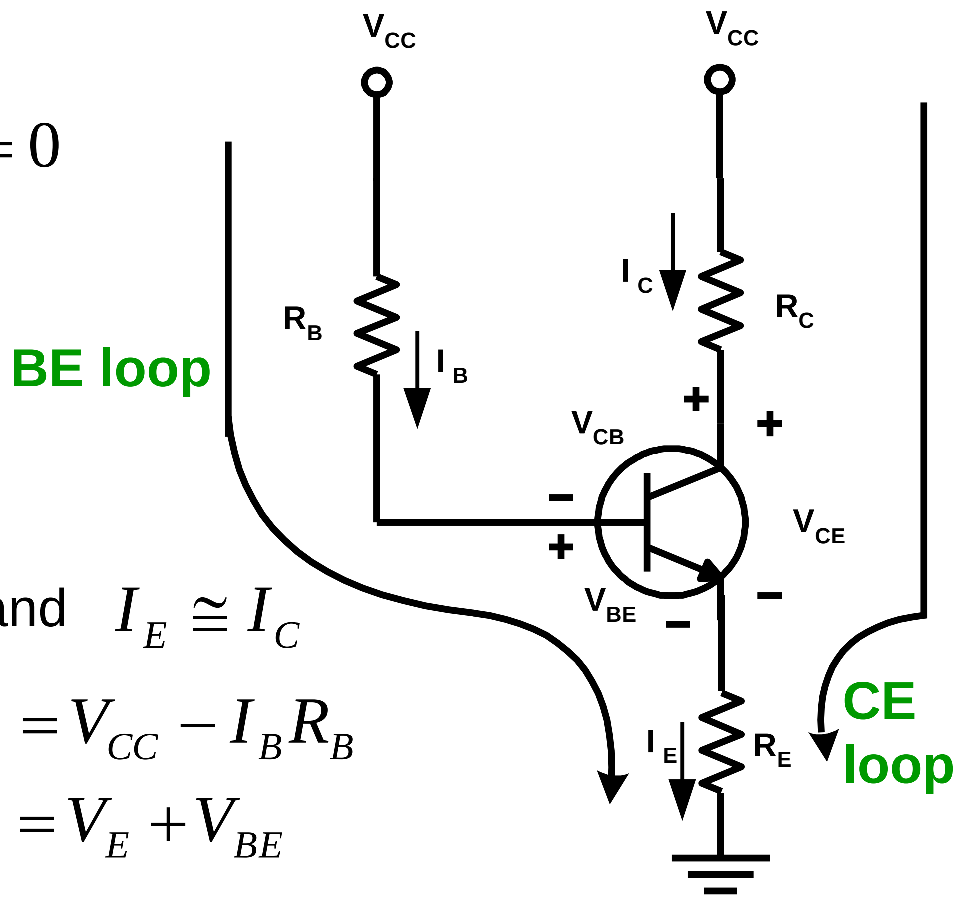
$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

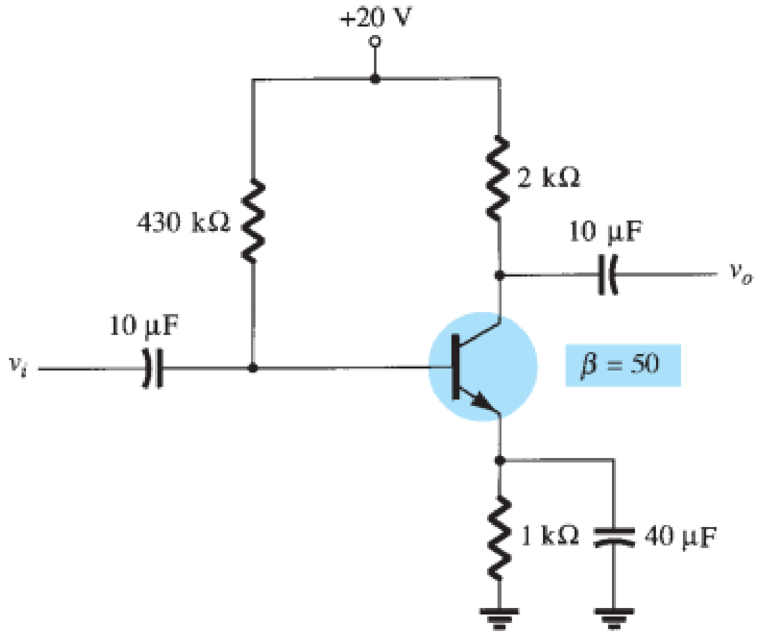
$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_E + V_{BE}$$



Fixed-Bias Circuit Configuration

- Example 4.3: Determine I_B, I_C, V_{CE}, V_C, V_E, V_B, V_{BC}.



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

$$I_C = \beta I_B$$
$$= (50)(40.1\ \mu\text{A})$$
$$\cong \mathbf{2.01\ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$
$$= \mathbf{13.97\ V}$$

$$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$
$$= \mathbf{15.98\ V}$$

$$V_E = V_C - V_{CE}$$
$$= 15.98\text{ V} - 13.97\text{ V}$$
$$= \mathbf{2.01\ V}$$

or

$$V_E = I_E R_E \cong I_C R_E$$
$$= (2.01\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.01\ V}$$

$$V_B = V_{BE} + V_E$$
$$= 0.7\text{ V} + 2.01\text{ V}$$
$$= \mathbf{2.71\ V}$$

$$V_{BC} = V_B - V_C$$
$$= 2.71\text{ V} - 15.98\text{ V}$$
$$= \mathbf{-13.27\ V}$$

Improved Bias Stability

Comparison between Fixed-Bias and Emitter-Bias Stability

PARAMETER					
Circuit	β	$I_B(\mu A)$	$I_C(mA)$	$V_{CE}(V)$	Remarks
Fixed-Bias	50	47.08	2.35	6.83	I_C changes by 100% V_{CE} changes by 76%
	100	47.08	4.71	1.64	
Emitter-Bias	50	40.1	2.01	13.97	I_C changes by 81% V_{CE} changes by 35% **(MORE STABLE!!)**
	100	36.3	3.63	9.11	

Temperature and transistor beta change resistance

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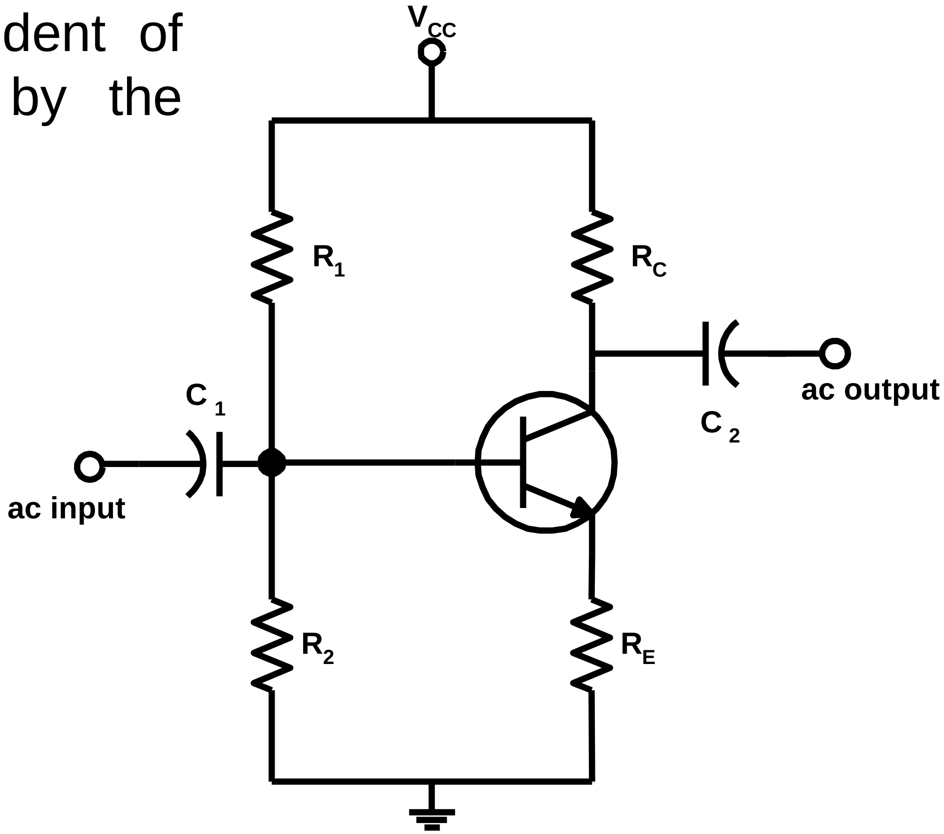
Voltage-Divider Bias Configuration

- A bias circuit that provide less dependent or totally independent of transistor β. (less affected by the temperature variation).

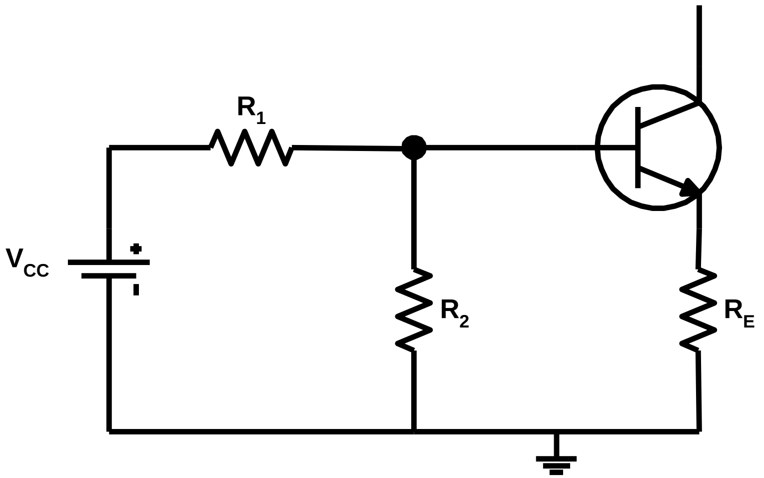
- Two analysis methods:
  - **Exact**
  - **Approximation**



Voltage-Divider Bias Configuration

Exact Analysis:

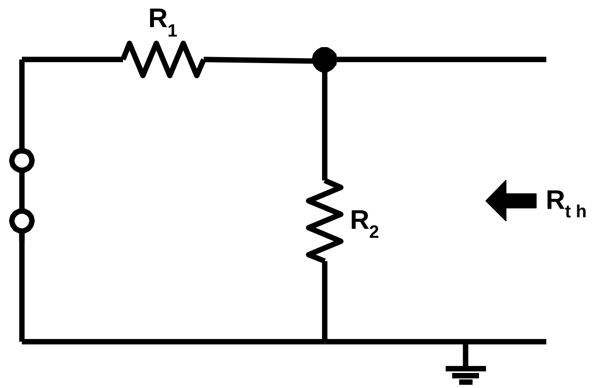
1. Redraw the input side of the voltage-divider circuit.



2. Obtain R_{th} and V_{th}.

- R_{th}, V_{CC} short Circuit.

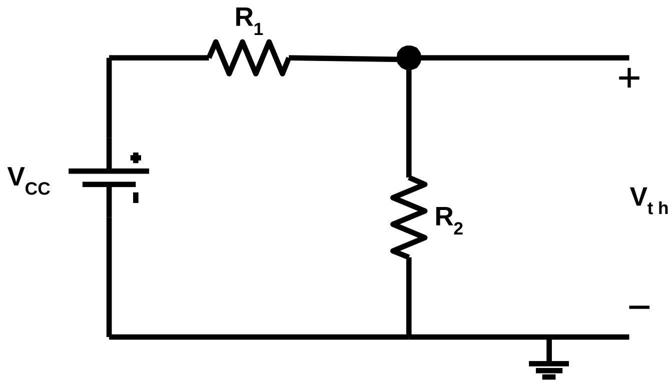
$$R_{th} = R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2}$$



Voltage-Divider Bias Configuration

- V_{th}?

$$V_{th} = V_{R2} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$



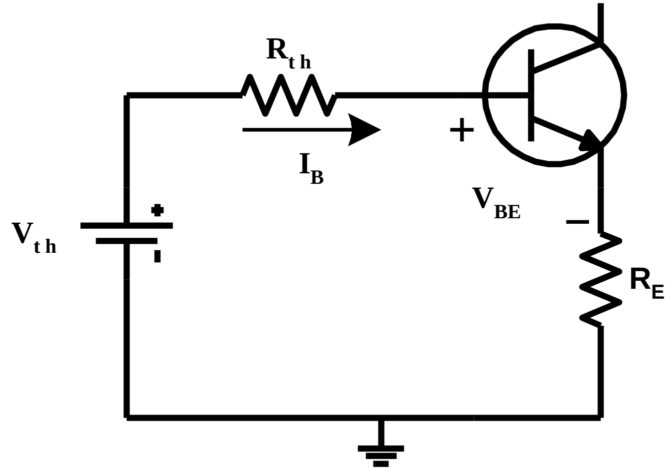
3. Combine R_{th} and V_{th},

$$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E = 0$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

$$I_E = (\beta + 1) I_B$$

$$I_E = (\beta + 1) \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$



Voltage-Divider Bias Configuration

$$I_E = \frac{V_{th} - V_{BE}}{R_E + R_{th}/(\beta + 1)}$$

If $R_E >> R_{th}/(\beta+1)$, then

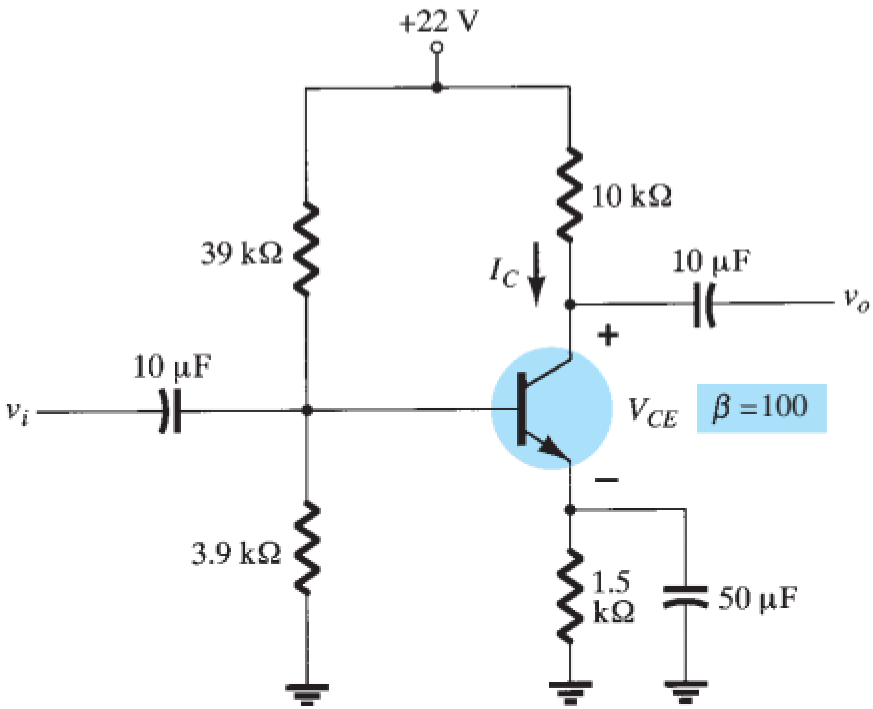
$$I_E = \frac{V_{th} - V_{BE}}{R_E}$$ **Independent of β……**

The output equation can be found using the same method as the emitter-bias circuit.

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right)$$

Voltage-Divider Bias Configuration

- Example 4.8: Determine I_C and V_{CE}.



$$R_{Th} = R_1 \| R_2 = \frac{(39\text{ k}\Omega)(3.9\text{ k}\Omega)}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 3.55\text{ k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\text{ k}\Omega)(22\text{ V})}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 2\text{ V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (101)(1.5\text{ k}\Omega)} = \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 151.5\text{ k}\Omega} = 8.38\ \mu\text{A}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 22\text{ V} - (0.84\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega) = 22\text{ V} - 9.66\text{ V} = \mathbf{12.34\ V}$$

$$I_C = \beta I_B = (100)(8.38\ \mu\text{A}) = \mathbf{0.84\ mA}$$

Voltage-Divider Bias Configuration

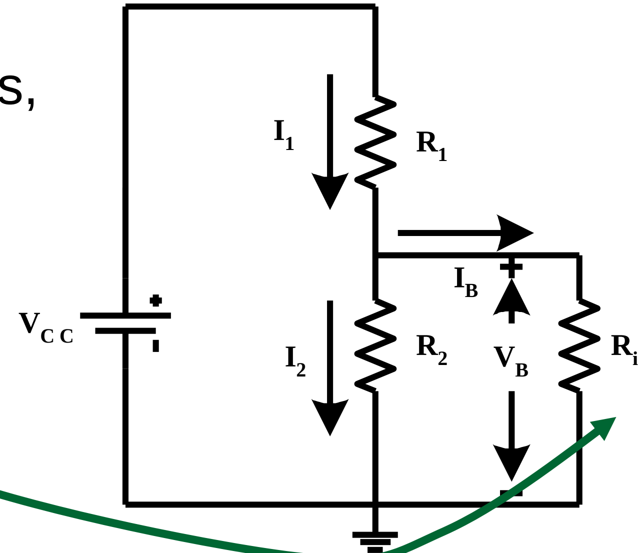
$$\beta R_E \geq 10 R_2$$

Approximate Analysis:

The input section can be approximated as,

→ Reflected resistance

$$R_i = (\beta + 1) R_E$$



Assume that I_B is small compared to I_1 and I_2,

$$I_1 = I_2$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Voltage-Divider Bias Configuration

$$R_i = (\beta + 1) R_E \cong \beta R_E$$

V_B equation as shown previously can only be used if, $\beta R_E \geq 10 R_2$

V_E can be calculated as

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

$$I_{CQ} \cong I_E$$

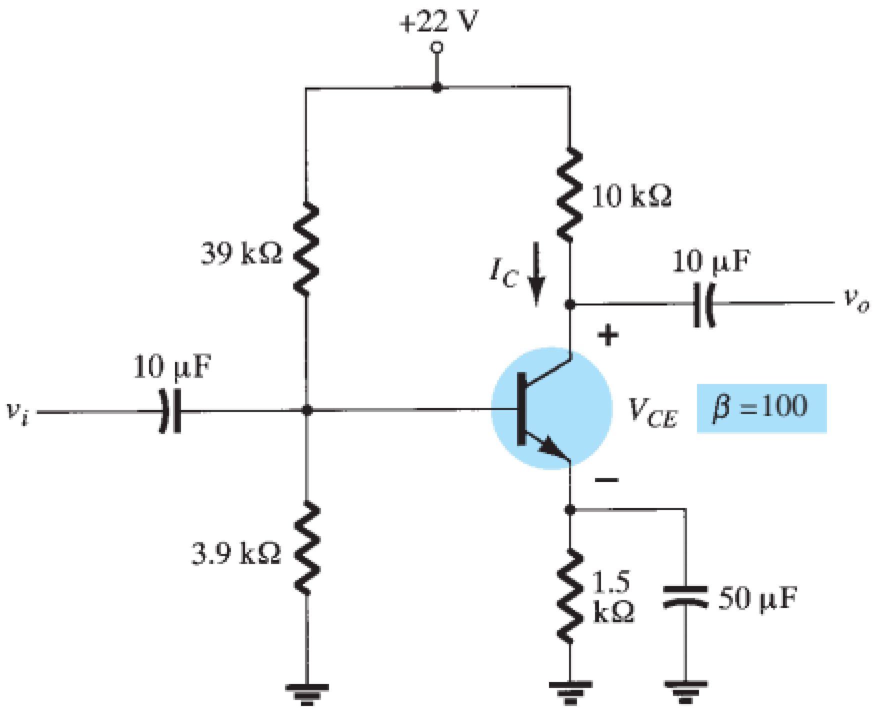
The output equation is

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \quad \text{or} \quad V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

Independent of β ……

Voltage-Divider Bias Configuration

- Example 4.9: Repeat example 4.9 using approximate analysis



Testing:

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\ \text{k}\Omega) \geq 10(3.9\ \text{k}\Omega)$$
$$150\ \text{k}\Omega \geq 39\ \text{k}\Omega\ (\textit{satisfied})$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ \text{V}$$

$$V_E = V_B - V_{BE} = 2\ \text{V} - 0.7\ \text{V} = 1.3\ \text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\ \text{V}}{1.5\ \text{k}\Omega} = \mathbf{0.867\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\ \text{V} - (0.867\ \text{mA})(10\ \text{kV} + 1.5\ \text{k}\Omega) = 22\ \text{V} - 9.97\ \text{V} = \mathbf{12.03\ V}$$

Voltage-Divider Bias Configuration

Transistor Saturation:

From the output collector-emitter circuit,

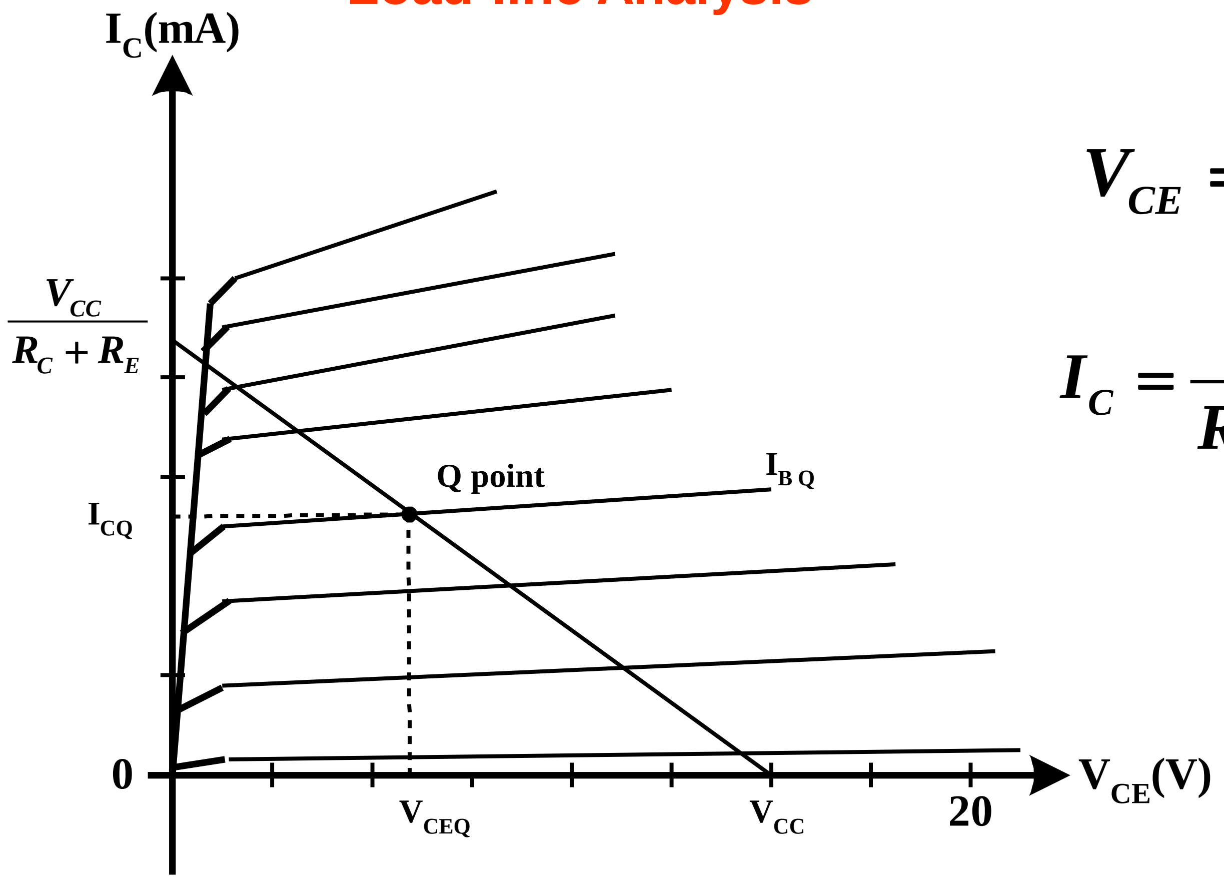
$$V_{CEQ} = V_{CC} - I_C\left(R_C + R_E\right)$$

For saturation, let V_{CE}=0, therefore

$$I_{Csat} = \frac{V_{CC}}{R_C + R_E}$$

Voltage-Divider Bias Configuration

Load-line Analysis



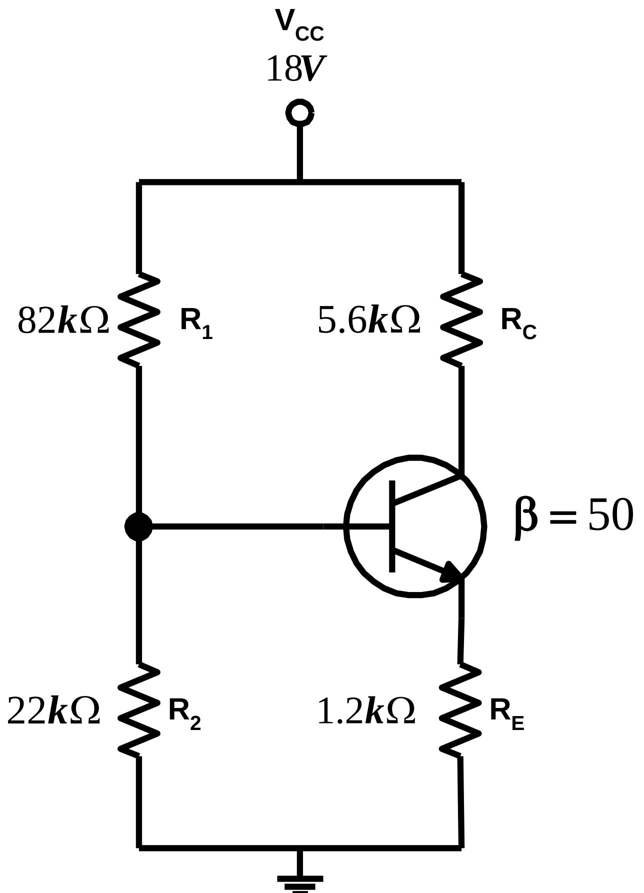
$$V_{CE} = V_{CC}\Big|_{I_C = 0mA}$$

$$I_C = \frac{V_{CC}}{R_C + R_E}\Bigg|_{V_{CE} = 0V}$$

Voltage-Divider Bias Configuration

Example 4.2

Determine the levels of I_{CQ} and V_{CEQ} for the circuit, using the exact & approximation techniques.



Exact Analysis:

$$R_{th} = R_1 \| R_2 = 82k\Omega \| 22k\Omega$$
$$= 17.35k\Omega$$

$$V_{th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22k(18V)}{82k + 22k}$$
$$= 3.81V$$

Voltage-Divider Bias Configuration

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

$$= \frac{3.81 - 0.7}{17.35k + (51)(1.2k)} = 39.6\mu A$$

$$I_{CQ} = \beta I_B = (50)(39.6\mu) = 1.98mA$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

$$= 18 - (1.98m)(5.6k + 1.2k)$$

$$= 4.54V$$

Approximate Analysis:

$$\beta R_E \geq 10 R_2 \qquad (50)(1.2k) \geq 10(22k) \qquad 60k \ngeq 220k$$

Voltage-Divider Bias

Cannot use this formula → $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$

$$V_B = V_{th} = 3.81V$$

$$V_E = V_B - V_{BE} = 3.81 - 0.7 = 3.11V$$

$$I_{CQ} = I_E = \frac{V_E}{R_E} = \frac{3.11}{1.2k} = 2.59mA$$

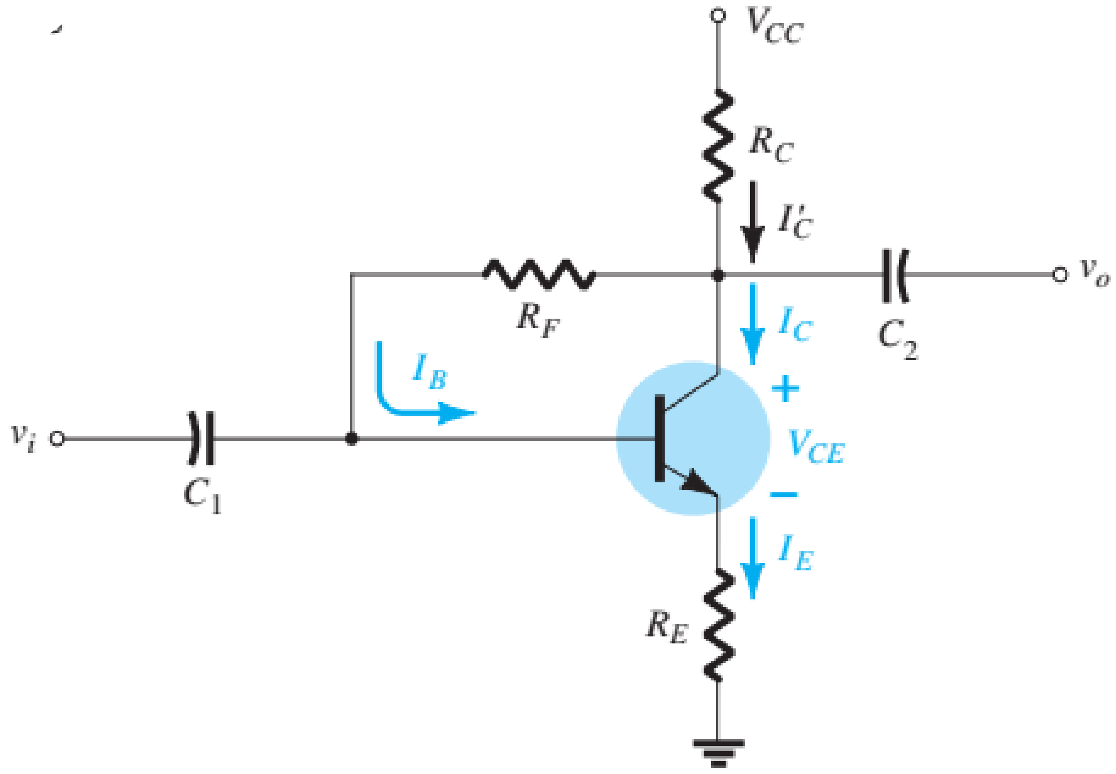
$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 18 - (2.59m)(5.6k + 1.2k)$$

$$= 3.88V$$

Collector Feedback Bias

- An improved level of stability (than fixed or emitter bias) can also be obtained by introducing a resistor between base and collector.



Collector Feedback Bias

- Base-Emitter (input) loop

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

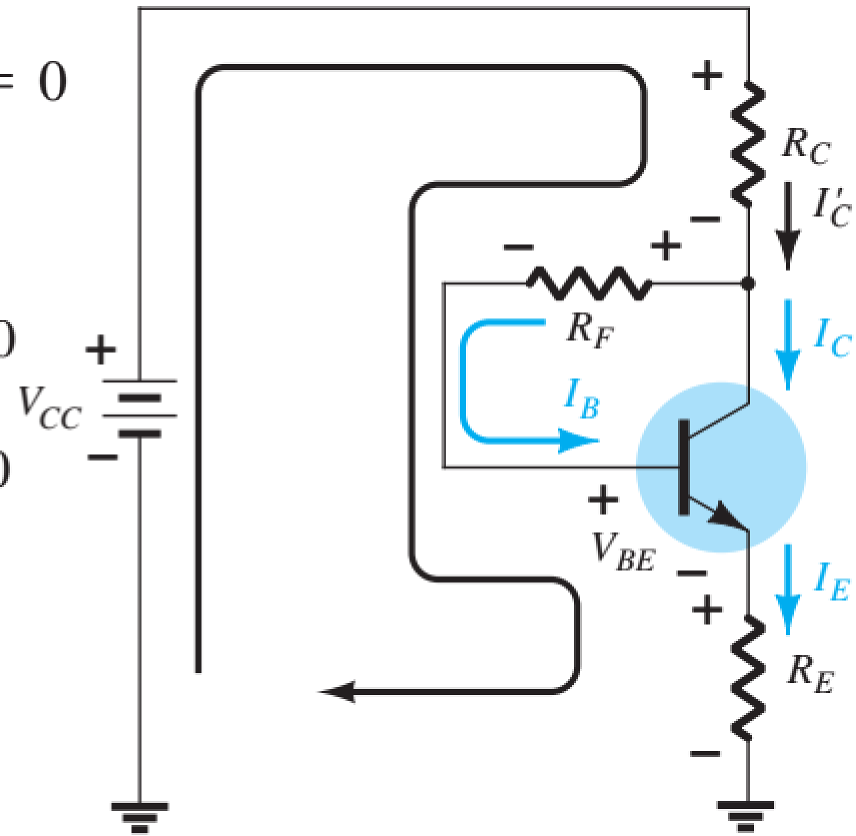
where $I'_C = I_C + I_B$

$$I'_C \cong I_C = \beta I_B \qquad I_E \cong I_C$$

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_F = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}}$$



Collector Feedback Bias

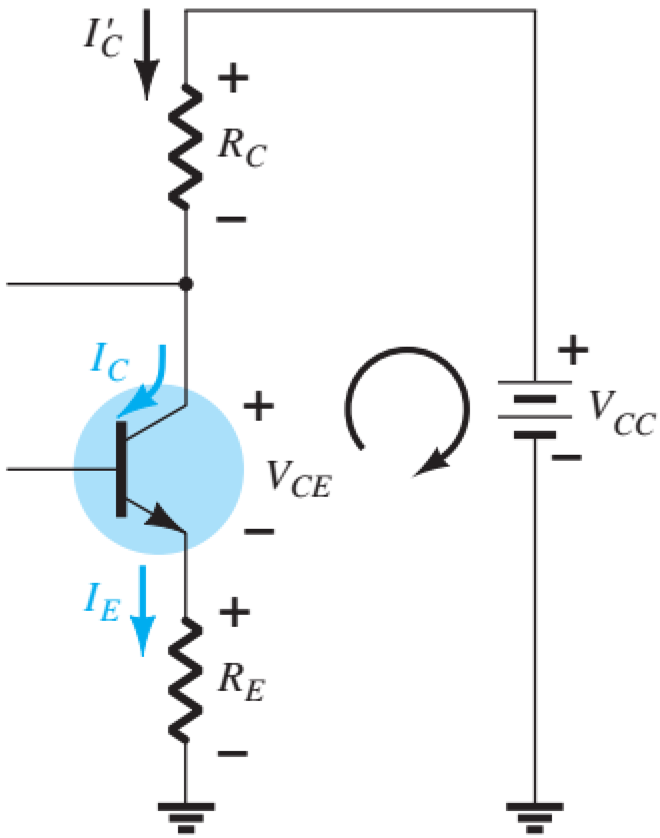
- Collector-Emitter (output) loop

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Because $I'_C \cong I_C$ and $I_E \cong I_C$, we have

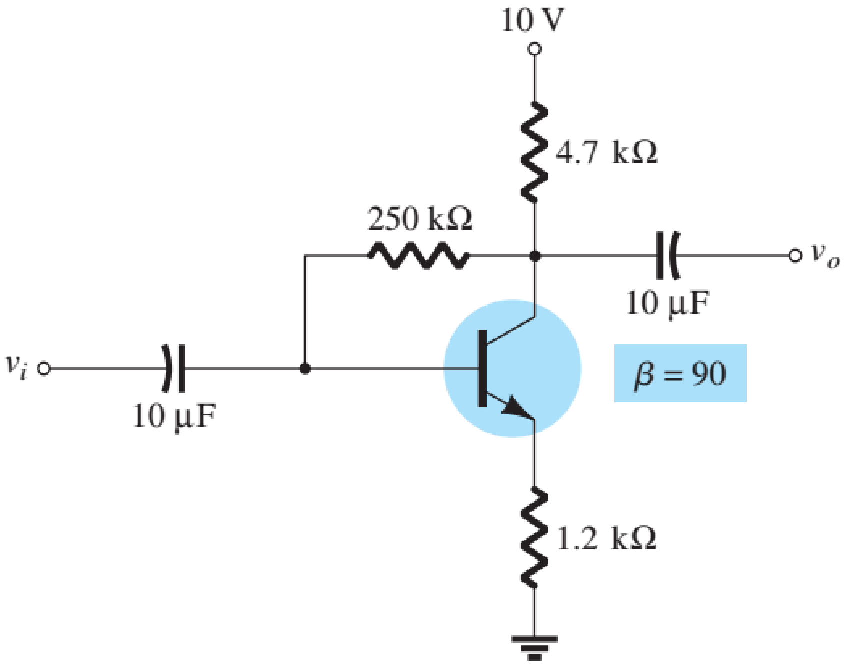
$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Collector Feedback Bias

- Example 4.12: Determine I_{CQ} and V_{CEQ}



$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\ mA}$$

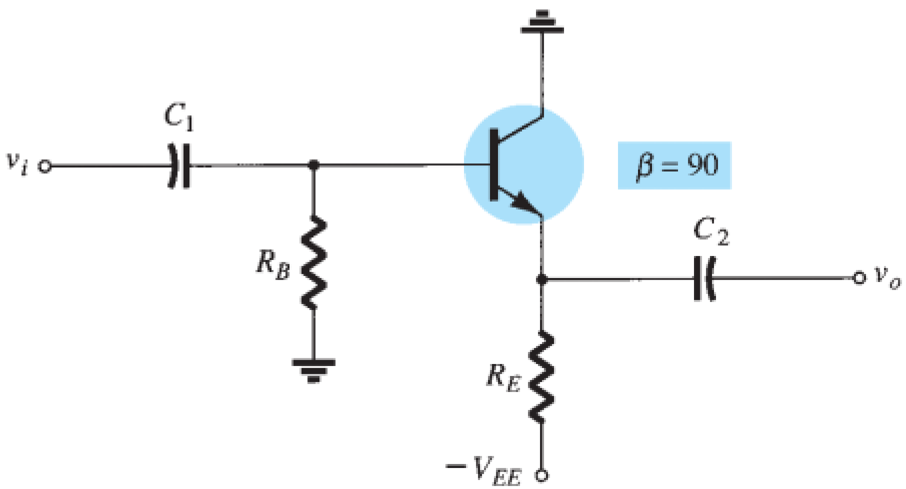
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

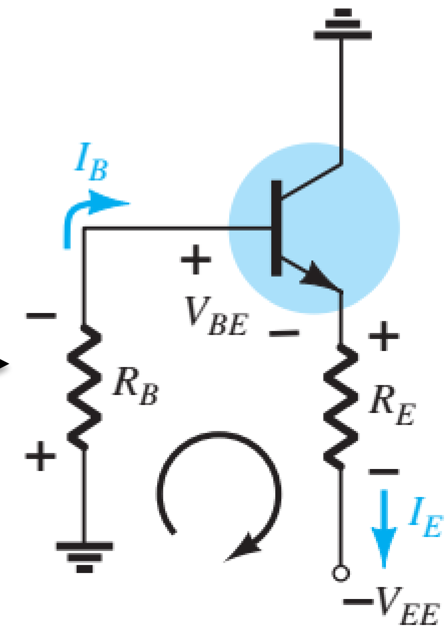
$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\ V}$$

Common Collector (Emitter-Follower)



DC Equivalent



For the Input loop

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

using $I_E = (\beta + 1) I_B$

$$I_B R_B + (\beta + 1) I_B R_E = V_{EE} - V_{BE}$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

For the output loop

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

What to Do This Week?

- Reading Assignment on DC biasing of
  - Common Base Configuration.
  - Miscellaneous bias configurations.
  - PNP BJTs

- Reading Task for next class
  - BJT Transistor small signal modelling.