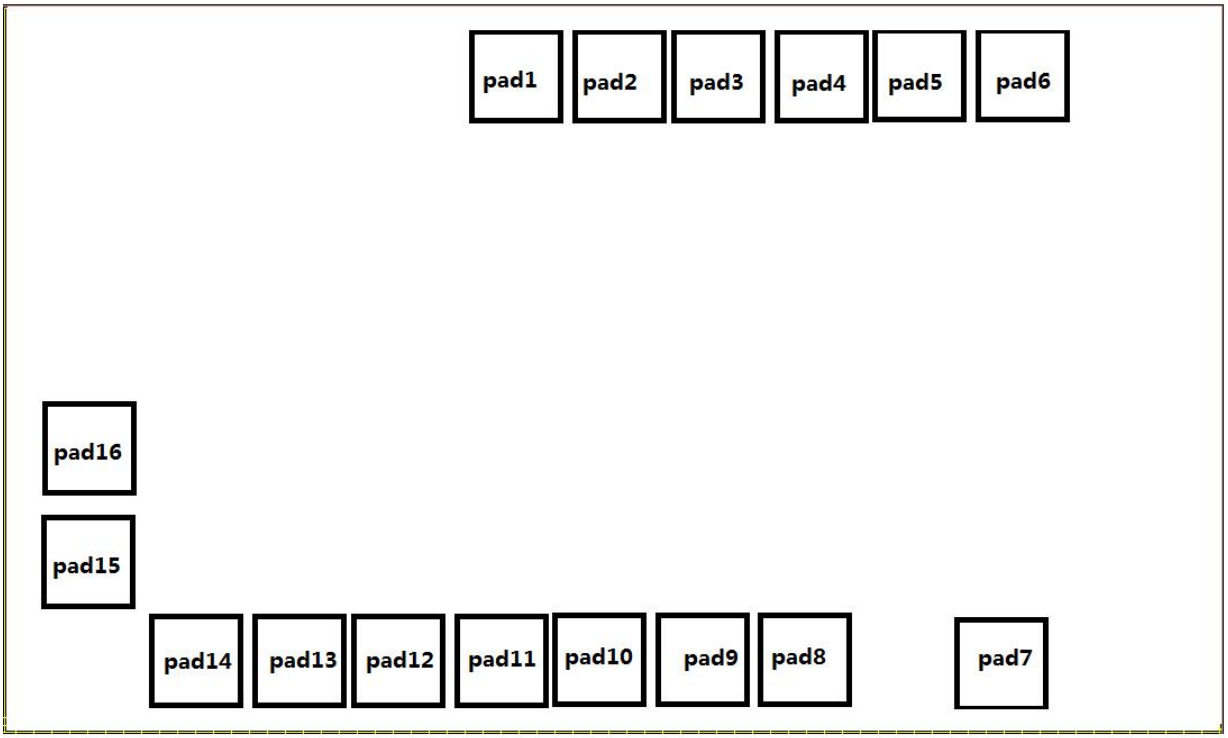
HS5130_D_Wafer_INFO

1. Wafer information

a) Layout pad location



b) Pin Definition（以左下角为坐标原点）

Pad	Pad Name	X 坐标	Y 坐标	PAD size（um*um）	功能
PAD1	PA3	429.660	545.000	60μm*60μm	IO
PAD2	VSS	508.210	545.000	60μm*60μm	Ground
PAD3	PB0	584.380	545.000	60μm*60μm	IO
PAD4	PB1	686.120	545.000	60μm*60μm	Serial Data Input/IO
PAD5	PB2	787.860	545.000	60μm*60μm	Serial Clock Input/IO
PAD6	PB3	889.600	545.000	60μm*60μm	IO
PAD7	PB4	865.465	53.000	60μm*60μm	Serial Model Input/IO
PAD8	PB5	640.235	53.000	60μm*60μm	IO
PAD9	VDD	561.685	53.000	60μm*60μm	Power supply
PAD10	PB6	485.515	53.000	60μm*60μm	IO
PAD11	PB7	403.215	53.000	60μm*60μm	IO
PAD12	PA0	320.915	53.000	60μm*60μm	IO
PAD13	PA4	238.615	53.000	60μm*60μm	IO
PAD14	PA5	156.315	53.000	60μm*60μm	IO
PAD15	PA1	53.000	130.680	60μm*60μm	IO
PAD16	PA2	53.000	213.080	60μm*60μm	IO

c) Process & Layout information

Wafer	HS5130_D
Top metal thickness	8K
Wafer size	200mm(8")
Chip thickness	725±25um
PAD window	60umx60um
Scribe lane	60um
Die size	X pitch: 1002um / Y pitch: 598um
ESD under pad	yes
Pad component	99.5% Al, 0.5%Cu