Name: Newman Ilgenfritz

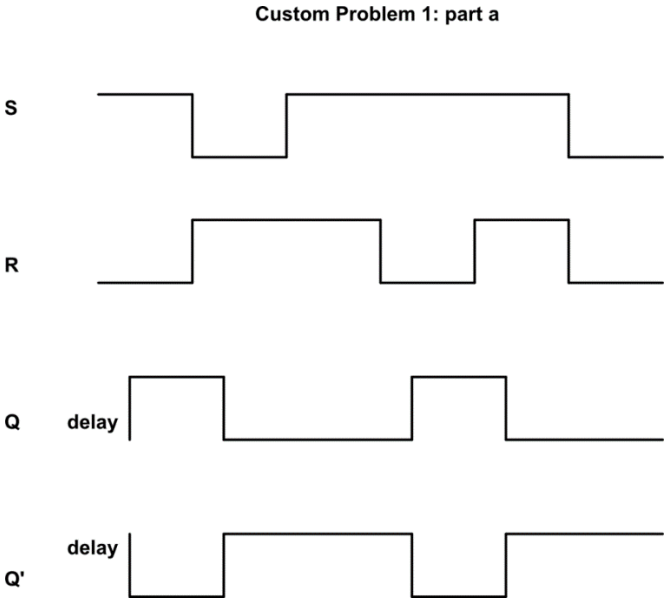
CIT 593 Module 4 Assignment: Sequential Logic & Memory

Remember that this is an individual assignment (NO group work).

Part 1: Sequential Logic – Latches & Flip/Flops

Custom Problem 1:

(a)



(b)

The five actions of this RS latch on the timing diagram is:

Action	S	R	Q	Q’
Set	1	0	0	1
Set	1	1	0	1
Reset	0	1	1	0
Reset	1	1	1	0
Invalid	0	0	1	1

(c)

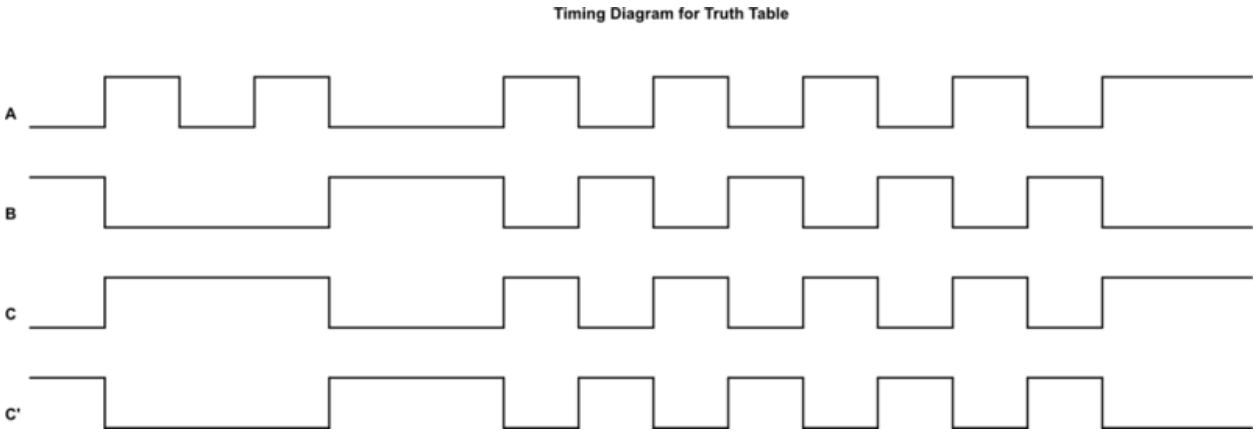
No. The only input combination not covered in this diagram is the invalid action when S and R are both 0. It is not covered because it is an invalid state.

Custom Problem 2:

(a)

Input A	Input B	Output C	Output C’
0	0	No change: latch	No change: latch
1	0	1	0
0	1	0	1
1	1	0	0

(b)



(c) The R-S latch discussed in lecture is a NAND latch and this is a NOR latch. The differences are that when both S and R =0 in the NAND latch it is invalid but in the NOR latch, the latch remains in the present state. When S and R = 0,1 and 1,0 these latch act inversely to each other. The NAND is reset when S,R = 0,1 and the NOR is set and vice versa. Lastly, when S and R are both 1, they act inversely again. The NAND latch remains in the present state while the NOR latch is invalid.

(d)

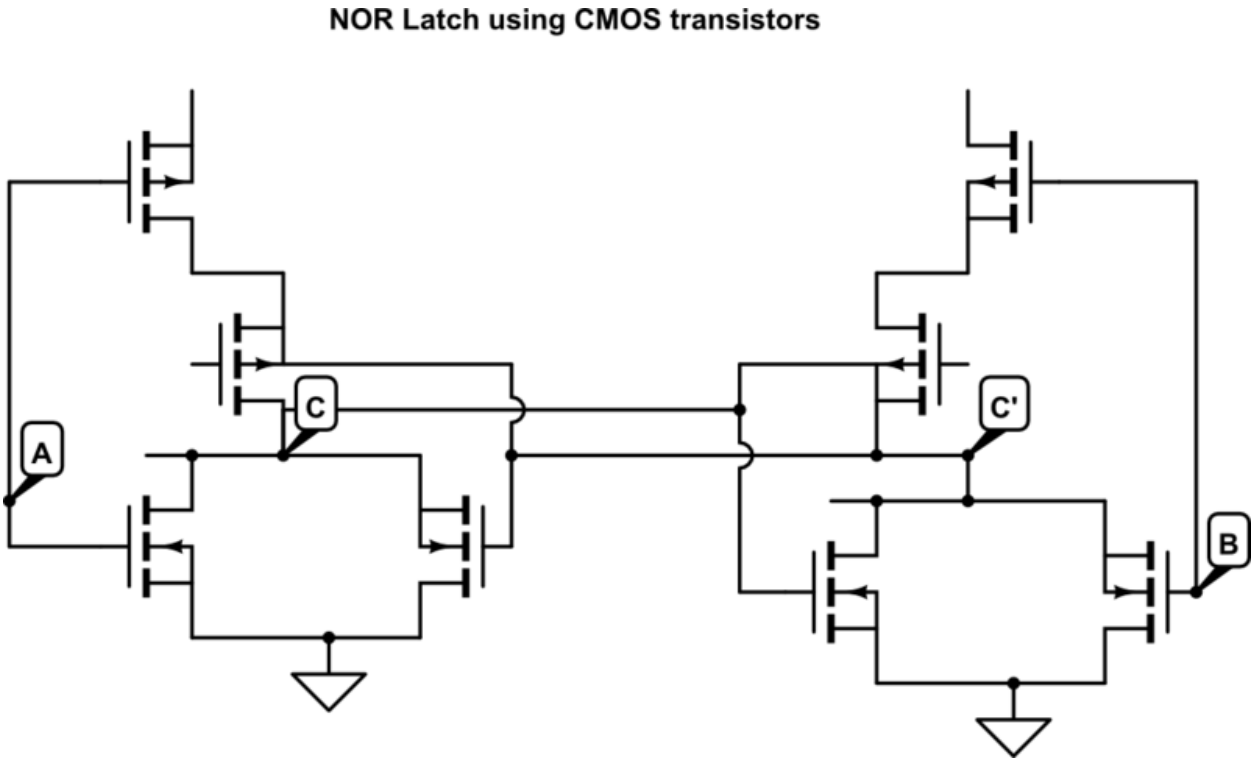
Input A =0 and Input B = 0, the outputs hold the previous value

Input A = 0 and Input B = 1, the outputs reset

Input A = 1 and Input B = 0, Sets output C to 1

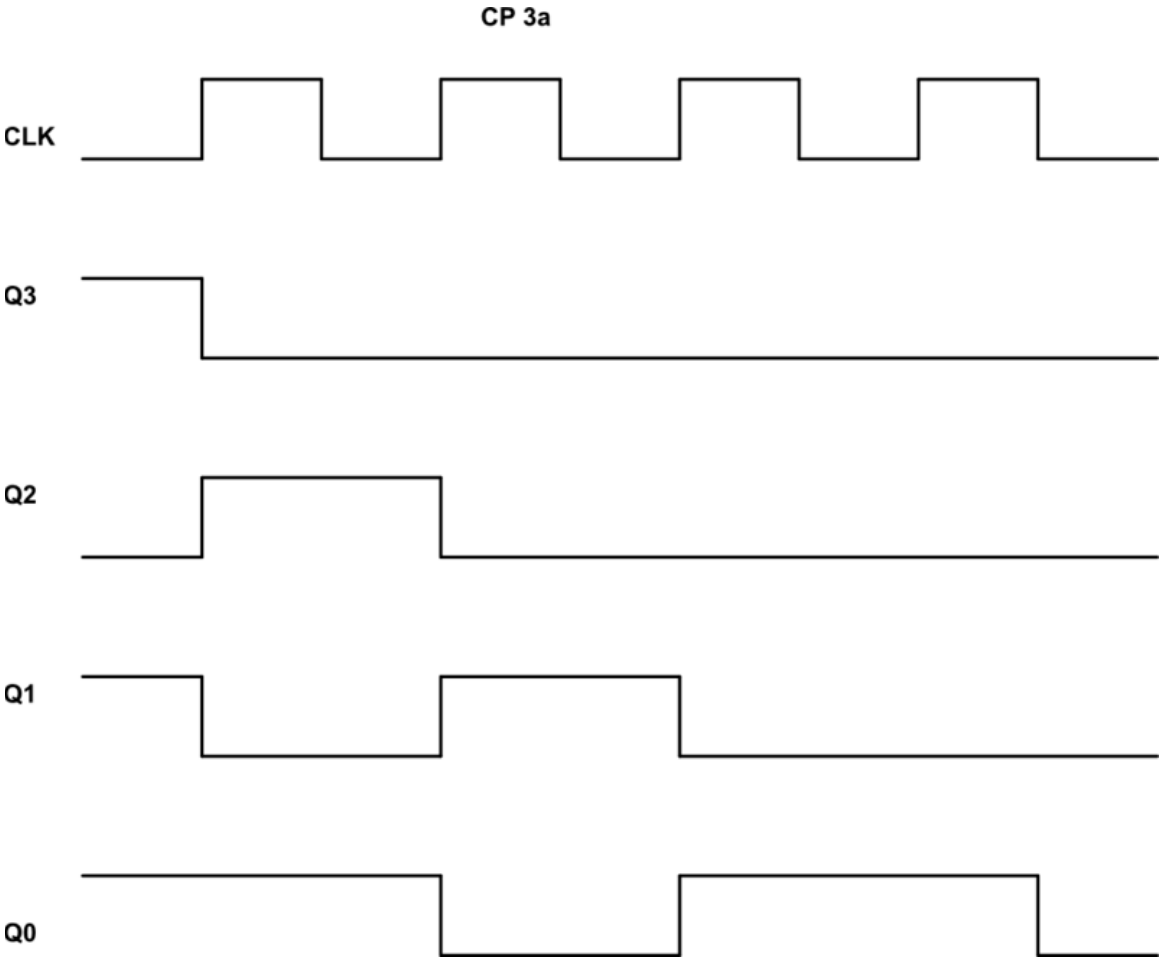
Input A = 1 and Input B = 1, Invalid action

(e)



Custom Problem 3:

(a)



There is a slight delay in each output.

(b)

This timing diagram implements a right shift register displayed in the below table.

Q3	Q2	Q1	Q0
1	0	1	1
0	1	0	1
0	0	1	0
0	0	0	1

(c) When I replace the DFF's with D-latches, the exact same operation is performed and has the same timing diagram as part a.

Textbook Problem 3.27:

From CIT 593 course textbook: "Intro to Computing Systems" by Patt & Patel

(a)

When S=0, the output Z is equal to A.

(b)

If S is switched to 1, Z = whatever its previous values was.

(c)

This logic circuit is a storage element.

Part 2: Sequential Logic -> Memory

Textbook Problems

From CIT 593 course textbook: "Intro to Computing Systems" by Patt & Patel

3.31: 8*(2^3) = 64 = total size of memory in bytes.

3.32:

Memory addressability refers to the number of bits of data that is stored in a memory location (how much), while the memory address is the location of the data.

3.33:

(a)

A [1:0] = 1,1

WE = 0

(b)

6 address lines are needed because 2^6 = 64. 2^60 bits are now required.

3.34:

a. Address space=3

b. Addressability = 4

c. Data =0001

3.35:

3* 2^22= 12582912

Optional Extra Credit (reading section 3.6 is necessary):

3.43:

a.

S1	S0	X	D1	D0	Z
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	1