Name: Newman Alexander Ilgenfritz

CIT 593 Module 6 Assignment: ISA

Remember that this is an individual assignment (NO group work).

Part 1: Problems from *Intro to Computing Systems* by Patt & Patel

Textbook Problem 1.16:

Data Type: Denotes the appropriate representations for data values.

Addressing: Specifies the location mechanism for memory.

Instruction Set: Indicates the instruction set that can be implemented by the computer.

Textbook Problem 1.17:

While the ISA is the set of instructions supported by a processor, the microarchitecture is concerned with the implementation, not definition. For example, different processors might utilize the same ISA, but not use the same microarchitecture.

Textbook Problem 1.23:

The ISA is unlikely to change between generations of microarchitectures because this would allow different computers with different microarchitectures to be compatible with the same instruction set. Also, it would allow a programmer the ability to execute the same code on different computers.

Textbook Problem 4.6:

The two components of an instruction are opcode and operands. The opcode identifies what the instruction does, and the operands dictates the values on which the instruction operates.

Part 2: Custom Problems

Custom Problem #1: Reverse Assembling (Disassembling machine code)

Address	Machine Instruction	Assembly Instruction
Example	*0001001010000011*	*ADD R1, R2, R3*
0	1001000000000010	Const,R0, #2
1	1001001000000011	Const,R1, #3
2	0001010000100000	ADD, R2, R0, #0
3	0010001100000001	CMPI, R1, 1
4	0000110000000011	BRnz, 3
5	0001010010001000	MUL,R2,R2, R0
6	0001001001111111	Add, R1,R1, #-1
7	0000111111111011	NRnzp, #-5

Your answers for Custom Problem #2 should be entered directly into Coursera.

	PCMux.CTL	rsMux.CTL	rtMux.CTL	rdMux.CTL	regFile.WE	regInputMux.CTL	Arith.CTL	ArithMux.CTL	LOGIC.CTL	LogicMux.CTL	SHIFT.CTL	COSNT.CTL	CMP.CTL	ALUMux.CTL	NZP.WE	DATA.WE
BRxxx	0	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0
ADD	1	0	0	0	1	0	0	0	x	x	x	x	x	0	1	0
MUL	1	0	0	0	1	0	1	0	x	x	x	x	x	0	1	0
SUB	1	0	0	0	1	0	2	0	x	x	x	x	x	0	1	0
DIV	1	0	0	0	1	0	3	0	x	x	x	x	x	0	1	0
ADD (immediate)	1	0	x	0	1	0	0	1	x	x	x	x	x	0	1	0
CMP	1	2	0	x	0	0	x	x	x	x	x	x	0	4	1	0
CMPU	1	2	0	x	0	0	x	x	x	x	x	x	1	4	1	0
CMPI	1	2	x	x	0	0	x	x	x	x	x	x	2	4	1	0
CMPIU	1	2	x	x	0	0	x	x	x	x	x	x	3	4	1	0
JSR	5	x	x	x	1	x	x	x	x	x	x	x	x	x	0	0
JSRR	3	1	x	x	1	x	x	x	x	x	x	x	x	x	0	0
AND	1	0	0	0	1	0	0	x	0	x	x	x	x	1	1	0
NOT	1	0	x	0	1	0	0	x	1	x	x	x	x	1	1	0
OR	1	0	0	0	1	0	0	x	2	x	x	x	x	1	1	0
XOR	1	0	0	0	1	0	0	x	3	x	x	x	x	1	1	0
AND (immediate)	1	0	x	0	1	0	0	x	0	1	x	x	x	1	1	0
LDR	1	0	x	0	1	1	0	2	x	x	x	x	x	0	1	0
STR	1	0	0	x	1	1	0	2	x	x	x	x	x	0	1	0
RTI	1	x	x	x	1	x	x	x	x	x	x	x	x	x	1	0
CONST	1	x	x	0	1	x	x	x	x	x	x	1	x	3	1	0
SLL	1	0	x	0	1	0	x	x	x	x	1	x	x	2	1	0
SRA	1	0	x	0	1	0	x	x	x	x	1	x	x	2	1	0
SRL	1	0	x	0	1	0	x	x	x	x	1	x	x	2	1	0
MOD	1	0	0	0	1	0	4	0	x	x	x	x	x	0	1	0
JMPR	3	0	x	x	1	x	x	x	x	x	x	x	x	x	0	0
JMP	2	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0
HICONST	1	x	x	0	1	x	x	x	x	x	x	x	x	x	0	0
TRAP	4	x	x	x	1	x	x	x	x	x	x	x	x	x	1	0