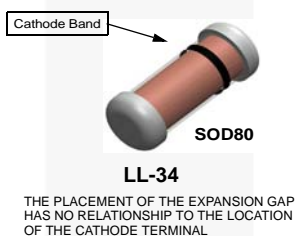
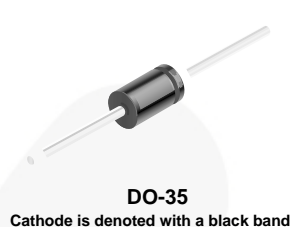




June 2015

1N/FDLL 914/A/B / 916/A/B / 4148 / 4448

Small Signal Diode



SOD-80 COLOR BAND MARKING

DEVICE 1ST BAND

FDLL914	BLACK
FDLL914A	BLACK
FDLL914B	BLACK
FDLL4148	BLACK
FDLL4448	BLACK

-1st band denotes cathode terminal
and has wider width

Ordering Information

Part Number	Marking	Package	Packing Method
1N914	914	DO-204AH (DO-35)	Bulk
1N914_T50A	914	DO-204AH (DO-35)	Ammo
1N914TR	914	DO-204AH (DO-35)	Tape and Reel
1N914ATR	914A	DO-204AH (DO-35)	Tape and Reel
1N914B	914B	DO-204AH (DO-35)	Bulk
1N914BTR	914B	DO-204AH (DO-35)	Tape and Reel
1N916	916	DO-204AH (DO-35)	Bulk
1N916A	916A	DO-204AH (DO-35)	Bulk
1N916B	916B	DO-204AH (DO-35)	Bulk
1N4148	4148	DO-204AH (DO-35)	Bulk
1N4148TA	4148	DO-204AH (DO-35)	Ammo
1N4148_T26A	4148	DO-204AH (DO-35)	Ammo
1N4148_T50A	4148	DO-204AH (DO-35)	Ammo
1N4148TR	4148	DO-204AH (DO-35)	Tape and Reel
1N4148_T50R	4148	DO-204AH (DO-35)	Tape and Reel
1N4448	4448	DO-204AH (DO-35)	Bulk
1N4448TR	4448	DO-204AH (DO-35)	Tape and Reel
FDLL914	Black	SOD-80	Tape and Reel
FDLL914A	Black	SOD-80	Tape and Reel
FDLL914B	Black	SOD-80	Tape and Reel
FDLL4148	Black	SOD-80	Tape and Reel
FDLL4148_D87Z	Black	SOD-80	Tape and Reel
FDLL4448	Black	SOD-80	Tape and Reel
FDLL4448_D87Z	Black	SOD-80	Tape and Reel

1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 — Small Signal Diode

Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{RRM}	Maximum Repetitive Reverse Voltage	100	V
I_O	Average Rectified Forward Current	200	mA
I_F	DC Forward Current	300	mA
I_{fr}	Recurrent Peak Forward Current	400	mA
I_{FSM}	Non-repetitive Peak Forward Surge Current	Pulse Width = 1.0 s	A
		Pulse Width = 1.0 μs	A
T_{STG}	Storage Temperature Range	-65 to +200	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Note:

1. These ratings are limiting values above which the serviceability of the diode may be impaired.

Thermal Characteristics

Symbol	Parameter	Max.	Unit
		1N/FDRL 914/A/B / 916/A/B / 4148 / 4448	
P_D	Power Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	300	$^\circ\text{C/W}$

Electrical Characteristics⁽²⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Max.	Unit
V _R	Breakdown Voltage		I _R = 100 μA	100		V
			I _R = 5.0 μA	75		V
V _F	Forward Voltage	914B / 4448	I _F = 5.0 mA	0.62	0.72	V
		916B	I _F = 5.0 mA	0.63	0.73	V
		914 / 916 / 4148	I _F = 10 mA		1.0	V
		914A / 916A	I _F = 20 mA		1.0	V
		916B	I _F = 20 mA		1.0	V
		914B / 4448	I _F = 100 mA		1.0	V
I _R	Reverse Leakage		V _R = 20 V		0.025	μA
			V _R = 20 V, T _A = 150°C		50	μA
			V _R = 75 V		5.0	μA
C _T	Total Capacitance	916/916A/916B/4448	V _R = 0, f = 1.0 MHz		2.0	pF
		914/914A/914B/4148	V _R = 0, f = 1.0 MHz		4.0	pF
t _{rr}	Reverse Recovery Time		I _F = 10 mA, V _R = 6.0 V (600 mA) I _{rr} = 1.0 mA, R _L = 100 Ω		4.0	ns

Note:

2. Non-recurrent square wave $P_W = 8.3 \text{ ms}$.

Typical Performance Characteristics

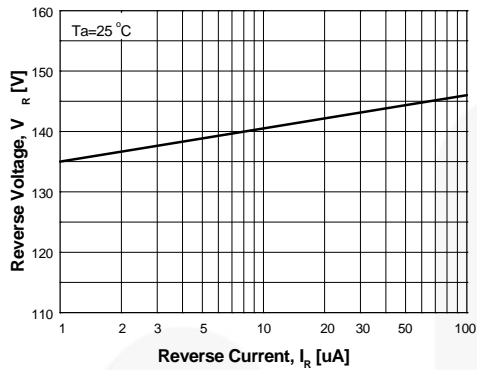


Figure 1. Reverse Voltage vs. Reverse Current
 V_R - 1.0 to 100 μ A

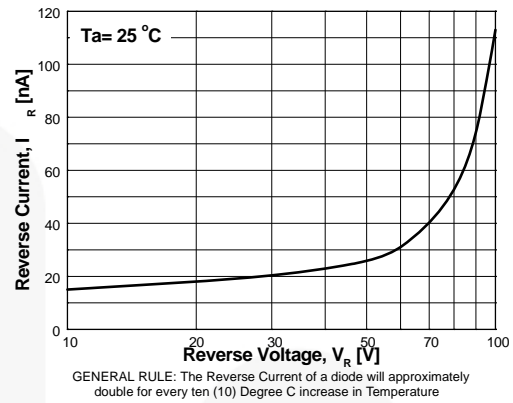


Figure 2. Reverse Current vs. Reverse Voltage
 I_R - 10 to 100 V

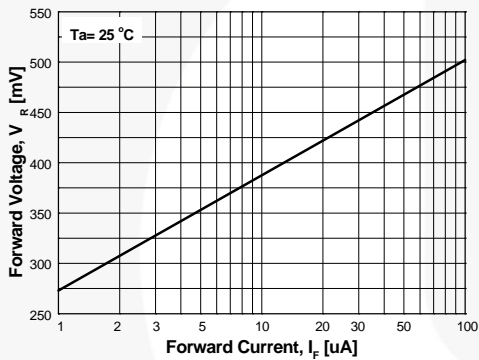


Figure 3. Forward Voltage vs. Forward Current
 V_F - 1 to 100 μ A

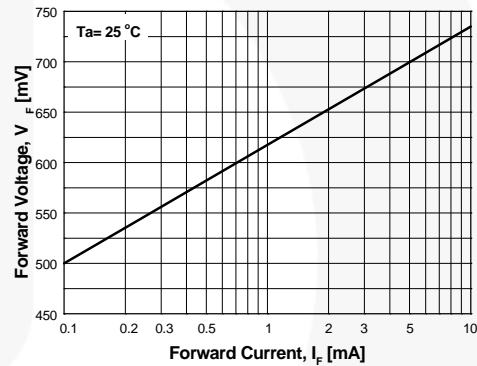


Figure 4. Forward Voltage vs. Forward Current
 V_F - 0.1 to 10 mA

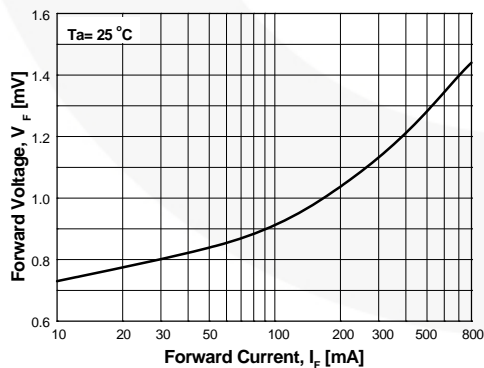


Figure 5. Forward Voltage vs. Forward Current
 V_F - 10 to 800 mA

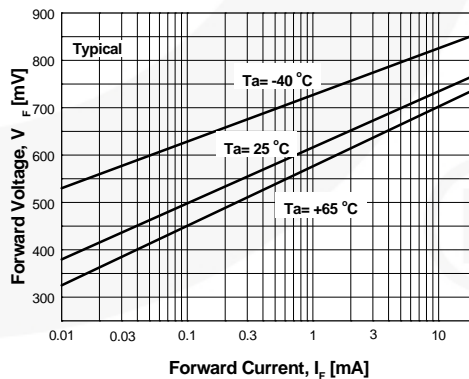


Figure 6. Forward Voltage vs. Ambient Temperature
 V_F - 0.01 - 20 mA (- 40 to +65°C)

Typical Performance Characteristics (Continued)

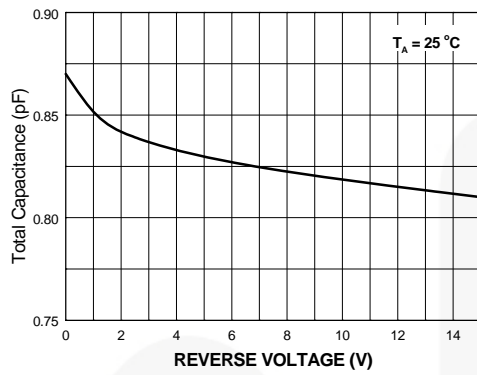


Figure 7. Total Capacitance

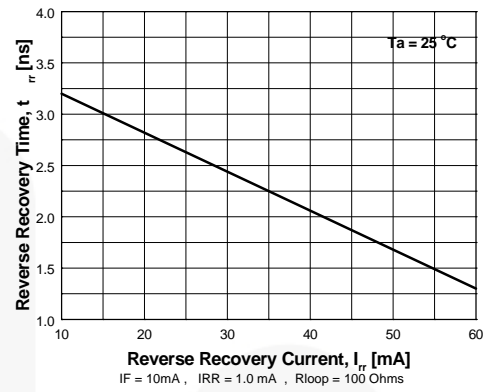


Figure 8. Reverse Recovery Time vs. Reverse Recovery Current

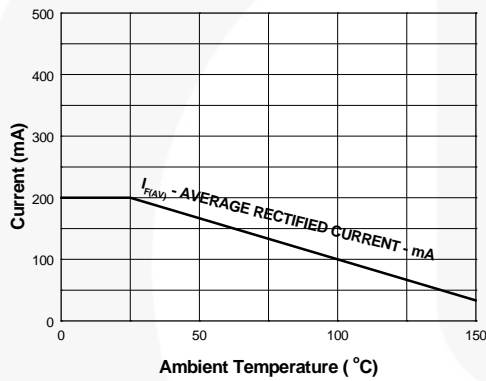


Figure 9. Average Rectified Current ($I_{F(AV)}$) vs. Ambient Temperature (T_A)

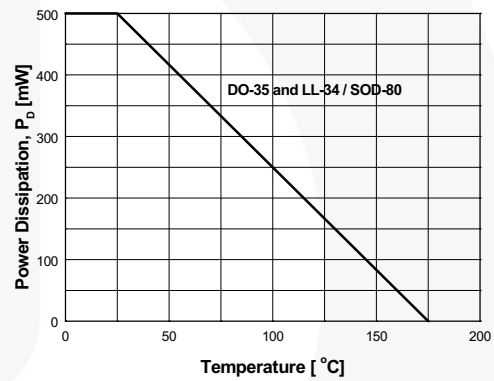


Figure 10. Power Derating Curve

Physical Dimensions

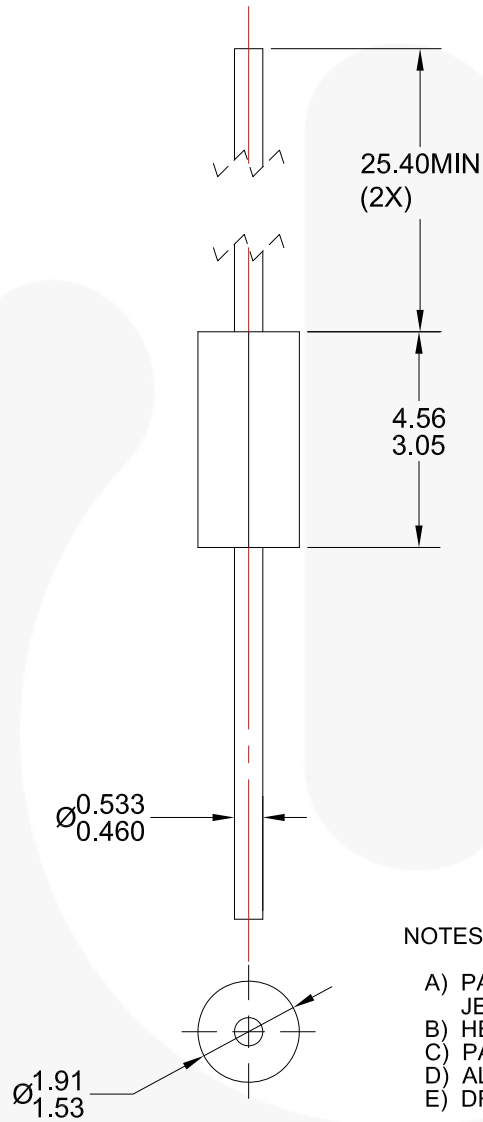
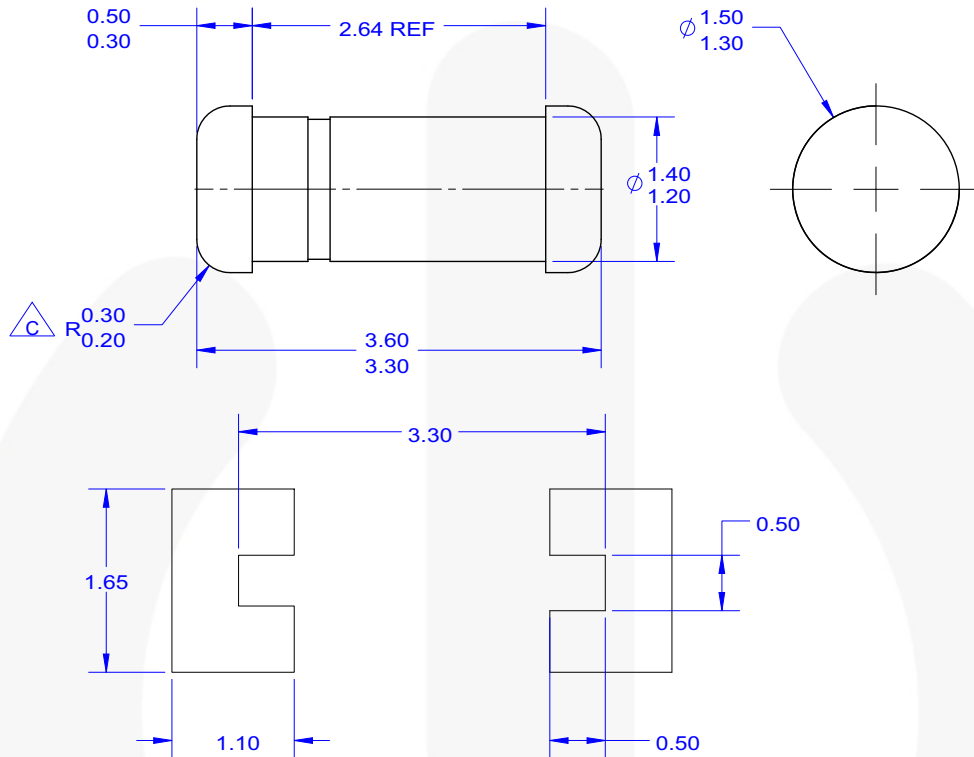


Figure 11. AXIAL LEADED, GLASS, JEDEC DO204, VARIATION AH, DO-204AH (DO-35)

Physical Dimensions (Continued)



LAND PATTERN RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE:
JEDEC DO-213, VARIATION AC.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

 CORNER RADIUS IS OPTIONAL.

D) LAND PATTERN RECOMMENDATION PER IPC DI0MELF3414N

E) DRAWING FILE NAME: SOD80A REV3



Figure 12. 2-TERMINAL, SOD-80, JEDEC DO-213AC, MINI-MELF





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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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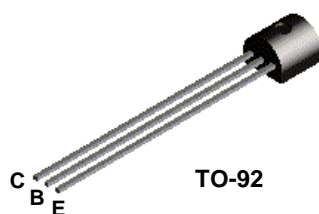
PRODUCT STATUS DEFINITIONS

Definition of Terms

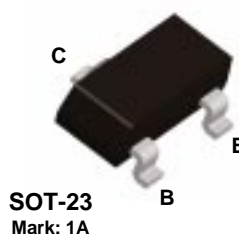
Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 174

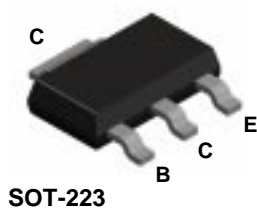
2N3904



MMBT3904



PZT3904



NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier. Sourced from Process 23.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V _{CEO}	Collector-Emitter Voltage	40	V
V _{CBO}	Collector-Base Voltage	60	V
V _{EBO}	Emitter-Base Voltage	6.0	V
I _C	Collector Current - Continuous	200	mA
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These ratings are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

NPN General Purpose Amplifier

(continued)

Electrical Characteristics

TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
--------	-----------	-----------------	-----	-----	-------

OFF CHARACTERISTICS

$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0 \text{ mA}, I_B = 0$	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10 \text{ }\mu\text{A}, I_E = 0$	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10 \text{ }\mu\text{A}, I_C = 0$	6.0		V
I_{BL}	Base Cutoff Current	$V_{CE} = 30 \text{ V}, V_{EB} = 0$		50	nA
I_{CEX}	Collector Cutoff Current	$V_{CE} = 30 \text{ V}, V_{EB} = 0$		50	nA

ON CHARACTERISTICS*

h_{FE}	DC Current Gain	$I_C = 0.1 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 1.0 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 10 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 50 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 100 \text{ mA}, V_{CE} = 1.0 \text{ V}$	40 70 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 1.0 \text{ mA}$ $I_C = 50 \text{ mA}, I_B = 5.0 \text{ mA}$		0.2 0.3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 1.0 \text{ mA}$ $I_C = 50 \text{ mA}, I_B = 5.0 \text{ mA}$	0.65	0.85 0.95	V V

SMALL SIGNAL CHARACTERISTICS

f_T	Current Gain - Bandwidth Product	$I_C = 10 \text{ mA}, V_{CE} = 20 \text{ V},$ $f = 100 \text{ MHz}$	300		MHz
C_{obo}	Output Capacitance	$V_{CB} = 5.0 \text{ V}, I_E = 0,$ $f = 1.0 \text{ MHz}$		4.0	pF
C_{ibo}	Input Capacitance	$V_{EB} = 0.5 \text{ V}, I_C = 0,$ $f = 1.0 \text{ MHz}$		8.0	pF
NF	Noise Figure (except MMPQ3904)	$I_C = 100 \text{ }\mu\text{A}, V_{CE} = 5.0 \text{ V},$ $R_S = 1.0 \text{ k}\Omega, f = 10 \text{ Hz to } 15.7 \text{ kHz}$		5.0	dB

SWITCHING CHARACTERISTICS (except MMPQ3904)

t_d	Delay Time	$V_{CC} = 3.0 \text{ V}, V_{BE} = 0.5 \text{ V},$		35	ns
t_r	Rise Time	$I_C = 10 \text{ mA}, I_{B1} = 1.0 \text{ mA}$		35	ns
t_s	Storage Time	$V_{CC} = 3.0 \text{ V}, I_C = 10 \text{ mA}$		200	ns
t_f	Fall Time	$I_{B1} = I_{B2} = 1.0 \text{ mA}$		50	ns

*Pulse Test: Pulse Width $\leq 300 \text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

Spice Model

NPN (Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259 Ise=6.734 Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)

NPN General Purpose Amplifier
(continued)

Thermal Characteristics

TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		2N3904	*PZT3904	
PD	Total Device Dissipation	625	1,000	mW
	Derate above 25°C	5.0	8.0	mW/°C
RθJC	Thermal Resistance, Junction to Case	83.3		°C/W
RθJA	Thermal Resistance, Junction to Ambient	200	125	°C/W

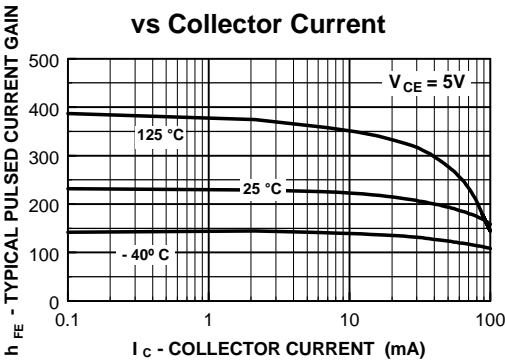
Symbol	Characteristic	Max		Units
		**MMBT3904	MMPQ3904	
PD	Total Device Dissipation	350	1,000	mW
	Derate above 25°C	2.8	8.0	mW/°C
RθJA	Thermal Resistance, Junction to Ambient Effective 4 Die Each Die	357	125	°C/W
			125	°C/W
			240	°C/W

* Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm².

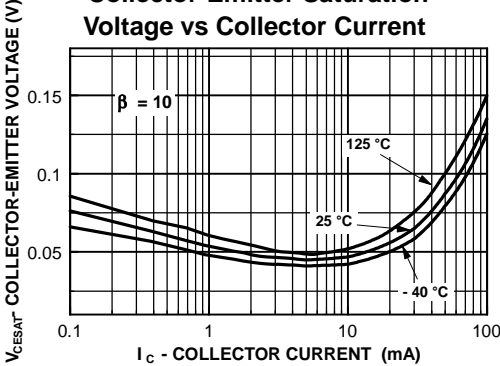
** Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

Typical Characteristics

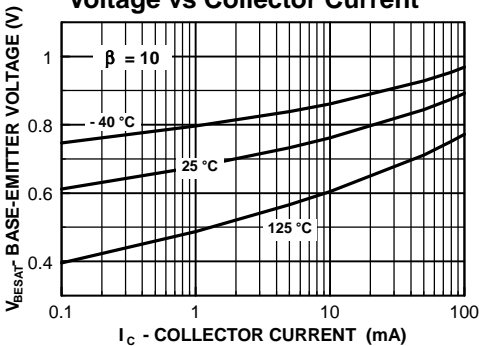
Typical Pulsed Current Gain
vs Collector Current



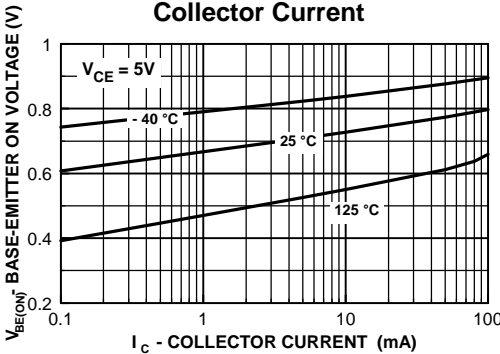
Collector-Emitter Saturation
Voltage vs Collector Current



Base-Emitter Saturation
Voltage vs Collector Current



Base-Emitter ON Voltage vs
Collector Current

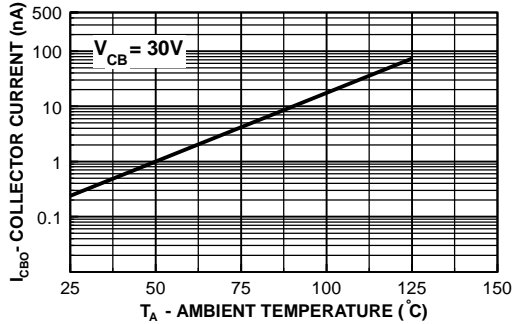


NPN General Purpose Amplifier (continued)

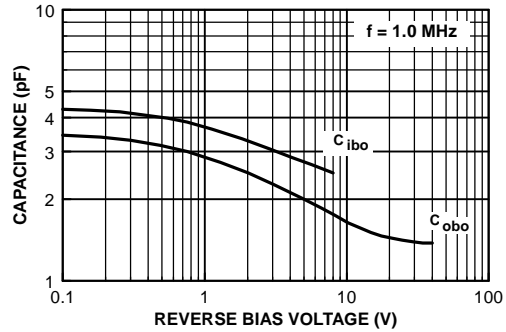
2N3904 / MMBT3904 / PZT3904

Typical Characteristics (continued)

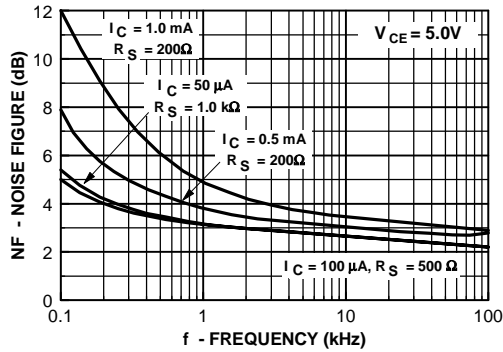
Collector-Cutoff Current
vs Ambient Temperature



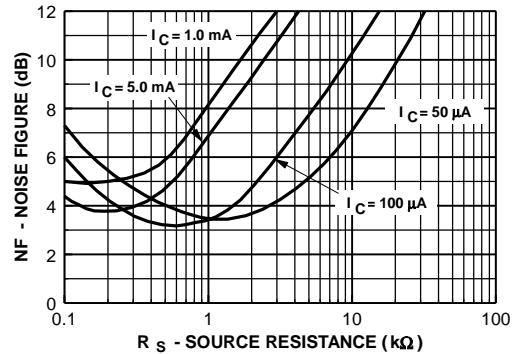
Capacitance vs
Reverse Bias Voltage



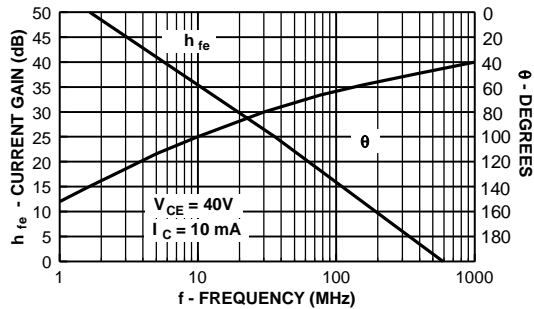
Noise Figure vs Frequency



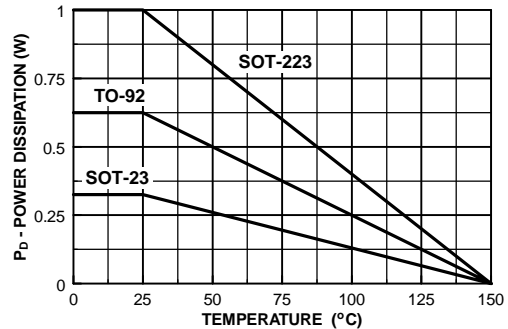
Noise Figure vs Source Resistance



Current Gain and Phase Angle
vs Frequency



Power Dissipation vs
Ambient Temperature

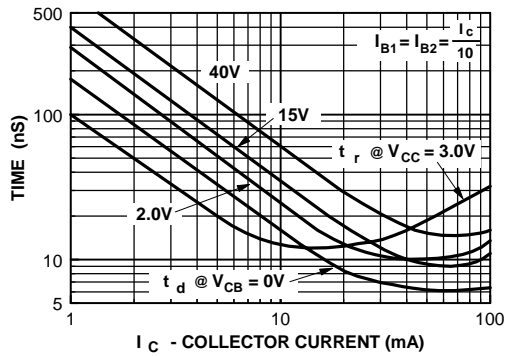


NPN General Purpose Amplifier (continued)

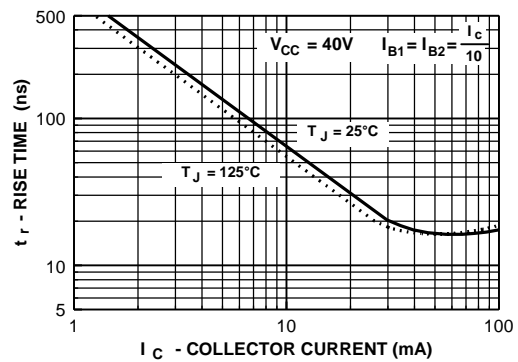
2N3904 / MMBT3904 / PZT3904

Typical Characteristics (continued)

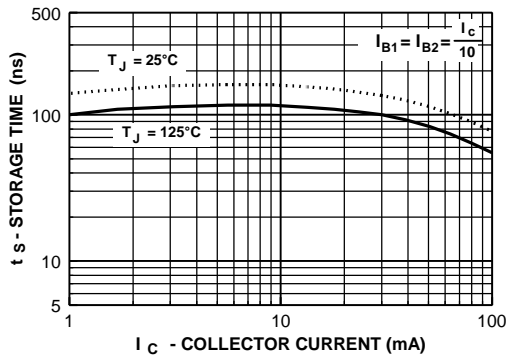
Turn-On Time vs Collector Current



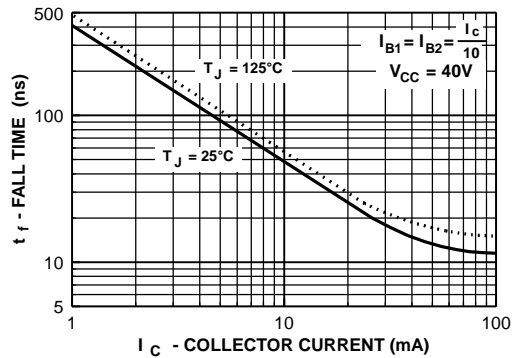
Rise Time vs Collector Current



Storage Time vs Collector Current



Fall Time vs Collector Current



Test Circuits

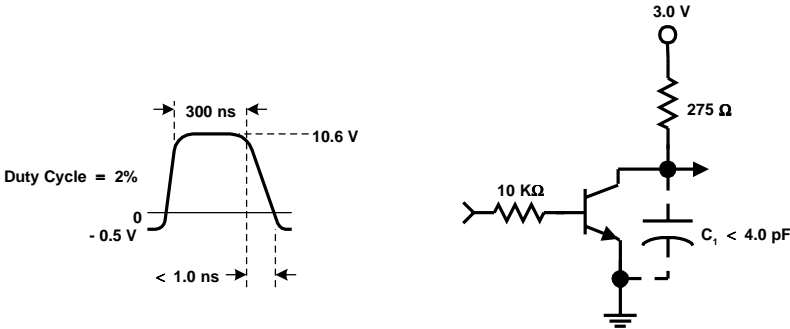


FIGURE 1: Delay and Rise Time Equivalent Test Circuit

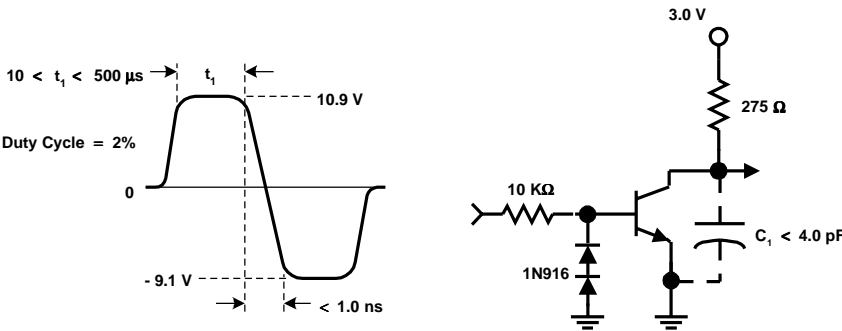


FIGURE 2: Storage and Fall Time Equivalent Test Circuit

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CROSSVOLT™	POP™
E ² CMOS™	PowerTrench™
FACT™	QS™
FACT Quiet Series™	Quiet Series™
FAST®	SuperSOT™-3
FASTr™	SuperSOT™-6
GTO™	SuperSOT™-8
HiSeC™	TinyLogic™

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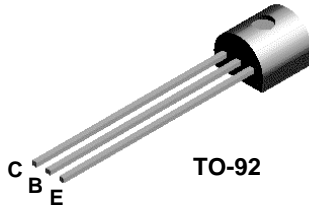
1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

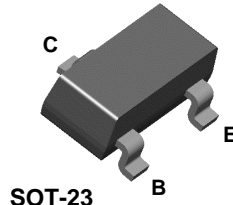
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

2N3906



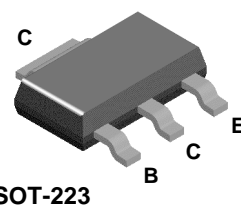
TO-92

MMBT3906



SOT-23
Mark: 2A

PZT3906



SOT-223

PNP General Purpose Amplifier

This device is designed for general purpose amplifier and switching applications at collector currents of 10 μ A to 100 mA.

Absolute Maximum Ratings*

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	40	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These ratings are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- 3) All voltages (V) and currents (A) are negative polarity for PNP transistors.

Thermal Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3906	*MMBT3906	**PZT3906	
P_D	Total Device Dissipation	625	350	1,000	mW
	Derate above 25°C	5.0	2.8	8.0	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	$^\circ\text{C/W}$

* Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

** Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2 .

PNP General Purpose Amplifier

(continued)

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
--------	-----------	-----------------	-----	-----	-------

OFF CHARACTERISTICS

$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	$I_C = 1.0\text{ mA}, I_B = 0$	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10\text{ }\mu\text{A}, I_E = 0$	40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\text{ }\mu\text{A}, I_C = 0$	5.0		V
I_{BL}	Base Cutoff Current	$V_{CE} = 30\text{ V}, V_{BE} = 3.0\text{ V}$		50	nA
I_{CEX}	Collector Cutoff Current	$V_{CE} = 30\text{ V}, V_{BE} = 3.0\text{ V}$		50	nA

ON CHARACTERISTICS

h_{FE}	DC Current Gain *	$I_C = 0.1\text{ mA}, V_{CE} = 1.0\text{ V}$ $I_C = 1.0\text{ mA}, V_{CE} = 1.0\text{ V}$ $I_C = 10\text{ mA}, V_{CE} = 1.0\text{ V}$ $I_C = 50\text{ mA}, V_{CE} = 1.0\text{ V}$ $I_C = 100\text{ mA}, V_{CE} = 1.0\text{ V}$	60 80 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$ $I_C = 50\text{ mA}, I_B = 5.0\text{ mA}$		0.25 0.4	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$ $I_C = 50\text{ mA}, I_B = 5.0\text{ mA}$	0.65	0.85 0.95	V V

SMALL SIGNAL CHARACTERISTICS

f_T	Current Gain - Bandwidth Product	$I_C = 10\text{ mA}, V_{CE} = 20\text{ V},$ $f = 100\text{ MHz}$	250		MHz
C_{obo}	Output Capacitance	$V_{CB} = 5.0\text{ V}, I_E = 0,$ $f = 100\text{ kHz}$		4.5	pF
C_{ibo}	Input Capacitance	$V_{EB} = 0.5\text{ V}, I_C = 0,$ $f = 100\text{ kHz}$		10.0	pF
NF	Noise Figure	$I_C = 100\text{ }\mu\text{A}, V_{CE} = 5.0\text{ V},$ $R_S = 1.0\text{ k}\Omega, f = 10\text{ Hz to } 15.7\text{ kHz}$		4.0	dB

SWITCHING CHARACTERISTICS

t_d	Delay Time	$V_{CC} = 3.0\text{ V}, V_{BE} = 0.5\text{ V},$		35	ns
t_r	Rise Time	$I_C = 10\text{ mA}, I_{B1} = 1.0\text{ mA}$		35	ns
t_s	Storage Time	$V_{CC} = 3.0\text{ V}, I_C = 10\text{ mA}$		225	ns
t_f	Fall Time	$I_{B1} = I_{B2} = 1.0\text{ mA}$		75	ns

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

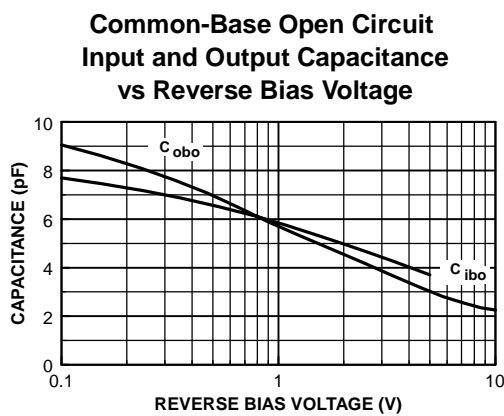
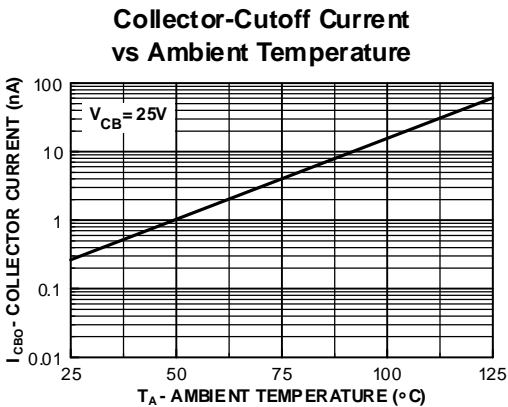
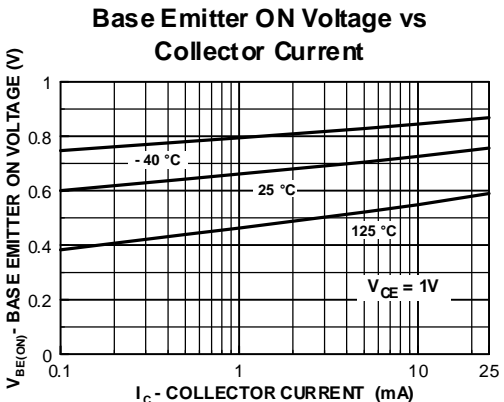
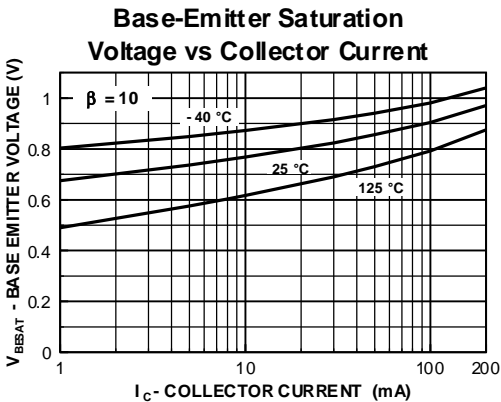
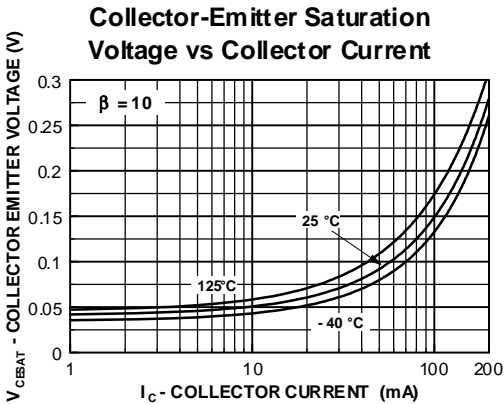
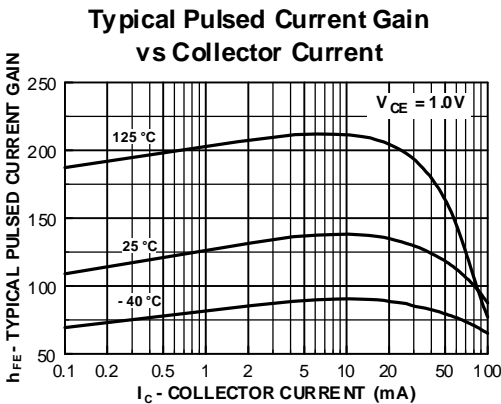
NOTE: All voltages (V) and currents (A) are negative polarity for PNP transistors.

Spice Model

PNP (Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)

2N3906 / MMBT3906 / PZT3906

Typical Characteristics



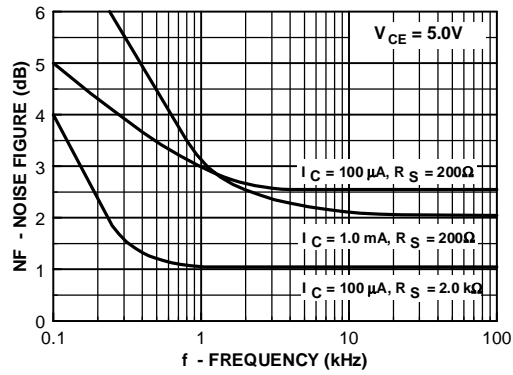
PNP General Purpose Amplifier

(continued)

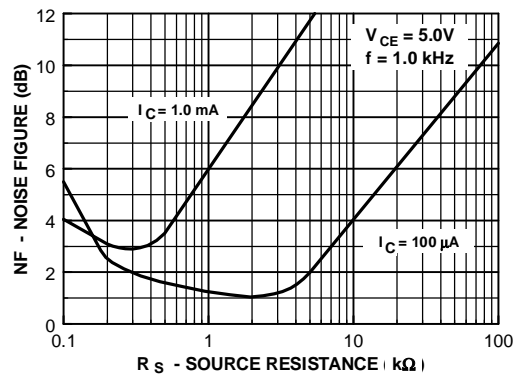
2N3906 / MMBT3906 / PZT3906

Typical Characteristics (continued)

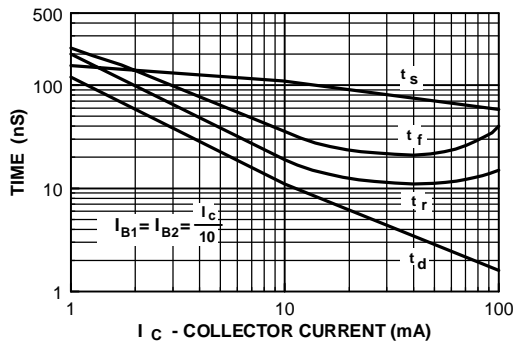
Noise Figure vs Frequency



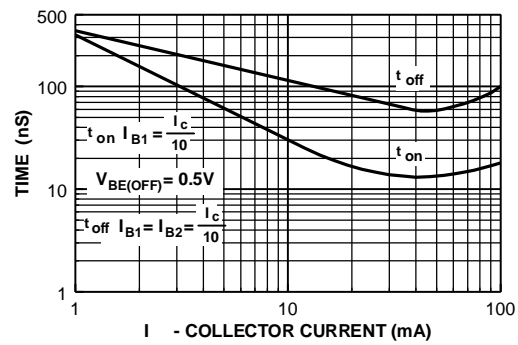
Noise Figure vs Source Resistance



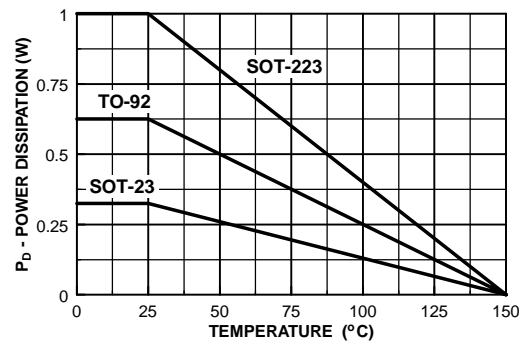
Switching Times vs Collector Current



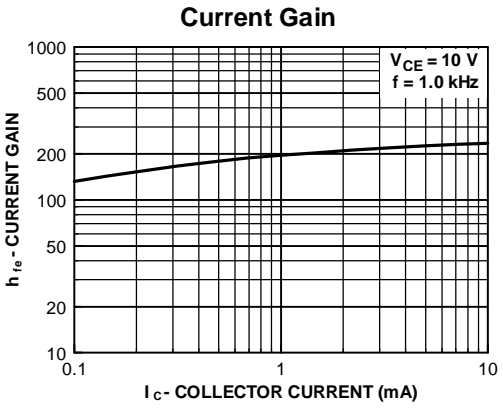
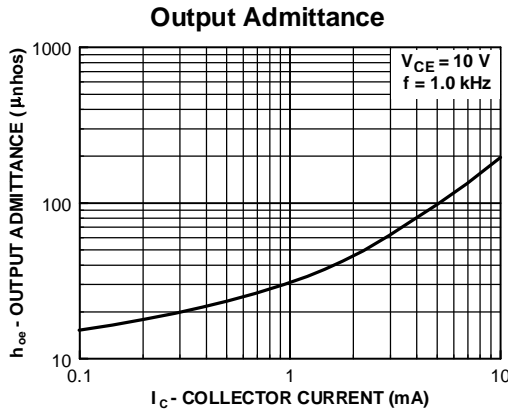
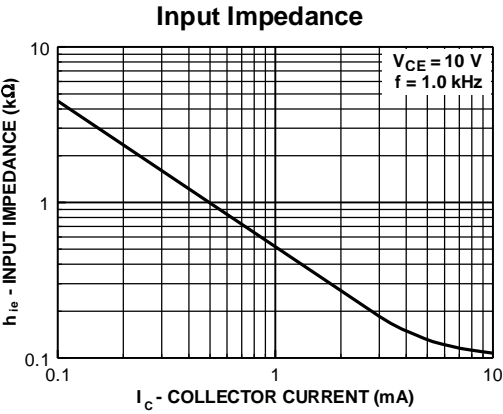
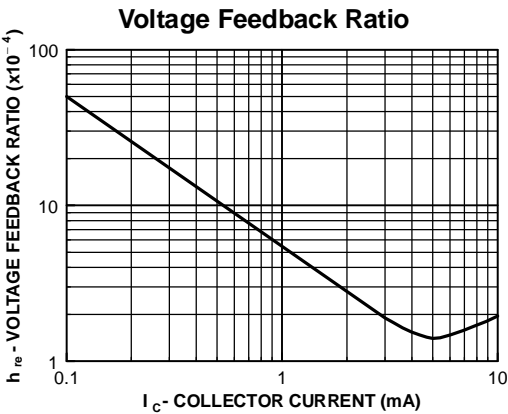
Turn On and Turn Off Times vs Collector Current



Power Dissipation vs Ambient Temperature



Typical Characteristics (continued)



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DOME TM	ISOPLANAR TM	Quiet Series TM	
E ² CMOS TM	MICROWIRE TM	SILENT SWITCHER [®]	
EnSigna TM	OPTOLOGIC TM	SMART START TM	
FACT TM	OPTOPLANAR TM	SuperSOT TM -3	
FACT Quiet Series TM	PACMAN TM	SuperSOT TM -6	
FAST [®]	POP TM	SuperSOT TM -8	

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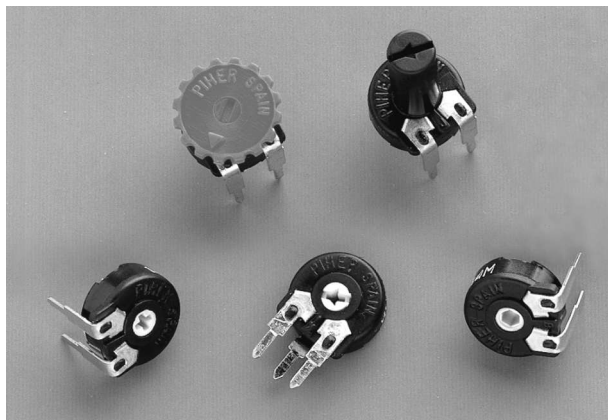
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Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.



FEATURES

- Carbon resistive element
- Dust proof enclosure
- Polyester substrate
- Also upon request:
 - Wiper positioned at 50% or fully clockwise.
 - Supplied in magazines for automatic insertion.
 - Long life model for low cost control potentiometer applications
 - Self extinguishable plastic UL 94V-0
 - Cut track option
 - Special tapers
 - Mechanical detents
 - Low & extra low torque versions

MECHANICAL SPECIFICATIONS

- Mechanical rotation angle: $235^\circ \pm 5^\circ$
- Electrical rotation angle: $220^\circ \pm 20^\circ$
- Torque: 0.4 to 2 Ncm.
(0.6 to 2.7 in-oz)
- Stop torque: > 5 Ncm. (> 7 in-oz)

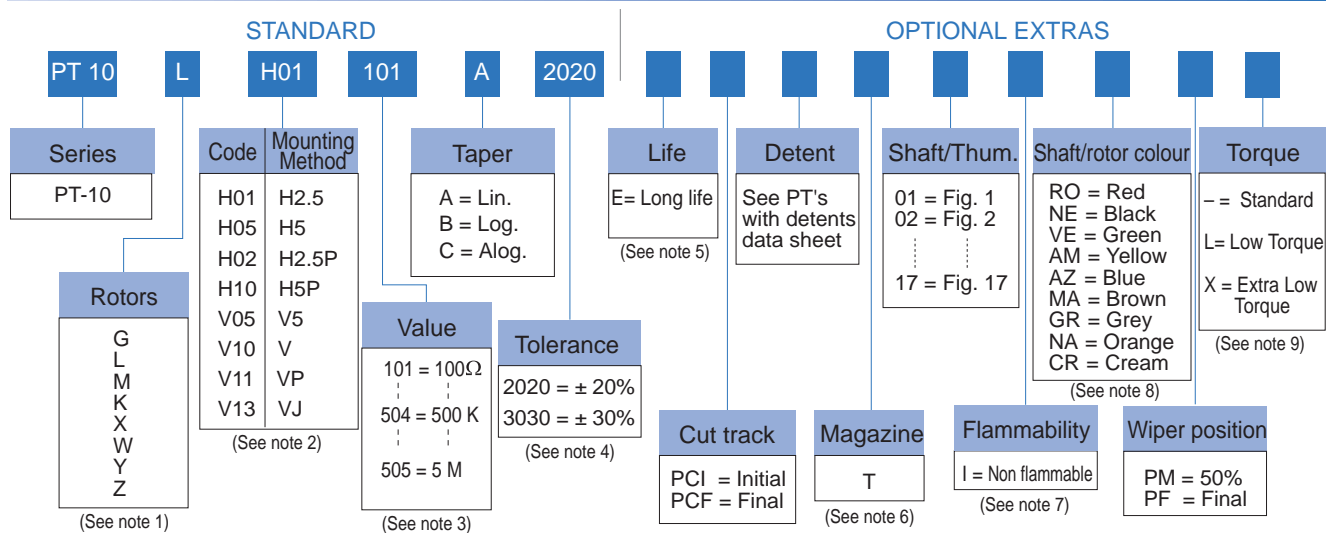
ELECTRICAL SPECIFICATIONS

- Range of values (*)
 $100\Omega \leq R_n \leq 5\text{ M}$ (Decad. 1.0 - 2.0 - 2.2 - 2.5 - 4.7 - 5.0)
- Tolerance (*): $100\Omega \leq R_n \leq 1\text{ M}\Omega$ $\pm 20\%$
 $1\text{ M}\Omega < R_n \leq 5\text{ M}\Omega$ $\pm 30\%$
- Max. Voltage: 200 VDC (lin) 100 VDC (no lin)
- Nominal Power 50°C (122°F) (see power rating curve)
0.15 W (lin) 0.07 W (no lin)
- Taper (*) (Log. & Alog. only $R_n > 1\text{ K}$) Lin ; Log; Alog.
- Residual resistance: $\leq 5 \cdot 10^{-3} R_n$ (2 Ω min.)
- Equivalent Noise Resistance: $\leq 3\% R_n$ (3 Ω min.)
- Operating temperature**: -25°C + 70°C (-13°F + 158°F)

(*) Others upon request

** Up to 85°C depending on application

HOW TO ORDER



NOTES:

- "Z" adjustment only available on "H" versions
- Terminals styles: "P" & "J" are crimped terminals
- Value Example: Code: 10 1 100 Ω
Numb of zeros
First two digits of the value.
- Non standard tolerance, upon request. Example: +7% Code: 07 05
-5% negative tolerance
positive tolerance
- Life
 - Standard 500 cycles
 - Long life 10000 cycles
- Magazines: not available with the H10, V05 and V13 models, nor with adjustment types X, W, Y, Z.
- Non flammable: housing, rotor and shaft.
- Colour shaft/rotor:
 - Potentiometer without shaft: only rotor
 - Potentiometer with shaft: only shaft
 - Cream colour only available in standard plastic.
- Low Torque: 0.25 to 1 Ncm (per pot.)
Extra Low Torque: 0.1 to 0.4 Ncm (per pot.)
No detent option available for low and extra low torque models

NOTE: The information contained here in may be changed without prior notice.

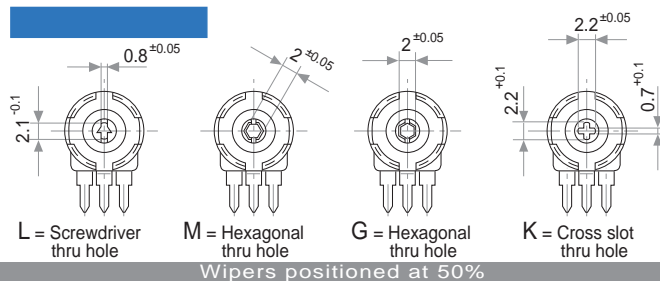
HOW TO ORDER CUSTOM DRAWING

PT-10 LH 01 + DRAWING NUMBER (Max. 16 characters)

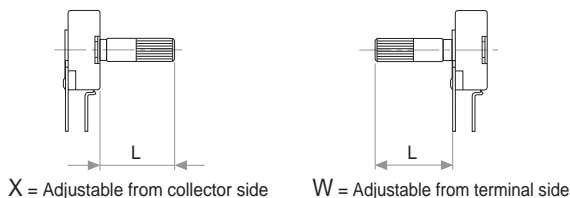
This way of ordering should be used for options which are not included in the "How to order" standard and optional extras.

STANDARD OPTIONS

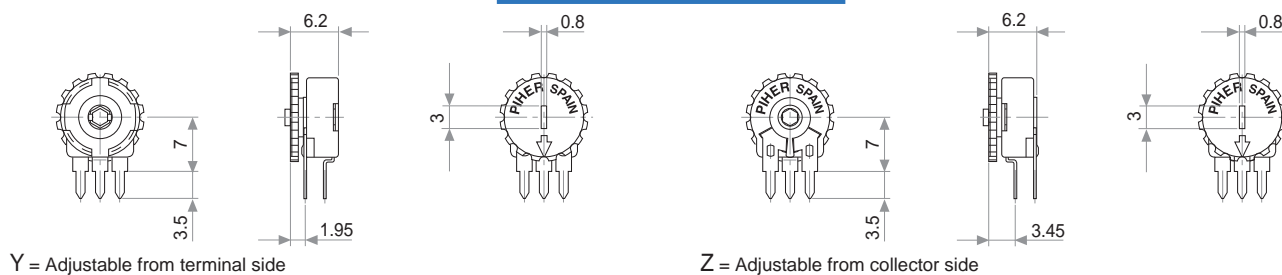
Mechanical Life	500 cycles
Cut track	No
Detents	None
Packing	Bulk
Non flammable	No
Rotor colour	White
Shaft colour	Natural
Wiper position	Initial
Torque	Standard



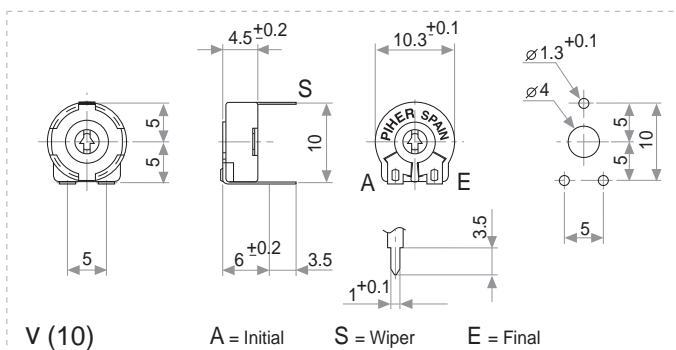
With shaft



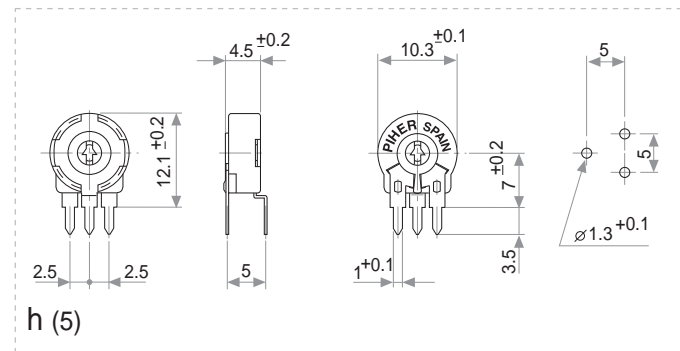
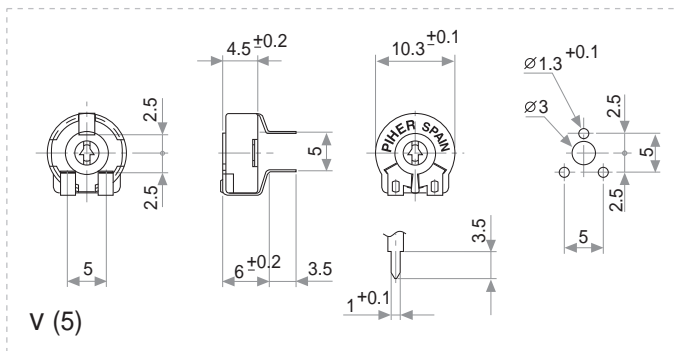
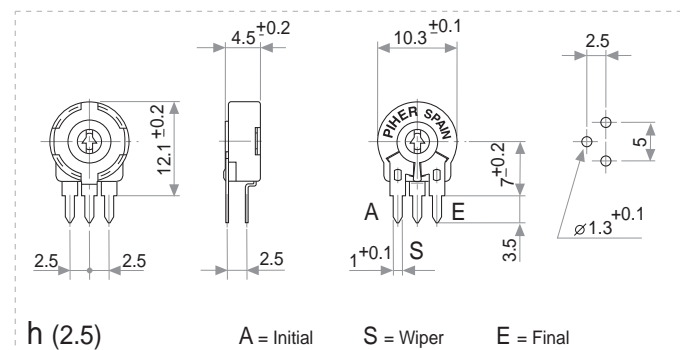
With thumbwheel



V = horizontal mount – vertical adjust

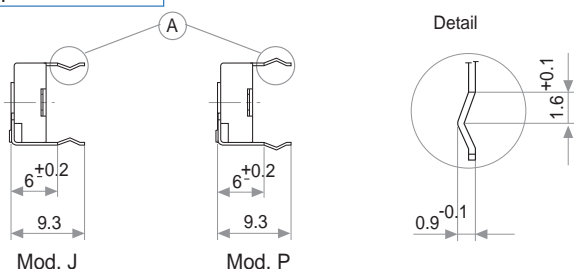


h = vertical mount – horizontal adjust

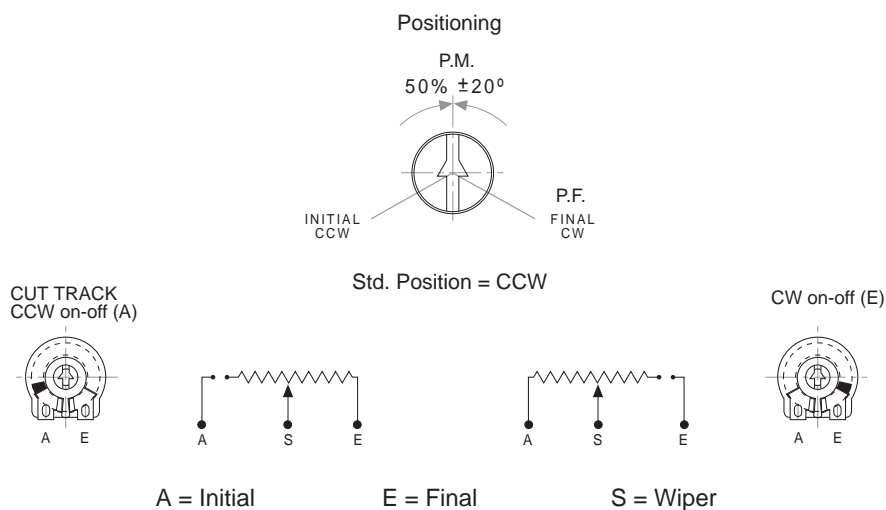


NOTE = Please note relative terminal positions when ordering non linear tapers.

Crimped terminals



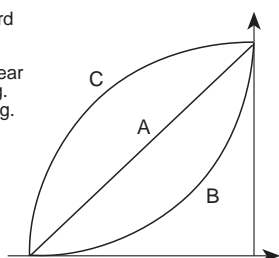
OPTIONS



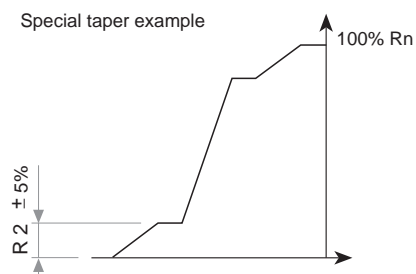
TAPERS

Standard

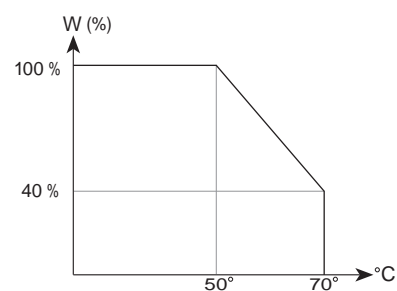
A = Linear
B = Log.
C = Alog.



Special taper example



POWER RATING CURVE



NOTE = Please note relative terminal positions when ordering non linear tapers.

TESTS

TYPICAL VARIATIONS

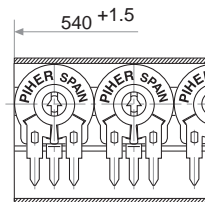
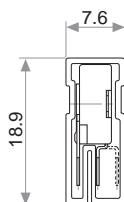
ELECTRICAL LIFE	1.000 h. @ 50°C; 0.15 W	±5 %
MECHANICAL LIFE (CYCLES)	500 @ 10 CPM ... 15 CPM	±3 % (Rn < 1 MΩ)
TEMPERATURE COEFFICIENT	-25°C; +70°C	±300 ppm (Rn < 100 K)
THERMAL CYCLING	16 h. @ 85°C; 2h. @ -25°C	±2.5 %
DAMP HEAT	500 h. @ 40°C @ 95% HR	±5 %
VIBRATION (for each plane X,Y,Z)	2 h. @ 10 Hz. ... 55 Hz.	±2 %

NOTE: Out of range values may not comply these results.

PACKAGING

BOXES

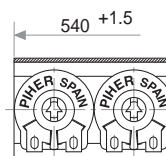
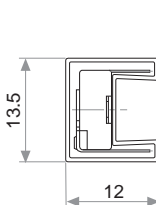
Model	Units
Without shaft	500 (40 x 85 x 185 mm.)
With thumbwheel	400 (40 x 85 x 185 mm.)
With shaft	200 (40 x 85 x 185 mm.)



Magazines for PT-10 h 2.5; h 5
Also crimped term. h 2.5 P

AUTOMATIC INSERTION

Magazines	Units per magazine
PT-10H & PT-10V	50 Pieces



Magazines for PT-10 V
Also crimped term. VP

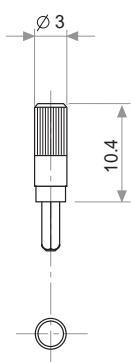


Fig. 1 / Ref. 5016

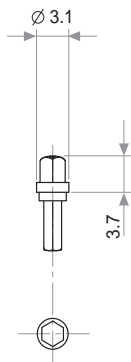


Fig. 2 / Ref. 5053

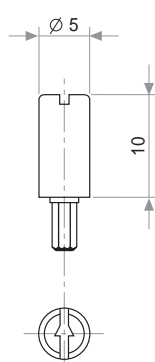


Fig. 3 / Ref. 5012

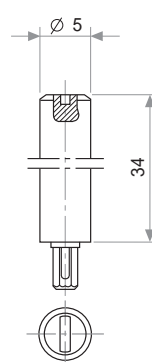


Fig. 4 / Ref. 6053

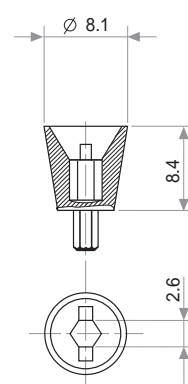


Fig. 6 / Ref. 5035

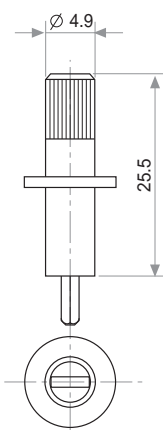


Fig. 7 / Ref. 5115

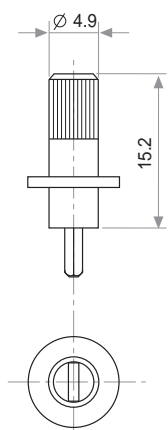


Fig. 8 / Ref. 5116

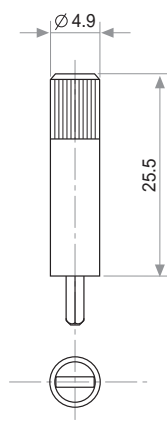


Fig. 9 / Ref. 5119

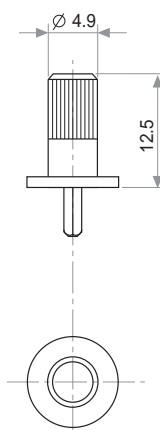


Fig. 10 / Ref. 5120

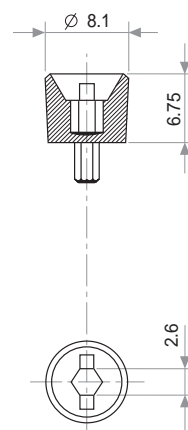


Fig. 11 / Ref. 5027

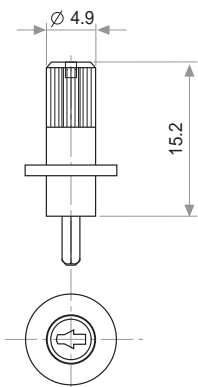


Fig. 12 / Ref. 6052

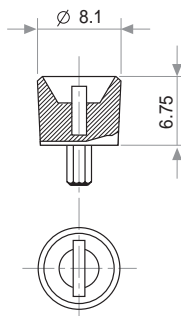


Fig. 13 / Ref. 5121

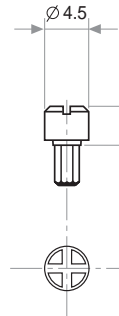


Fig. 14 / Ref. 5055

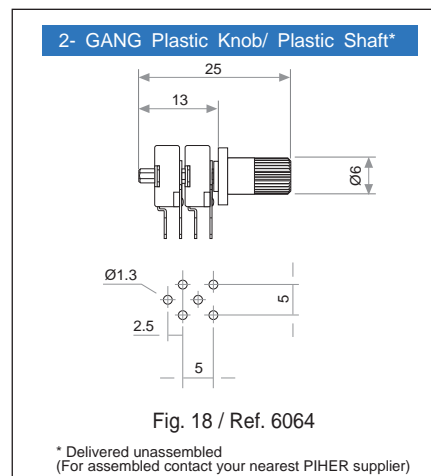


Fig. 18 / Ref. 6064

THUMBWHEELS

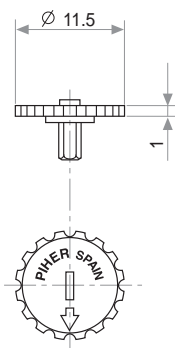


Fig. 5 / Ref. 5034

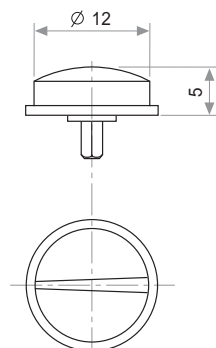


Fig. 15 / Ref. 6008

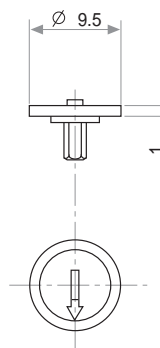


Fig. 16 / Ref. 5039

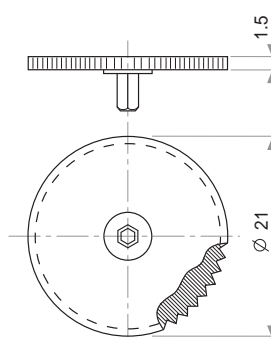


Fig. 17 / Ref. 5062

xx555 Precision Timers

1 Features

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up to 200 mA
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Fingerprint Biometrics
- Iris Biometrics
- RFID Reader

3 Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
xx555	PDIP (8)	9.81 mm × 6.35 mm
	SOP (8)	6.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

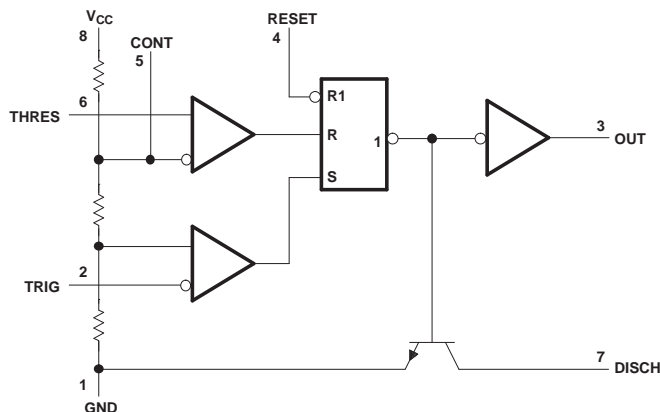


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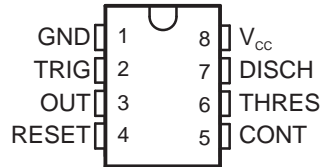
1 Features	1	8.1 Overview	9
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5 Revision History

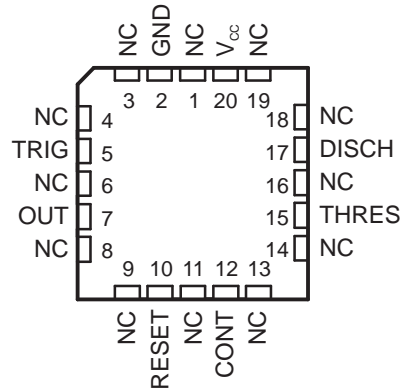
Changes from Revision H (June 2010) to Revision I	Page
• Updated document to new TI enhanced data sheet format.	1
• Deleted Ordering Information table.	1
• Added Military Disclaimer to Features list.	1
• Added Applications.	1
• Added Device Information table.	1
• Moved T_{stg} to Handling Ratings table.	4
• Added DISCH switch on-state voltage parameter.	5
• Added Device and Documentation Support section.	19
• Added ESD warning.	19
• Added Mechanical, Packaging, and Orderable Information section.	19

6 Pin Configuration and Functions

**NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)**



**SE555...FK PACKAGE
(TOP VIEW)**



NC – No internal connection

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, P, PS, PW, JG	FK		
	NO.			
CONT	5	12	I/O	Controls comparator thresholds, Outputs 2/3 VCC, allows bypass capacitor connection
DISCH	7	17	O	Open collector output to discharge timing capacitor
GND	1	2	–	Ground
NC		1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	–	No internal connection
OUT	3	7	O	High current timer output signal
RESET	4	10	I	Active low reset input forces output and discharge low.
THRES	6	15	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	5	I	Start of timing input. TRIG < ½ CONT sets output high and discharge open
V _{CC}	8	20	–	Input supply voltage, 4.5 V to 16 V. (SE555 maximum is 18 V)

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾			18	V
V _I	Input voltage	CONT, RESET, THRES, TRIG		V _{CC}	V
I _O	Output current			±225	mA
θ _{JA}	Package thermal impedance ^{(3) (4)}	D package		97	°C/W
		P package		85	
		PS package		95	
		PW package		149	
θ _{JC}	Package thermal impedance ^{(5) (6)}	FK package		5.61	°C/W
		JG package		14.5	
T _J	Operating virtual junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	JG package		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A) / θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Maximum power dissipation is a function of T_{J(max)}, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is P_D = (T_{J(max)} - T_C) / θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with MIL-STD-883.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V _I	Input voltage	CONT, RESET, THRES, and TRIG		V _{CC}	V
I _O	Output current			±200	mA
T _A	Operating free-air temperature	NA555	-40	105	°C
		NE555	0	70	
		SA555	-40	85	
		SE555	-55	125	

7.4 Electrical Characteristics

 $V_{CC} = 5\text{ V to }15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	$V_{CC} = 15\text{ V}$		9.4	10	10.6	8.8	10	11.2	V
	$V_{CC} = 5\text{ V}$		2.7	3.3	4	2.4	3.3	4.2	
THRES current ⁽¹⁾				30	250		30	250	nA
TRIG voltage level	$V_{CC} = 15\text{ V}$		4.8	5	5.2	4.5	5	5.6	V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	3		6				
	$V_{CC} = 5\text{ V}$		1.45	1.67	1.9	1.1	1.67	2.2	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			1.9				
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	$T_A = -55^\circ\text{C to }125^\circ\text{C}$				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			-0.4	-1		-0.4	-1.5	
DISCH switch off-state current				20	100		20	100	nA
DISCH switch on-state voltage	$V_{CC} = 5\text{ V}$, $I_O = 8\text{ mA}$						0.15	0.4	V
CONT voltage (open circuit)	$V_{CC} = 15\text{ V}$		9.6	10	10.4	9	10	11	V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	9.6		10.4				
	$V_{CC} = 5\text{ V}$		2.9	3.3	3.8	2.6	3.3	4	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	2.9		3.8				
Low-level output voltage	$V_{CC} = 15\text{ V}$, $I_{OL} = 10\text{ mA}$			0.1	0.15		0.1	0.25	V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			0.2				
	$V_{CC} = 15\text{ V}$, $I_{OL} = 50\text{ mA}$			0.4	0.5		0.4	0.75	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			1				
	$V_{CC} = 15\text{ V}$, $I_{OL} = 100\text{ mA}$			2	2.2		2	2.5	
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$			2.7				
	$V_{CC} = 15\text{ V}$, $I_{OL} = 200\text{ mA}$			2.5			2.5		
	$V_{CC} = 5\text{ V}$, $I_{OL} = 3.5\text{ mA}$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$			0.35				
				0.1	0.2		0.1	0.35	
	$V_{CC} = 5\text{ V}$, $I_{OL} = 5\text{ mA}$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$			0.8				
				0.15	0.25		0.15	0.4	
High-level output voltage	$V_{CC} = 15\text{ V}$, $I_{OH} = -100\text{ mA}$		13	13.3		12.75	13.3		V
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	12						
	$V_{CC} = 15\text{ V}$, $I_{OH} = -200\text{ mA}$			12.5			12.5		
	$V_{CC} = 5\text{ V}$, $I_{OH} = -100\text{ mA}$		3	3.3		2.75	3.3		
		$T_A = -55^\circ\text{C to }125^\circ\text{C}$	2						
Supply current	Output low, No load	$V_{CC} = 15\text{ V}$		10	12		10	15	mA
		$V_{CC} = 5\text{ V}$		3	5		3	6	
	Output high, No load	$V_{CC} = 15\text{ V}$		9	10		9	13	
		$V_{CC} = 5\text{ V}$		2	4		2	5	

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of [Figure 12](#). For example, when $V_{CC} = 5\text{ V}$, the maximum value is $R = R_A + R_B \neq 3.4\text{ M}\Omega$, and for $V_{CC} = 15\text{ V}$, the maximum value is $10\text{ M}\Omega$.

7.5 Operating Characteristics

 $V_{CC} = 5\text{ V to }15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval ⁽²⁾	Each timer, monostable ⁽³⁾	$T_A = 25^\circ\text{C}$		0.5	1.5 ⁽⁴⁾		1	3	%
	Each timer, astable ⁽⁵⁾			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable ⁽³⁾	$T_A = \text{MIN to MAX}$		30	100 ⁽⁴⁾		50		ppm/ °C
	Each timer, astable ⁽⁵⁾			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable ⁽³⁾	$T_A = 25^\circ\text{C}$		0.05	0.2 ⁽⁴⁾		0.1	0.5	%/V
	Each timer, astable ⁽⁵⁾			0.15			0.3		
Output-pulse rise time		$C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$		100	200 ⁽⁴⁾		100	300	ns
Output-pulse fall time		$C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$		100	200 ⁽⁴⁾		100	300	ns

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
- (2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
- (3) Values specified are for a device in a monostable circuit similar to [Figure 9](#), with the following component values: $R_A = 2\text{ k}\Omega$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$.
- (4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (5) Values specified are for a device in an astable circuit similar to [Figure 12](#), with the following component values: $R_A = 1\text{ k}\Omega$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$.

7.6 Typical Characteristics

Data for temperatures below -40°C and above 105°C are applicable for SE555 circuits only.

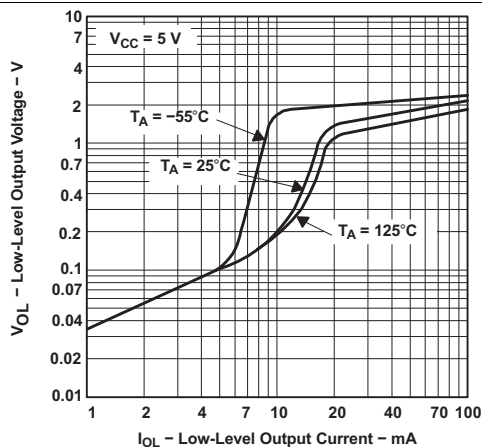


Figure 1. Low-Level Output Voltage vs Low-Level Output Current

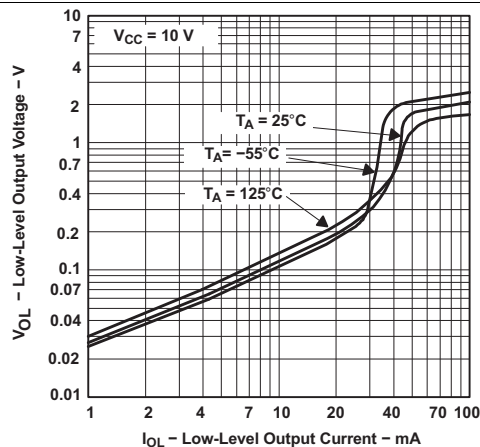


Figure 2. Low-Level Output Voltage vs Low-Level Output Current

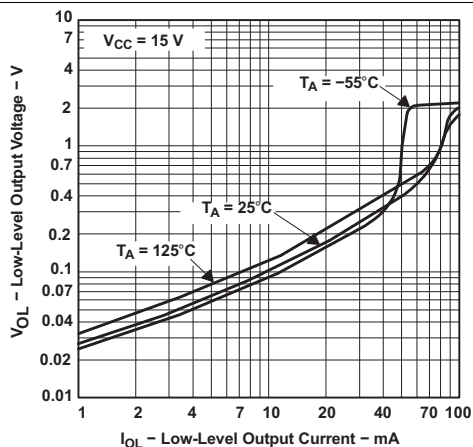


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

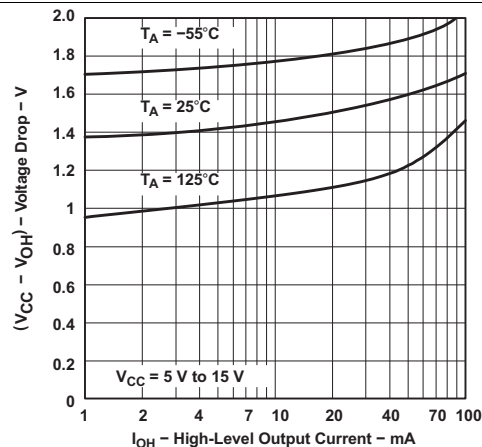


Figure 4. Drop Between Supply Voltage and Output vs High-Level Output Current

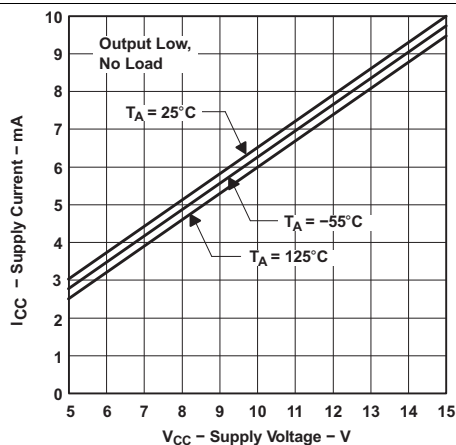


Figure 5. Supply Current vs Supply Voltage

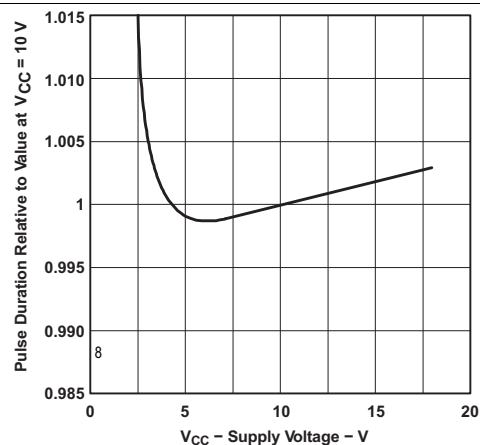


Figure 6. Normalized Output Pulse Duration (Monostable Operation) vs Supply Voltage

Typical Characteristics (continued)

Data for temperatures below -40°C and above 105°C are applicable for SE555 circuits only.

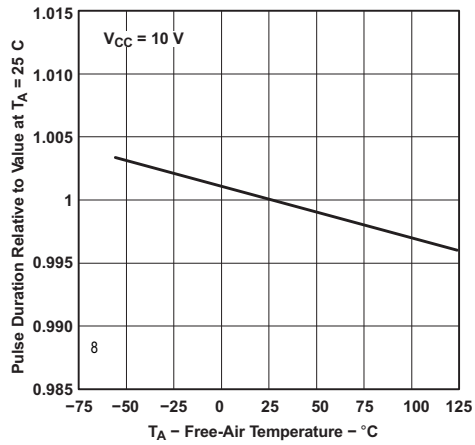


Figure 7. Normalized Output Pulse Duration (Monostable Operation) vs Free-Air Temperature

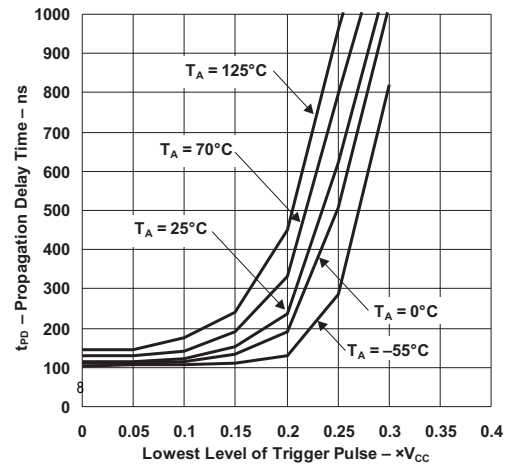


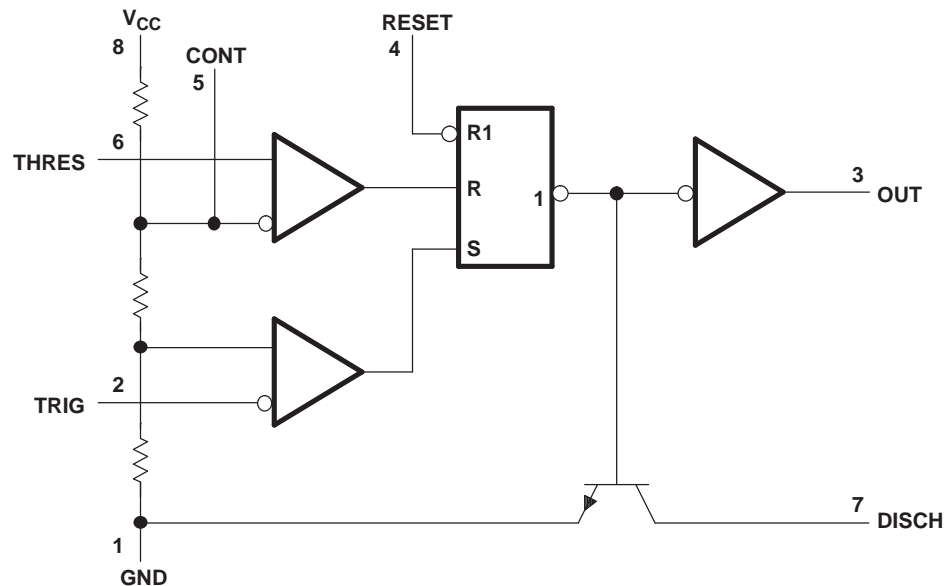
Figure 8. Propagation Delay Time vs Lowest Voltage Level of Trigger Pulse

8 Detailed Description

8.1 Overview

The xx555 timer is a popular and easy to use for general purpose timing applications from 10 μ s to hours or from < 1mHz to 100 kHz. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor. Maximum output sink and discharge sink current is greater for higher VCC and less for lower VCC.

8.2 Functional Block Diagram



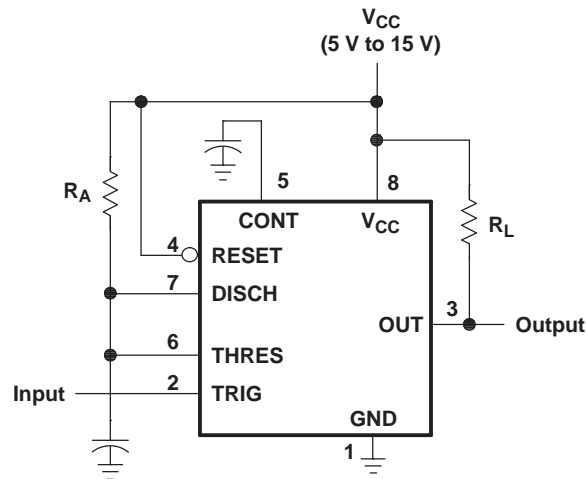
- A. Pin numbers shown are for the D, JG, P, PS, and PW packages.
- B. RESET can override TRIG, which can override THRES.

8.3 Feature Description

8.3.1 Mono-stable Operation

For mono-stable operation, any of these timers can be connected as shown in [Figure 9](#). If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop (\bar{Q} goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop (\bar{Q} goes high), drives the output low, and discharges C through Q1.

Feature Description (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 μ s before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 μ s, which limits the minimum monostable pulse width to 10 μ s. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_A C$. [Figure 11](#) is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC} .

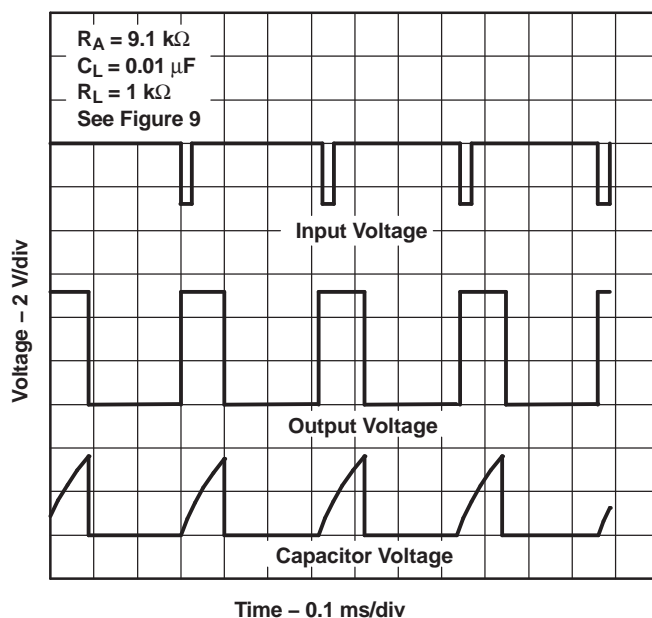


Figure 10. Typical Monostable Waveforms

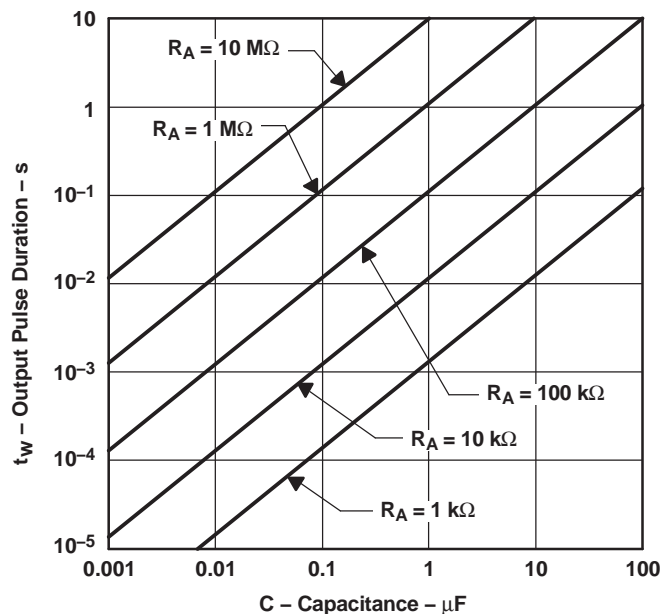


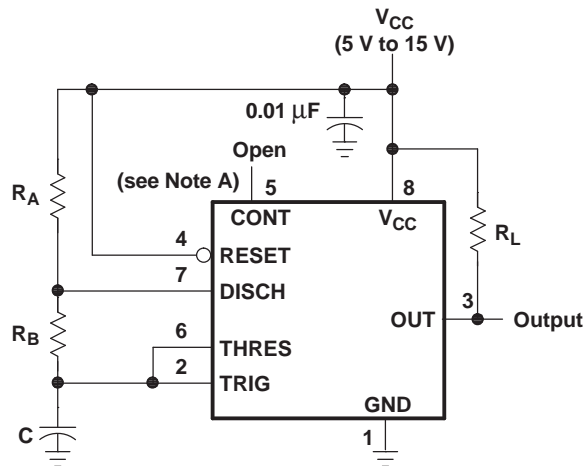
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

8.3.2 A-stable Operation

As shown in Figure 12, adding a second resistor, R_B , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

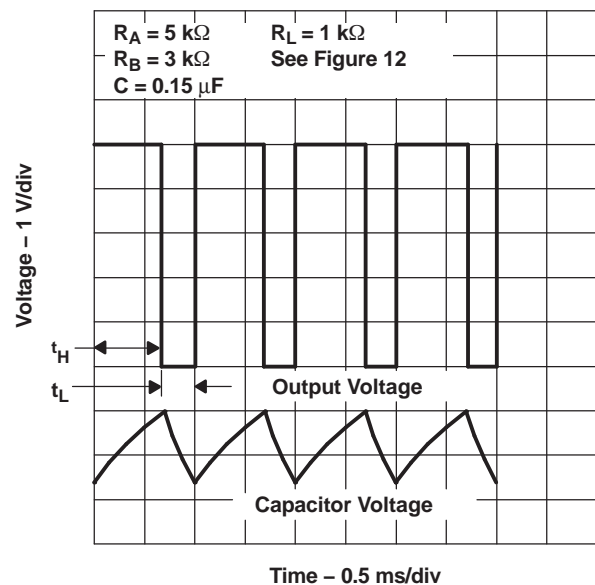


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Feature Description (continued)

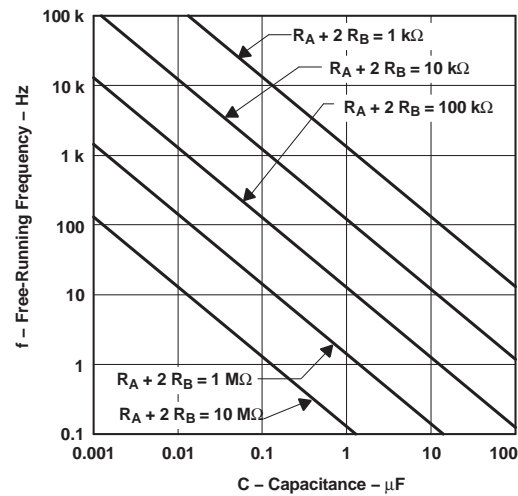


Figure 14. Free-Running Frequency

8.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of [Figure 9](#) can be made to operate as a frequency divider. [Figure 15](#) shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

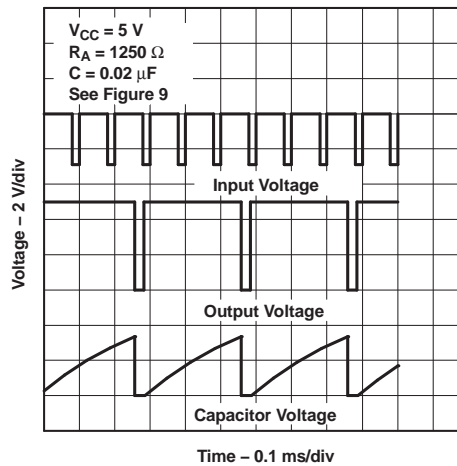


Figure 15. Divide-by-Three Circuit Waveforms

8.4 Device Functional Modes

Table 1. Function Table

RESET	TRIGGER VOLTAGE ⁽¹⁾	THRESHOLD VOLTAGE ⁽¹⁾	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V _{CC}	Irrelevant	High	Off
High	>1/3 V _{CC}	>2/3 V _{CC}	Low	On
High	>1/3 V _{CC}	<2/3 V _{CC}	As previously established	

(1) Voltage levels shown are nominal.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

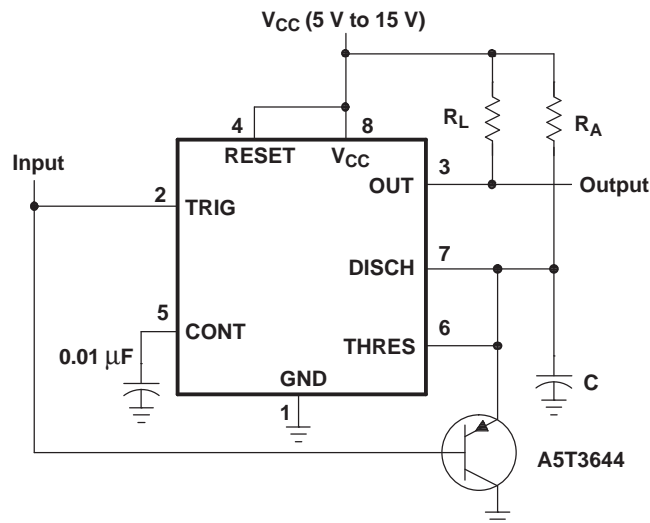
9.1 Application Information

The xx555 timer devices use resistor and capacitor charging delay to provide a programmable time delay or operating frequency. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Missing-Pulse Detector

The circuit shown in [Figure 16](#) can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in [Figure 17](#).



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 16. Circuit for Missing-Pulse Detector

9.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. Input stuck low will not be detected because timing capacitor "C" will remain discharged.

9.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C > [\text{maximum normal input high time}]$. R_L improves V_{OH} , but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.1.3 Application Curves

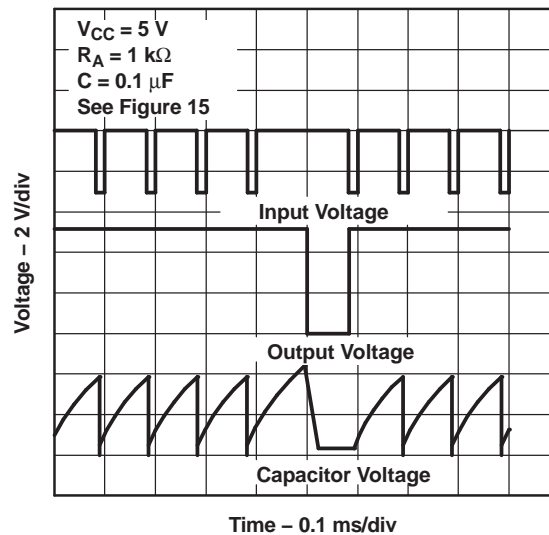
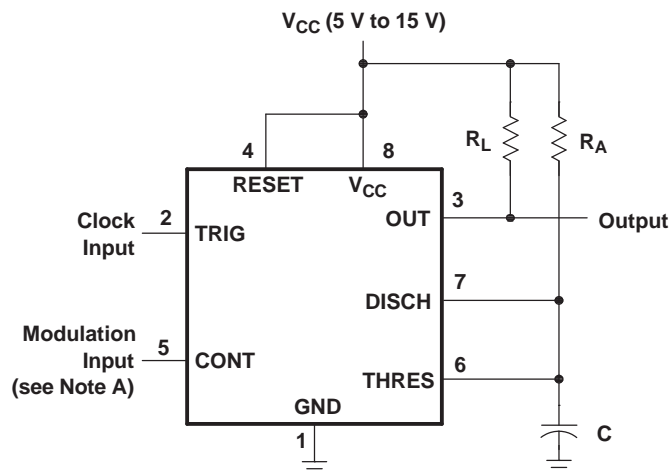


Figure 17. Completed Timing Waveforms for Missing-Pulse Detector

9.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. [Figure 18](#) shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. [Figure 19](#) shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

Typical Applications (continued)

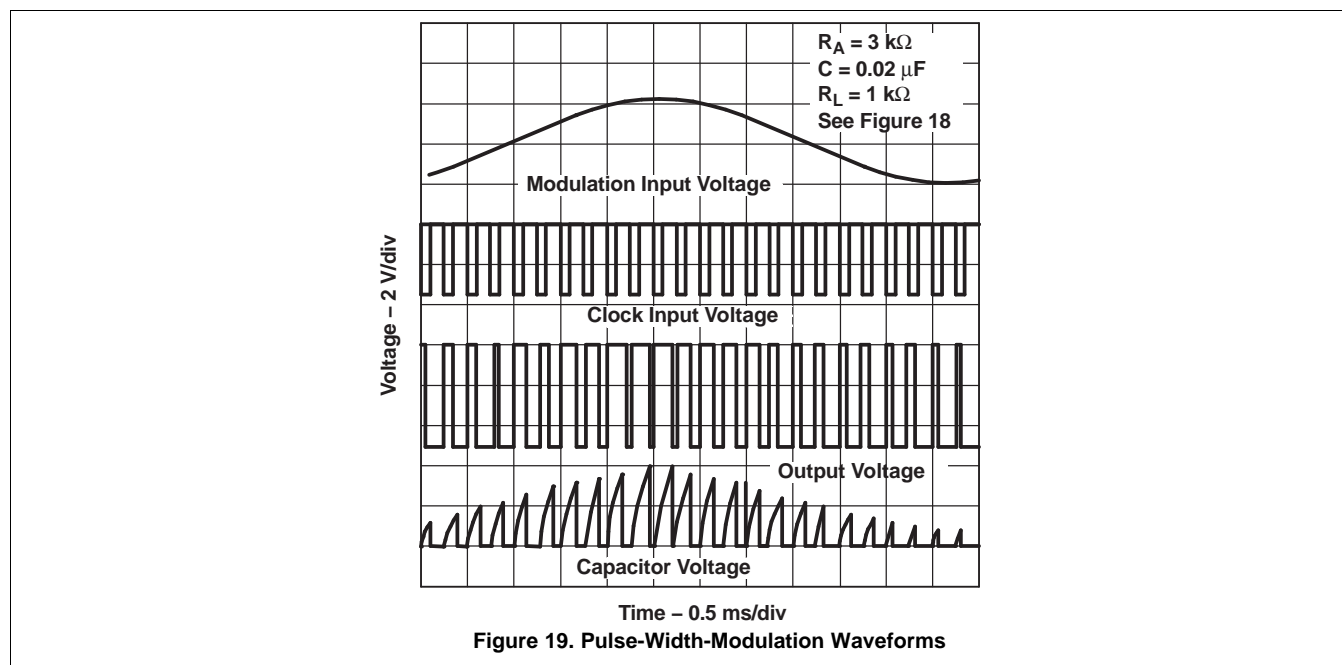
9.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than $1/3 V_{CC}$. Modulation input can vary from ground to V_{CC} . The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based RC on an negative exponential curve.

9.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH} , but it is not required for TTL compatibility.

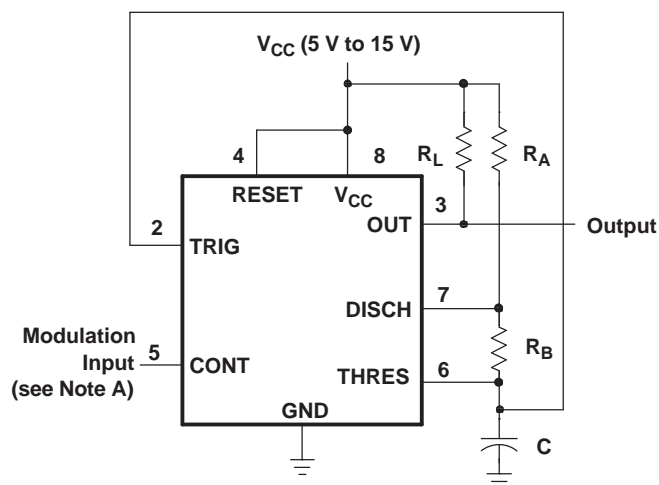
9.2.2.3 Application Curves



9.2.3 Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

Typical Applications (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

9.2.3.1 Design Requirements

Both DC and AC coupled modulation input will change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle will vary with the modulation voltage.

9.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in A-stable Operation section. R_L improves V_{OH} , but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.3.3 Application Curves

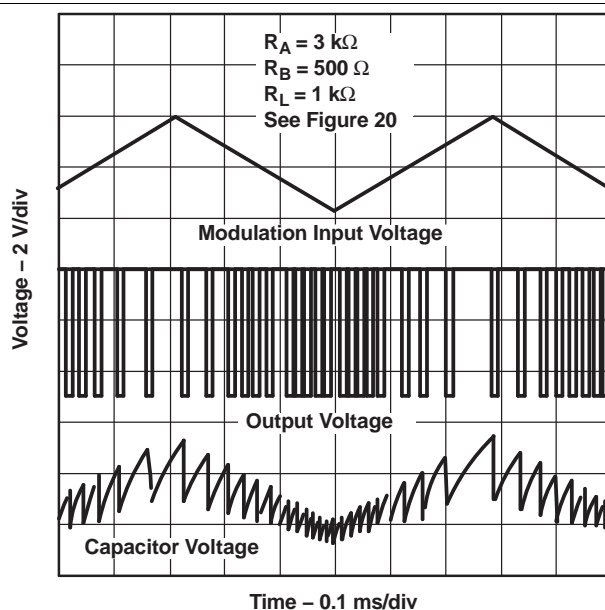


Figure 21. Pulse-Position-Modulation Waveforms

9.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

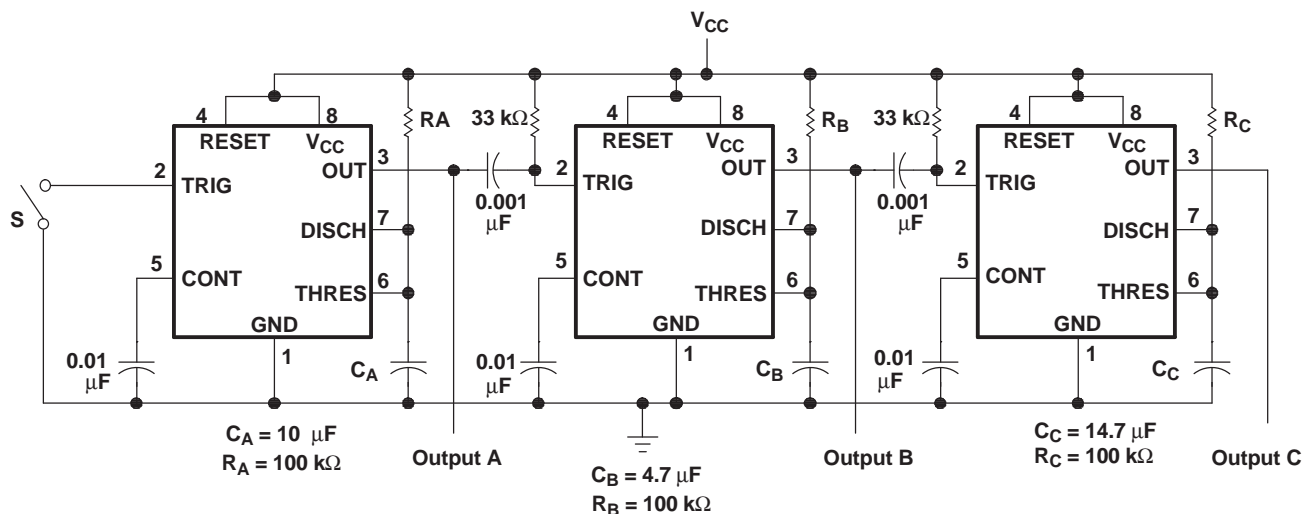


Figure 22. Sequential Timer Circuit

Typical Applications (continued)

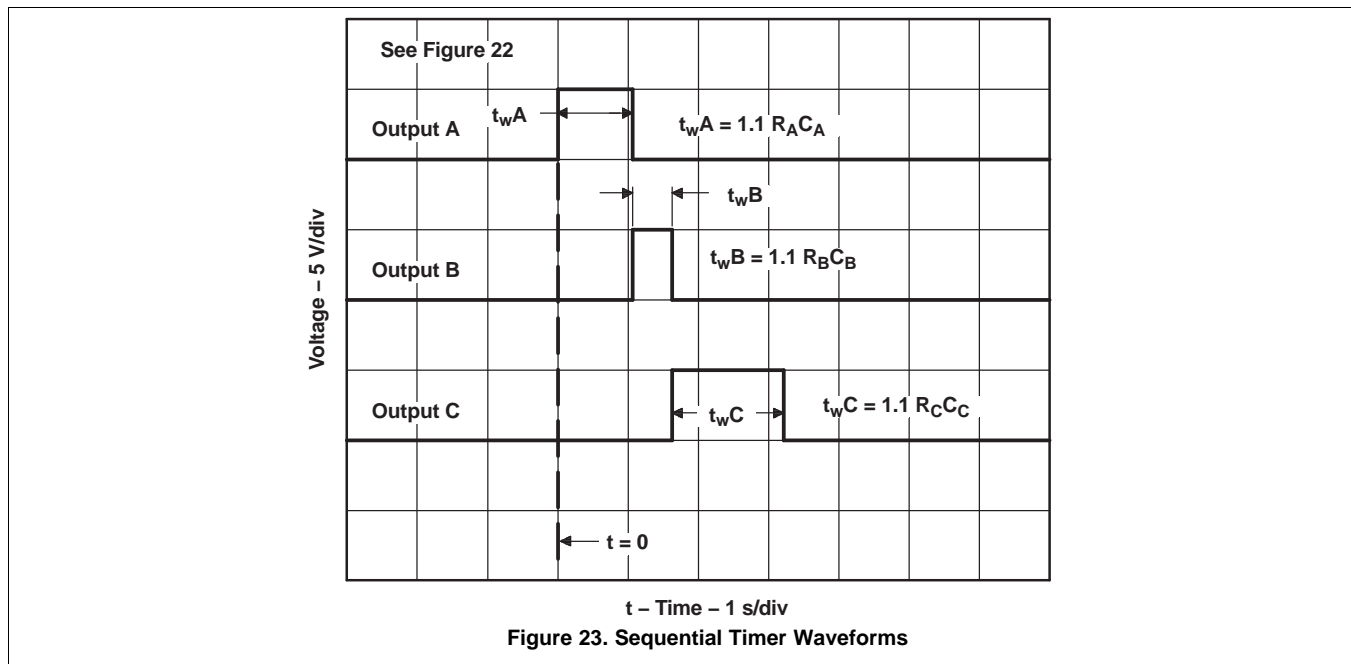
9.2.4.1 Design Requirements

The sequential timer application chains together multiple mono-stable timers. The joining components are the 33-kΩ resistors and 0.001-μF capacitors. The output high to low edge passes a 10-μs start pulse to the next monostable.

9.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula. $t_w = 1.1 \times R \times C$.

9.2.4.3 Application Curves



10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 16 V. (18 V for SE555). A bypass capacitor is highly recommended from VCC to ground pin; ceramic 0.1 μF capacitor is sufficient.

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
NA555	Click here	Click here	Click here	Click here	Click here
NE555	Click here	Click here	Click here	Click here	Click here
SA555	Click here	Click here	Click here	Click here	Click here
SE555	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual $\div 2$ and $\div 5$ Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

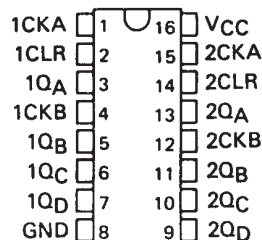
description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

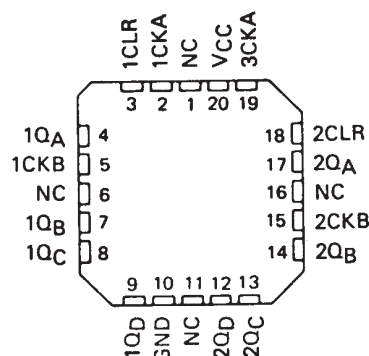
Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C .

SN54390, SN54LS390 . . . J OR W PACKAGE SN74390 . . . N PACKAGE SN74LS390 . . . D OR N PACKAGE

(TOP VIEW)

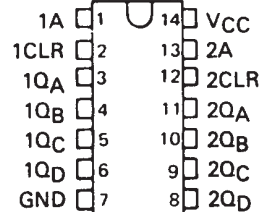


SN54LS390 . . . FK PACKAGE (TOP VIEW)

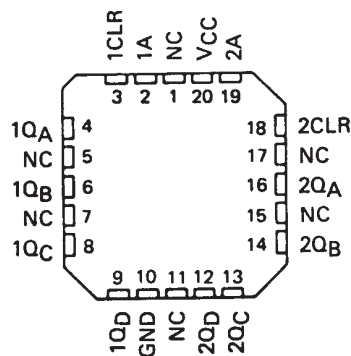


SN54393, SN54LS393 . . . J OR W PACKAGE SN74393 . . . N PACKAGE SN74LS393 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS393 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

FUNCTION TABLES
'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

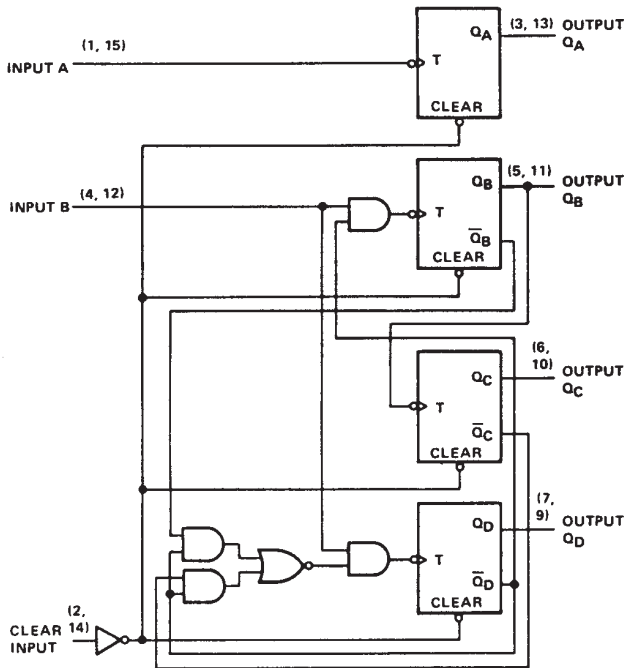
'393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

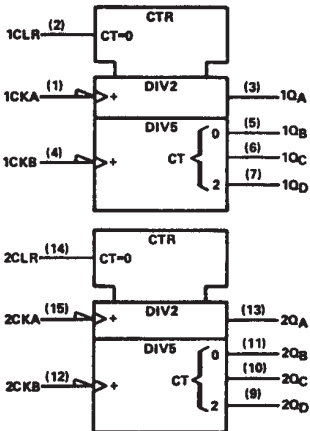
logic diagrams (positive logic)

'390, 'LS390

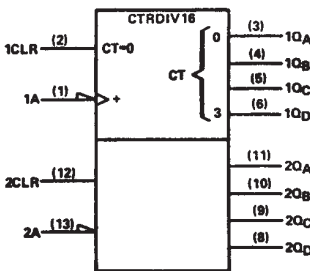


logic symbols†

'390, 'LS390



'393, 'LS393



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

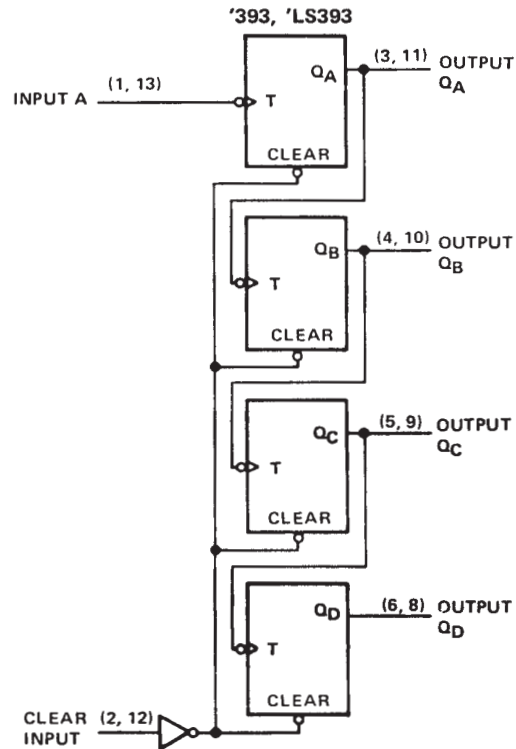
Pin numbers shown are for D, J, N, and W packages.



SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

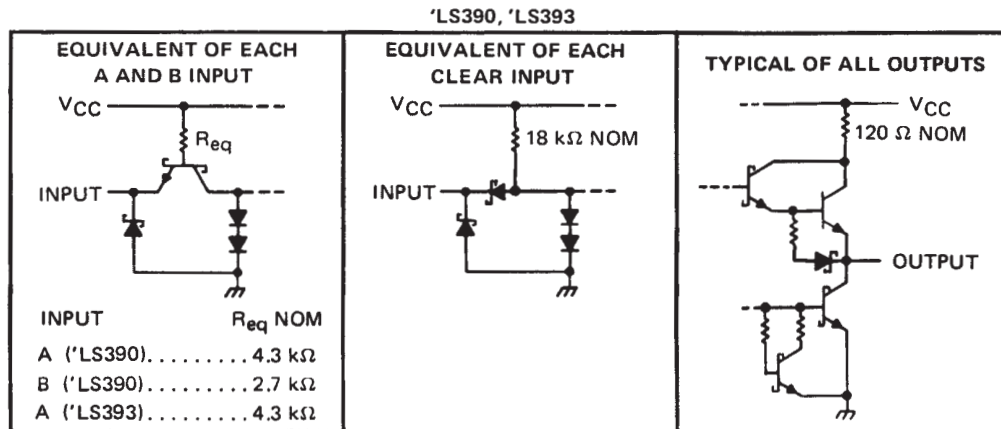
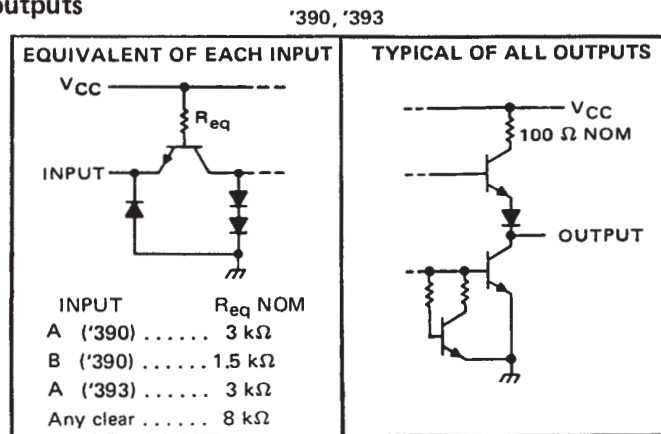
SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

logic diagrams (continued)



Pin numbers shown are for D, J, N and W packages.

schematics of inputs and outputs



SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	–55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54390 SN54393			SN74390 SN74393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–800			–800	μ A
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		20	0		20	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	25			25			
	Clear high	20			20			
Clear inactive-state setup time, t_{SU}		25↓			25↓			ns
Operating free-air temperature, T_A		–55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'390			'393			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage			0.8			0.8			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = –12 mA		–1.5			–1.5			V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = –800 μA		2.4	3.4		2.4	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1			mA
I _{IH}	High-level input current	Clear	V _{CC} = MAX, V _I = 2.4 V	40			40			μA
		Input A		80			80			
		Input B		120						
I _{IL}	Low-level input current	Clear	V _{CC} = MAX, V _I = 0.4 V	–1			–1			mA
		Input A		–3.2			–3.2			
		Input B		–4.8						
I _{OS}	Short-circuit output current §	V _{CC} = MAX	SN54'	–20	–57	–20	–57	mA		
			SN74'	–18	–57	–18	–57			
I _{CC}	Supply current	V _{CC} = MAX, See Note 2		42	69	38	64	mA		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ The Q_A outputs of the '390 are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



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SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

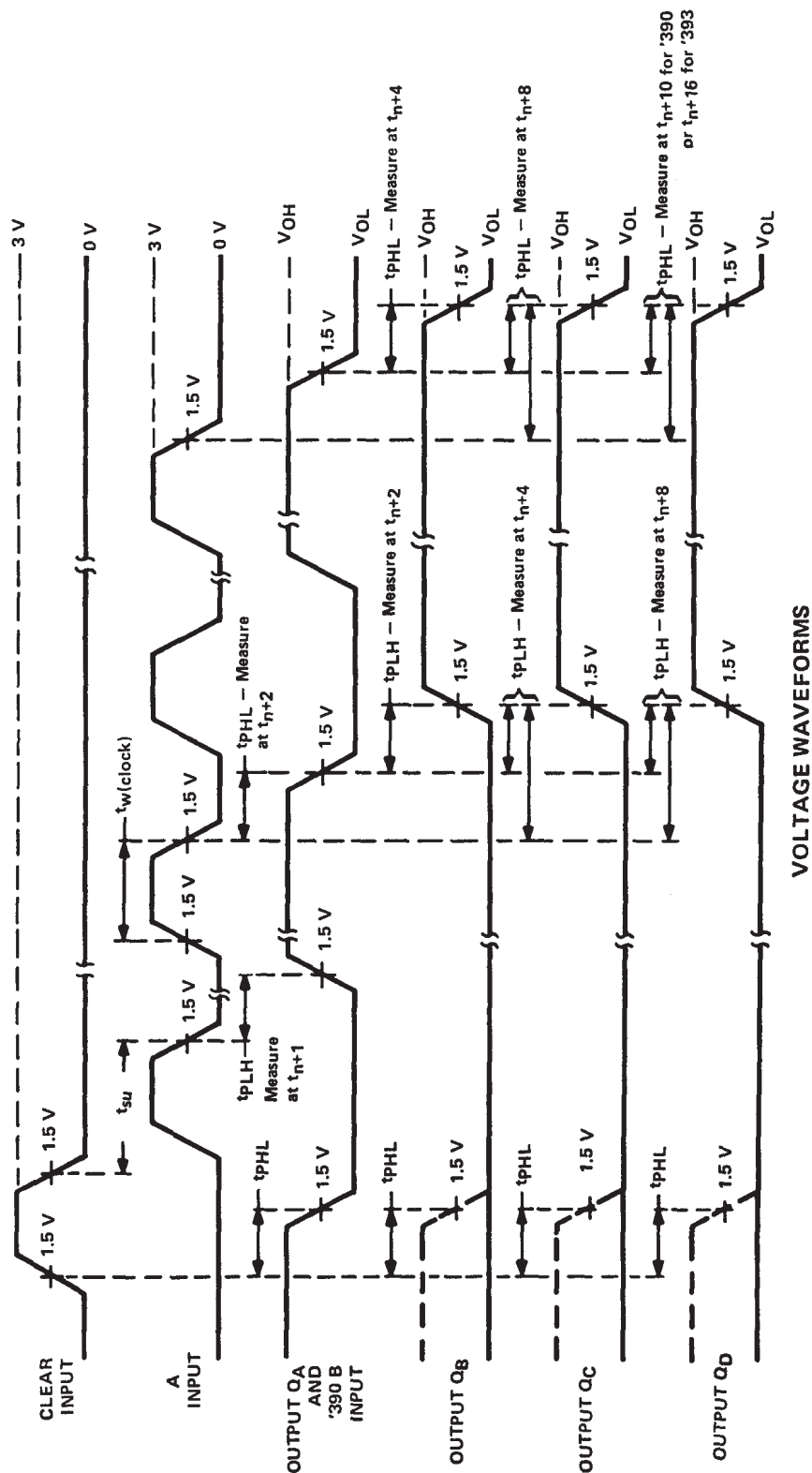
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 3 and Figure 1	25	35		25	35		MHz
	B	Q _B		20	30					
t _{PLH}	A	Q _A			12	20		12	20	ns
t _{PHL}					13	20		13	20	
t _{PLH}	A	Q _C of '390 Q _D of '393			37	60		40	60	ns
t _{PHL}					39	60		40	60	
t _{PLH}	B	Q _B			13	21				ns
t _{PHL}					14	21				
t _{PLH}	B	Q _C			24	39				ns
t _{PHL}					26	39				
t _{PLH}	B	Q _D			13	21				ns
t _{PHL}					14	21				
t _{PHL}	Clear	Any			24	39		24	39	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

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PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $PRR = 1 \text{ MHz}$, duty cycle = 50%, $Z_{out} \approx 50 \text{ ohms}$.

FIGURE 1

SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Clear input voltage	7 V
Any A or B clock input voltage	5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393	–55°C to 125°C
SN74LS390, SN74LS393	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		–400			–400			μ A
Low-level output current, I_{OL}		4			8			mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		12.5	0		12.5	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	40			40			
	Clear high	20			20			
Clear inactive-state setup time, t_{su}		25↓			25↓			ns
Operating free-air temperature, T_A		–55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				–1.5			–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$	$I_{OL} = 4 \text{ mA}^\S$	0.25	0.4		0.25	0.4		V
			$I_{OL} = 8 \text{ mA}^\S$				0.35	0.5		
I_I	Input current at maximum input voltage	Clear Input A Input B $V_{CC} = \text{MAX}$	$V_I = 7 \text{ V}$			0.1			0.1	mA
			$V_I = 5.5 \text{ V}$			0.2			0.2	
						0.4			0.4	
I_{IH}	High-level input current	Clear Input A Input B $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				0.02			0.02	mA
						0.1			0.1	
						0.2			0.2	
I_{IL}	Low-level input current	Clear Input A Input B $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				–0.4			–0.4	mA
						–1.6			–1.6	
						–2.4			–2.4	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		–20		–100	–20		–100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS390	15		26	15		26	mA
			'LS393	15		26	15		26	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ The Q_A outputs of the 'LS390 are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

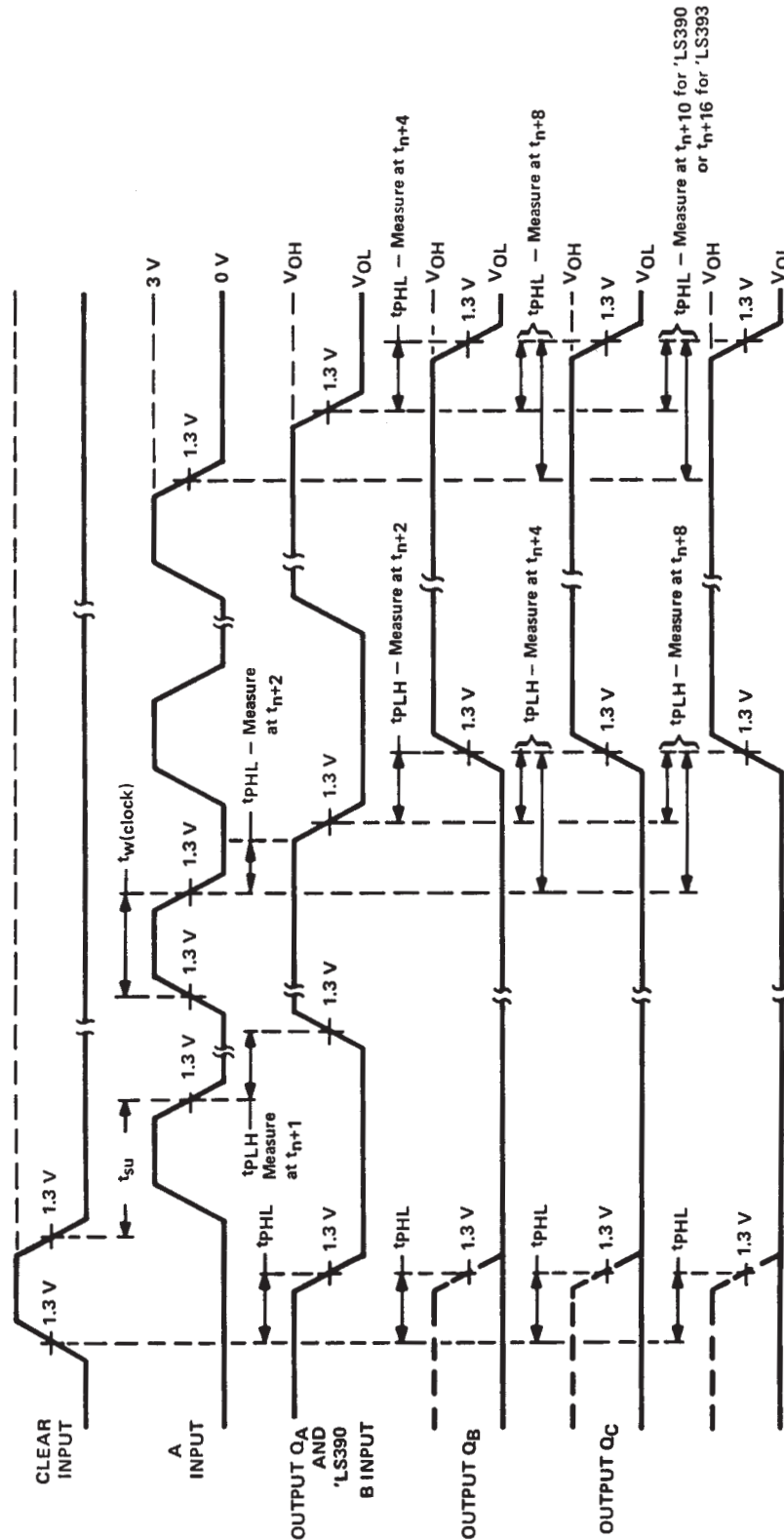
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 2 kΩ, See Note 4 and Figure 2	25	35		25	35		MHz
	B	Q _B		12.5	20					
t _{PLH}	A	Q _A			12	20		12	20	ns
t _{PHL}					13	20		13	20	
t _{PLH}	A	Q _C of 'LS390 Q _D of 'LS393			37	60		40	60	ns
t _{PHL}					39	60		40	60	
t _{PLH}	B	Q _B			13	21				ns
t _{PHL}					14	21				
t _{PLH}	B	Q _C			24	39				ns
t _{PHL}					26	39				
t _{PLH}	B	Q _D			13	21				ns
t _{PHL}					14	21				
t _{PHL}	Clear	Any			24	39		24	39	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE A: Input pulses are supplied by a generator having the following characteristics $t_f \leq 15$ ns, $t_r \leq 6$ ns, PRR = 1 MHz, duty cycle = 50 %, $Z_{out} \approx 50$ ohms.

FIGURE 2

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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'46A, '47A, 'LS47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

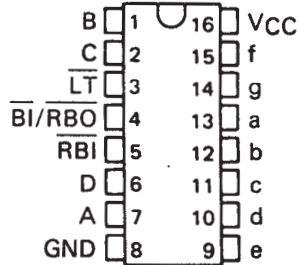
'48, 'LS48 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

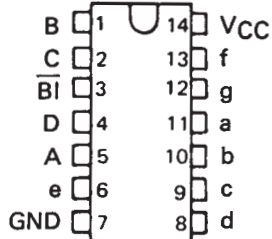
'LS49 feature

- Open-Collector Outputs
- Blanking Input

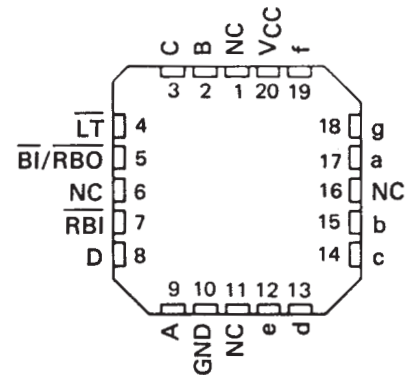
SN5446A, SN5447A, SN54LS47, SN5448,
SN54LS48 . . . J PACKAGE
SN7446A, SN7447A,
SN7448 . . . N PACKAGE
SN74LS47, SN74LS48 . . . D OR N PACKAGE
(TOP VIEW)



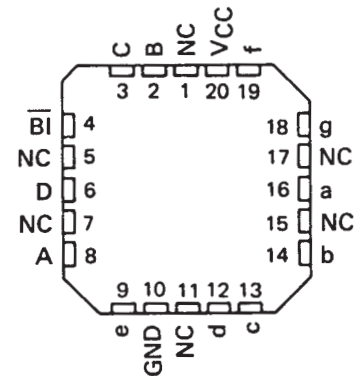
SN54LS49 . . . J OR W PACKAGE
SN74LS49 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS47, SN54LS48 . . . FK PACKAGE
(TOP VIEW)



SN54LS49 . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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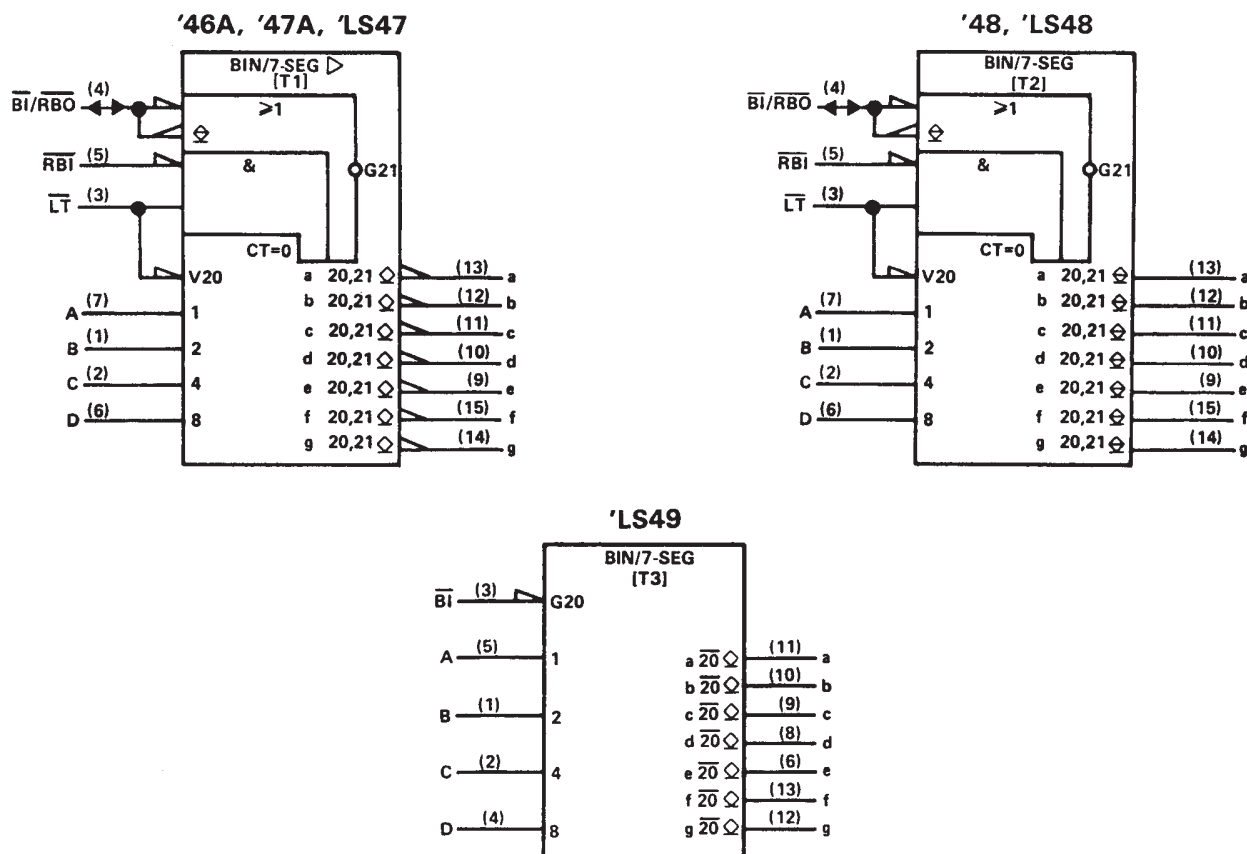
SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-k Ω pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-k Ω pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for D, J, N, and W packages.



SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

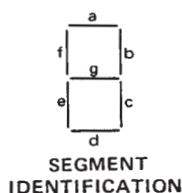
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description

The '46A, '47A, and 'LS47 feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. The '48, 'LS48, and 'LS49 feature active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits except 'LS49 have full ripple-blanking input/output controls and a lamp test input. The 'LS49 circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{\text{RBI}}$ and $\overline{\text{RBO}}$). Lamp test ($\overline{\text{LT}}$) of these types may be performed at any time when the $\overline{\text{BI/RBO}}$ node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ($\overline{\text{BI}}$), which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 and '247 and the SN54LS247/SN74LS247 and 'LS248 compose the  and the  with tails and were designed to offer the designer a choice between two indicator fonts.



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'LS47 FUNCTION TABLE (T1)

DECIMAL OR FUNCTION	INPUTS						$\overline{\text{BI/RBO}}^\dagger$	OUTPUTS							NOTE
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a low level (response condition).

4. When the blanking input/ripple blanking output ($\overline{\text{BI/RBO}}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

$^\dagger \overline{\text{BI/RBO}}$ is wire AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$).

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
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'48, 'LS48
 FUNCTION TABLE (T2)

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}^\dagger$	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	L	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	L	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	L	H	L	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	L	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (\overline{BI}) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (\overline{RBI}) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (\overline{BI}), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (\overline{RBI}) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (\overline{RBO}) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

$^\dagger \overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input (\overline{BI}) and/or ripple-blanking output (\overline{RBO}).

'LS49
 FUNCTION TABLE (T3)

DECIMAL OR FUNCTION	INPUTS						OUTPUTS							NOTE
	D	C	B	A	\overline{BI}		a	b	c	d	e	f	g	
0	L	L	L	L	H		H	H	H	H	H	H	L	1
1	L	L	L	H	H		L	H	H	L	L	L	L	
2	L	L	H	L	H		H	H	L	H	H	L	H	
3	L	L	H	H	H		H	H	H	H	L	L	H	
4	L	H	L	L	H		L	H	H	L	L	H	H	
5	L	H	L	H	H		H	L	H	H	L	H	H	
6	L	H	H	L	H		L	L	H	H	H	H	H	
7	L	H	H	H	H		H	H	H	L	L	L	L	
8	H	L	L	L	H		H	H	H	H	H	H	H	
9	H	L	L	H	H		H	H	H	L	L	H	H	
10	H	L	H	L	H		L	L	L	H	H	L	H	
11	H	L	H	H	H		L	L	H	H	L	L	H	
12	H	H	L	L	H		L	H	L	L	L	H	H	
13	H	H	L	H	H		H	L	L	L	H	L	H	
14	H	H	H	L	H		L	L	L	H	H	H	H	
15	H	H	H	H	H		L	L	L	L	L	L	L	
BI	X	X	X	X	L		L	L	L	L	L	L	L	2

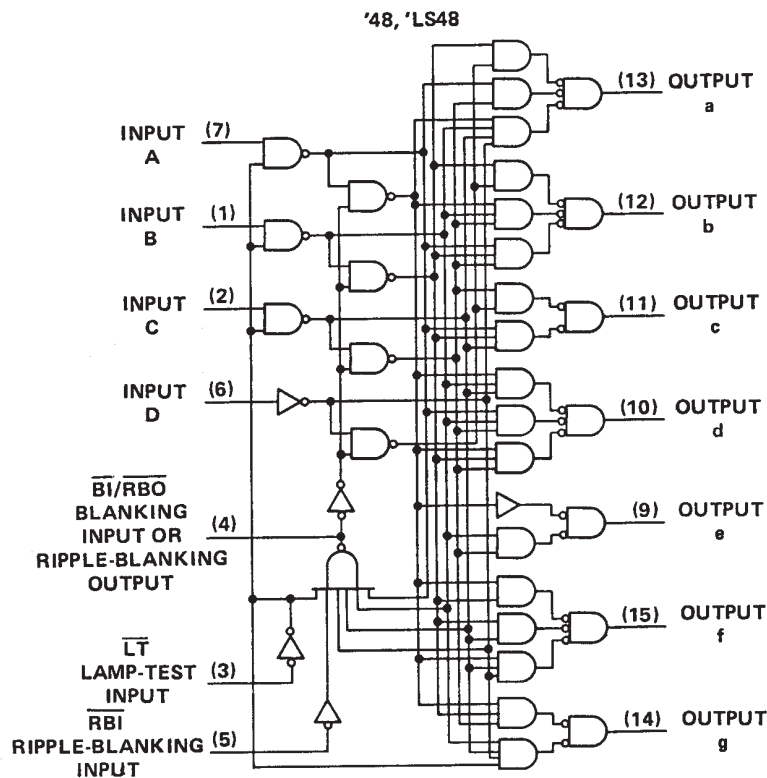
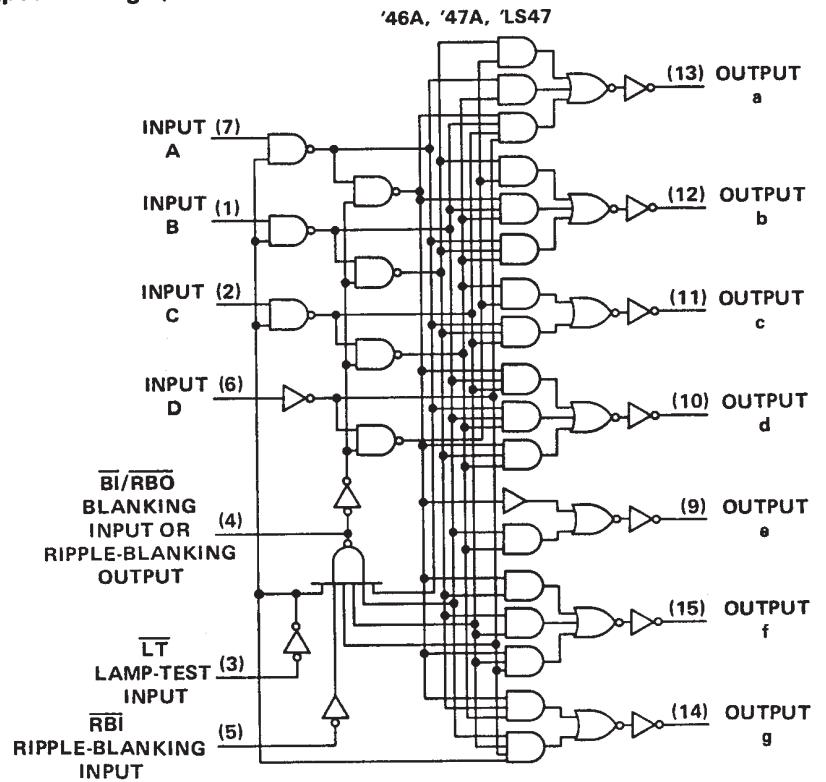
H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (\overline{BI}) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (\overline{BI}), all segment outputs are low regardless of the level of any other input.

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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logic diagrams (positive logic)

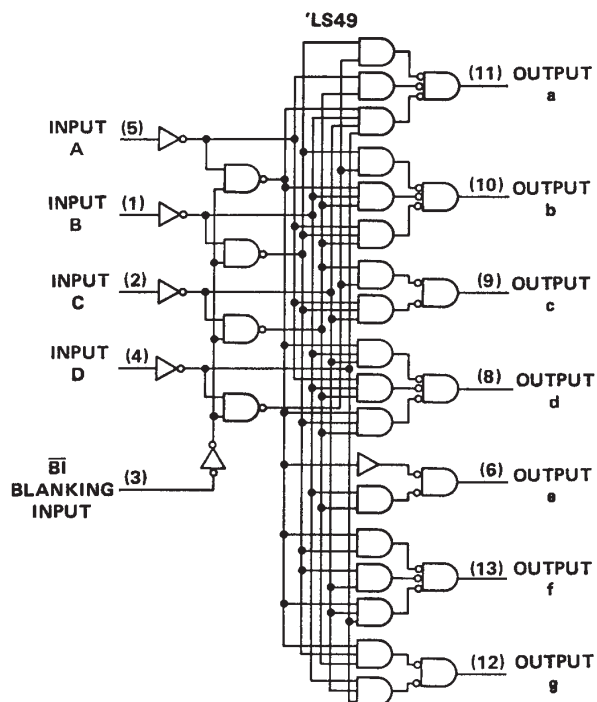


Pin numbers shown are for D, J, N, and W packages.

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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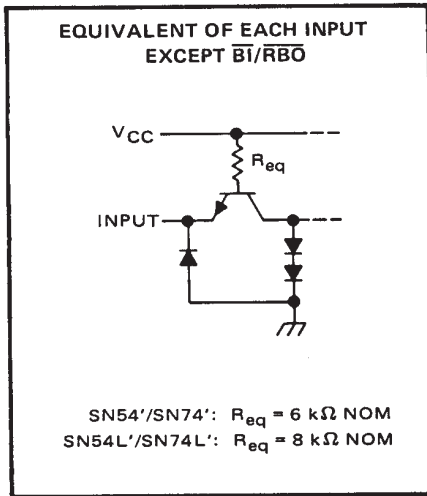
logic diagrams (continued)



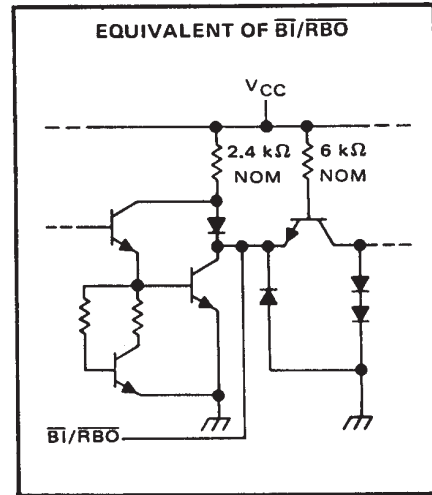
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

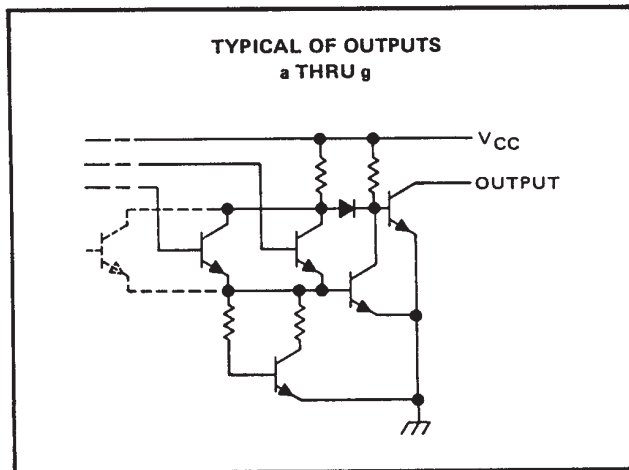
'46A, '47A, '48



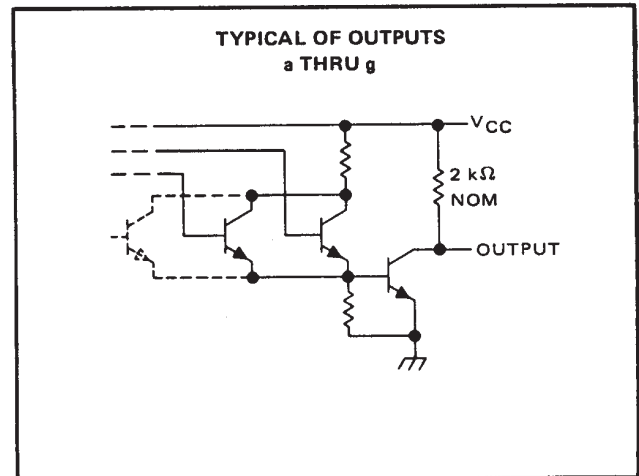
'46A, '47A, '48



'46A, '47A



'48



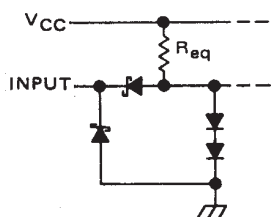
SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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schematics of inputs and outputs

'LS47, 'LS48, 'LS49

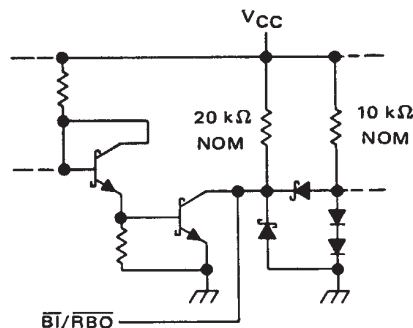
EQUIVALENT OF EACH INPUT
 EXCEPT $\overline{\text{BI}}/\overline{\text{RBO}}$



$\overline{\text{LT}}$ and $\overline{\text{RB}}\overline{\text{I}}$ ('LS47, 'LS48): $R_{eq} = 20 \text{ k}\Omega \text{ NOM}$
 $\overline{\text{BI}}$ ('LS49): $R_{eq} = 20 \text{ k}\Omega \text{ NOM}$
 A, B, C, and D: $R_{eq} = 25 \text{ k}\Omega \text{ NOM}$

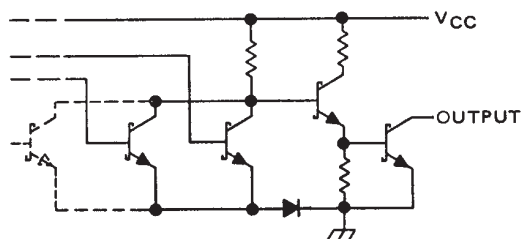
'LS47, 'LS48, 'LS49

EQUIVALENT OF $\overline{\text{BI}}/\overline{\text{RBO}}$



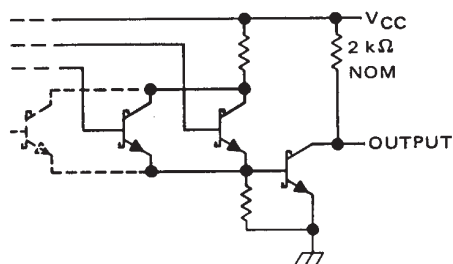
'LS47

TYPICAL OF OUTPUTS
 a THRU g



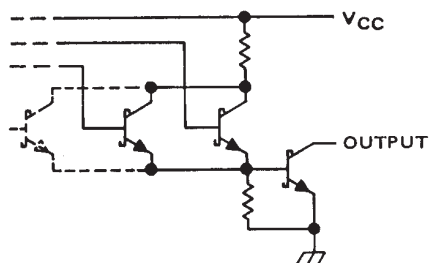
'LS48

TYPICAL OF OUTPUTS
 a THRU g



'LS49

TYPICAL OF OUTPUTS
 a THRU g



SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN5446A, SN5447A	–55°C to 125°C
SN7446A, SN7447A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	$\overline{BI}/\overline{RBO}$			–200			–200			–200			–200	μA
Low-level output current, I_{OL}	$\overline{BI}/\overline{RBO}$			8			8			8			8	mA
Operating free-air temperature, T_A		–55		125	–55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = −12 mA				−1.5	V
V _{OH}	High-level output voltage	$\overline{BI}/\overline{RBO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = −200 μA		2.4	3.7		V
V _{OL}	Low-level output voltage	$\overline{BI}/\overline{RBO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 8 mA			0.27	0.4	V
I _{O(off)}	Off-state output current	a thru g	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = 0.8 V, V _{O(off)} = MAX				250	μA
V _{O(on)}	On-state output voltage	a thru g	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{O(on)} = 40 mA			0.3	0.4	V
I _I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 5.5 V				1	mA
I _{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 2.4 V				40	μA
I _{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 0.4 V				−1.6	mA
		$\overline{BI}/\overline{RBO}$					−4	
I _{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$	V _{CC} = MAX				−4	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 2	SN54'		64	85	mA
				SN74'		64	103	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	$C_L = 15 \text{ pF}, R_L = 120 \Omega,$ See Note 3			100		ns
t_{on}	Turn-on time from A input				100		
t_{off}	Turn-off time from \overline{RBI} input				100		ns
t_{on}	Turn-on time from \overline{RBI} input				100		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5448	–55°C to 125°C
SN7448	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5448			SN7448			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			–400			–400	μ A
	$\overline{BI}/\overline{RBO}$			–200			–200	
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	$\overline{BI}/\overline{RBO}$			8			8	
Operating free-air temperature, T_A		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				–1.5	V
V_{OH}	High-level output voltage	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	4.2		V
		$\overline{BI}/\overline{RBO}$		2.4	3.7		
I_O	Output current	a thru g	$V_{CC} = \text{MIN}, V_O = 0.85 \text{ V},$ Input conditions as for V_{OH}	–1.3	–2		mA
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$		0.27	0.4	V
I_I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μ A
I_{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–1.6	mA
		$\overline{BI}/\overline{RBO}$				–4	
I_{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$	$V_{CC} = \text{MAX}$			–4	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN5448		53	76	mA
			SN7448		53	90	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$ See Note 3			100	ns
t_{PLH} Propagation delay time, low-to-high-level output from A input				100	
t_{PHL} Propagation delay time, high-to-low-level output from \overline{RBI} input				100	ns
t_{PLH} Propagation delay time, low-to-high-level output from \overline{RBI} input				100	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS
SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_W \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS47	-55°C to 125°C
SN74LS47	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS47			SN74LS47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			15			15	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	$\overline{BI}/\overline{RBO}$			-50			-50	μA
Low-level output current, I_{OL}	$\overline{BI}/\overline{RBO}$			1.6			3.2	mA
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS47			SN74LS47			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -50 \mu\text{A}$	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$ $I_{OL} = 3.2 \text{ mA}$	0.25	0.4		0.25	0.4		V
$I_{O(off)}$	Off-state output current	a thru g $V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, V_{O(off)} = 15 \text{ V}$			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{O(on)} = 12 \text{ mA}$ $I_{O(on)} = 24 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$ $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}$	-0.3		-2	-0.3		-2	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	7		13	7		13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input			100	ns
t_{on}	Turn-on time from A input			100	
t_{off}	Turn-off time from \overline{RBI} input, outputs (a-f) only			100	ns
t_{on}	Turn-on time from \overline{RBI} input, outputs (a-f) only			100	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS48	–55°C to 125°C
SN74LS48	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS48			SN74LS48			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	a thru g	−100			−100			μA
	$\overline{BI}/\overline{RBO}$	−50			−50			
Low-level output current, I _{OL}	a thru g	2			6			mA
	$\overline{BI}/\overline{RBO}$	1.6			3.2			
Operating free-air temperature, T _A		−55			0			70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS48		SN74LS48		UNIT	
				MIN	TYP‡ MAX	MIN	TYP‡ MAX		
V _{IH}	High-level input voltage			2		2		V	
V _{IL}	Low-level input voltage			0.7		0.8		V	
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = −18 mA		−1.5		−1.5		V
V _{OH}	High-level output voltage	a thru g and $\overline{BI}/\overline{RBO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX		2.4	4.2	2.4	4.2	V
I _O	Output current	a thru g	V _{CC} = MIN, V _O = 0.85 V, Input conditions as for V _{OH}		−1.3	−2	−1.3	−2	mA
V _{OL}	Low-level output voltage	a thru g	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 2 mA	0.25	0.4	0.25	0.4	V
				I _{OL} = 6 mA			0.35	0.5	
	$\overline{BI}/\overline{RBO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 1.6 mA	0.25	0.4	0.25	0.4	V	
			I _{OL} = 3.2 mA			0.35	0.5		
I _I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
I _{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
I _{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 0.4 V		−0.4		−0.4		mA
		$\overline{BI}/\overline{RBO}$			−1.2		−1.2		
I _{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$	V _{CC} = MAX		−0.3	−2	−0.3	−2	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 2		25	38	25	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}$, $R_L = 4 \text{ k}\Omega$,		100		ns
t_{PLH} Propagation delay time, low-to-high-level output from A input	See Note 3		100		
t_{PHL} Propagation delay time, high-to-low-level output (a-f only) from \overline{RBI} input	$C_L = 15 \text{ pF}$, $R_L = 6 \text{ k}\Omega$,		100		ns
t_{PLH} Propagation delay time, low-to-high-level output (a-f only) from \overline{RBI} input	See Note 3		100		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS49	–55°C to 125°C
SN74LS49	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS49			SN74LS49			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS49			SN74LS49			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage					0.8			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA	−1.5			−1.5			V
I _{OH}	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _{OH} = 5.5 V	250			250			μA
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25	0.4	V
		I _{OL} = 8 mA				0.35	0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V	0.1			0.1			mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V	20			20			μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	−0.4			−0.4			mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	8	15		8	15		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}$, $R_L = 4 \text{ k}\Omega$,			100	ns
t_{PLH} Propagation delay time, low-to-high-level output from A input	See Note 3			100	
t_{PHL} Propagation delay time, high-to-low-level output (a-f only) from \overline{RBI} input	$C_L = 15 \text{ pF}$, $R_L = 6 \text{ k}\Omega$,			100	ns
t_{PLH} Propagation delay time, low-to-high-level output (a-f only) from \overline{RBI} input	See Note 3			100	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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TO-92 MELODY
TRANSISTOR TYPE

電晶體包裝音樂 IC

MELODY

M66T.



FEATURES 功能敘述

Operating mode :

Continuous mode : Normal.

OSH mode : Optional.

P/N	SONG LIST
M66T.-32	CUCKOO WALTZ
M66T.-19	FOR ALICE
M66T.-08	HAPPY BIRTHDAY
M66T.-05	SWEET HOME
M66T.-68	SMALL WORLD
M66T.-11	LOVE ME TENDER
M66T.-26	ROCK-A-BY BABY
M66T.-18	WEDDING MARCH
M66T.-01	XMAS 3 SONGS

APPLICATION 產品應用

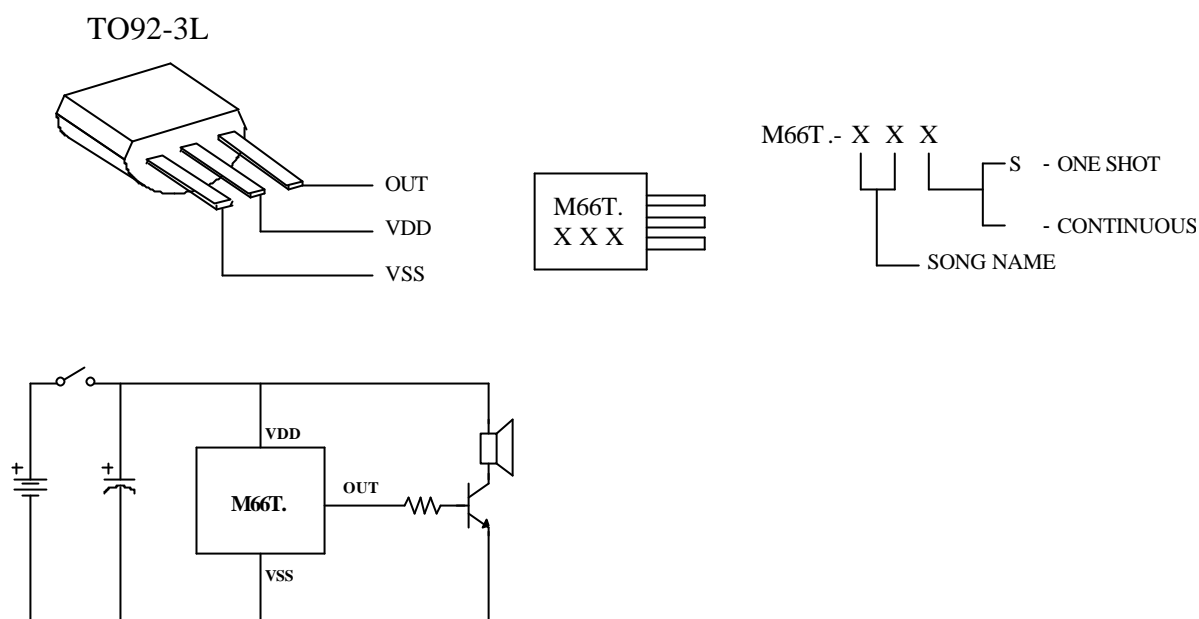
Telephone system, Musical instruments etc..

ELECTRICAL CHARACTERISTICS 電氣規格

(@ $V_{DD}=3V$ unless otherwise specified)

Characteristics	Sym.	Min.	Typ.	Max.	Unit	REMARKS
工作電壓 Operating Voltage	V_{DD}		3	3.5	V	
工作電流 Operating Current	I_{OP}		0.1	0.5	mA	No load
推動電流 BZ Driving Current	I_O	1			mA	@ $V_{DS}=1V$
振盪頻率 Oscillator Frequency	F_{OSC}		100		KHz	$\pm 30\%$ TOL.
工作溫度 Operating Temperature	Temp.	0	25	60		

APPLICATION DIAGRAM 參考電路圖



*All specs and applications shown above subject to change without prior notice.

(以上電路及規格僅供參考,本公司得逕行修正)



TAIWAN OASIS LED DATA SHEET

PART NO. : TOL-30aUReDAa-U4M

DESCRIPTION

SOURCE MATERIAL ----- AlGaInP
COLOR ----- Ultra Red
LENS ----- Red Diffused

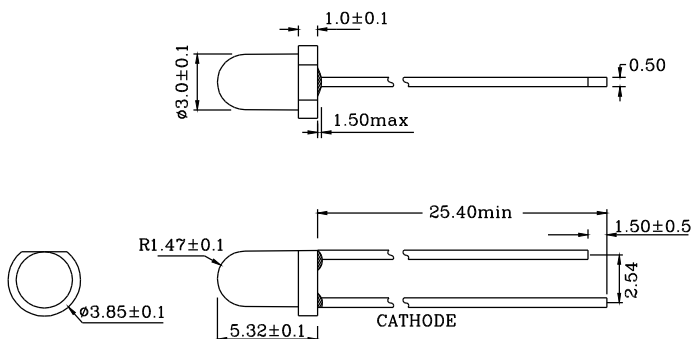
ABSOLUTE MAXIMUM RATING (Ta=25°C)

PULSE CURRENT (1/10 DUTY, CYCLE 0.1ms PULSE WIDTH) ----- 100mA
REVERSE VOLTAGE ----- 5.0V
CONTINUOUS FORWARD CURRENT ----- 25mA
RECOMMEND OPERATING CURRENT ----- 15mA
OPERATING TEMPERATURE ----- -25°C TO 85°C
STORAGE TEMPERATURE ----- -30°C TO 100°C
LEAD SOLDERING TEMPERATURE ----- 260°C FOR 3 SECONDS
(2mm from body)

CHARACTERISTICS (Ta=25°C)

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNITS
POWER DISSIPATION		Pd			90	mW
DOMINANT WAVELENGTH	If=20mA	λ_d		630		nm
SPECTRUM HALF WIDTH	If=20mA	$\Delta\lambda$		15		nm
FORWARD VOLTAGE	If=20mA	V _F		2.0	2.3	V
REVERSE CURRENT	V _R =5V	I _R			100	μA
LUMINOUS INTENSITY	If=20mA	I _v	75	150		mcd
FULL VIEWING ANGLE	If=20mA	2θ _{1/2}		50		deg.

INTERNAL CIRCUIT DIAGRAM



DATE	2002/3/20'	SCALE	2.5:1	TOLERANCE	±0.25 ANGLE ±5°	DRAWN	D Q H	CHECKED	
UNIT	M/M	SHEET NO.	1/1	DRAWING NO.	S-30aUReDAa-U4M-A	CUSTOMER		APPROVED	



TAIWAN OASIS LED DATA SHEET

PART NO. : TOL-30aUGbCAa-U4M

DESCRIPTION

SOURCE MATERIAL ----- AlGaInP
 COLOR ----- Super Green
 LENS ----- Water Clear

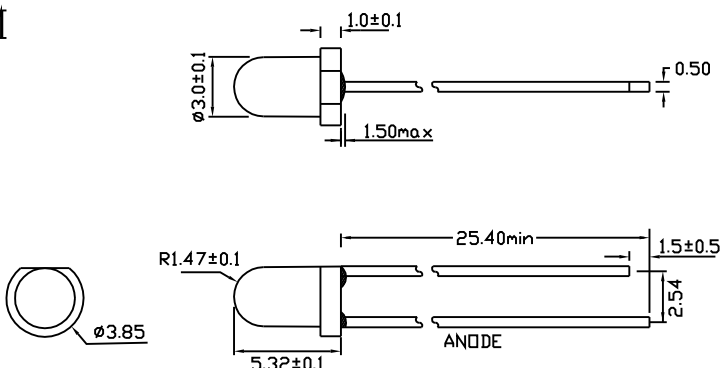
ABSOLUTE MAXIMUM RATING (Ta=25°C)

PULSE CURRENT (1/10 DUTY, CYCLE 0.1mS PULSE WIDTH) ----- 100mA
 REVERSE VOLTAGE ----- 5.0V
 CONTINUOUS FORWARD CURRENT ----- 25mA
 RECOMMEND OPERATING CURRENT ----- 15mA
 OPERATING TEMPERATURE ----- -25°C TO 85°C
 STORAGE TEMPERATURE ----- -30°C TO 100°C
 LEAD SOLDERING TEMPERATURE ----- 260°C FOR 3 SECONDS
 (2mm from body)

CHARACTERISTICS (Ta=25°C)

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNITS
POWER DISSIPATION		Pd			90	mW
DOMINANT WAVELENGTH	If=20mA	λ_d		574		nm
SPECTRUM HALF WIDTH	If=20mA	$\Delta\lambda$		15		nm
FORWARD VOLTAGE	If=20mA	V _F		2.0	2.3	V
REVERSE CURRENT	V _R =5V	I _R			100	μA
LUMINOUS INTENSITY	If=20mA	I _v	560	1000		mcd
FULL VIEWING ANGLE	If=20mA	2θ _{1/2}		18		deg.

PACKAGE DIMENSIONS & INTERNAL CIRCUIT DIAGRAM



DATE	2002/9/4'	SCALE	2.5:1	TOLERANCE	±0.25 ANGLE ±5°	DRAWN	Daisy	CHECKED	
UNIT	M/M	SHEET NO.	1/1	DRAWING NO.	S-30aUGbCAa-U4M-A	CUSTOMER		APPROVED	



TAIWAN OASIS LED DATA SHEET (FOR INFRARED)

PART NO. : TOIR-50b94bCEa

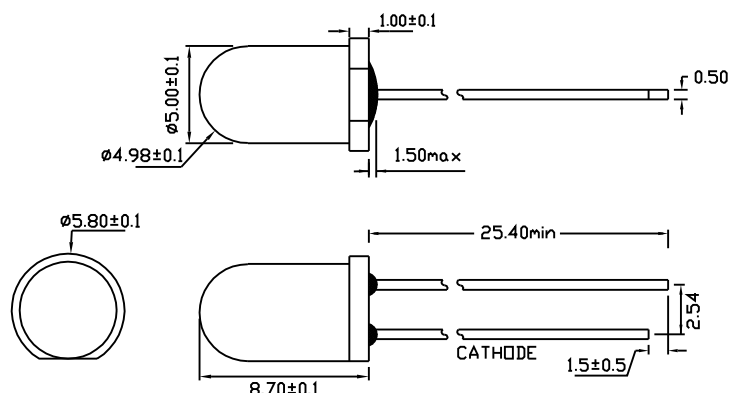
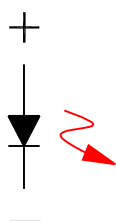
ABSOLUTE MAXIMUM RATINGS AT TA=25°C

PARAMETER	SYMBOL	DATA	UNIT
Forward Current	I_{FM}	100	mA
Peak Forward Current (duty=1:100, f=100KHZ)	I_{FP}	1000	mA
Reverse Voltage	V_R	6	V
Power Dissipation	P_D	150	mW
Operating Temperature Range		-25 to +85	°C
Storage Temperature Range		-30 to +85	°C
Lead Sold Temperature (1/10 Inch Below Seating Plane)		260°C for 3 sec.	

ELECTRICAL/OPTICAL CHARACTERISTICS AT TA=25°C

PARAMETER	SYMBOL	DATA	UNIT	TEST CONDITION
Radiated Output Power	$P_O(TYP.)$	12.0	mW	Distance: 10cm $I_F=50mA$ Detector Area: 1cm ²
Forward Voltage	V_F	TYP: 1.25 MAX: 1.45	V	$I_F=20mA$
Wavelength	λ_P	940	nm	$I_F=20mA$
Spectrum Width of Half Value	$\Delta\lambda$	50	nm	$I_F=20mA$
Reverse Current	I_R	10	μA	$V_R=5V$
Full Viewing Angle	$2 \times \frac{1}{2}\theta$	25	°	$I_F=20mA$
Lens		Water Clear		
Radiation Material		GaAs/GaAs		

PACKAGE DIMENSIONS & INTERNAL CIRCUIT DIAGRAM



DATE	01/10/01'	SCALE	2.5:1	TOLERANCE	±0.25 ANGLE ±5°	DRAWN	华明亮	CHECKED	
UNIT	M/M	SHEET NO.	1/2	DRAWING NO.	S-50b94bCEa-A	CUSTOMER		APPROVED	

Silicon PIN Photodiode
Silizium-PIN-Fotodiode
Version 1.1

SFH 213, SFH 213 FA



SFH 213



SFH 213 FA

Features:

- Wavelength range ($S_{10\%}$) 400 nm to 1100 nm (SFH 213) and 750 nm to 1100 nm (SFH 213 FA)
- Short switching time (typ. 5 ns)
- 5 mm LED plastic package

Applications

- High speed photointerrupters
- Industrial electronics
- For control and drive circuits

Besondere Merkmale:

- Wellenlängenbereich ($S_{10\%}$) 400nm bis 1100nm (SFH 213) und 750 nm bis 1100 nm (SFH 213 FA)
- Kurze Schaltzeit (typ. 5 ns)
- 5 mm-Plastikbauform im LED-Gehäuse

Anwendungen

- Schnelle Lichtschranken
- Industrieelektronik
- Messen / Steuern / Regeln

Ordering Information

Bestellinformation

Type: Typ:	Photocurrent Fotostrom $V_R = 5\text{ V}$, Std. Light A, $E_V = 1000\text{ lx}$ (SFH 213) $V_R = 5\text{ V}$, $\lambda = 870\text{ nm}$, $E_e = 1\text{ mW/cm}^2$ (SFH 213 FA) $I_P\text{ }[\mu\text{A}]$	Ordering Code Bestellnummer
SFH 213	135 (≥ 100)	Q62702P0930
SFH 213 FA	90 (≥ 65)	Q62702P1671

Maximum Ratings ($T_A = 25\text{ }^{\circ}\text{C}$)

Grenzwerte

Parameter Bezeichnung	Symbol Symbol	Values Werte		Unit Einheit
		SFH 213	SFH 213 FA	
Operating and storage temperature range Betriebs- und Lagertemperatur	$T_{op}; T_{stg}$	-40 ... 100		$^{\circ}\text{C}$
Reverse voltage Sperrspannung	V_R	20		V
Reverse voltage Sperrspannung ($t < 2\text{ min}$)	V_R	50		V
Total power dissipation Verlustleistung	P_{tot}	150		mW

Characteristics ($T_A = 25\text{ }^{\circ}\text{C}$)

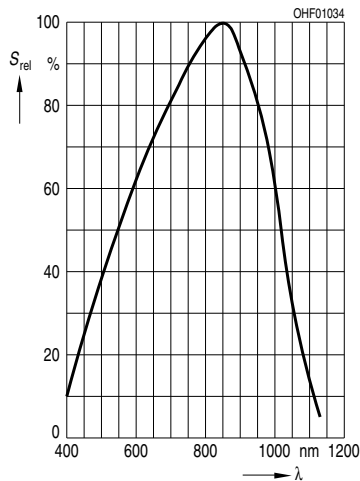
Kennwerte

Parameter Bezeichnung	Symbol Symbol	Values Werte		Unit Einheit
		SFH 213	SFH 213 FA	
Photocurrent Fotostrom ($E_v = 1000\text{ lx}$, Std. Light A, $V_R = 5\text{ V}$, $T = 2856\text{ K}$)	I_p	135 (≥ 100)		μA
Photocurrent Fotostrom ($V_R = 5\text{ V}$, $\lambda = 870\text{ nm}$, $E_e = 1\text{ mW/cm}^2$)	I_p		90 (≥ 65)	μA
Wavelength of max. sensitivity Wellenlänge der max. Fotoempfindlichkeit	$\lambda_{S\text{ max}}$	850	900	nm
Spectral range of sensitivity Spektraler Bereich der Fotoempfindlichkeit	$\lambda_{10\%}$	400 ... 1100	750 ... 1100	nm
Radiant sensitive area Bestrahlungsempfindliche Fläche	A	1.00		mm^2
Dimensions of radiant sensitive area Abmessung der bestrahlungsempfindlichen Fläche	L x W	1 x 1		mm x mm
Half angle Halbwinkel	ϕ	± 10		$^{\circ}$

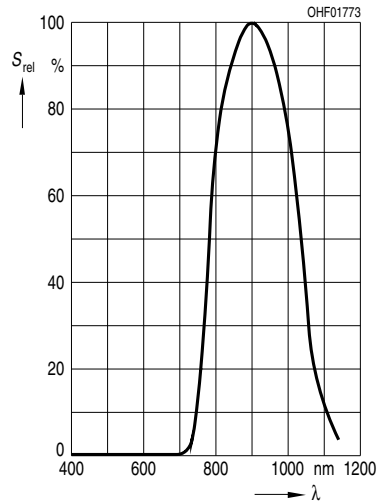
Parameter Bezeichnung	Symbol Symbol	Values Werte		Unit Einheit
		SFH 213	SFH 213 FA	
Dark current Dunkelstrom ($V_R = 20\text{ V}$)	I_R	1 (≤ 5)		nA
Spectral sensitivity of the chip Spektrale Fotoempfindlichkeit des Chips ($\lambda = 870\text{ nm}$)	$S_{\lambda\text{ typ}}$	0.65		A / W
Quantum yield of the chip Quantenausbeute des Chips ($\lambda = 870\text{ nm}$)	η	0.93		Electrons /Photon
Open-circuit voltage Leerlaufspannung ($E_v = 1000\text{ lx, Std. Light A}$)	V_O	430 (≥ 350)		mV
Open-circuit voltage Leerlaufspannung ($E_e = 0.5\text{ mW/cm}^2, \lambda = 870\text{ nm}$)	V_O		380 (≥ 300)	mV
Short-circuit current Kurzschlussstrom ($E_v = 1000\text{ lx, Std. Light A}$)	I_{SC}	125		μA
Short-circuit current Kurzschlussstrom ($E_e = 0.5\text{ mW/cm}^2, \lambda = 870\text{ nm}$)	I_{SC}		42	μA
Rise and fall time Anstiegs- und Abfallzeit ($V_R = 20\text{ V}, R_L = 50\text{ }\Omega, \lambda = 850\text{ nm}$)	t_r, t_f	0.005		μs
Forward voltage Durchlassspannung ($I_F = 100\text{ mA}, E = 0$)	V_F	1.3		V
Capacitance Kapazität ($V_R = 0\text{ V}, f = 1\text{ MHz}, E = 0$)	C_0	11		pF
Temperature coefficient of V_O Temperaturkoeffizient von V_O	TC_V	-2.6		mV / K
Temperature coefficient of I_{SC} Temperaturkoeffizient von I_{SC} (Std. Light A)	TC_I	0.18		% / K

Parameter Bezeichnung	Symbol Symbol	Values Werte		Unit Einheit
		SFH 213	SFH 213 FA	
Temperature coefficient of I_{SC} Temperaturkoeffizient von I_{SC} ($\lambda = 870\text{ nm}$)	TC_I		0.1	% / K
Noise equivalent power Rauschäquivalente Strahlungsleistung ($V_R = 20\text{ V}$, $\lambda = 870\text{ nm}$)	NEP	0.028		pW / $\text{Hz}^{1/2}$
Detection limit Nachweisgrenze ($V_R = 20\text{ V}$, $\lambda = 870\text{ nm}$)	D^*	3.6e12		$\text{cm} \times \text{Hz}^{1/2} / \text{W}$

Relative Spectral Sensitivity
Relative spektrale Empfindlichkeit
SFH 213 $S_{rel} = f(\lambda)$



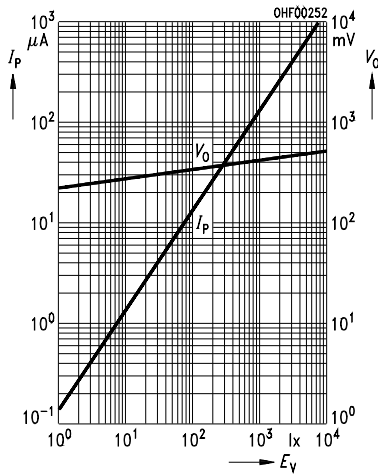
Relative Spectral Sensitivity
Relative spektrale Empfindlichkeit
SFH 213 FA $S_{rel} = f(\lambda)$



Photocurrent / Open-Circuit Voltage

Fotostrom / Leerlaufspannung

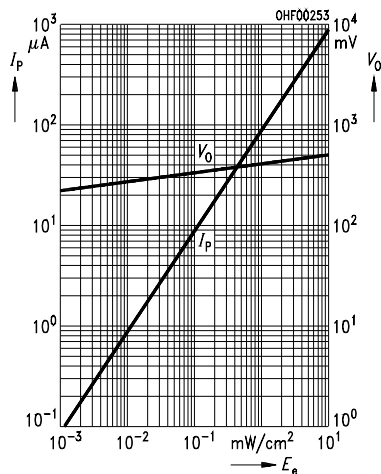
SFH 213 I_P ($V_R = 5 \text{ V}$) / $V_O = f(E_V)$



Photocurrent / Open-Circuit Voltage

Fotostrom / Leerlaufspannung

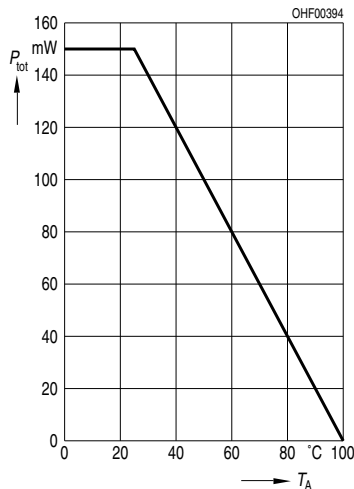
SFH 213 FA I_P ($V_R = 5 \text{ V}$) / $V_O = f(E_e)$



Total Power Dissipation

Verlustleistung

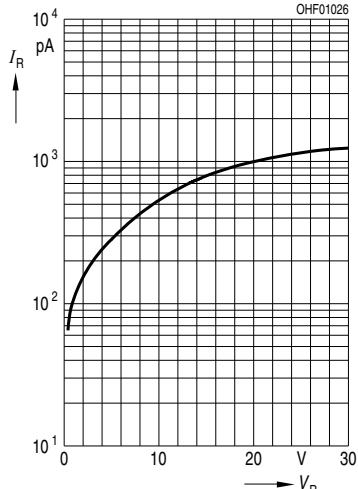
$P_{\text{tot}} = f(T_A)$



Dark Current

Dunkelstrom

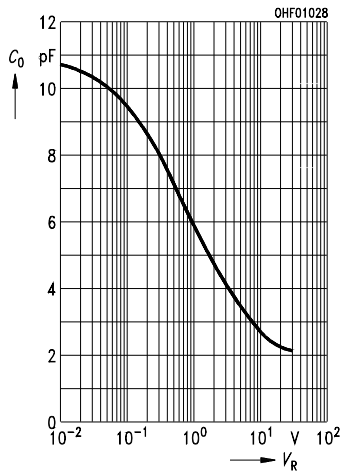
$I_R = f(V_R), E = 0$



Capacitance

Kapazität

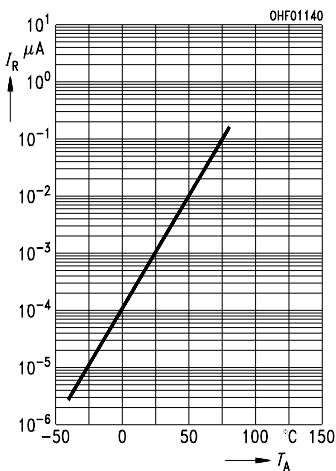
$C = f(V_R), f = 1 \text{ MHz}, E = 0$



Dark Current

Dunkelstrom

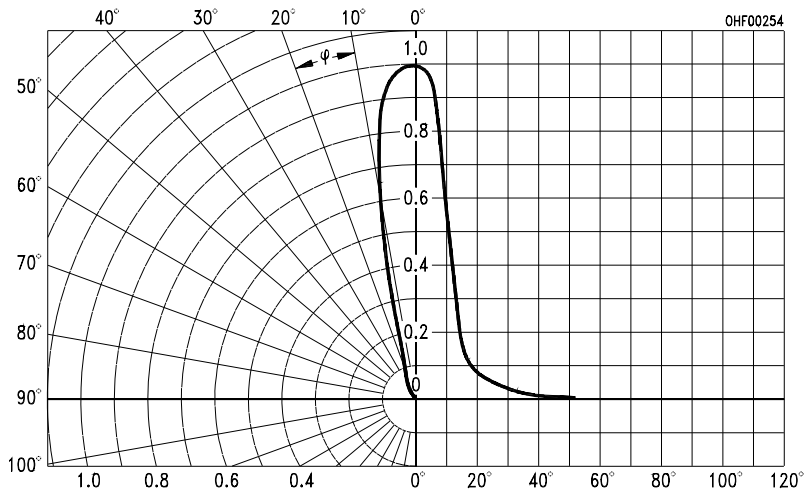
$I_R = f(T_A), V_R = 20 \text{ V}, E = 0$



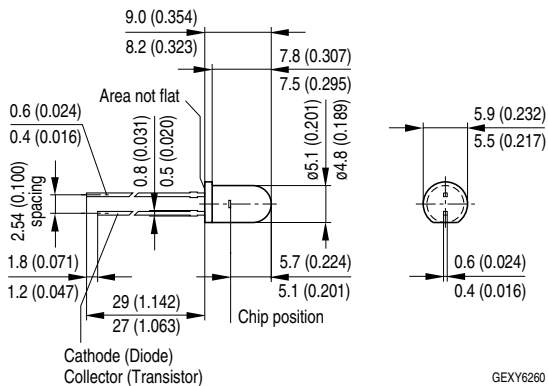
Directional Characteristics

Winkeldiagramm

$S_{\text{rel}} = f(\varphi)$



Package Outline Maßzeichnung



Dimensions in mm (inch). / Maße in mm (inch).

Package

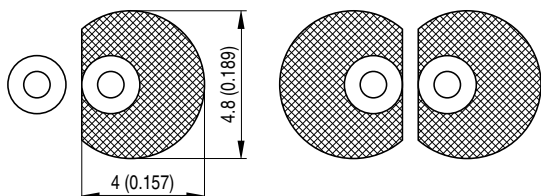
5mm Radial (T 1 ¾), Epoxy

Gehäuse

5mm Radial (T 1 ¾), Harz

Recommended Solder Pad**Empfohlenes Lötpaddesign**

TTW Soldering / Wellenlöten (TTW)



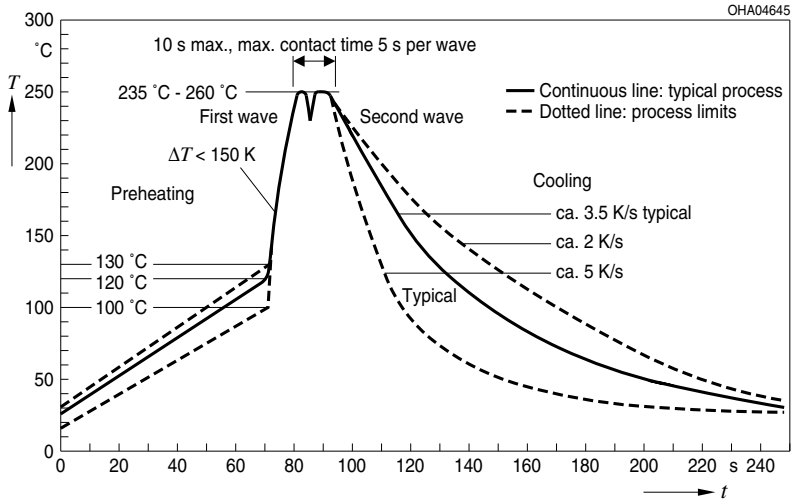
OHLPY985

Dimensions in mm (inch). / Maße in mm (inch).

TTW Soldering

Wellenlöten (TTW)

IEC-61760-1 TTW / IEC-61760-1 TTW



Disclaimer

Attention please!

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

Due to technical requirements components may contain dangerous substances.

For information on the types in question please contact our Sales Organization.

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Critical components* may only be used in life-support devices** or systems with the express written approval of OSRAM OS.

*) A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or the effectiveness of that device or system.

**) Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health and the life of the user may be endangered.

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EU RoHS and China RoHS compliant product



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按照中国的相关法规和标准，不含有毒有害物质或元素。



TAIWAN OASIS LED DATA SHEET

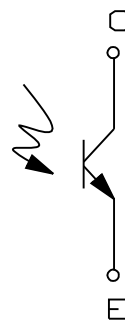
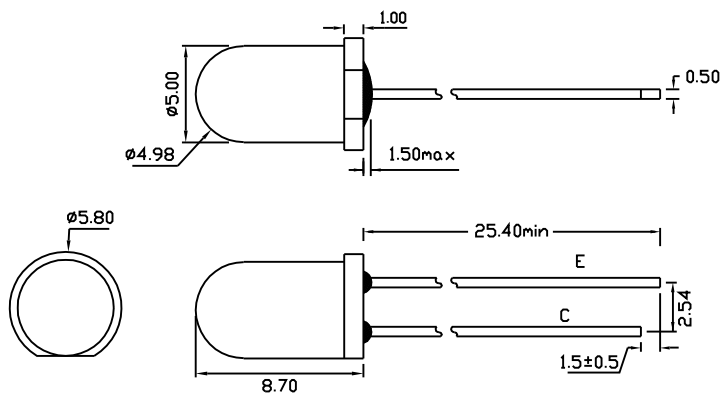
PART NO. : TOPS-050aTB₂

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Parameter	Symbol	Data	Unit	Test Condition
Collector-Emitter Breakdown Voltage	BV _{ceo}	30	v	I _c =100uA I _b =0
Emitter-Collector Breakdown Voltage	BV _{eco}	5	v	I _e =100uA I _b =0
Collector Dark Current	I _d	0.1	uA	V _{ce} =10v H=0mW/cm ²
Collector Light Current	I _L	4.0	mA	V _{ce} =10v 2856k 1000lx
Collect Power Dissipation	P _{cm}	140	mW	
Rise/Fall Time	Tr/Tf	5	uS	R=50 V _{ce} =10v I _c =1mA
Life Time	H	100'000	Hrs	V _{ce} =10v
Peak collection Wavelength	P	900	nm	
Spectral Range		750~1050	nm	
Operating Temperature Rang		-25 °C	to	70 °C
Storage Temperature Range		-30 °C	to	100° C
Lens Color		Black		

PACKAGE DIMENSIONS:

INTERNAL CIRCUIT DIAGRAM:



DATE	11/07/00'	SCALE	2.5:1	TOLERANCE	± 0.25 ANGLE $\pm 6^\circ$	DRAWN	华明亮	CHECKED	
UNIT	M/M	SHEET NO.	1/1	DRAWING NO.	S-050aTB ₂ -A	CUSTOMER		APPROVED	

Photo Conductive Cell, CdS, LDR

1-07-04-11

Model No. : KE-10715

General Description:

By using the sintering film fabrication method, the manufacturing process of the photo conductive layer can offer high sensitivity and easy fabrication of large sensitive areas, a large mass production effect, and relatively superior production profitability

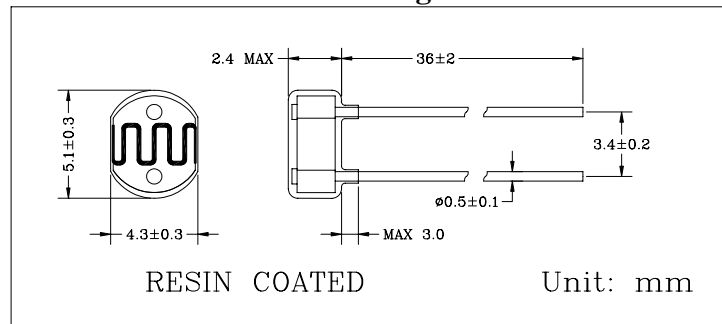
Features:

- Low Cost
- Exceptional temperature stability
- Fast response time
- Excellent chopping capability

Applications:

- ☐ Automatic dimmer
- ☐ Automatic flasher
- ☐ Optical relay

Outline Dimensional Drawing



Electrical Characteristics

(Ta=25°C)

Descriptions	Symbol	Min.	Typ.	Max.	Unit
Photo Resistance at 10 Lux (Light Source: 2856K)	R _L	10		15	kΩ
Dark Resistance After 10 sec. Removal of 10 Lux	R _D	0.5			MΩ
Gamma Value at 10 ~ 100 Lux	γ_{10}^{100}		0.7		
Maximum Power Dissipation	P _D			35	mW
Maximum Breakdown Voltage	V _{MAX}			100	V _{DC}
Peak Spectral Response	λ _p	550		650	nm
Rise Response Time at 1 fc	t _r		35		ms
Fall Response Time at 1 fc	t _f		5		ms
Ambient Temperature	T _A	-30 ~ +60			°C

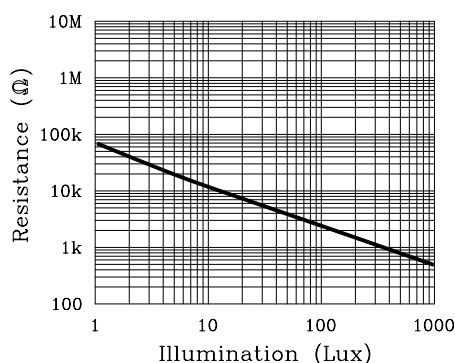
* Pre-measurement condition: Exposed in 500 Lux for more than 3 hours.

γ value: Standard gradient rate of resistance ranged by 10 ~ 100 Lux
(±0.1 unless otherwise stated)

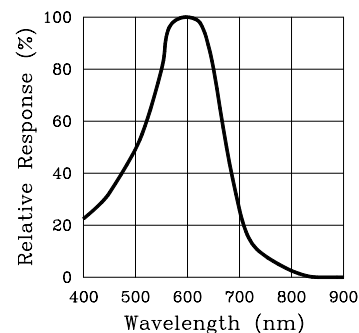
$$\gamma_a^b = \left| \frac{\text{Log}(R_b) - \text{Log}(R_a)}{\text{Log}(E_b) - \text{Log}(E_a)} \right|$$

Where: R_x : Photo resistance as lighting x
E_x : Illumination as lighting x

Resistance vs Illumination



Relative Spectral Response



POWER RELAY

2 POLES—5 A LOW PROFILE TYPE

FTR-F1 SERIES

■ FEATURES

- Low profile power relay (height 16.5 mm) employing unique construction
DPST/DPDT 5 A, TV-3 rating available
- Higher isolation by employing reinforced insulation construction
Insulation distance: 8 mm (between coil and contact)
Dielectric strength: 5 kV (between coil and contact)
Surge strength: 10 kV (between coil and contact)
- Plastic sealed relay
- Pin configuration compatible to VB/FBR620
- UL, CSA, VDE, SEMKO, BSI recognized
- Conforms to FIMKO, IMQ, DEMKO (under approval)
- Environmentally friendly cadmium free contact type is available



■ ORDERING INFORMATION

[Example] $\frac{\text{FTR-F1}}{\text{(a)}}$ $\frac{\text{A}}{\text{(b)}}$ $\frac{\text{A}}{\text{(c)}}$ $\frac{\text{005}}{\text{(d)}}$ $\frac{\text{V}}{\text{(e)}}$ $\frac{\text{— **}}{\text{(f)}}$

(a)	Series Name	FTR-F1 : FTR-F1 Series			
(b)	Contact Arrangement	A	: 2 form A (DPST-NO)		
		C	: 2 form C (DPDT)		
(c)	Coil Type	A	: Standard type (0.53 W)		
		D	: High sensitive type (0.4W)		
(d)	Nominal Voltage	005	: 5 VDC	012:	12 VDC
		006	: 6 VDC	024:	24 VDC
		009	: 9 VDC	048:	48 VDC
(e)	Contact Material/TV Type	V	: Gold plate silver alloy (standard type)		
		T	: Gold plate silver alloy (TV-3 rating type, only standard make type)		
(f)	Custom Designation	To be assigned custom specification			

Ordering Code: Actual Marking:
FTR-F1AA005V F1AA005V

FTR-F1 SERIES

■ SAFETY STANDARD AND FILE NUMBERS

UL508, 873 (File No. E63614)

C 22.2 No. 14 (File No. LR40304-30/ LR107822)

VDE 0435, 0631, 0700, 0860 (File No. 11039-4940-1019)

	Type	Nominal voltage	Contact rating
TV-Rating	FTR-F1AA()T	5 to 48 VDC	TV-3 120 VAC 1/6 HP 125 VAC 1/4 HP 250 VAC 5 A 24 VDC/250 VAC resistive Pilot duty R 300
Standard/ sensitive	FTR-F1CA(V)	5 to 48 VDC	Same as above without TV-3 2A 250VAC inductive (PF=0.4)

■ SPECIFICATIONS

Item			Standard Type		Sensitive Type		TV-3 Rating Type	
Contact	Arrangement		2 form A (DPST-NO), 2 form C (DPDT)				2 form A (DPST-NO)	
	Material		Gold plate silver alloy					
	Style		Single					
	Resistance (initial)		Maximum100 mΩ (at 1 A 6 VDC)					
	Rating (resistive)		5 A 250 VAC/24 VDC					
	Maximum Carrying Current		7 A					
	Maximum Switching Rating		1,250 VA/120 W					
	Maximum Switching Voltage		400 VAC 300 VDC					
	Maximum Switching Current		5 A					
	Minimum Switching Load*1		10 mA 5 VDC					
	Maximum Inrush Current		—				51 A 120 VAC (at lamp load)	
	Coil	Nominal Power (at 20°C)		0.53 W		0.4 W		0.53 W
Operate Power (at 20°C)		0.26 W		0.225W		0.26W		
Operating Temperature		−40°C to +75°C (no frost) (refer to the CHARACTERISTIC DATA)						
Time Value	Operate (at nominal voltage)		Maximum 15 ms					
	Release (at nominal voltage)		Maximum 5 ms					
Insulation	Resistance (at 500 VDC)		Minimum 1,000 MΩ					
	Dielectric Strength	between open contacts	1,000 VAC 1 minute (3,000 VAC between adjacent contacts)					
		between coil and contacts	5,000 VAC 1 minute					
	Surge Strength		10,000 V (at 1.2 × 50 μs)					
Life	Mechanical		2 × 10 ⁷ operations minimum					
	Electrical	Contact Rating	1 × 10 ⁵ operations minimum					
		Lamp Load	—				2.5 x 10 ⁴ ops. minimum	
Other	Vibration Resistance	Misoperation	10 to 55 Hz (double amplitude of 1.65 mm)					
		Endurance	10 to 55 Hz (double amplitude of 3.3 mm)					
	Shock Resistance	Misoperation	100 m/s ² (11 ±1 ms)					
		Endurance	1,000 m/s ² (6 ±1 ms)					
	Weight		Approximately 12 g					

*1 Minimum switching loads mentioned above are reference values. Please perform the confirmation test with the actual load before production since reference values may vary according to switching frequencies, environmental conditions and expected reliability levels.

FTR-F1 SERIES

■ COIL DATA CHART

MODEL		Nominal voltage	Coil resistance (±10%)	Must operate voltage	Must release voltage
Standard Type	TV-3 Rating Type				
FTR-F1 (C, A) A005 V	FTR-F1AA005 T	5 VDC	47 Ω	3.5 VDC	0.5 VDC
FTR-F1 (C, A) A006 V	FTR-F1AA006 T	6 VDC	68 Ω	4.2 VDC	0.6 VDC
FTR-F1 (C, A) A009 V	FTR-F1AA009 T	9 VDC	155 Ω	6.3 VDC	0.9 VDC
FTR-F1 (C, A) A012 V	FTR-F1AA012 T	12 VDC	270 Ω	8.4 VDC	1.2 VDC
FTR-F1 (C, A) A024 V	FTR-F1AA024 T	24 VDC	1,100 Ω	16.8 VDC	2.4 VDC
FTR-F1 (C, A) A048 V	FTR-F1AA048 T	48 VDC	4,400 Ω	33.6 VDC	4.8 VDC

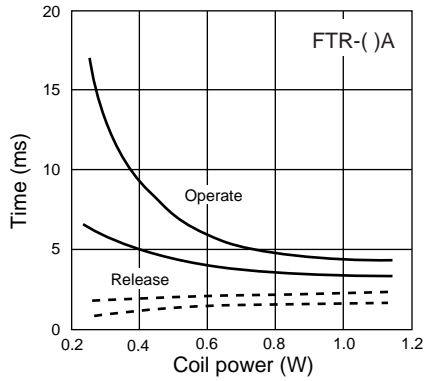
Note: All values in the table are measured at 20°C.

Sensitive Type

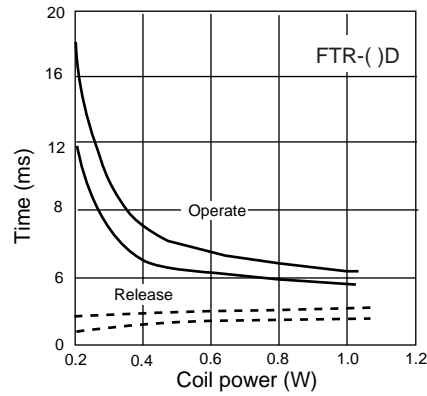
MODEL	Nominal voltage	Coil resistance (±10%)	Must operate voltage	Must release voltage
Standard Type				
FTR-F1 (C, A) D005 V	5 VDC	62 Ω	3.75 VDC	0.5 VDC
FTR-F1 (C, A) D006 V	6 VDC	90 Ω	4.5 VDC	0.6 VDC
FTR-F1 (C, A) D009 V	9 VDC	202 Ω	6.75 VDC	0.9 VDC
FTR-F1 (C, A) D012 V	12 VDC	360 Ω	9.0 VDC	1.2 VDC
FTR-F1 (C, A) D024 V	24 VDC	1,440 Ω	18.0 VDC	2.4 VDC
FTR-F1 (C, A) D048 V	48 VDC	5,760 Ω	36.0 VDC	4.8 VDC

CHARACTERISTIC DATA

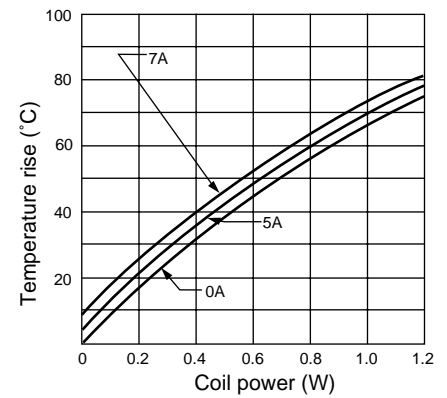
Timing



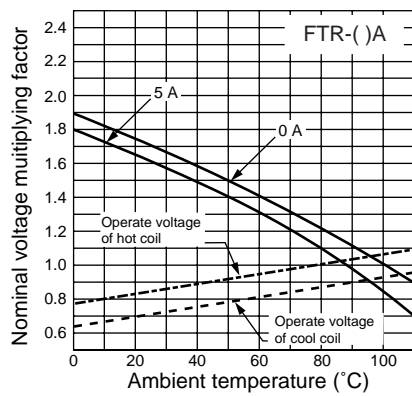
Timing



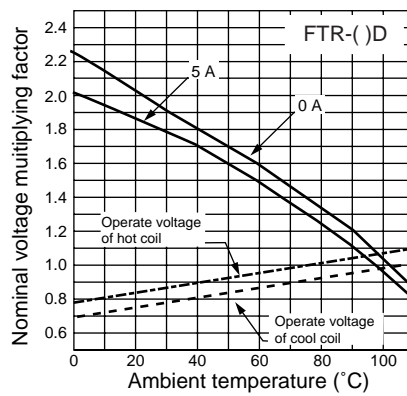
Coil temperature rise



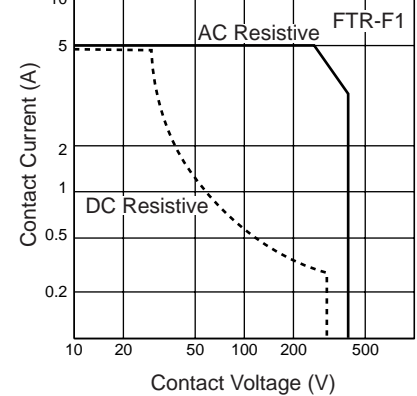
Operating range



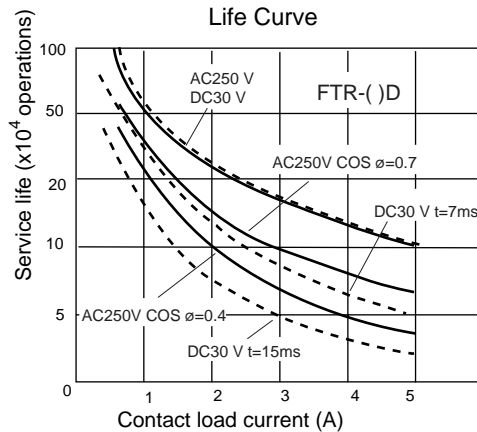
Operating range



Maximum Switching Power

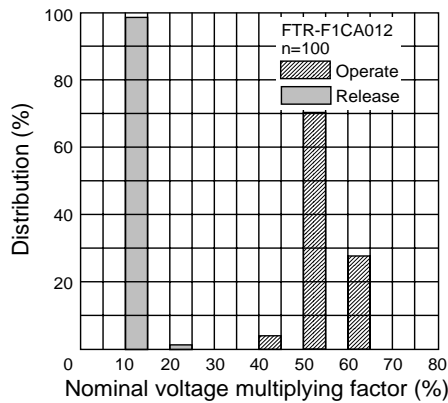


Life Curve

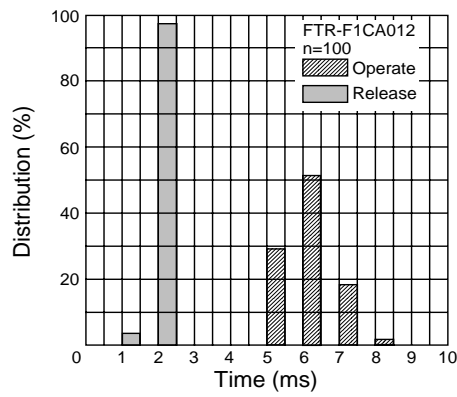


REFERENCE DATA

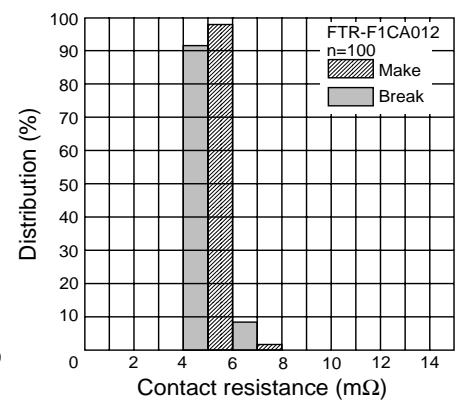
Distribution of operate and release voltage



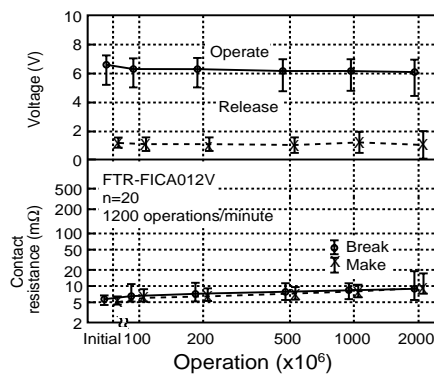
Distribution of operate and release time



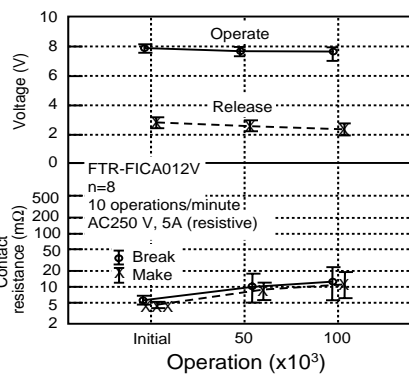
Distribution of contact resistance



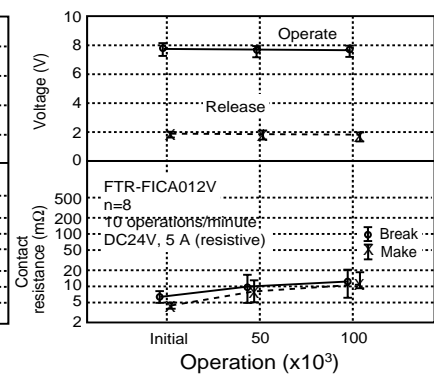
Mechanical life test



Electrical life test



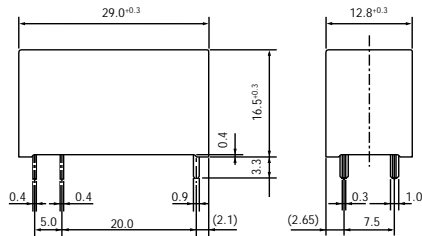
Electrical life test



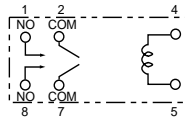
■ DIMENSIONS

● Dimensions

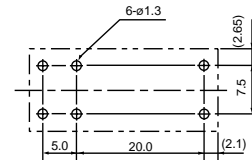
FTR-F1A type



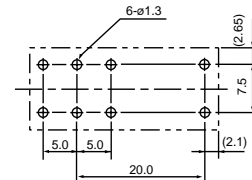
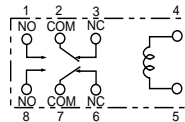
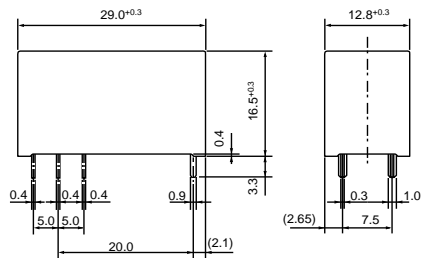
● Schematics (BOTTOM VIEW)



● PC board mounting hole layout (BOTTOM VIEW)



FTR-F1C type



Unit: mm

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Fax: (65) 273-3021

TOD-2281BG-4G

Dual Digit Display LED

Part Number	Chip		Face Color	Segment Color
	Material	Source Color		
TOD-2281BG-4G	GaP	Green	Gray	Green

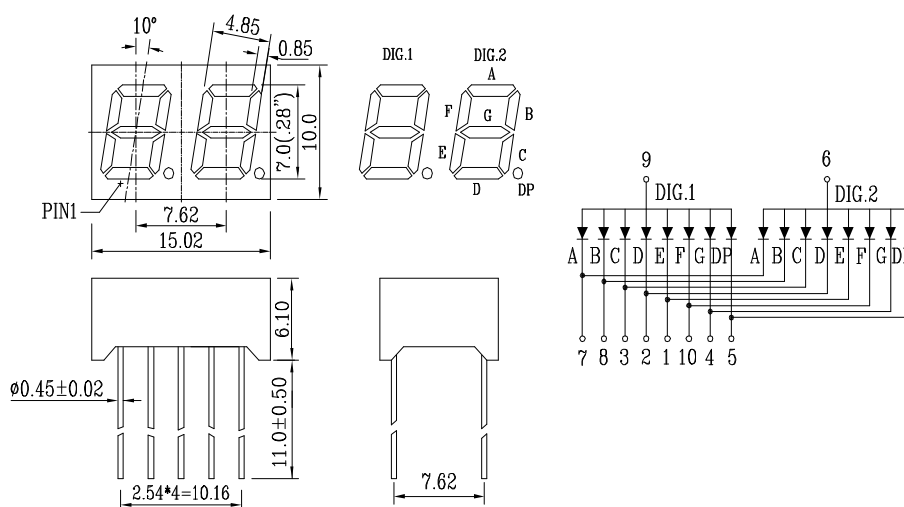
Features

- (0.28") 7.00mm digit height
- Common anode
- I.C. compatible
- Low power requirement
- RoHS compliant

Applications

- Audio equipment
- Instrument panels
- Digital read out display

Package Dimensions & Internal Circuit Diagram



Notes:

1. All dimensions are in millimeters, tolerance: ± 0.25 ; Angle: $\pm 0.1^\circ$ unless otherwise noted.
2. Specifications are subject to change without notice.

Absolute Maximum Rating @ Ta=25°C

Parameter	Maximum Rating	Unit
Peak Forward Current (1/10 Duty Cycle, 0.1ms Pulse Width) Per Dice	80	mA
Power Dissipation Per Dice	75	mW
Continuous Forward Current Per Dice	20	mA
Recommend Operating Current Per Dice	12	mA
Reverse Voltage Per Dice	5	V
Operating Temperature Range	-25°C to +85°C	
Storage Temperature Range	-30°C to +85°C	
Lead-Free Solder Temperature(1/16 Inch Below Seating Plane)	260°C for 3 Sec	

Electrical / Optical Characteristic @ Ta=25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Grade
Luminous Intensity Per Segment	I _v		4113		ucd	I _F =1mA	
Dominant Wavelength	λ _d		570		nm	I _F =20mA	
Spectral Line Half-Width	△λ		30		nm	I _F =20mA	
Forward Voltage Per Dice	V _F	1.9	2.2	2.5	V	I _F =20mA	
Reverse Current Per Dice	I _R			20	μA	V _R =5V	
Luminous Intensity Matching Rate	I _v -m			1.5:1		I _F =20mA	

The DISPLAYS should be kept at 30°C or less and 60%RH or less. The DISPLAYS should be used within one year.

	SPECIFICATIONS	MODEL NO. OBO-1206C-A2
	PART NAME Magnetic Transducer	SHEET 2 OF 4

MODEL NO : OBO-1206C-A2

Features : Conformity RoHS Directive (2002/95/EC) Requests.
Wave Solder and Wash Allowed

1.General Specifications :

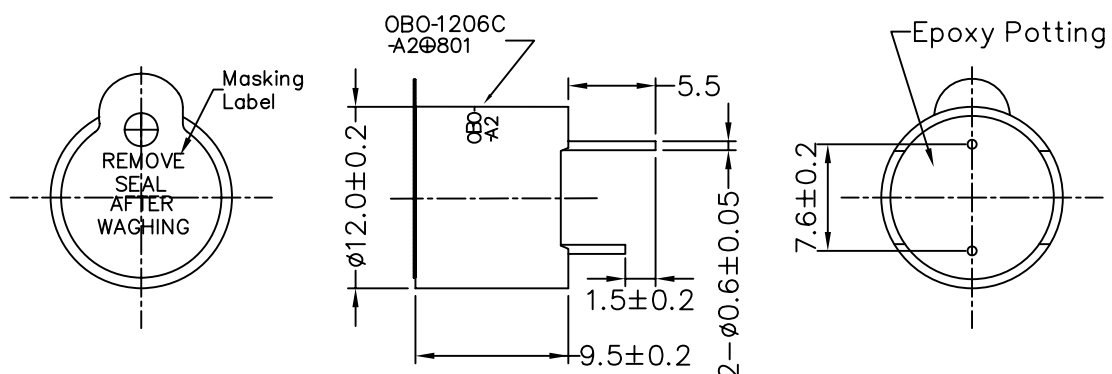
Items	Specification
※ Sound Pressure Level	85 dB min./10cm/DC 6.0V
Rated Voltage	DC 6.0V
※ Resonant Frequency	2300 ± 300 Hz
※ Rated Current	30 mA max./DC 6.0V
Operating Voltage	DC 3 to 8V
Housing Material	NORYL
Pin Material	Red Copper
Operating Temp. Range	-20°C to +70°C
Storage Temp Range	-30°C to +80°C
Weight	2.0 gms

2.Mechanical Layout and Dimensions :

※ Value applying rated voltage.(DC)

2.1 Shape & Dimensions

Unit: mm Tolerance: ±0.5



	SPECIFICATIONS	MODEL NO. OBO-1206C-A2
	PART NAME Magnetic Transducer	SHEET 3 OF 4

2.2 Meaning of Stamp Mark

801 : Production Period

8 : Year 2008 (last 1 figures of the year)

01 : Week (01~55)

3. Soldering Condition : *2

3.1 Wave Soldering

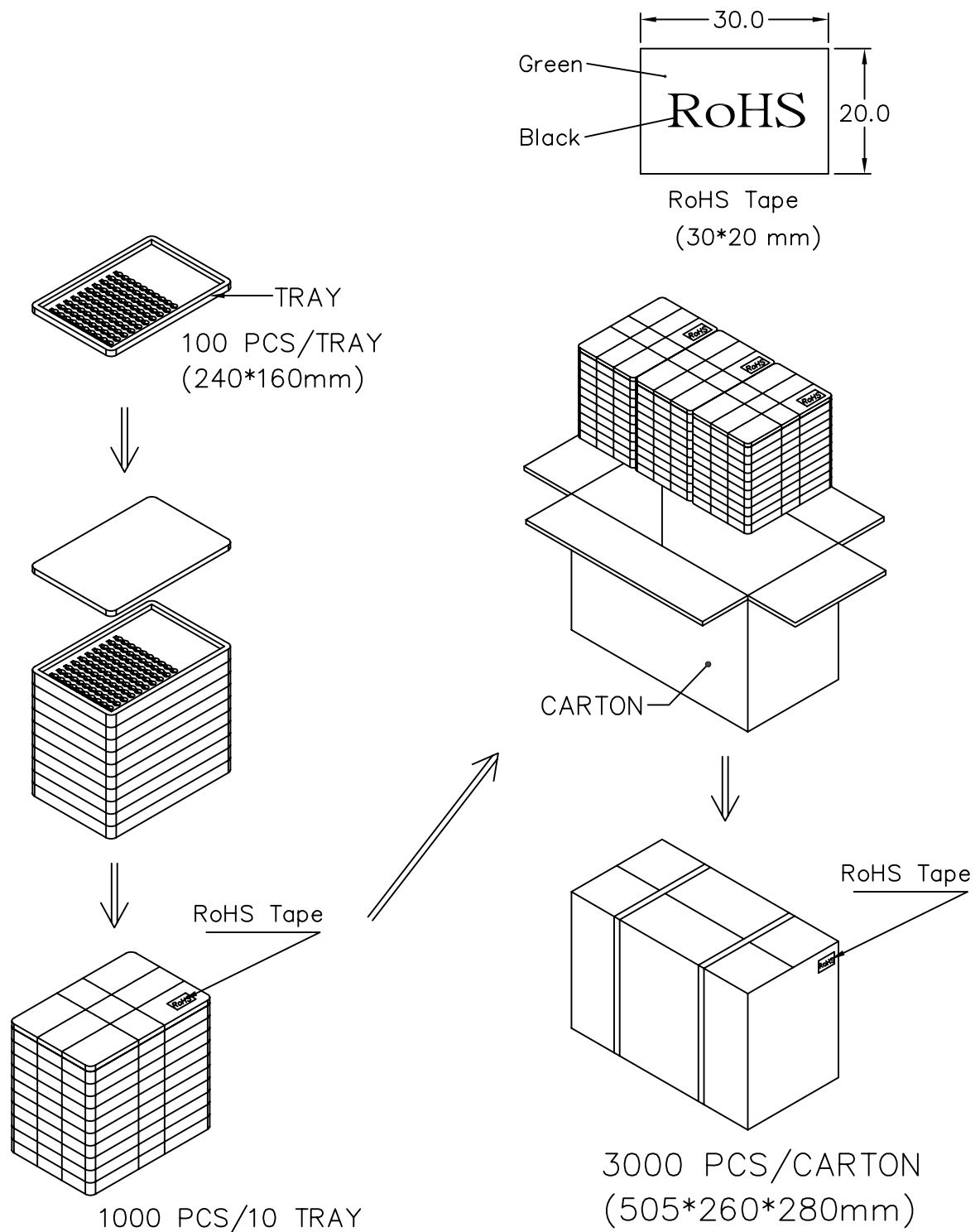
Peak temperature	Dipping time	Soldering
+ 260°C	5 seconds	1 time

3.2 Hand Soldering

Iron Tip Temperature	Soldering time
+ 380°C Max.	Duration 3 seconds Max.

	SPECIFICATIONS	MODEL NO. OBO-1206C-A2
	PART NAME Magnetic Transducer	SHEET 4 OF 4

4.Packing Information:



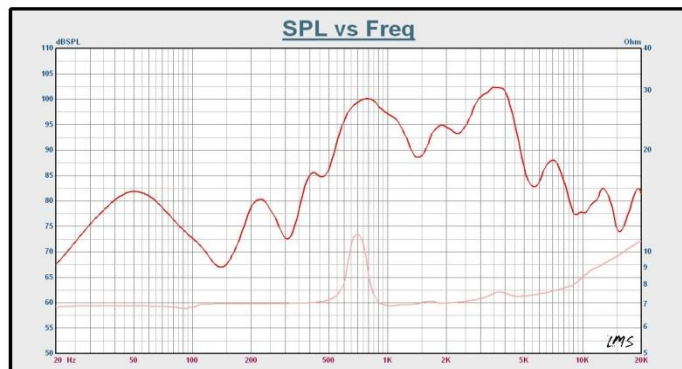
泉州强盛电子有限公司

QUANZHOU QIANGSHENG ELECTRONIC CO., LTD

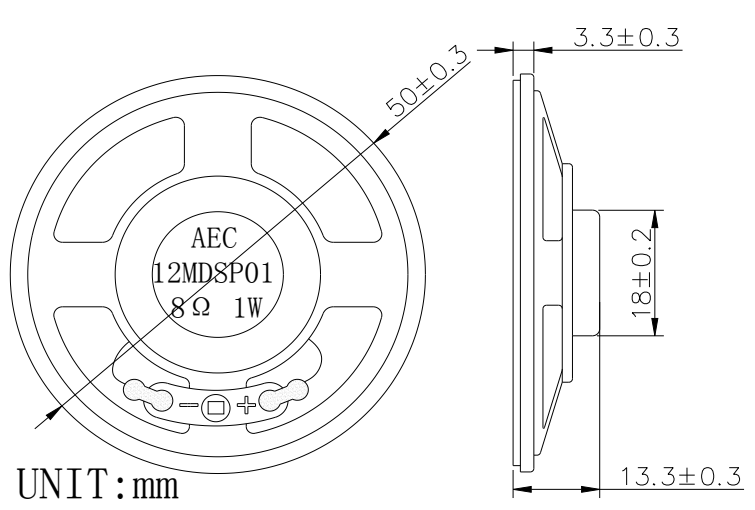
TEL:+86-0595-28290669 FAX:22356508 Email: fiona@aecspeaker.cn

Http://www.laba.co ADD:中国福建省泉州市浔美工业区海西电子信息产业育成基地

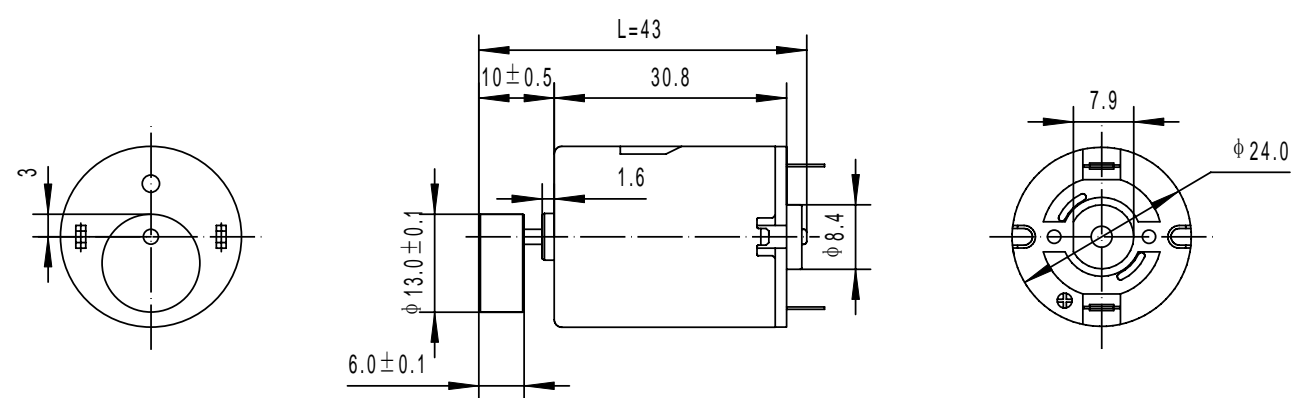
型号 Model	QP50CP08-66-R
尺寸 Dimension	Outer Diameter50mm Baffle Opening13.3mm Height Refer to drawing in details;
阻抗 Nominal Impedance	8 Ohm \pm 15% At1000 HZ
额定功率 Power Rating	1.0 watt Maximum 1.5 Watt
最低共振频率 Lowest Resonant Frequency	630 \pm 20% HZ.
灵敏度 Output Sound Pressure Level (S.P.L)	93 \pm 3db/1 Watt. 1Meter. Average at800, 1000, 1200, 1500HZ.
频率范围 Frequency Range	F0-5KHZ, Average SPL \pm 10db
失真率 Distortion	3%Maximum At1000HZ 1.0 W
极性 Polarity	Diaphragm shall move forward when Apply a Postive DC current the "+" or"Marked" Terminal
寿命测试 Load Test	Bt Audio Singnal Generator At 2.83 Volts.total 48 hours and20~20KHZ Resonant Frequency
异音测试 Abnormal Sound Test	Must be Normally tested Bt 2.83 Volts Sinwave
工作温度 Operation Temperature	- 20 $^{\circ}$ C ~ + 50 $^{\circ}$ C
储藏温度 Storage Temperature	- 40 $^{\circ}$ C ~ + 60 $^{\circ}$ C



Imp	53 QP50CP08-66 SPL
Notes	
Data Measured	May 6, 2013 Mon. 8:58 pm
LMS	4.6.6.371 五月 30-2007
Person:	Company:
Product:	File: 20130504.lib
May 6, 2013 Mon 8:58 pm	LINEAR



TRE-280SA VIBRATION MOTOR




MOTOR Specification(For Reference):

Operation voltage:12.0V DC

Rated Load: $\phi 13 \times 6$ mm Eccentric Weight

1、 Load Speed:4150±10%rpm

2、 load current:50mA(100mA)

TITLE:TRE-280SA VIBRATION MOTOR		Customer No: ES		Drafted By: kevin		6
				Checked By:		
Dwg. NO: 10440-001		Date: 2011.04.08		Approved By:		
TT MOTOR (HK) INDUSTRAIL CO.,LTD		Scale: 1:1		Units: mm	EDITION No: A	
				Angular: =1° Decimal: X.XX ±0.05		
				X.X ±0.2		
				X ±0.3		