

Lecture 23 - Three-phase SPWM Inverters

Output voltage control of the three-phase inverter

Available methods are:

- Input DC voltage regulation - not suitable for voltage source inverters except for slow adjustment of output voltage.
- SPWM – the method now widely used for low to medium power applications.

Unlike the case of a single-phase inverter, variable phase displacement between inverter legs cannot be used as a means for output voltage variation. This is due to the restriction that phase displacement of $2\pi/3$ (120°) between phases must be maintained in order to obtain balanced three-phase output voltage.

Three-phase SPWM Inverter

Three-phase SPWM inverters are controlled in the same way as a single-phase SPWM inverter. Three sinusoidal modulating signals at the frequency of the desired output but displaced from each other by 120° are compared with a triangular carrier waveform of suitably high frequency. The resulting switching signals from each comparator are used to drive the inverter switches of the corresponding leg. The switching signals for each inverter leg are complementary, and the switching signals for each switch has 180° of conduction. These are shown in figure 23.2 for the inverter of figure 23.1.

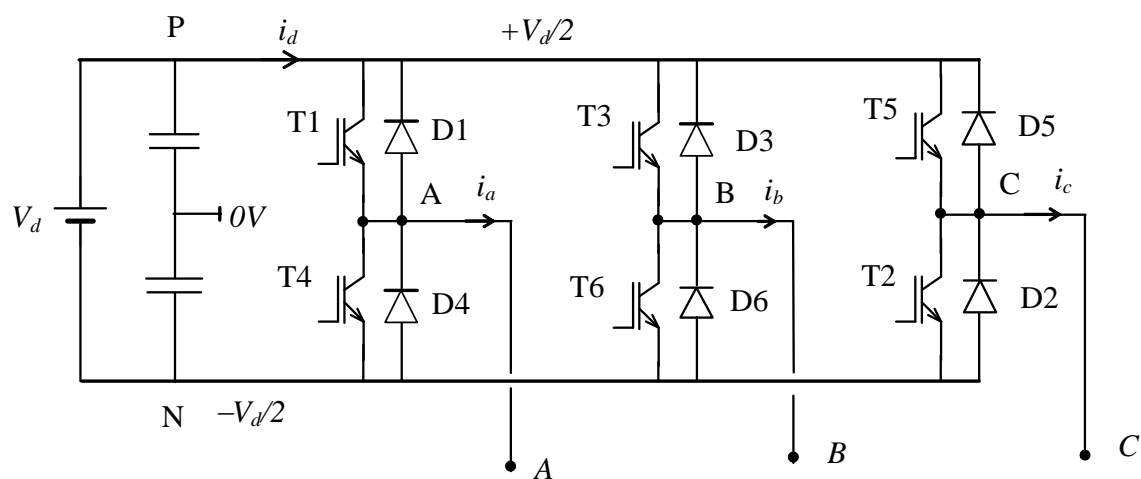
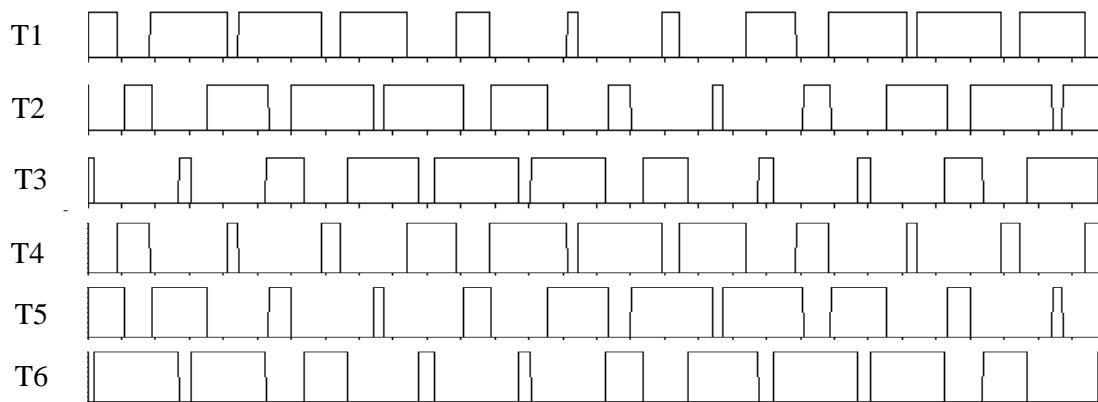
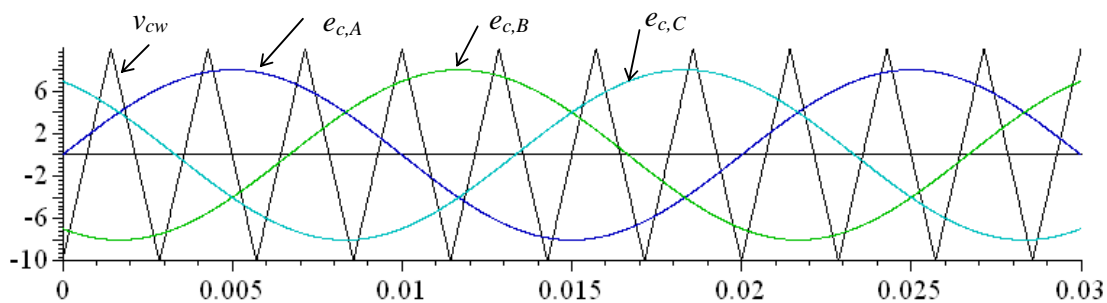


Figure 23.1



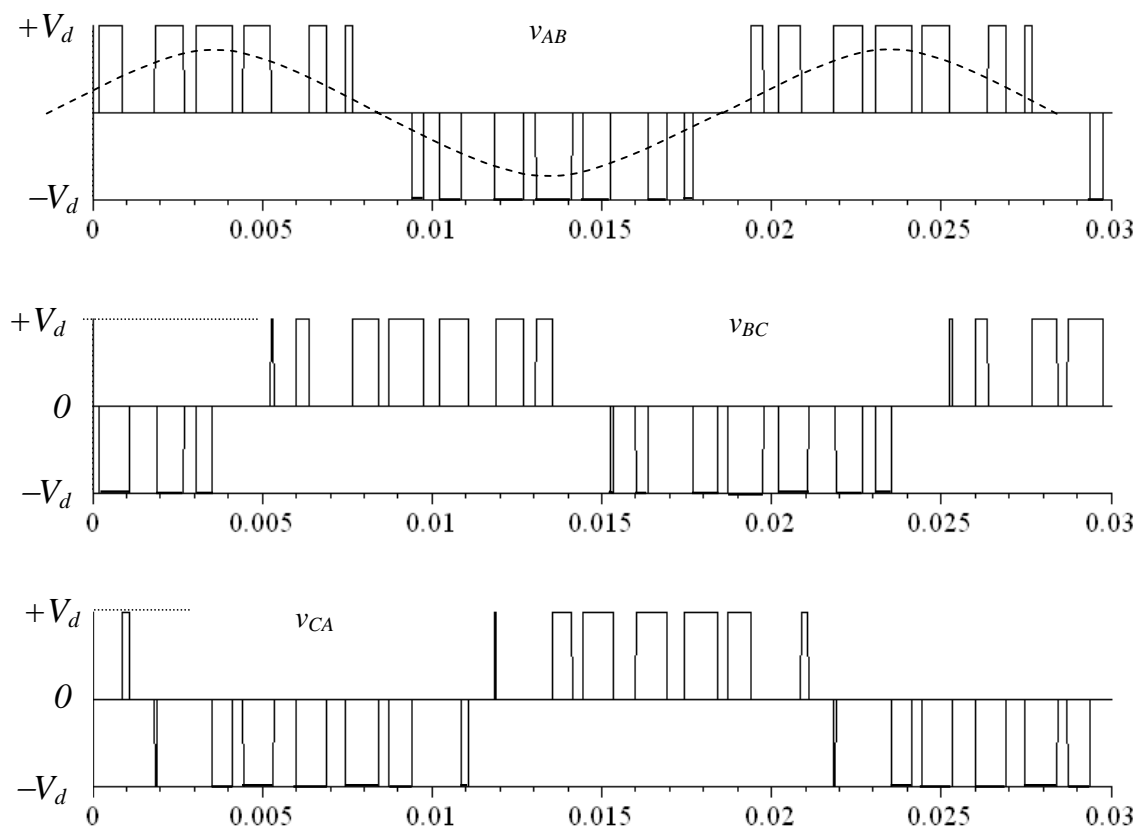


Figure 23.2

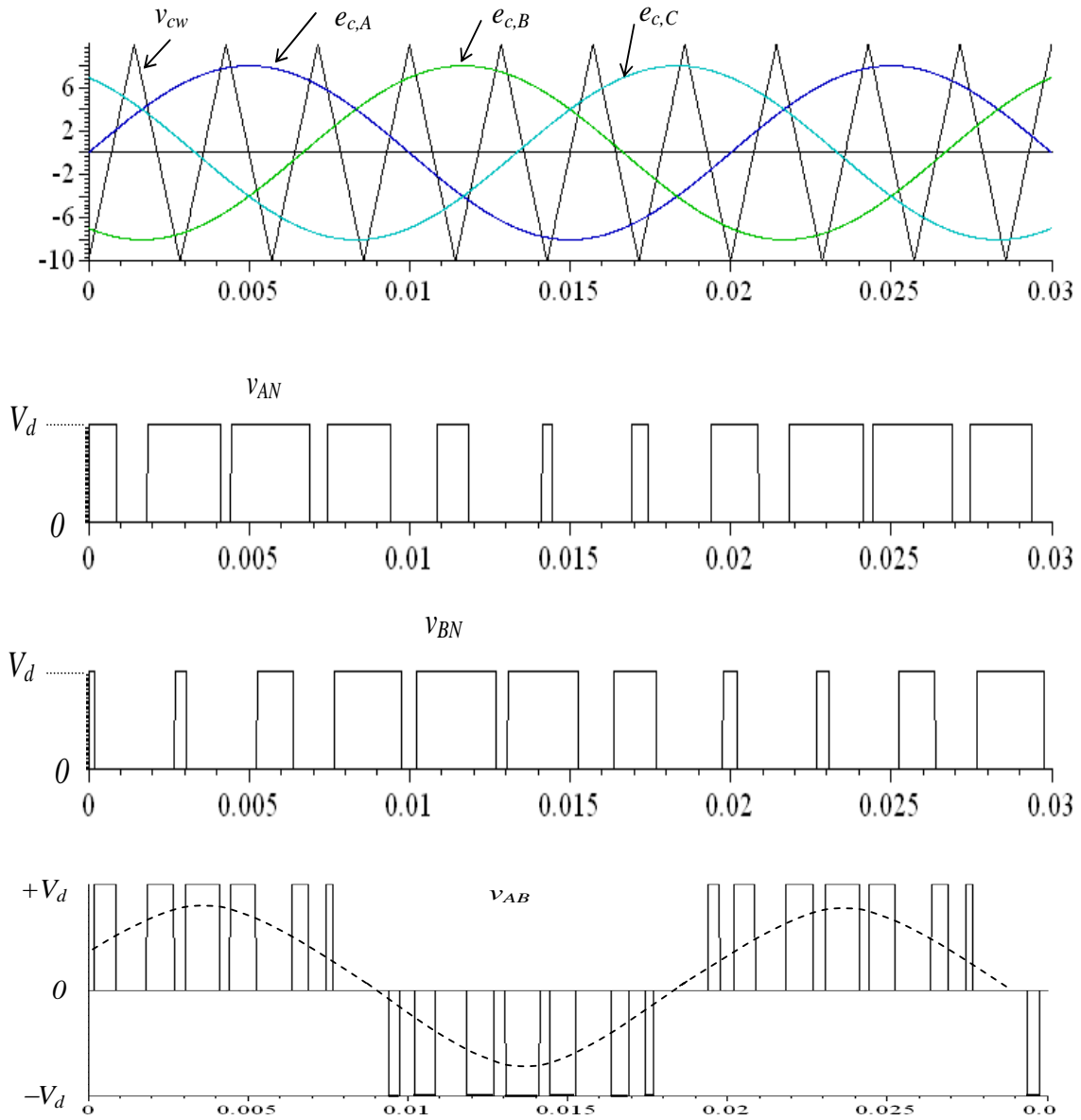


Figure 23.3

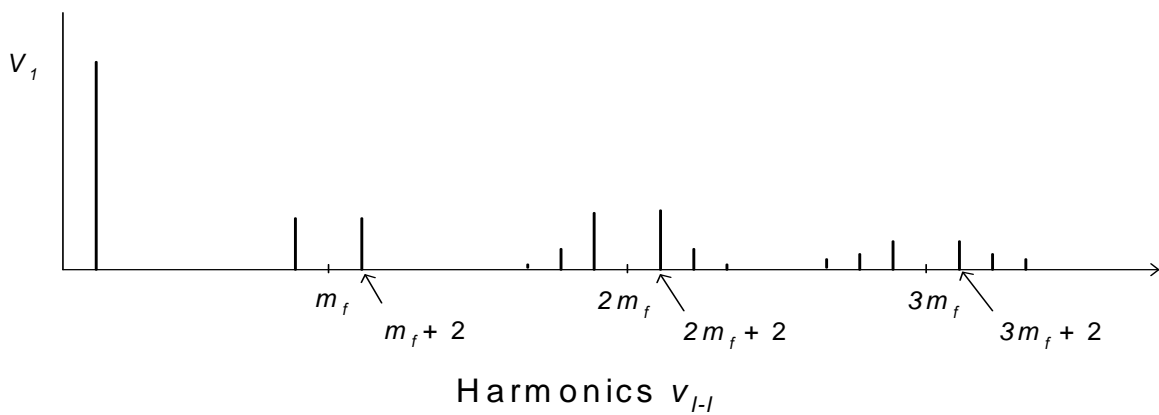


Figure 23.4

It should be noted from the above waveforms in figure 23.2-3 that an identical amount of DC voltage exists in each line-neutral voltage v_{AN} and v_{BN} when these are measured with respect to the negative DC link voltage bus. The DC components are canceled when v_{AB} is obtained by subtracting v_{BN} from v_{AN} . It should also be noted that the v_{AB} waveform is 30° ahead of the control voltage (e_{cA}) for phase A.

The considerations for selecting the triangular carrier frequency and their synchronization with the modulating waveforms are similar to what have been described for single-phase SPWM inverters. Thus, m_f should be an odd integer which is also a multiple of three when it is less than 21 and that the slopes of the modulating waveforms and the carrier waveforms at the zero crossings of the modulating waveforms should be opposite.

When frequency variation in addition to voltage variation is required, the above restrictions should be maintained at all frequencies. In order to improve the inverter efficiency, it is desirable to keep m_f constant when the output frequency is low, otherwise, too many switchings would occur unnecessarily.

Linear Modulation Range, $m < 1$

Considering that the positive DC bus voltage is $+V_d/2$ and the negative DC bus voltage is $-V_d/2$ with respect to the center-tap of the DC supply, the output voltage waveform of a phase leg is a pulsewidth modulated

bipolar AC waveform of magnitude $\frac{V_d}{2}$. The RMS value of the fundamental of this voltage varies linearly with the depth of modulation m . Thus,

$$V_{An,l} = m \cdot \frac{V_d}{2\sqrt{2}} = 0.354m \cdot V_d \quad (23.1)$$

where m is the depth of modulation. This has been indicated as the line-neutral voltage because, with SPWM and balanced three-phase load, the potential of the load neutral point and that of the DC supply center-tap should be the same. The RMS value of the fundamental line-line voltage is

$$V_{AB,l} = m \cdot \frac{\sqrt{3}V_d}{2\sqrt{2}} = 0.612m \cdot V_d \quad (23.2)$$

The calculation of harmonics in the output of a three phase inverter is rather involved. It is best managed on a computer. Figure 23.3 and Table I shows the relative harmonic amplitudes of line-line RMS voltages for a large and odd m_f .

Table I (Source: N. Mohan et al, Power Electronics)

$m \backslash n$	0.2	0.4	0.6	0.8	1.0
1	0.122	0.245	0.367	0.490	0.612
$m_f \pm 2$	0.010	0.037	0.080	0.135	0.195
$m_f \pm 4$				0.005	0.011
$2m_f \pm 1$	0.116	0.200	0.227	0.192	0.111
$2m_f \pm 5$				0.008	0.020
$3m_f \pm 2$	0.027	0.085	0.124	0.108	0.038
$3m_f \pm 4$		0.007	0.029	0.064	0.096
$4m_f \pm 1$	0.100	0.096	0.005	0.064	0.042
$4m_f \pm 5$			0.021	0.051	0.073
$4m_f \pm 7$				0.010	0.030

Over-modulation, $m > 1$

If the peak amplitude of the control voltage is greater than the peak of the carrier waveform, the fundamental output voltage will increase, eventually becoming $0.78V_d$ when m is infinite and the line-line output waveform becomes a square-wave. Over-modulation is thus a means of increasing the output voltage range of a SPWM inverter. When over-modulation is used, more lower-order and sideband harmonics and their multiples will exist around m_f . However, the dominant harmonics will not be as large in amplitude as with operation in the linear range.

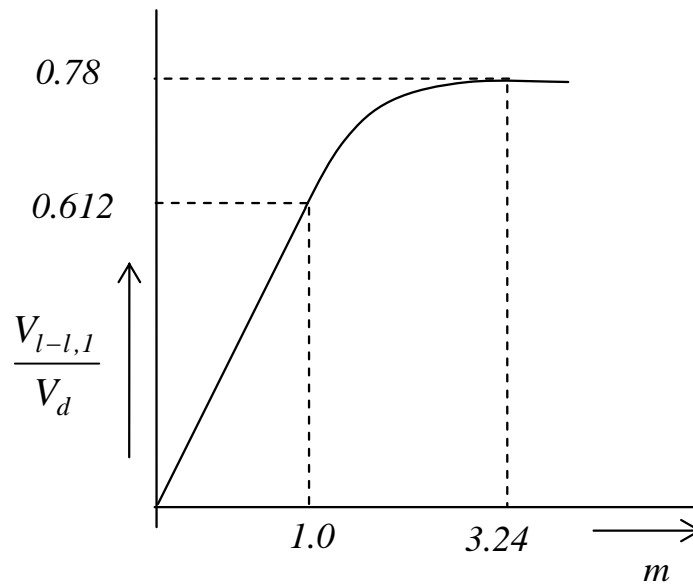


Figure 23.5

The amplitude of the fundamental can be increased further by adding a third harmonic to the modulating waveform as indicated in the figure below. If the modulating waveform is

$$e_{c,A} = m \times \sin(\omega_o t) + \frac{1}{6} \times m \times \sin(3\omega_o t) \quad (23.3)$$

for $m \leq 1$.

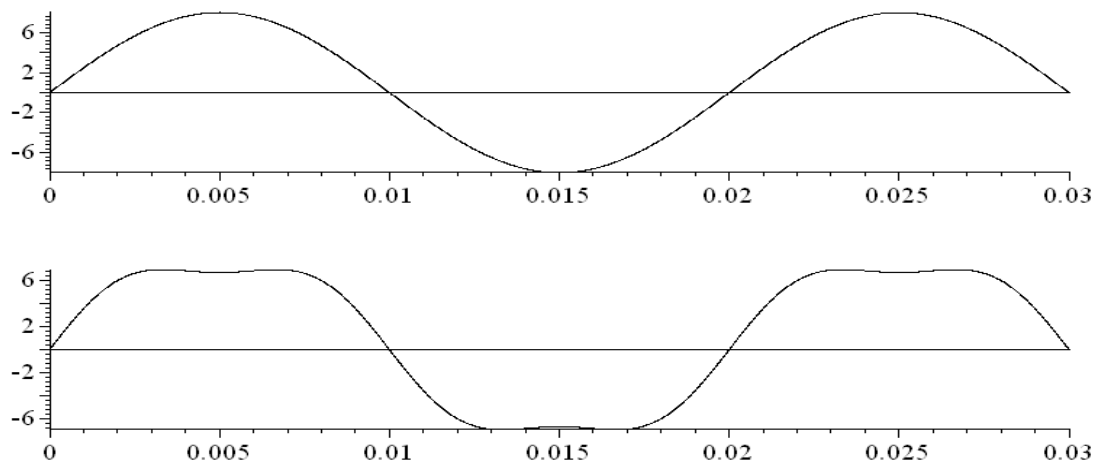


Figure 23.6

It can be shown that the fundamental line-line output voltage can be raised to 1.155 of what is obtained with only the fundamental frequency modulating waveform. Although some third harmonic is added to the modulating waveform, the third harmonic phase currents in a star connected load will always cancel.

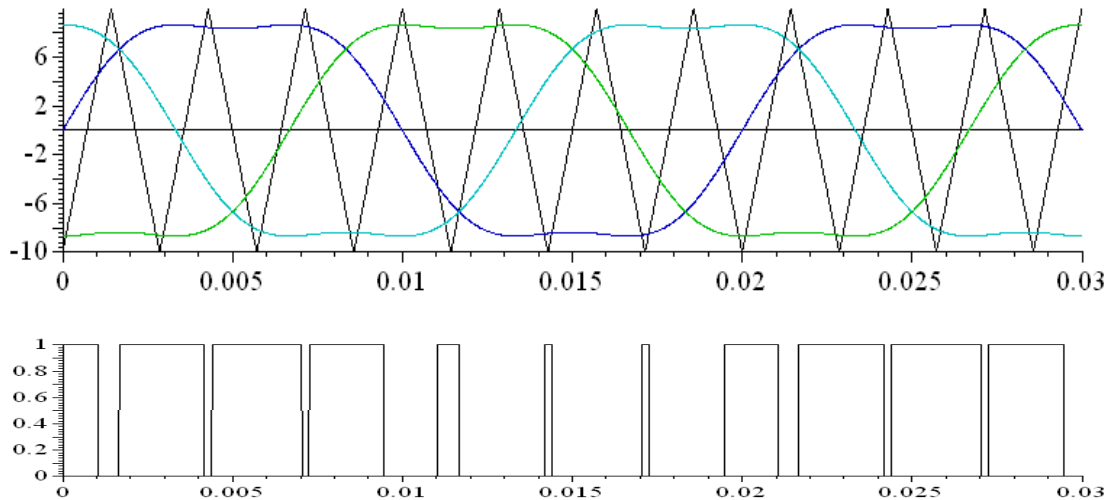


Figure 23.7 PWM switching signal for phase leg A.

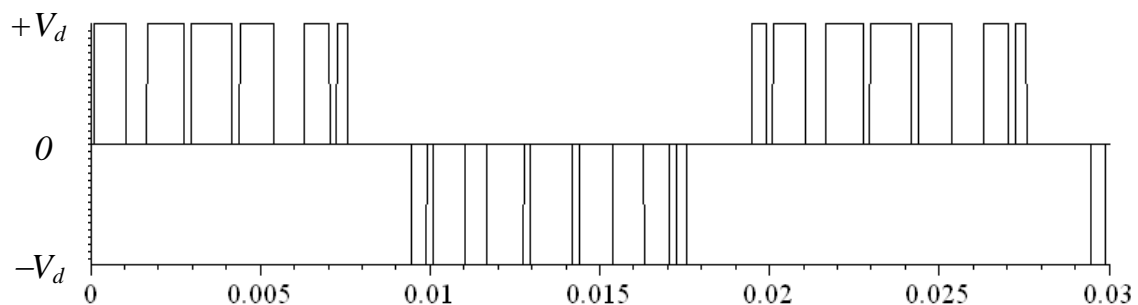


Figure 23.8. For $m = 1$, and $1/6^{\text{th}}$ of third harmonic injection

Note from figure 23.6 that even with $m = 1$ and 16.67% of third harmonic injection in the reference voltages, the amplitude of the modulating waveform does not exceed

the amplitude of the carrier. Additional low-order harmonics that are present in v_{AB} is thus not as much as they would be if m was increased beyond 1 to increase the output voltage.

The DC Link current

With a sinusoidal output current which is at a phase angle ϕ (lagging) with respect to the line-neutral voltage, the mean DC link current I_d is

$$I_d = \frac{3\sqrt{2}}{\pi} \cdot I_{o1} \cos \phi \quad (23.4)$$

where I_{o1} is the RMS fundamental phase current of a Y-connected load.

Effect of dead time on inverter output waveform

In the forgoing sections on inverter circuits, it has been assumed that switches in an inverter leg turn ON and OFF instantly and that their switching signals have complementary logic. However these switches have finite turn-on and -off times, the off-times being generally much longer than turn-on times. If a switch in a leg turns on ahead of the other switch in the same leg turning off, a catastrophic short-circuit of the DC source may occur, because of the very low source impedance of the DC source. Furthermore, gate drive signals are often delayed through isolation circuits, with some the likelihood for overlap of simultaneous conduction (short-circuit). It is thus necessary to introduce dead-time between the transition of switching from the top transistor in a leg to the bottom transistor in the same leg and vice versa as indicated in figure 23.8.

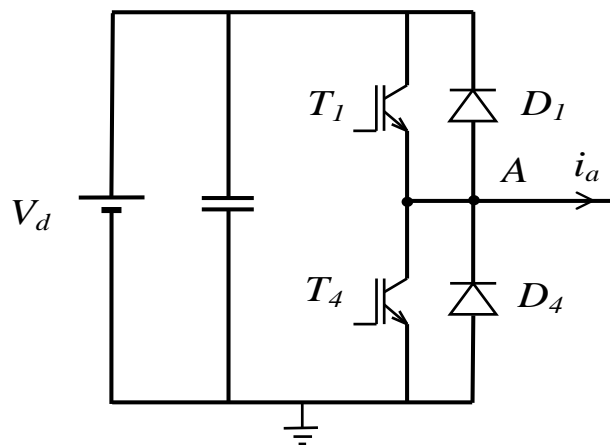


Figure 23.9

To prevent overlap of conduction, dead-time is interposed into the switching signals as indicated in

figure 23.8. The dead-time can be of the order of a few microseconds for fast devices (such as MOSFETs) to a few tens of microseconds for slower devices. Note that both devices in an inverter leg are off during the dead-time. Obviously, the dead-time affects the voltage at the load terminals of an inverter. Depending on the direction of load current flow the load terminal is clamped either to the positive bus or to the negative bus which leads to clamping of the load voltage to $+V_d/2$ or $-V_d/2$.

Consider the single-phase full-bridge inverter of figure 23.7 in which the bipolar switching scheme is employed. Once dead-time T_d is incorporated, the switching signals T1 and T4 are modified to T1' and T4', so that both switches remain off for T_d at transitions. The dead-time T_d is selected according to the worst case requirement for complete turn-off of a device in a circuit. Compared to the ideal case of having no dead-time, it can be seen that if $i_A > 0$ and when T4 is turned off, the delay in turning switch T1 ON means that the load terminal A continues to have $-V_d/2$ due to the diode D4 conducting, instead of $+V_d/2$. The shaded voltage pulse of amplitude $+V_d$ and duration T_d is therefore lost from the incoming output PWM voltage pulse.

Similarly, compared to the ideal case of having no dead-time, it can be seen that if $i_A < 0$ and when T1 is turned off, the delay in turning switch T4 means that the load terminal A continues to have $+V_d/2$ due to the diode D1 conducting, instead of $-V_d/2$. The shaded voltage pulse of

amplitude $+V_d$ and duration T_d is therefore gained by the outgoing output PWM voltage pulse.

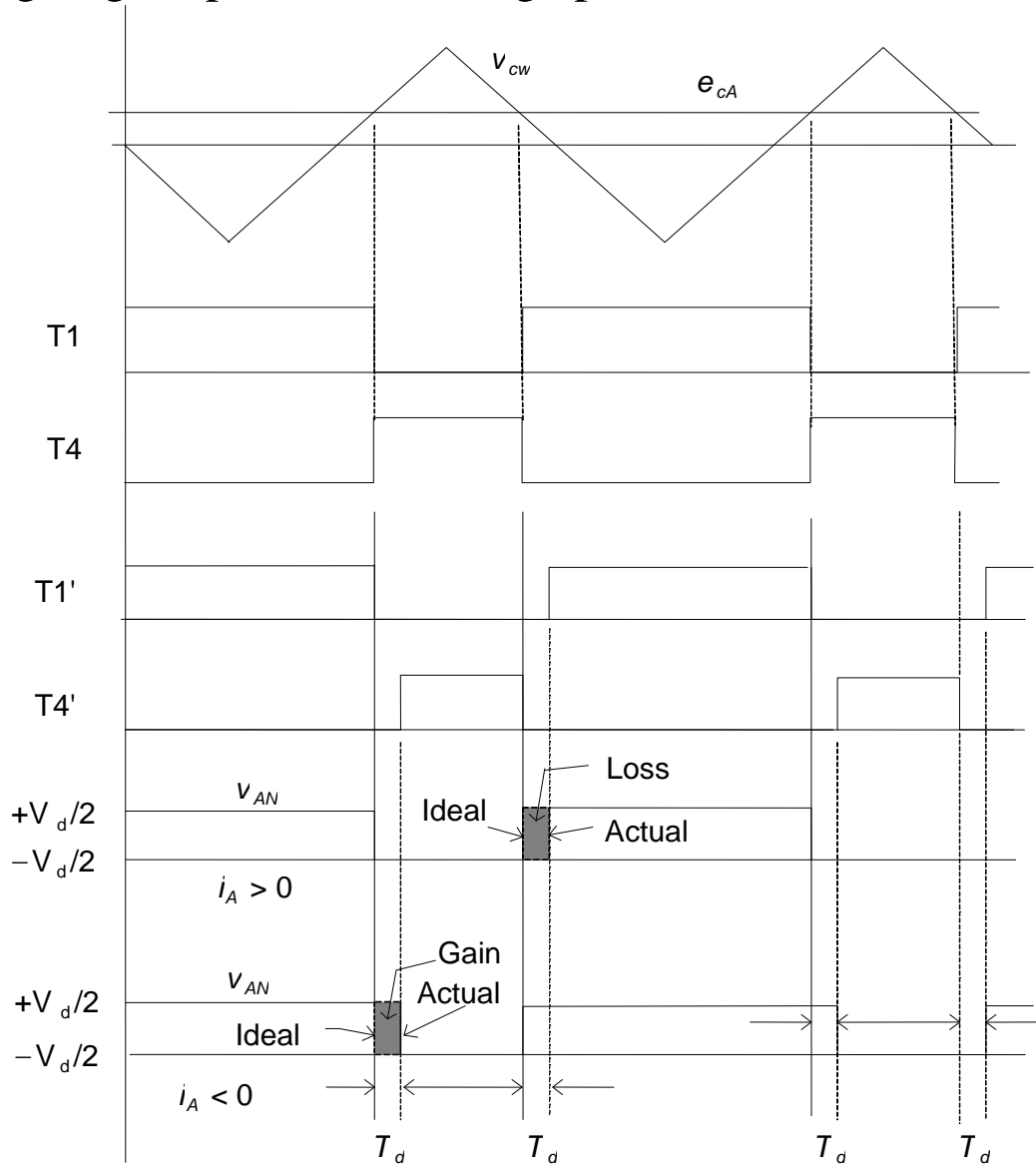


Figure 23.10

Thus, for $i_a > 0$, the average loss of potential at terminal A over a PWM switching period T_s is given by

$$\Delta V_{AN} = -\frac{T_d V_d}{T_s} \quad (23.5)$$

Similarly, for $i_a < 0$, the average gain of potential at terminal A over a PWM switching period T_s is given by

$$\Delta V_{AN} = \frac{T_d V_d}{T_s} \quad (23.6)$$

Note that over each PWM switching period T_s , transitions of the switches from T1 to T4 or from T4 to T1 occur once each PWM cycle. Thus, for a single-phase, half-bridge SPWM inverter, the output voltage

suffers a voltage drop of $-\frac{T_d V_d}{T_s}$ when $i_o > 0$ and a voltage increase of $\frac{T_d V_d}{T_s}$ when $i_o < 0$.

For a single-phase full-bridge inverter, note that the positive current at terminal A (current out of terminal A) is actually a negative current at terminal B (current into terminal B). Thus, the average gain of potential at terminal B over switching period T_s for $i_A > 0$ is

$$\Delta V_{BN} = \frac{T_d V_d}{T_s} \quad (23.7)$$

Similarly, the average loss of potential at terminal B over switching period T_s for $i_A < 0$ is

$$\Delta V_{BN} = -\frac{T_d V_d}{T_s} \quad (23.8)$$

Since $v_o = v_{AN} - v_{BN}$, the change of output voltage due to the dead-time T_d is

$$\Delta V_o = \Delta V_{AN} - \Delta V_{BN} = -\frac{2T_d}{T_s} \cdot V_d \quad \text{for } i_A > 0. \quad (23.9)$$

$$= \frac{2T_d}{T_s} \cdot V_d \quad \text{for } i_A < 0. \quad (23.10)$$

The figure 23.11 shows the effect of dead-time on the fundamental output voltage waveform of a full-bridge single-phase SPWM inverter. Note that output voltage level changes at the zero crossings of the load currents imply that there is now a low order harmonic voltage in the output which is at twice the output frequency. This occurs in all inverter circuits.

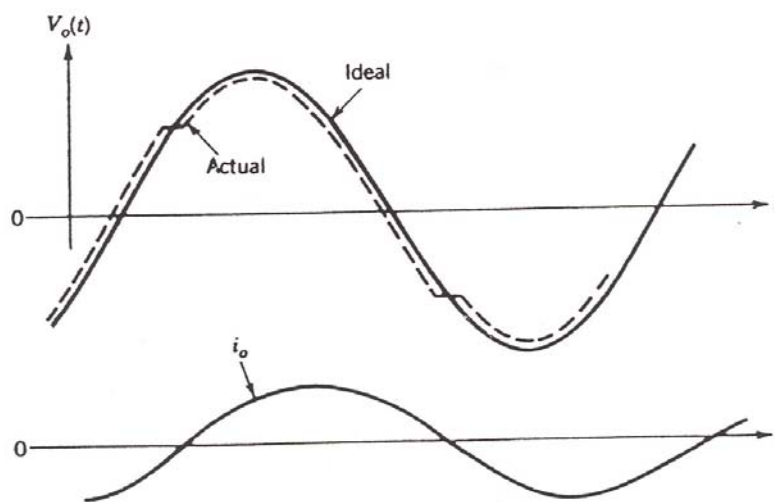
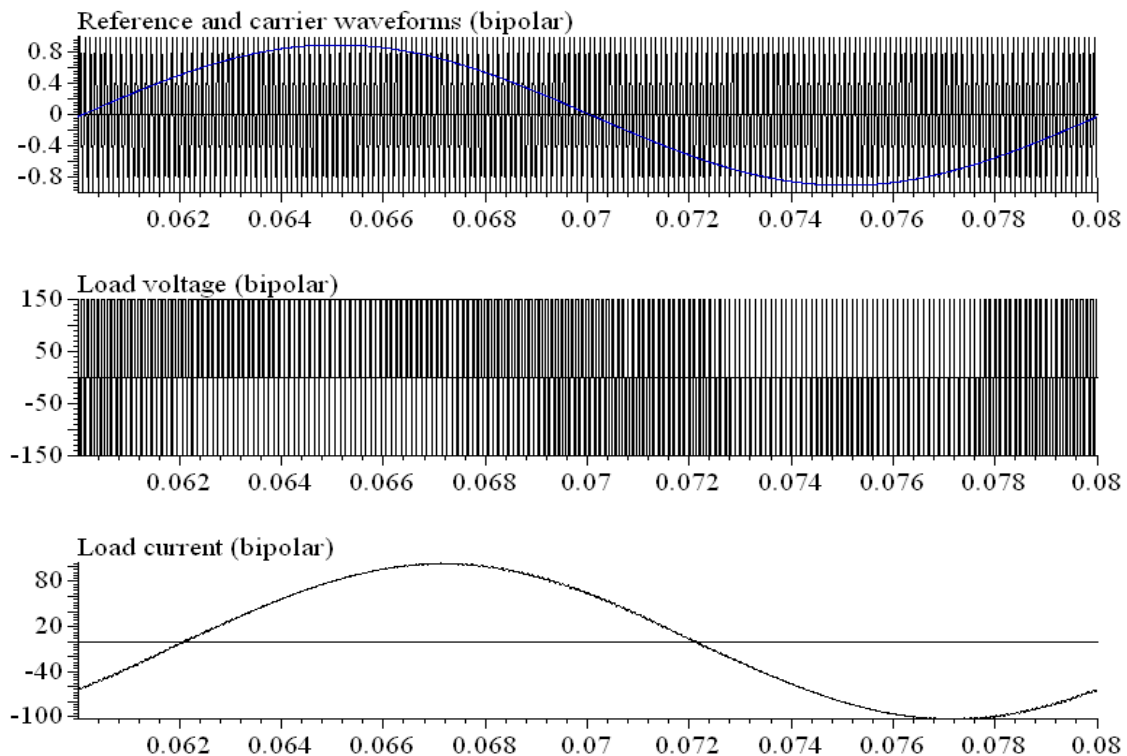


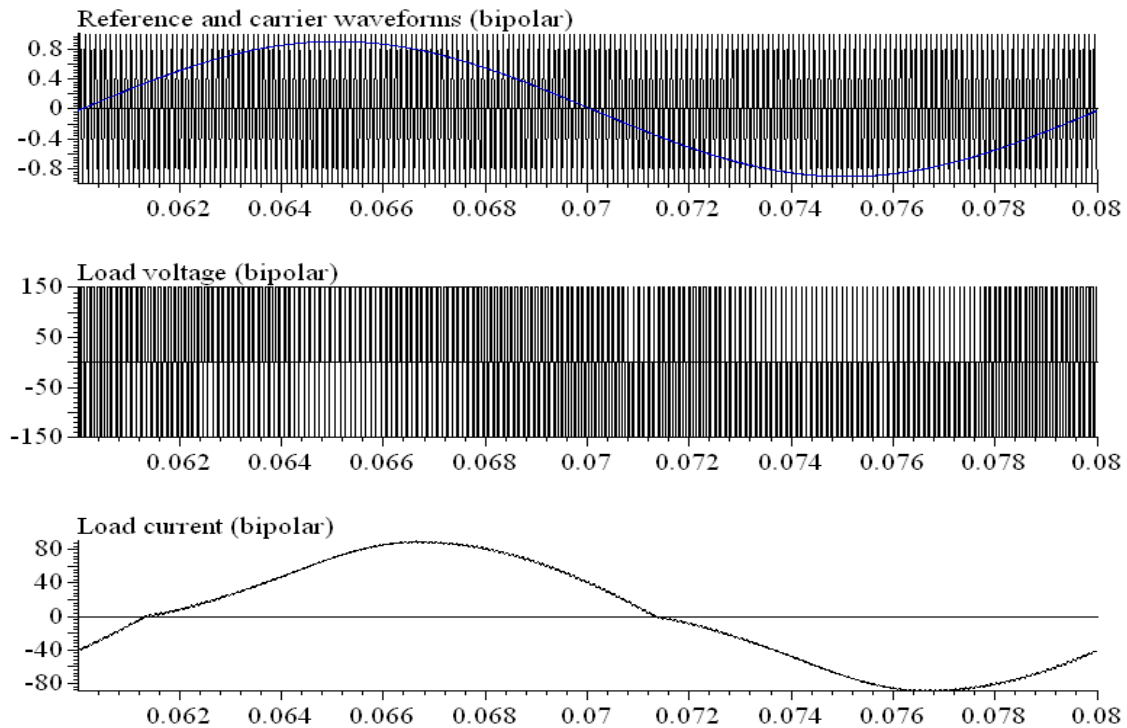
Figure 23.11

It should be appreciated that the distortion (ΔV_o) in the output voltage and current due to dead-time is more significant when T_d is comparable to T_s , as it happens

when the switching frequency is high and the dead-time requirement for the switching devices in the inverter is also large. With longer turn-off times of slower devices, this problem is more prevalent. This is another reason for the trend towards faster switching devices. Figure 23.11 show a few inverter output waveforms for such cases.



(a) $f_s = 10 \text{ kHz}$, $T_d = 1 \text{ } \mu\text{s}$



(b) $f_s = 10 \text{ kHz}$, $T_d = 10 \mu\text{s}$

Figure 23.12

Because the fundamental voltage waveform contains two shifts per cycle, the load voltage and current harmonics will include second order harmonics.

Current Source Inverters – Not included for 2010

Single-phase CSI

Current source inverters are supplied from current sources. Figure 23.13 shows a circuit in which the DC link inductor L help render the supply a stiff current source. If the supply current can not change appreciably over one complete cycle of the output voltage or current waveform because of the source inductance, then the input source can be regarded as a stiff current source. A sufficiently large inductance L is all that is required. If the phase-controlled thyristor AC-DC converter (on the left-hand side) is continuously regulated using firing angle (α) control to maintain the DC link current to a desired level, then the required DC link inductance size can be further reduced. In some cases, the inductance in the load may be sufficient to achieve the required current source performance.

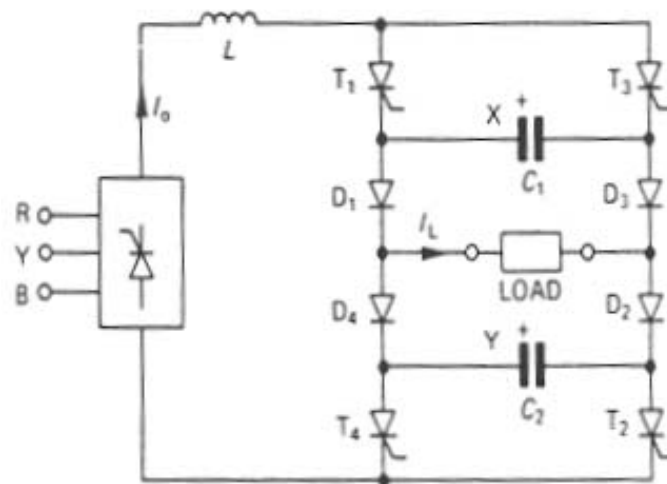


Figure 23.13

The four inverter thyristor switches T1 – T4 are switched as in a bipolar switched full-bridge inverter to produce an AC output current waveform as shown in figure 23.14. The switching scheme is T1T2 – T3T4 – T1T2 and so on. If the DC link supply current I_L is assumed to be constant the load current waveform can be expressed as

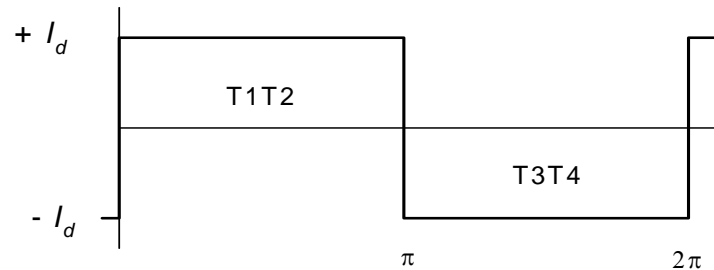


Figure 23.14

The capacitors C1, C2 and diodes D1 – D4 allow the four thyristor switches to turn-off in pairs as required. Note that thyristors can not naturally turn off in this circuit. Consider a load current cycle in which the switches T1 and T2 are ON, and the load carries the DC link current I_d . Capacitors C1 and C2 are both charged through D3, D4, and T2 to the load voltage which is positive on the left-hand terminal. When T3 and T4 are triggered ON at π , capacitors C1 and C2 apply reverse bias to the anode-cathode terminals of the thyristors. T3 and T4 divert the currents in T1 and T2 respectively turning them off. From this point, capacitors C1 and C2 start to recharge towards an opposite polarity voltage, ultimately reaching the amplitude of the negative load voltage. While capacitors C1 and C2 charge negatively, load current falls to zero and then rises to the DC link current I_d . If constant I_d is assumed, the capacitor and load currents

must at times add up to I_d . Note that diodes D1 – D4 also prevent discharging of the capacitors into the load.

If the thyristor switches of figure 23.13 are replaced by gate turn-off devices, the capacitors C1 and C2 can be eliminated. These devices now allow quasi-square current output waveforms in the load, allowing output current control. This is achieved by allowing the DC link current to be carried entirely by the left or right legs of the inverter for part of the AC cycle.

The three-phase current source inverter circuit of figure 23.15 operates in same way as described in the above paragraph. The switching signals (of 180° conduction angle) for each inverter leg are displaced by 120° from those of adjacent legs. For a constant DC link current I_d , quasi-square phase currents of amplitude I_d and duration 120° (δ) in a Y-connected load occur, as indicated in figure 23.16.

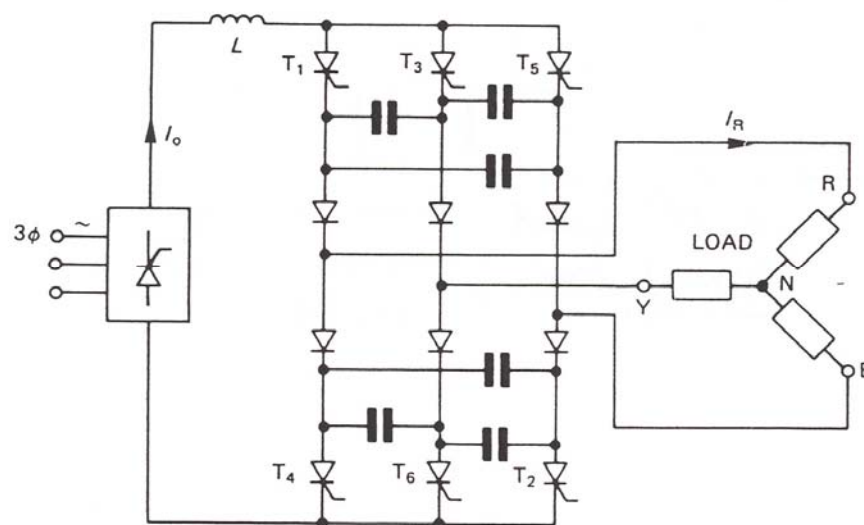


Figure 23.15

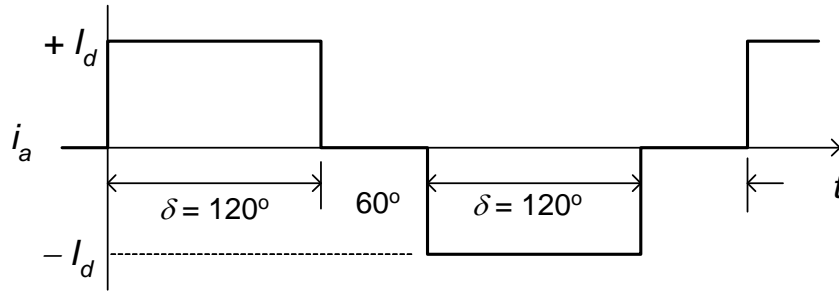


Figure 23.16

Note that with a CSI employing gate turn-off switches, the quality of the current supply to load can be improved by using SPWM and modified SPWM.