School of Electrical Engineering and Telecommunications

Topic 4: Elective Topics

Power Electronics – Distribution Grid Networks

Context and Objectives

Microgrids can be defined as a subsystem of a larger power system. This subsystem may include a set of local generation sources and associated loads. Microgrids can be operated in grid-connected mode (GCM) when connected to a larger network or islanded mode (IM) when disconnected from the grid. In islanded mode, the microgrid can autonomously manage the local generation and demand offering a great potential to improve local energy reliability.

In this elective task, you will design a three-phase (3-ph) microgrid with two inverters as shown in Figure 1. Inverter 1 will be designed to operate as a grid-feeding inverter during the GCM operation of the microgrid and grid-forming inverter during the IM operation of the microgrid. Inverter 2 will be designed to operate as a grid feeding inverter in either GCM or IM mode. Inverter 1 should also have some form of islanding detection, to detect disconnection from the grid, which should prompt the change from grid-feeding to grid-forming.

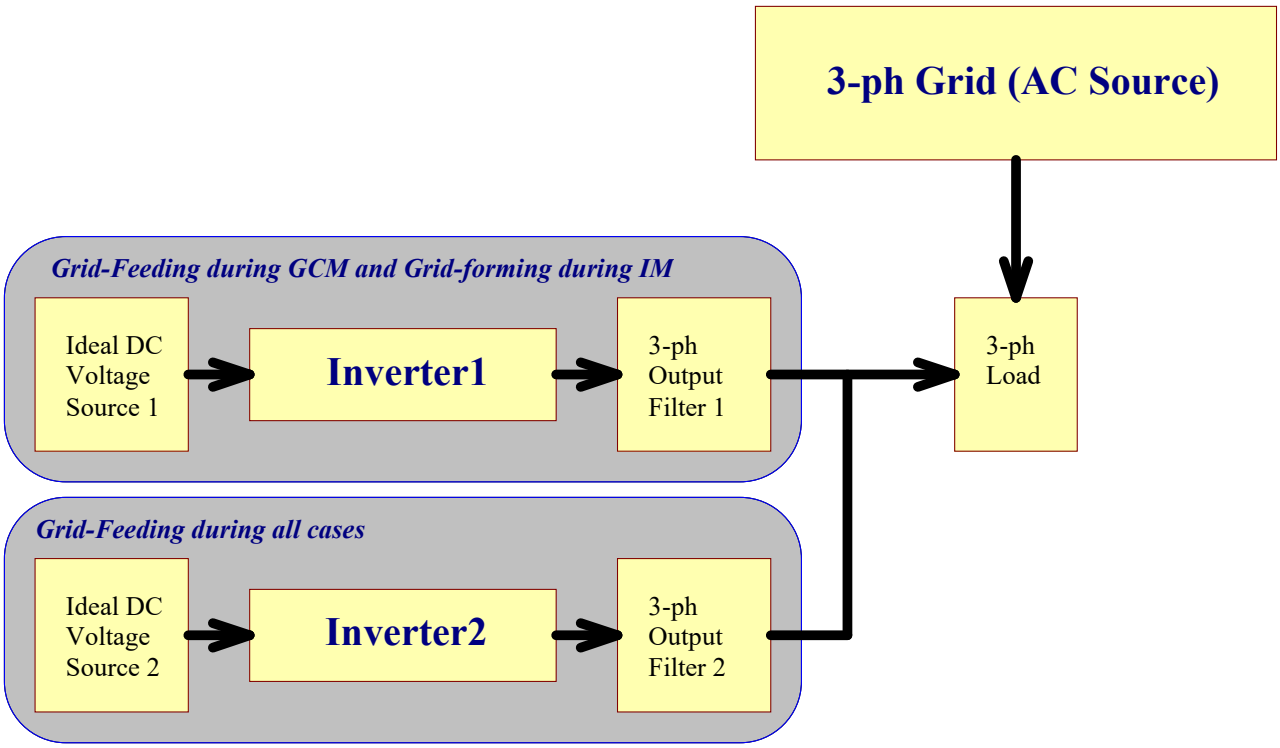

Figure 1. Overall combined tasks overview.

Detailed Description

There are 4 deliverables or levels for this task: Basic, Satisfactory, High, and Outstanding levels, with higher difficulty in later levels. The overall requirement mark that you can receive for this elective topic is based on how many levels you can complete successfully (total 10% of your assessment for the course). For instance, you have the choice to complete only one level, and if successful, a Basic mark is awarded. The more levels you complete, the higher your final requirements mark will be. But you may want to strategies for balancing your workload and not necessarily try to push your group to complete all tasks but rather focusing on the first and the second levels and do a good job on them so you can guarantee a minimum Satisfactory mark for this topic.

Basic Level: Phase Lock Loop (PLL)

One popular technique that is used to synchronize a generator output voltage to the grid voltage is to use a phase lock loop (PLL) to measure the amplitude, frequency, and phase angle of the three phase grid voltages. Many generation sources use an inverter to synchronize to an AC grid and these inverters typically use a PLL to perform this grid voltage synchronization. A PLL must accurately estimate the amplitude, frequency and phase angle of the fundamental component of the grid voltages during steady-state conditions. It must also quickly respond to any changes in the grid voltage amplitude, frequency or phase angle. These changes in the grid voltage are often caused by grid voltage disturbances.

Grid Voltage Disturbances

Two common types of grid voltage disturbance are a phase angle jump and a voltage sag. A phase angle jump is where the grid voltage phase angle suddenly jumps by a specific amount. For example, the grid voltage phase angle might suddenly jump from 40° to 65° due to fault somewhere in the network. After a phase jump occurs, the PLL must synchronize to the new phase angle value within a specific time or the generation source must be disconnected from the grid, which is undesired.

Another grid voltage disturbance is a sudden reduction of the rms voltage which is called an undervoltage or voltage sag. These sags are typically caused by an electrical short circuit occurring at some point in the electricity supply system. The high short-circuit current yields large voltage drops in the impedances of the supply system, which lower the rms voltage of the network. Practically, a sag will typically only occur in a distribution network for a short duration of time until a protection device isolates the source of short-circuit current. Yet again during this fault type, the PLL must stay synchronized to avoid needing to take an energy generation source offline.

The minimum design constraints for this system are as follows:

- You are provided with a basic template in Simulink as shown in Figure 2 to help saving time and build your system. The solver and the fundamental step size are already configured in this template for your convenience.
- **No** Simulink integrated blocks are allowed to be used, including built-in PLL block, DQ transform.
- **No** discrete transfer function blocks are allowed to be used to implement your controller, only basic Simulink blocks like unit delay, gain and summing junction are allowed to be used to implement the controller.

Basic Level Deliverable:

The 3-phase PLL must accurately track a set of perfectly sinusoidal three-phase voltage signals with an amplitude of $\mathbf{230\sqrt{2}V}$ (nominal value) and any grid frequency in between **48-52 Hz** during steady-state conditions, during a voltage sag and during a phase jump.

To do this:

1. The PLL must track the **frequency** with a peak-to-peak ripple of **< ±0.0001 Hz** during steady-state conditions with zero average steady-state error.
2. The PLL must track the signal **amplitude** with a peak-to-peak ripple of **< ±1 mV** during steady-state conditions with zero average steady-state error.
3. The difference between the actual phase angle and PLL phase angle estimate must not exceed **±0.1°** during steady-state conditions.
4. During a phase jump of 15°, the frequency and amplitude responses must have a settling time **(< 0.05% final value) < 150 ms** and a percentage overshoot of **< 10%**.
5. During a voltage sag of 0.2 p.u, the frequency and amplitude responses must have a settling time **< 50 ms** and a percentage overshoot of **< 2%**.

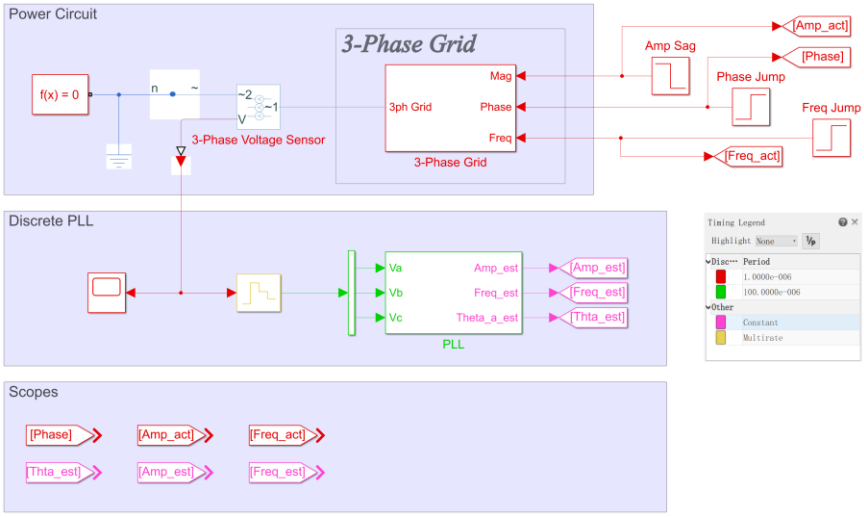

Figure 2. Basic Simulink template.

Satisfactory Level: Grid-Forming Inverters

A grid-forming inverter will convert the dc bus voltage from the output of a renewable energy source (RES) to an AC grid voltage with a voltage frequency and amplitude input reference. In Australia, standards dictate that the nominal three-phase AC grid voltage and frequency is 400 Vrms,l-l and 50 Hz respectively, so these values should be used as the input references for a grid-forming inverter in Australia. Standards also require that inverters use an output low-pass filter to remove any high frequency switching current harmonics to ensure that the inverter output current is sinusoidal when interfacing to the grid. Ideally, a filter with a low cut-off frequency and high attenuation at the high switching frequency is desirable to better eliminate switching current ripple.

Inverter Output Filters

Typically, an L, LC or LCL circuit is used to perform the inverter output filtering. The L-filter is popular and simple to use but has a low attenuation and high required inductance value, which makes the filter size large. The LCL-filter produces the best attenuation at the inverter switching frequency and can provide the best decoupling between the filter and the grid impedance out of these three filter topologies. However, the three-order nature of the LCL-filter circuit means that it is difficult to design as there are many important design considerations. The LC-filter is a trade-off for simple design and better attenuation to the switching frequency. A high-level block diagram of grid-forming system is shown in Figure 3.

Additional minimum design constraints for this system are as follows:

- The inverter must be three-phase and must have **the conventional six-switch configuration**.
- The inverter must **use individual IGBT semiconductor switching components** from the electrical Simscape library. Note that you cannot simply use a universal bridge or inverter block.
- The dc bus voltage must be chosen to be large enough to supply the required grid voltages but **not be unnecessarily oversized**.
- The inverter must have an inner current control loop (using PI **or** PR controllers).
- The inverter must have an output filter which has practical component values.
- A three-phase wye-connected **10 kW RL load with a lagging power factor of 0.95 @ 50 Hz** must be used as the load.
- The inverter must have **deadtime** included in the switching PWM algorithm to avoid short circuiting the dc bus voltage source during a switching event.

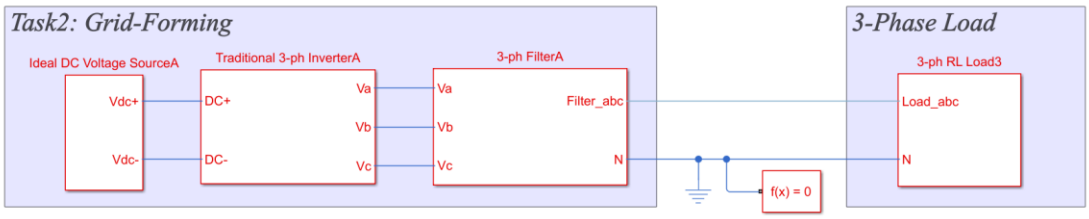

Figure 3. Grid-forming block diagram.

Satisfactory Level Deliverable:

1. An LC-filter has been used with practical values. The filter values must be chosen to give:
   - An inverter output current with maximum peak-to-peak ripple, $\Delta i_{inv} < 1A$, at the rated load current to avoid necessarily high practical IGBT current ratings.
   - A reactive power drop across the capacitor which is $< 5\%$ of the rated power, to avoid high reactive power consumption in the capacitor.

$$\frac{V_{rated}^2}{X_c} < 5\% \times S_{rated}$$

   - The total impedance of the inductors is $< 10\%$ of the base impedance to avoid large voltage drops across the inductors.

$$X_L < 10\% \times \frac{V_{rated}^2}{S_{rated}}$$

2. The **inner current control** loop has been tuned appropriately for the LC-filter and RL load. The inverter current controller can accurately track a step change in the amplitude of the load current from zero to the rated value and obtain a settling time $< 120ms$, percentage overshoot $< 20\%$ and steady state error $< 0.5\%$.

You must provide a setting to switch between voltage and current control. An **outer voltage control** loop has been tuned appropriately to provide an AC grid voltage with fundamental component amplitude of $400\ V_{rms,l-l}$ ($\pm 2\%$ error allowed) and a frequency of $50Hz$ ($\pm 2\%$ error allowed) during steady state conditions. The voltage controller can also achieve a setting time $< 800ms$ and percentage overshoot $< 5\%$, when the load power demand is stepped from 0kW to 10kW. Ensure THD is $< 5\%$ for the load voltage and currents.

<u>High Level</u>: Grid-Forming and Grid-Feeding Inverters

Typically, a grid-forming inverter contains an inner current control loop and an outer voltage control loop. The outer voltage control loop possesses the desired grid voltage amplitude and frequency as input references. This allows the grid-forming inverter to generate the desired ac voltages. A PLL is not required for a grid-forming inverter as it is effectively setting the phase angle of the grid voltage. Whereas, a grid-feeding inverter contains an inner current control loop, an outer power control loop and a PLL. The PLL locks onto the phase and frequency of the grid voltage and ensures that the grid-feeding inverter is supplying voltages at the correct grid frequency and phase angle. The outer power control loop possesses the desired real and reactive power as input references. Note that these power references are often chosen by higher level control systems which is beyond the scope of this course. Also, note that you cannot have a grid feeding inverter in an islanded microgrid without the presence of a grid-forming inverter to set the ac grid voltage. A high-level block diagram of grid-forming system is shown in Figure 4.

Additional minimum design constraints for this system are as follows:

- The grid-feeding inverter must have an inner current control loop and must have real and reactive input power references for the outer control loop.
- The grid network bus must be represented by a set of sinusoidal voltage sources with an amplitude of 400 Vrms,l-l and a frequency of between 48-52 Hz.

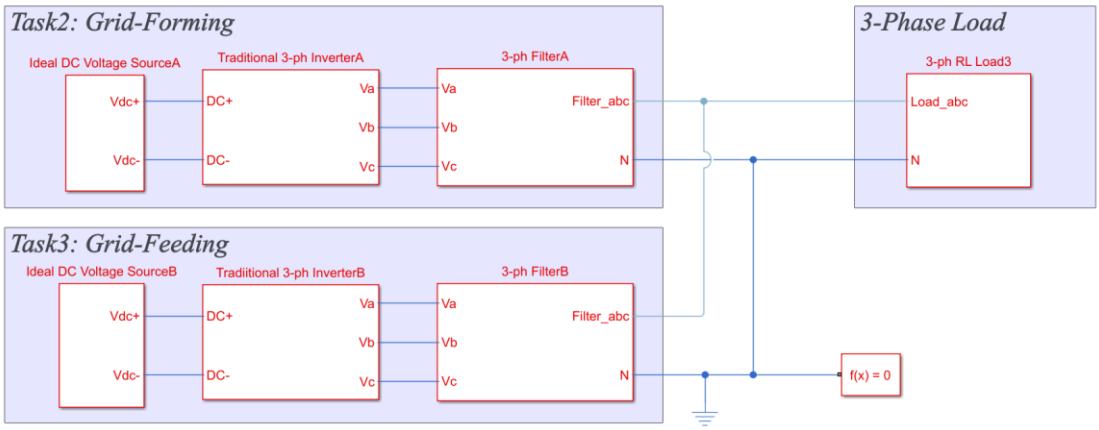

Figure 4. Grid-forming and Grid-Feeding Inverters block diagram.

High Level Deliverable:

A LC-filter has been used with the inverter. The same filter specifications as shown in SF feature requirement one.

1. The grid-feeding inverter can supply $5kW \pm 10\%$ and $0kVAR \pm 1kVAR$ at the filter output during steady-state conditions.
2. The inverter can track a step change in the real power from 0 to 5kW with a settling time $< 150ms$ and a percentage overshoot of 15%.

<u>Outstanding Level</u>: Grid-connected Mode and Islanded Mode Switch

Outstanding Level Deliverable:

1. The inverter one must have the ability to automatically switch between grid-connected and islanded mode during live operation, when the grid-network bus is connected or disconnected to the microgrid. Note that you should include a signal to detect the connection status of the grid-network bus to determine the operating mode of the inverter. A high-level block diagram of for this task is shown in Figure 5.

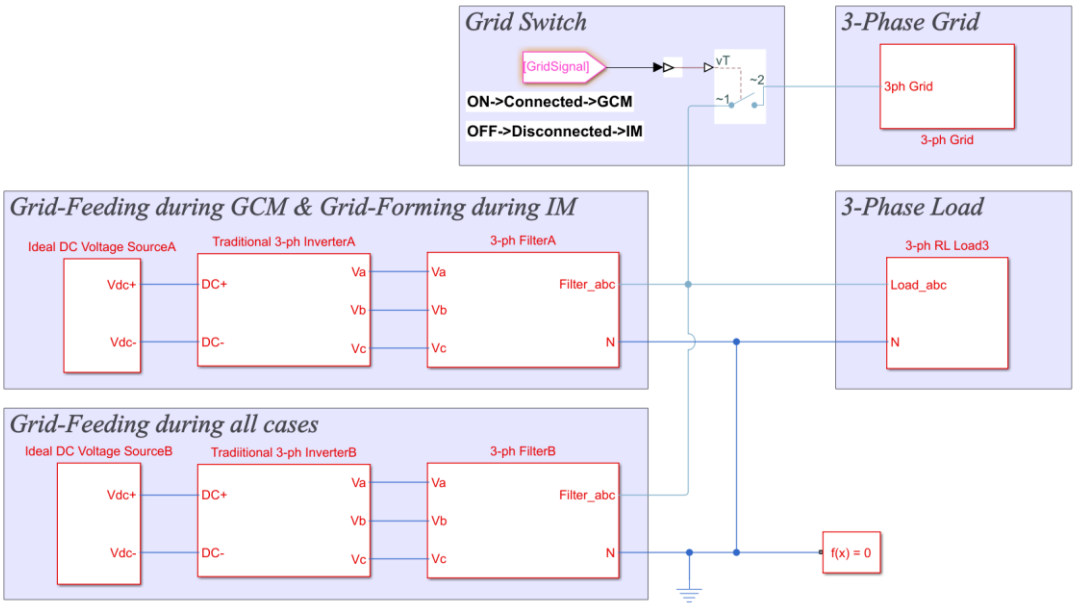

Figure 5. Grid-connected Mode and Islanded Mode Switch block diagram.

Simulink solver and Local Solver settings

Continuous Time vs Discrete Time States

When modelling a system, it is important to think about what which parts are continuous time, and which are discrete time. Note that continuous time is where the signal/state is defined for all time t and contains no sampling. Whereas discrete time is where there signal/state is sampled at a specific sampling frequency. It is important to realize that MATLAB Simulink treats continuous states differently to discrete states and hence solves them differently. Note that a digital processor should be modelled in discrete time to create an accurate represent of a practical model. You will find that designing controller in the continuous time-domain is quite simple. However, designing a practical controller in the discrete time-domain is much more difficult as stability becomes as issue as your controller bandwidth approaches the controller sampling time.

Simulink Solver

You must carefully select your Simulink solver depending on the nature of the states of your system. For example, a mostly continuous state system should use a variable-step auto solver as this has a fast-solving time and yields enough accuracy for this assignment. However, a simulation with discrete states like a PWM inverter should use a fixed-step discrete solver with a fixed step size.

Solver settings!!!

In this task, you need to use Fixed-step discrete (no continuous states) as your solver selection. And your fixed-step size (fundamental sample time) is $T_s = 1us$ as shown in Figure 6.

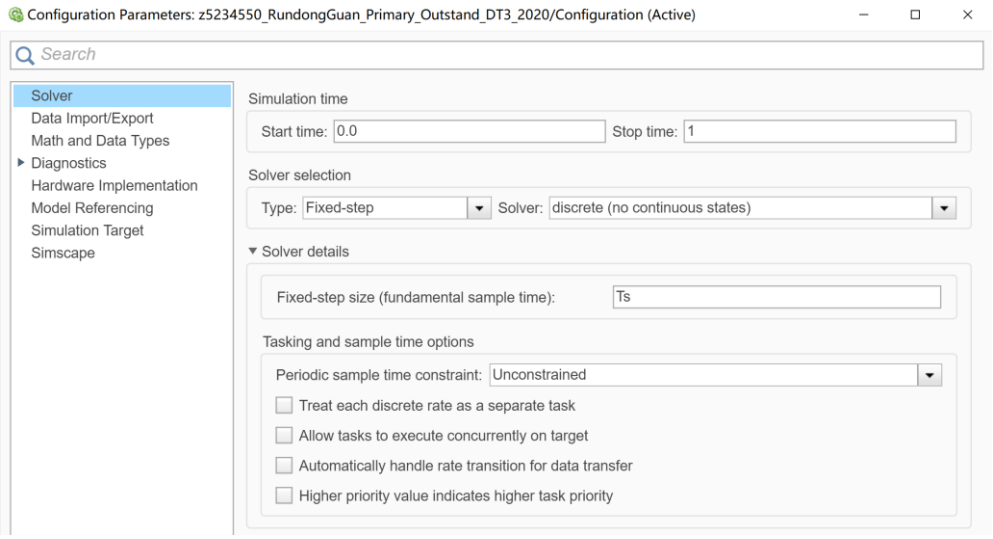

Figure 6. Simulink Configuration Paramaters window.

Then, in your Simscape Solver Configuration, use local solver and set the sample time to be $T_s = 1us$ with Solver type as Backward Euler, which means your circuits minimum time step is 1us as shown in Figure 7 (this is the F(x)=0 block in the Simulink template file).

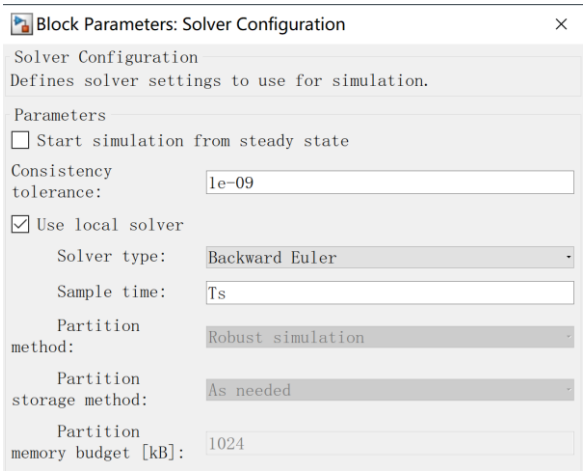

Figure 7. Setting local solver in the Simulink templet file.

For your controller, the minimum time step should be set to $T_{cs} = 100us$, which is 100 times larger than the sample time, T_s, so that the circuit can be regarded as a relatively continuous system.

You can refer to the basic level template Simulink file.

Project Report

Note that the design requirements are very open; there are many solutions to the problem, some good, some not so good. The same can be said about the requirements to the report. It is left for the students to judge what makes up a good design, good supporting simulations, and a convincing report, keeping the following in mind: the report must answer all questions asked and implied in the project description, it must document the work done, and it must show that the authors understand the material.

Note: The draft report must contain at least a close approximation to the final design. Informal notes can provide any remaining details by the time of marking. The draft report must also identify the individual sections written by (or that will be written by) each team member.

Furthermore, requirements to the report include:

- one report per group
- research section
- reasoning for design choices
- inclusion of complete schematic
- inclusion of relevant simulation plots
- calculation of performance measures: At the least, you need calculations for all of the circuit components.

Draft design plan: This serves as a milestone to make sure you are heading in the right direction. This review is compulsory, and must be ticked off either Tue or Fri of Week 9. It should consist of a summary of your current research, possible design choices, as well as a complete system block diagram (including power and peripherals) with Inputs/Outputs labelled.

It is not necessary to have a schematic or full design constructed

--- End of Power Electronics Task ---