[0022]

The outputs of two identical open-drain logic gates are connected together. When both gates output a zero logic level (0 V), the voltage of the output node, V_{OUT} will stablize to:

- (a) Dependent on the capacitive load connected to ground (GND).
- (b) $0\ V \leq V_{OUT} \leq V_{OL}$.
- (c) Dependent on the capacitive load connected to supply (V_{DD}).
- (d) $V_{OL} \leq V_{OUT} \leq V_{OH}$.

The output resistance, R_{OL}, will be the parallel of the output resistances of the two gates connected in parallel, hence lower than each of the them.

Since with either of the gates alone the the output voltage V_{OUT} would not have exceeded V_{OL} by definition, then the lower output resistance due to the parallel of the outputs would also keep V_{OUT} below V_{OL}.

[0008]

The propagation time from input to output for a CMOS NAND gate with 2 inputs when it drives a load capacitance C_L = 0.2 fF is t_P = 200 ps. Which is the propagation time t_P of the gate if it drives 2 inputs of 2 other CMOS NAND gates, which have a total gate capacitance C_G = 0.8 fF?

- (a) 5 times higher.
- (b) depends on the pull-up resistor.
- (c) 800 ps.
- (d) 1.6 ns.

The propagation time is $t_{\mathrm{P}} = 0.69 R_{\mathrm{ON}} C_{\mathrm{L}}$, with R_{ON} the equivalent output resistance of the gate and C_{L} the equivalent load capacitance on the output.

The propagation time t_{P} is proportional to C_{L}. Hence the propagation time increases four times when the load capacitance increases four times.

[0028]

A Look-Up Table with 4 inputs

- (a) Has 4 memory cells.
- (b) Uses 2^4 1-bit memory cells
- (c) Has 512 memory cells.
- (d) Has 2^8 memory cells.

Four input can address at most $2^4 = 16$ memory cells.

[0033]

The conversion time of a flash ADC:

- (a) Is proportional with the number of bits on output, N.
- (b) Is independent on the input signal level.
- (c) Depends as 2^N on the number of the bits in output, N.
- (d) Depends as log N on the number of the bits in output, N.

Flash ADCs make all the comparisons with the levels in parallel, hence independent on the number of output bits, N, or the input signal level.

[0007]

A half-wave rectifier supplied with 220 V and 60 Hz has an output capacitor of 1000 µF.

What is the maximum current consumed by the load I_L = ____ mA that ensures the ripple on the output voltage is at most 3%?

How does the ripple amplitude change if the load current remains unchanged but the input voltage increases by 50%?

- ○ decreases by 50%
- ○ doubles
- ○ unchanged
- ○ increases by 50%

The amplitude of the ripple voltage is:

$$V_\mathrm{R} = \frac{I_\mathrm{L}\Delta t}{C}$$

in which Δt is $\frac{1}{60\ \mathrm{Hz}}$ for half-wave rectifiers.

Without load, the peak voltage on the output is $220\ \mathrm{V} \cdot \sqrt{2} = 311\ \mathrm{V}$ of which V_R should be at most 3 %.

Hence, $I_\mathrm{L} = 1000 \cdot 10^{-3}\ \mathrm{F} \cdot 220\ \mathrm{V} \cdot \sqrt{2} \cdot 3\ \% \cdot 60\ \mathrm{Hz} = 560\ \mathrm{mA}$

The ripple amplitude does not depend on the input voltage amplitude, provided that the load current remains the same.

[0024]

All DDR4 DRAM memories transfer at most:

- (a) 4 bytes on each bus clock cycle.
- (b) 1 word on each bus clock transition.
- (c) 2 words on each bus clock transition,
- (d) 1 word on each bus clock cycle.

Double datat rate (DDR) DRAM memories transfer two words per bus clock cycle, or one word for each bus clock transition.

[0023]

The steady state voltage on a transmission line:

- (a) Can depend on the output resistance of the driver.
- (b) Does not depend on the termination resistance of the line.
- (c) Is independent on the output resistance of the driver.
- (d) Depends on the characteristic impedance of the line, Z_{∞}.

The steady state voltage of a transmission line depends on the output resistance of the driver in the cases where there is a steady-state current over the line due to termination resistance.

The steady state voltage of a transmission line also depends on termination resistance of the line when it is connected to a voltage different than the steady state voltage on the line.

The steady state voltage of a transmission line is independent on the characteristic impedance of the line.

[0031]

A parasitic series resistance of the inductor of a buck-boost dc-dc converter:

- (a) Increases the power dissipated by the switches.
- (b) Increases the active power dissipated by the capacitors.
- (c) Decreases the switching frequency.
- (d) Dissipates power in the inductor.

A parasitic series resistance of the inductor of a buck-boost dc-dc converter dissipates power due to the current that crosses the inductor. The switching frequency is provided independently by an external circuit. Ideal capacitors and switches do not dissipate active power.

Given the memory in Figure 1:

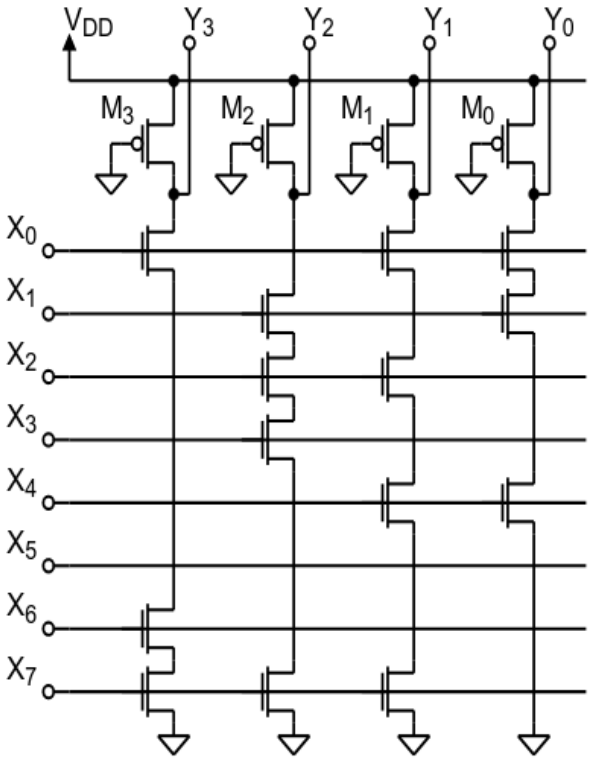

Figure 1.

1. What is the memory type?

○ FLASH ○ ROM NAND ○ ROM NOR ○ EEPROM

2. What is the purpose of the signals Y_0–Y_3?

○ Address lines ○ Bit lines ○ Preload lines ○ Word lines

3. What is the purpose of the signals X_0–X_7?

○ Word lines ○ Preload lines ○ Bit lines ○ Address lines

4. What is the function of transistors M_0–M_3?

○ Precharge ○ Differential reading ○ Pull-down ○ Pull-up

5. How many words are stored in the memory?

○ 8 ○ 4 ○ 32 ○ 7

6. How many bits are stored in the memory?

○ 8 ○ 14 ○ 18 ○ 32

7. What is the binary value stored at address 5 in the memory?

The memory is a ROM of type NAND.

The Y signals are bit lines.

The X signals are word lines, active high.

The M transistors are used as pull-up resistors for the bit lines.

Each word line controls a word of the memory. Hence there are eight words stored in the memory.

Each word has four bits, as many as the bit lines Y. Hence, the memory stores $8 \cdot 4 = 32$ bits.

Address 5 of the memory is controlled by the word line X_5. When this lines becomes active (high), all bit lines remain connected to the ground (0 V), hence the binary value stored on address 5 is 0000.