Applied Electronics

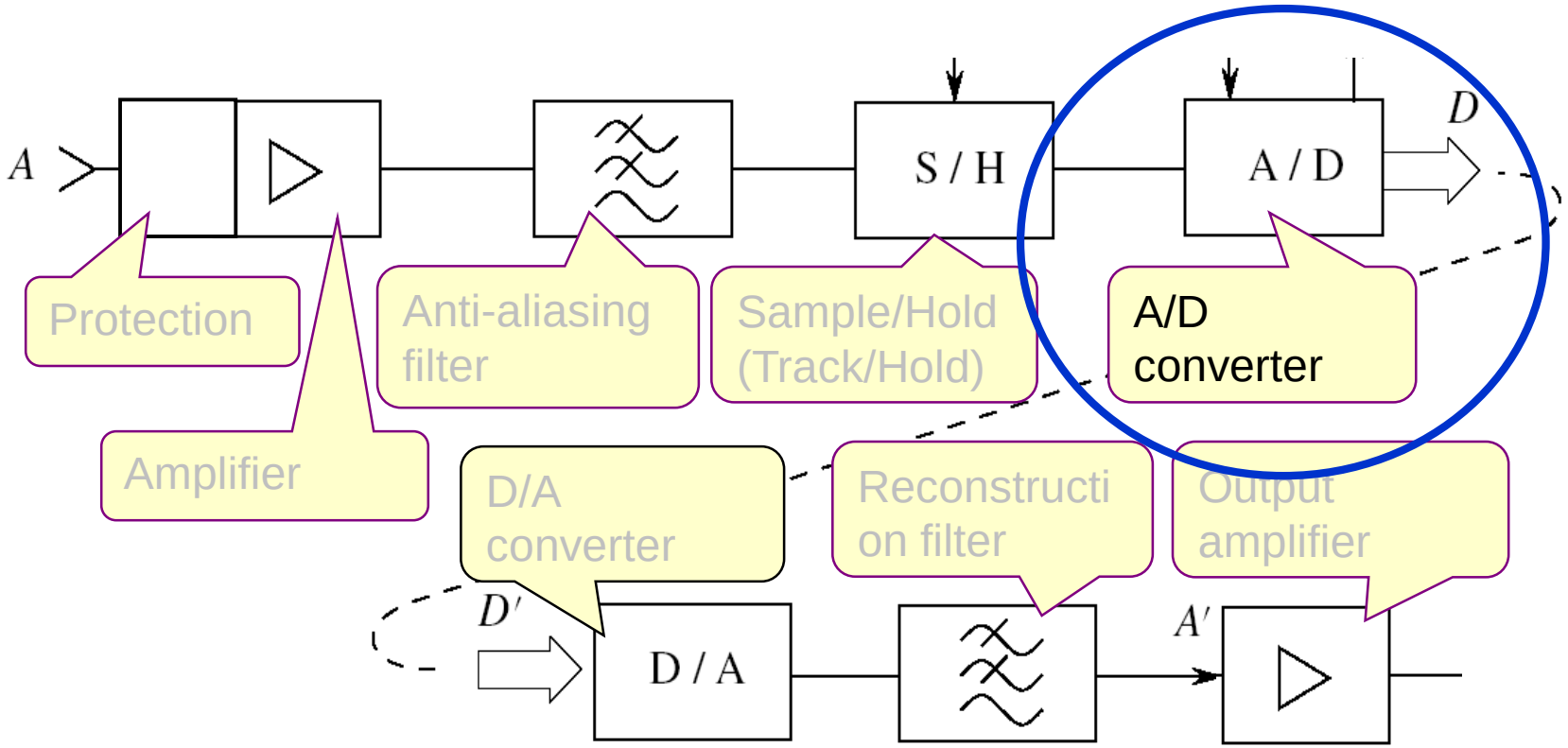
A/D Converters

Errors in A/D Converters

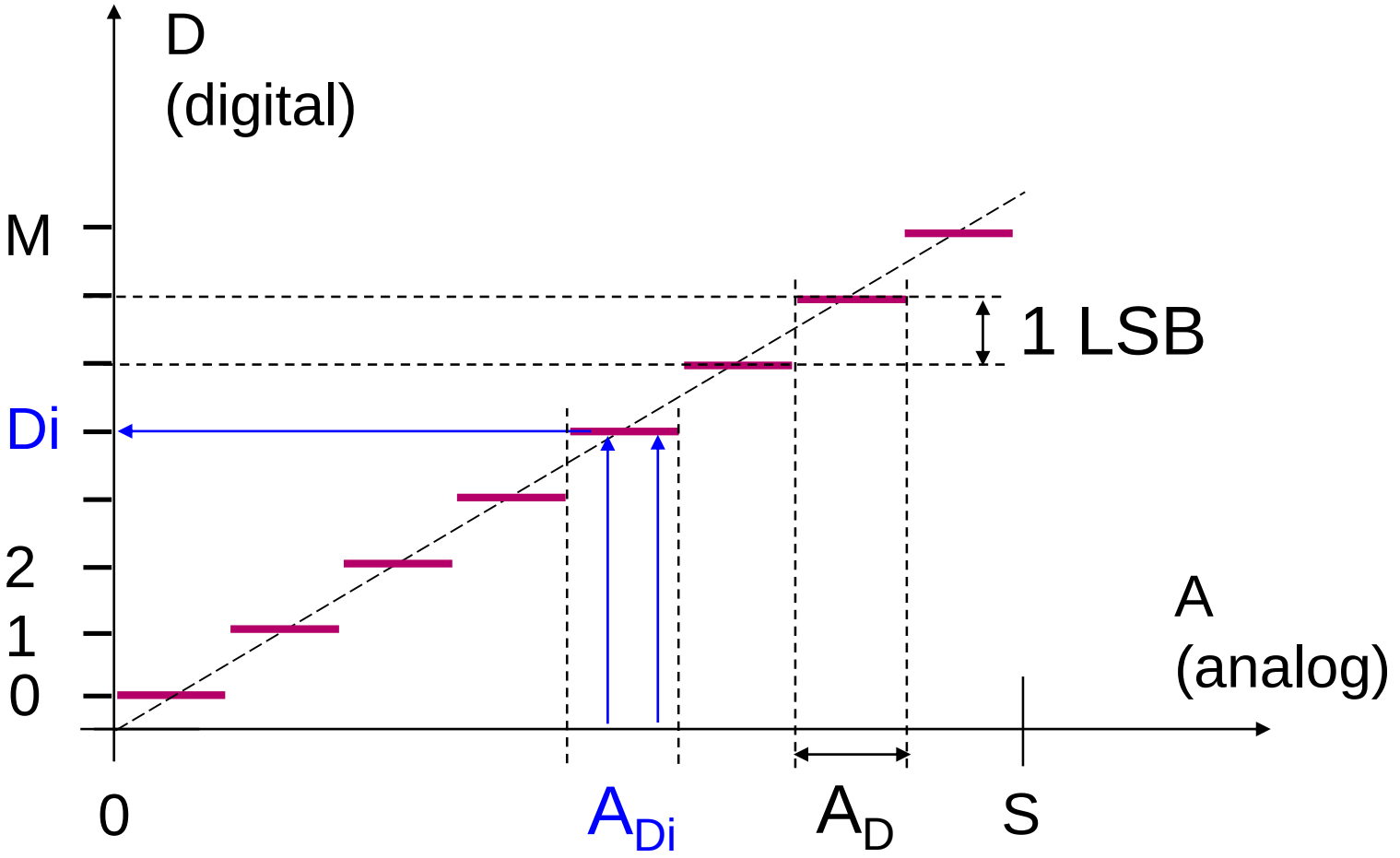
- Dual transfer function vs D/A
  - X axis: analog values (continuous)
  - Y axis: numeric values (discrete)

- Each A_{Di} interval corresponds to a D_i value
  - "stair" transfer function
  - If N is large, the transfer function looks like a continuous line
  - Same error classification as D/A
    - Linear: offset and gain
    - Nonlinearity: differential and integral
    - Dynamic parameters

A/D Converters



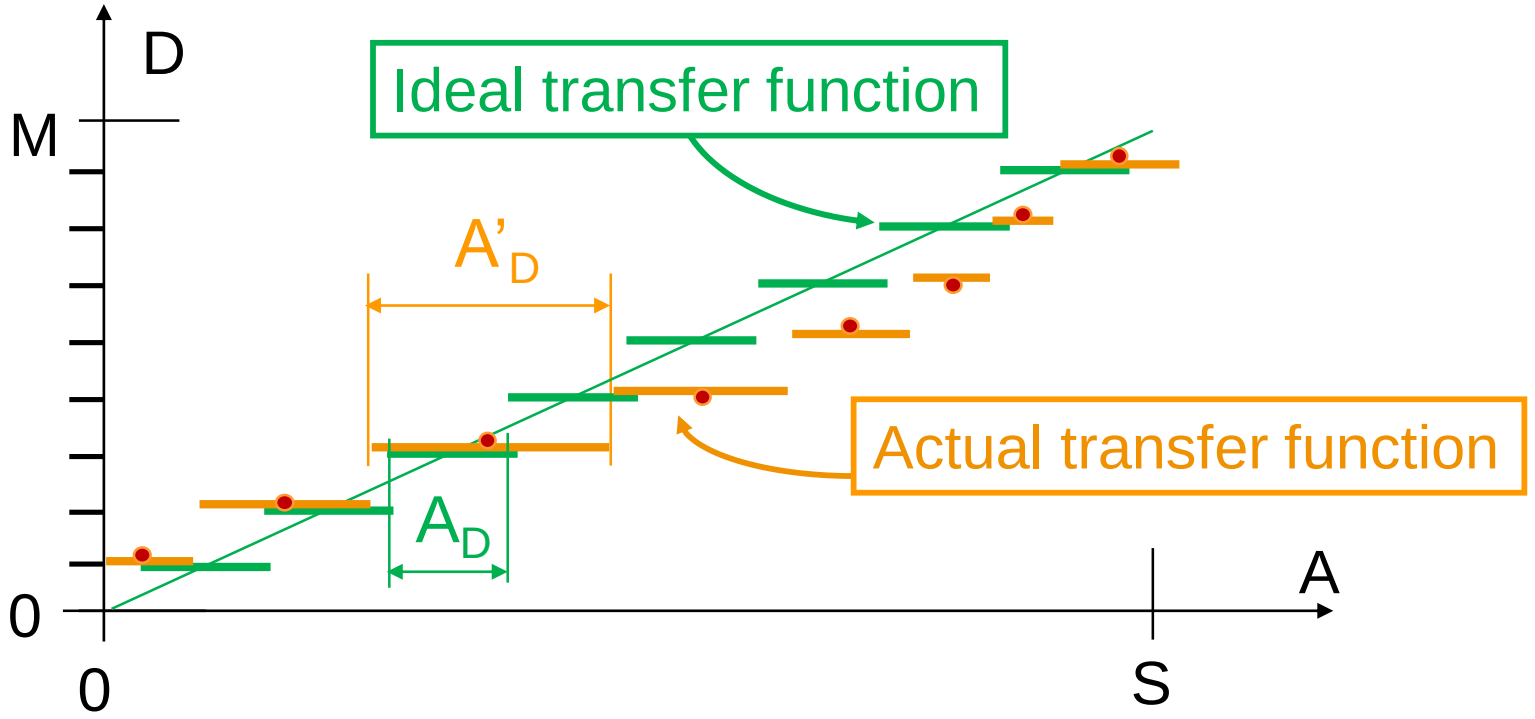
Ideal A/D Transfer Function



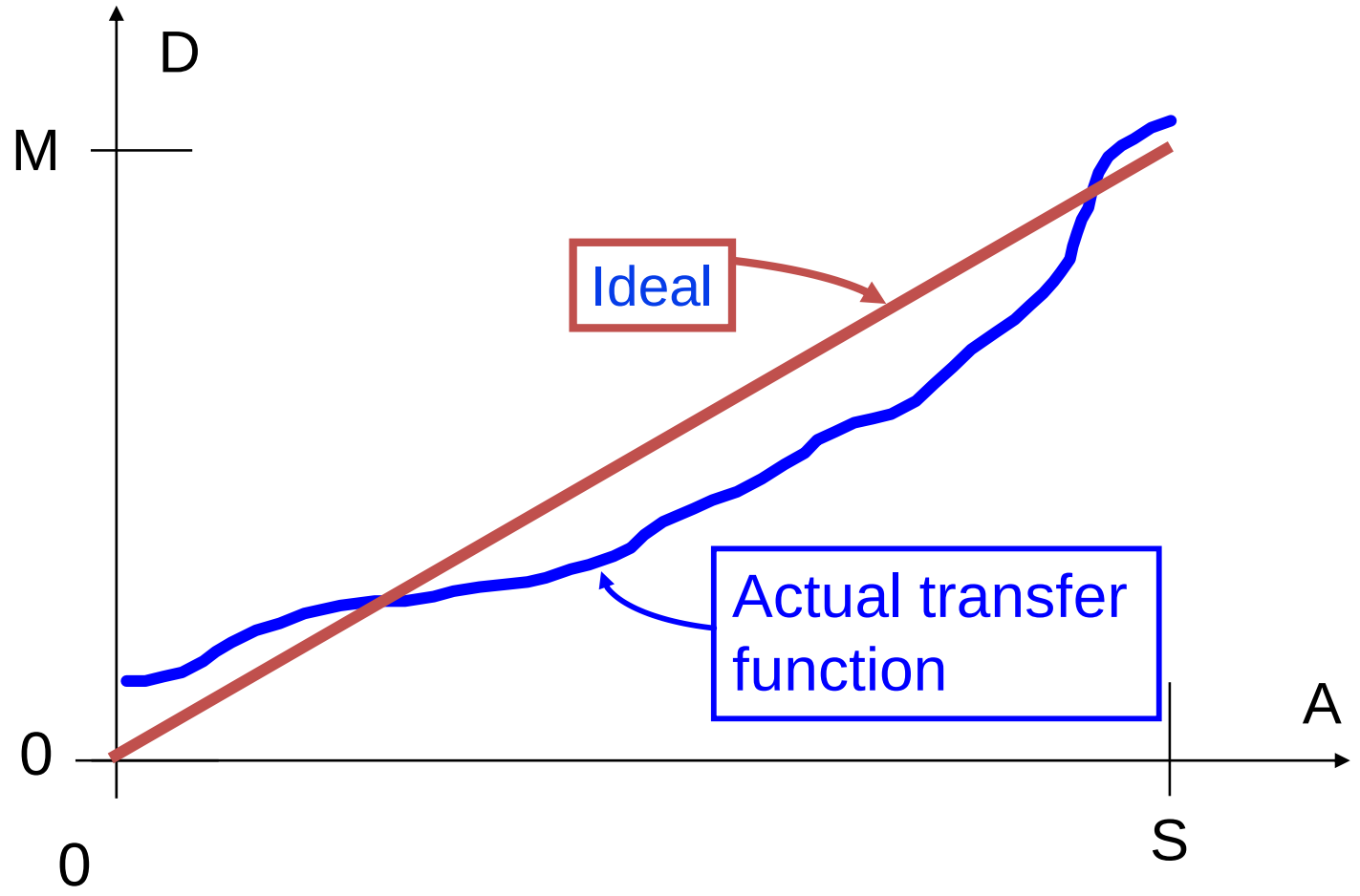
Static Errors: Two-Steps Analysis

- Real transfer function is not linear
  - Find the best approximating line of the real transfer function
- Compare the ideal and the real characteristics in 2 steps
- Real transfer function → best approximating line
  - Nonlinearity errors: integral and differential
- Best approximating line → ideal transfer function
  - Linear errors: offset and gain

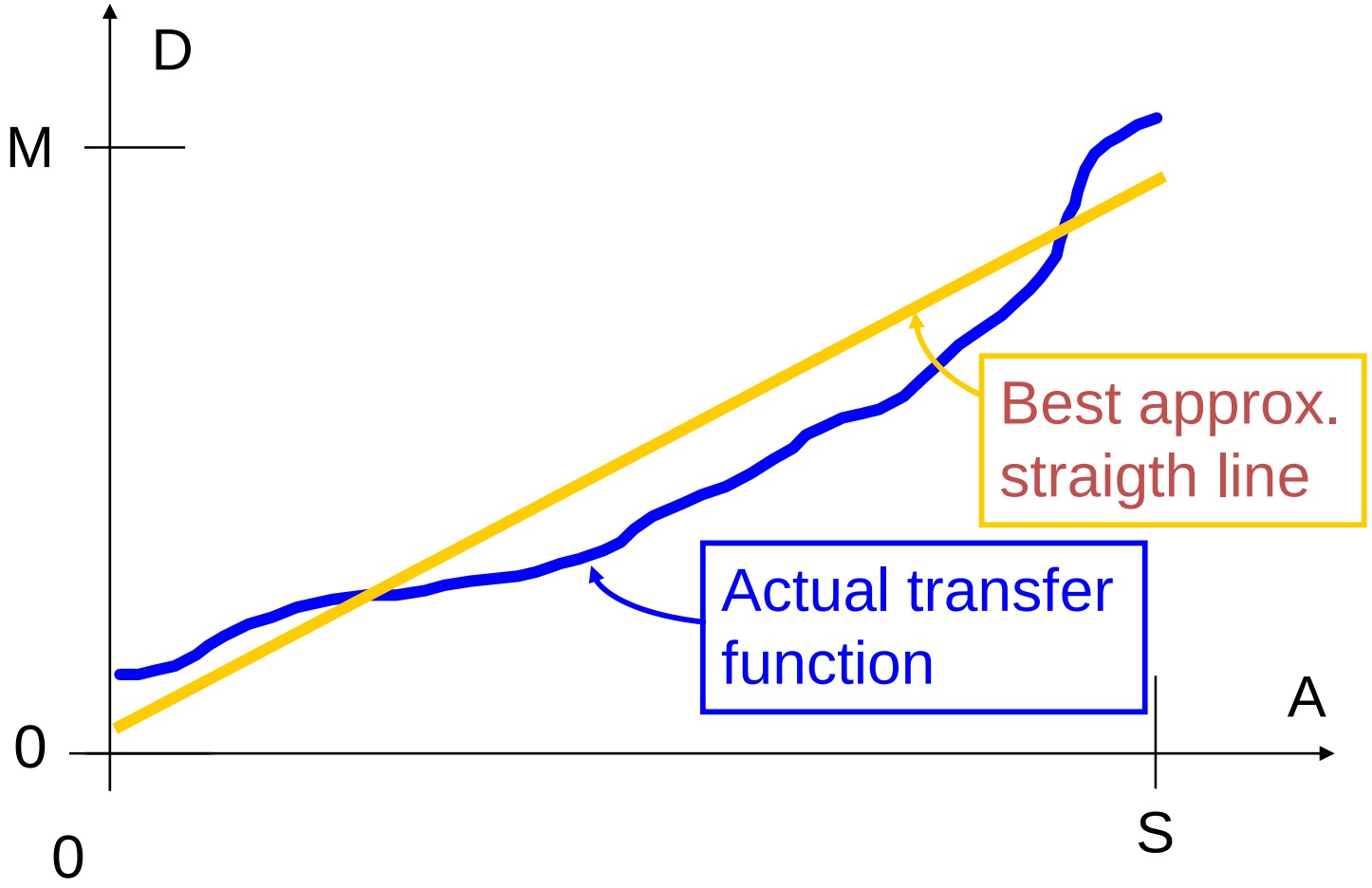
ADC Ideal and Real Transfer Functions



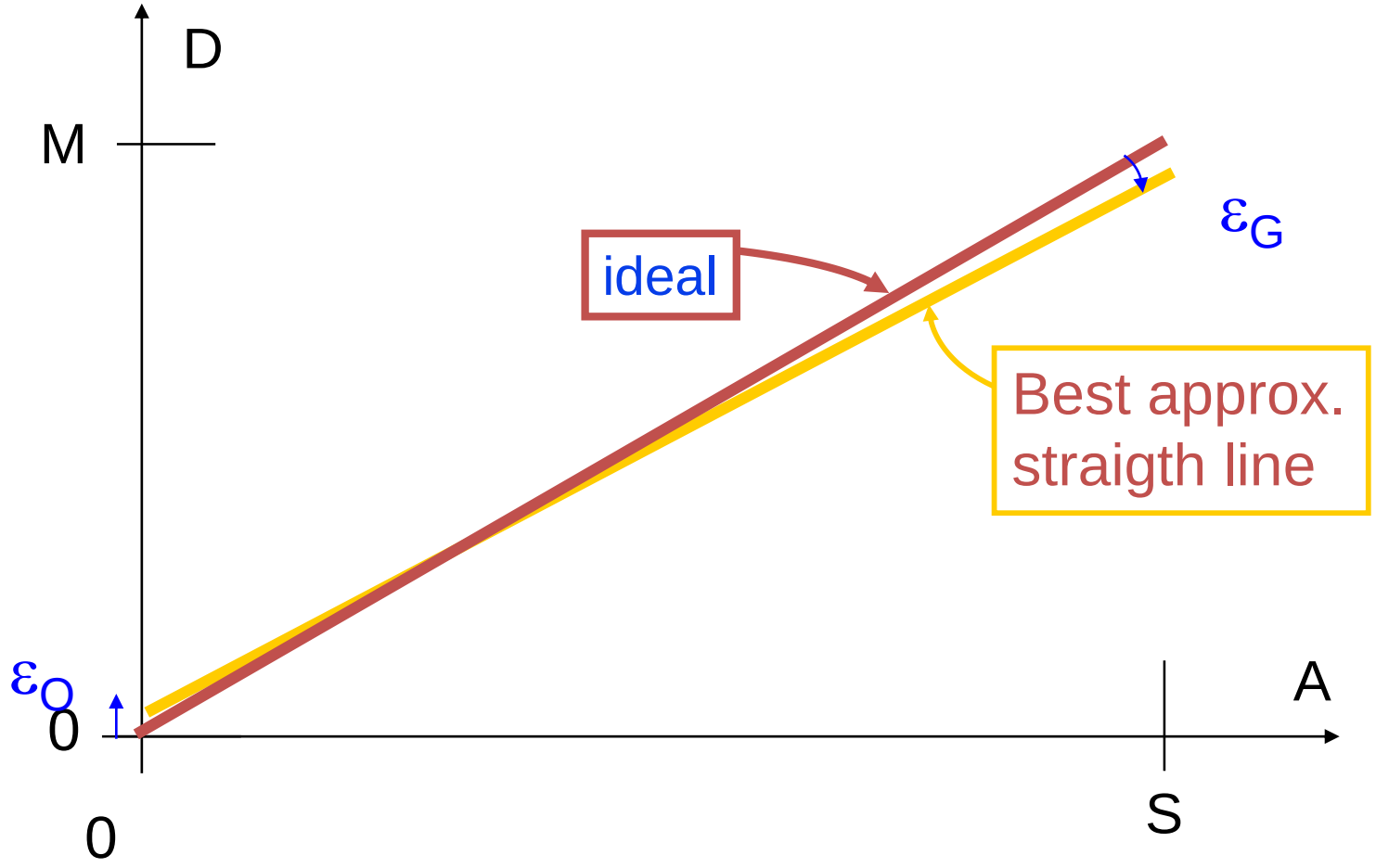
Actual vs Ideal Transfer Functions



Best Approximating Line

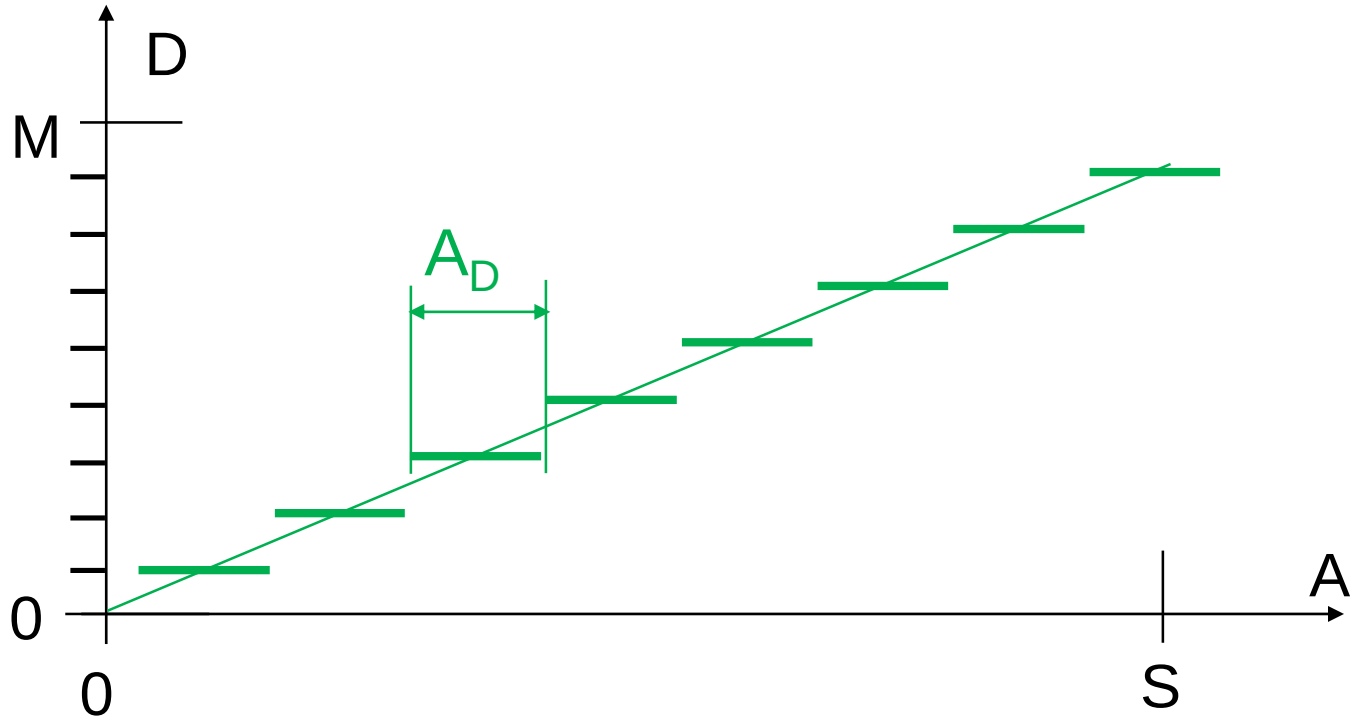


Linear Approx. vs Ideal Transf. Function



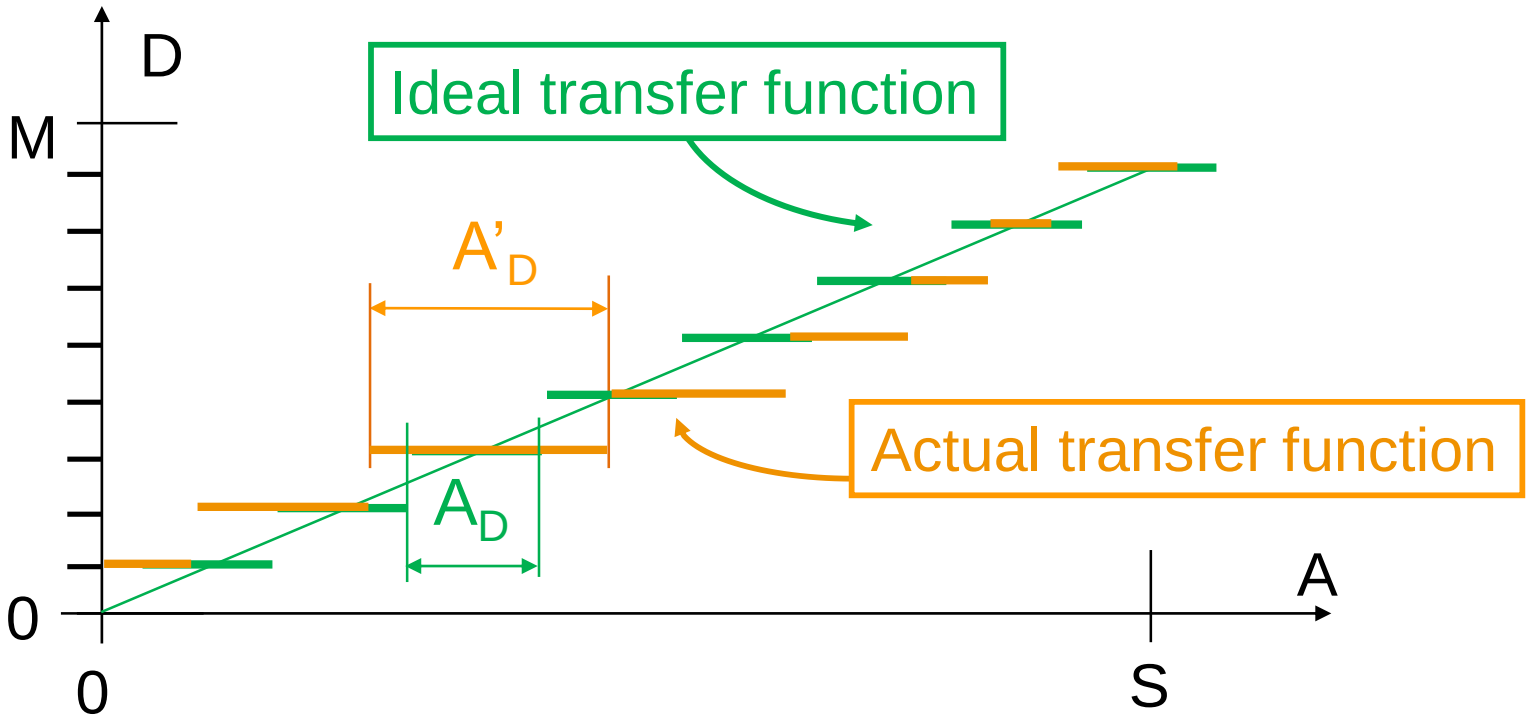
Ideal A/D Transfer Function

- Uniform quantization
  - All quantization intervals A_D have the same amplitude



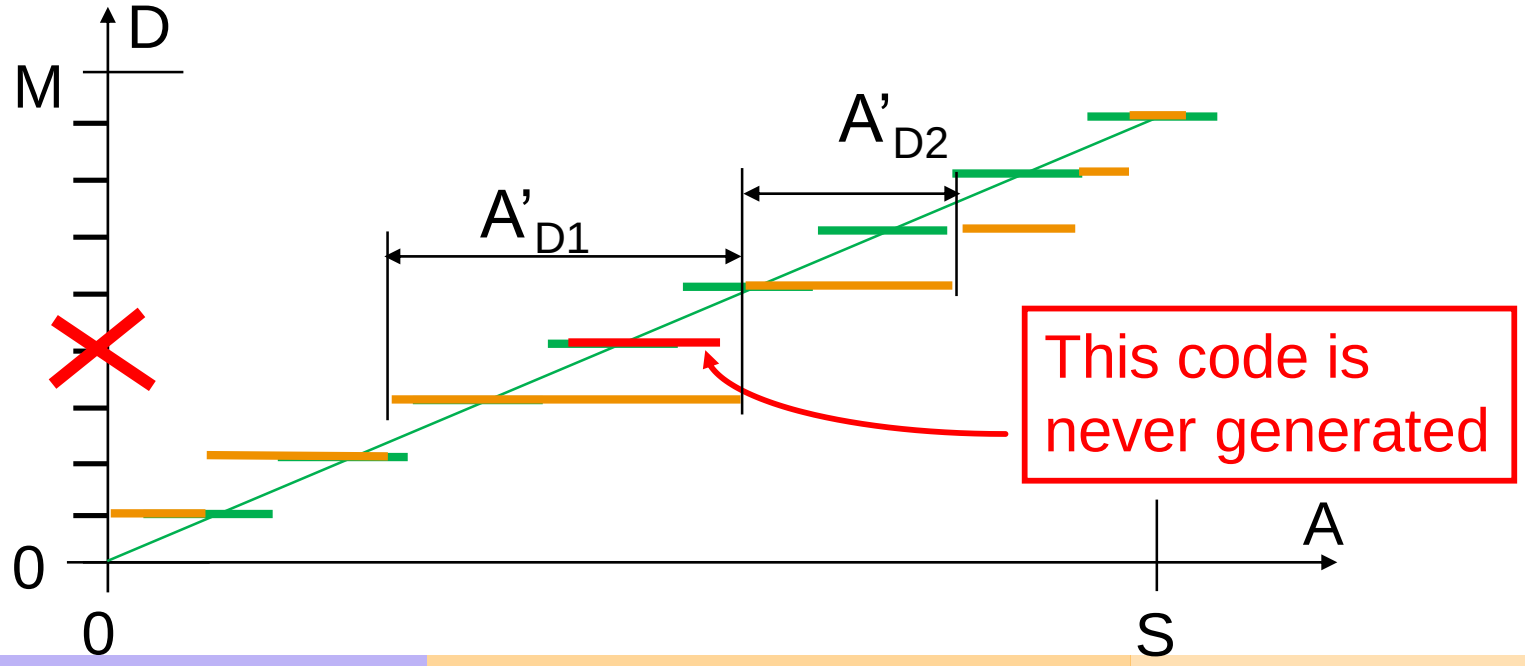
Differential Nonlinearity Error

- Actual quantization intervals: $A'_{\mathrm{D}} \neq A_{\mathrm{D}}$
  - Differential nonlinearity: $\varepsilon_{\mathrm{dnl}} = A_{\mathrm{D}} - A'_{\mathrm{D}}$

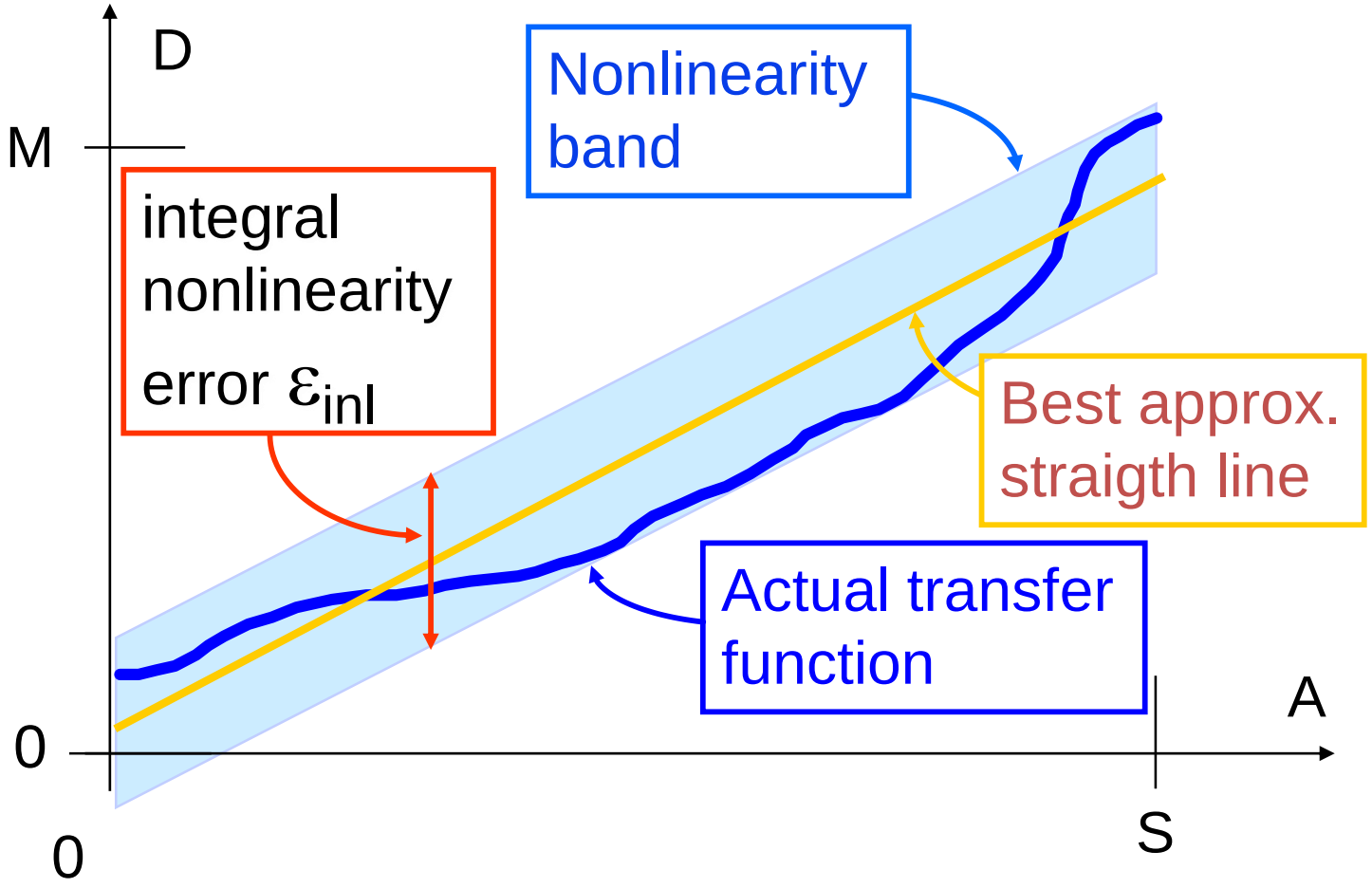


Missing Code Error

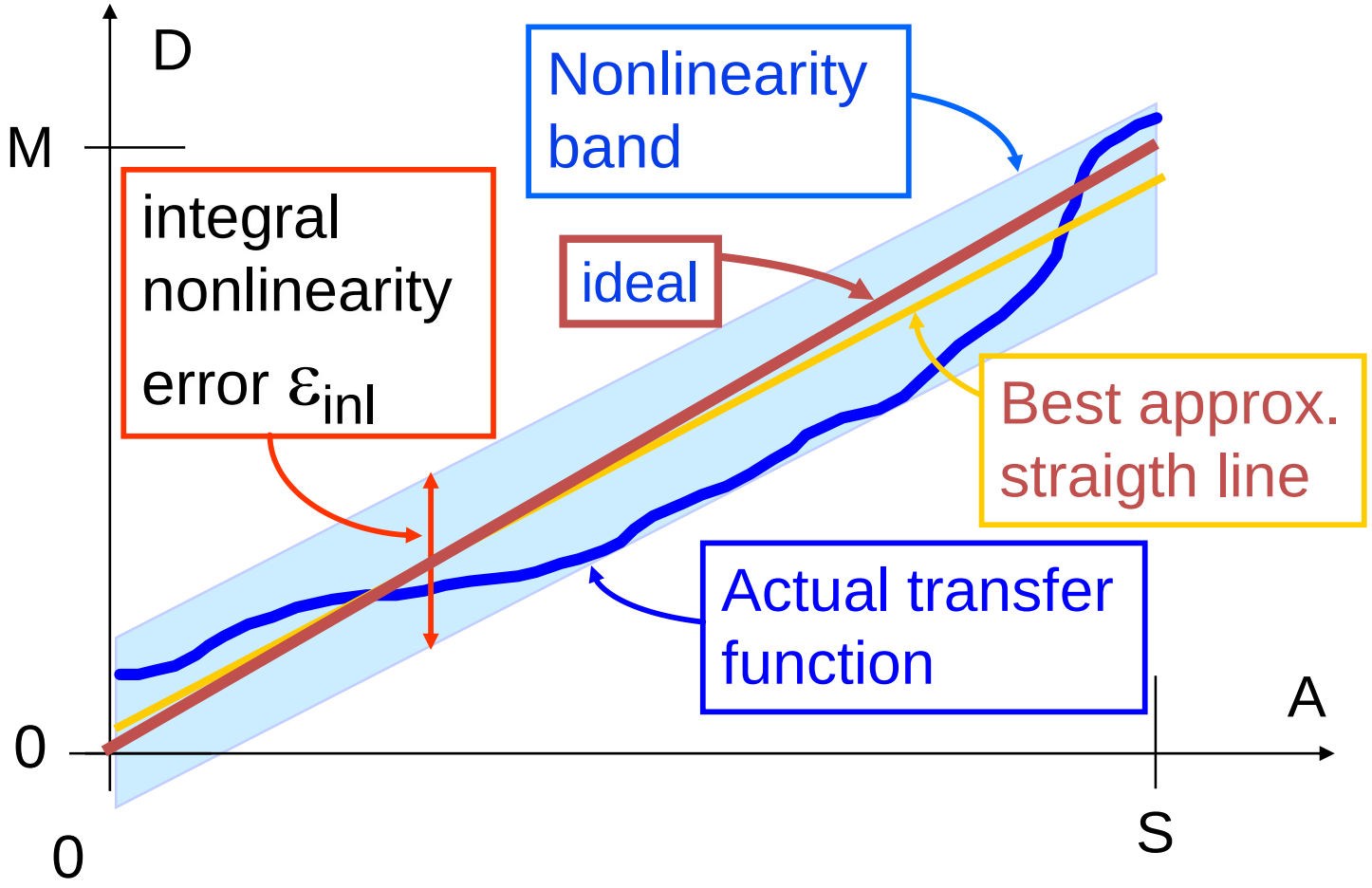
- Wide intervals reduce adjacent ones
- Very wide intervals can suppress adjacent ones
  - Missing code error: $\varepsilon_{dnl} > 1$ LSB



Integral Nonlinearity Error



Full View


D
M
integral
nonlinearity
error ε_{inl}
Nonlinearity
band
ideal
Best approx.
straigth line
Actual transfer
function
A
0
0
S

Linear and Nonlinear Errors

- Offset error
  - Shift of the output
- Gain errors
  - Rotation of the transfer function
- Both can be compensated with gain and offset corrections in the signal chain
- Integral nonlinearity error ε_{inl}
  - Depends on single points
  - Cannot be compensated

ADC Error Summary

- Linear errors
  - Gain: $\mathcal{E}_{\mathrm{G}}$ Offset: $\mathcal{E}_{\mathrm{O}}$
- Nonlinearity errors
  - Integral nonlinearity: $\mathcal{E}_{\mathrm{inl}}$ Differential NL: $\mathcal{E}_{\mathrm{dnl}}$
- Dynamic parameters
  - Conversion time: T_{C}
  - Tracking rate: $\mathrm{d}V/\mathrm{d}t$

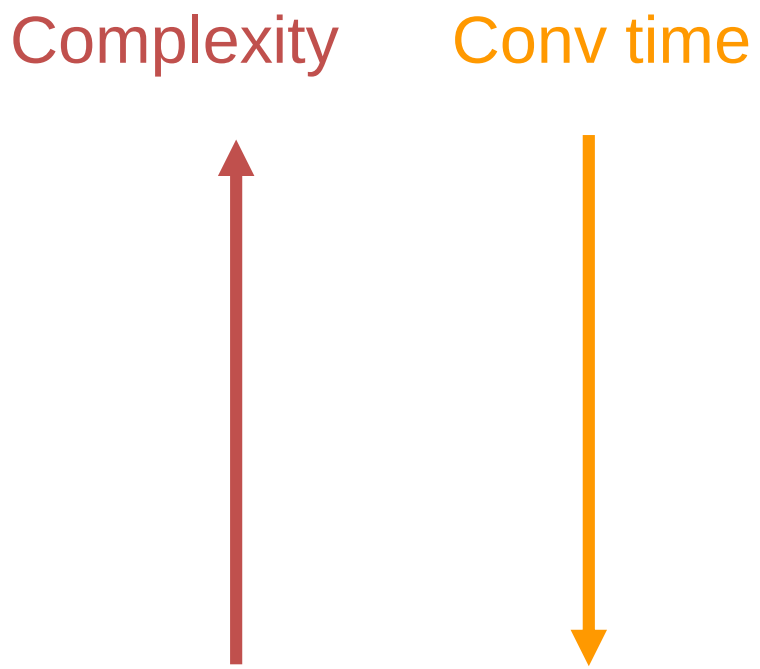
Dynamic Parameters

- A to D conversion takes time Tc
- In most cases
  - The ADC receives a “Conversion Start” (CS) command
  - After Tc, the ADC raises an “End Of Conversion” (EOC) flag
- Some ADC can follow a (slowly) changing signal
  - Tracking converters
  - Dynamic behavior specified by max track rate (Slew Rate)

A/D Converter Architectures

- Various types of ADC, which can be classified into
  - Complexity
    - Number of comparators in the circuit
    - Simpler if few comparators
  - Conversion time *T*c
    - Or conversion rate, *F*c, inverse of *T*c
    - Better if low *T*c (high speed, high *F*c)
- Linked parameters
  - High speed converters are more complex
  - High speed and high resolution are expensive

A/D Converters Classification



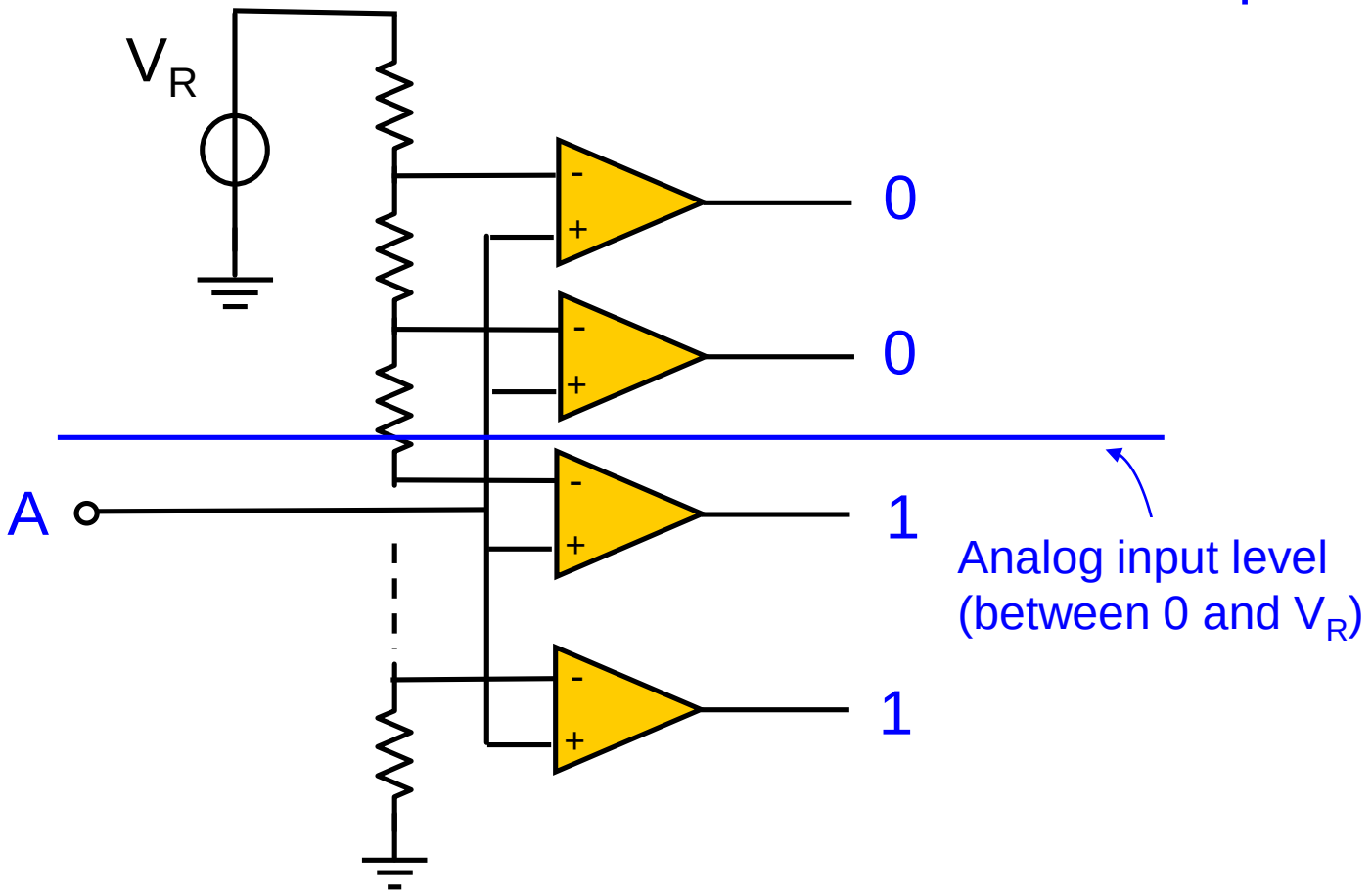
- Parallel (flash)
- Successive approximation
- Tracking, ramp

Complexity: number of comparators

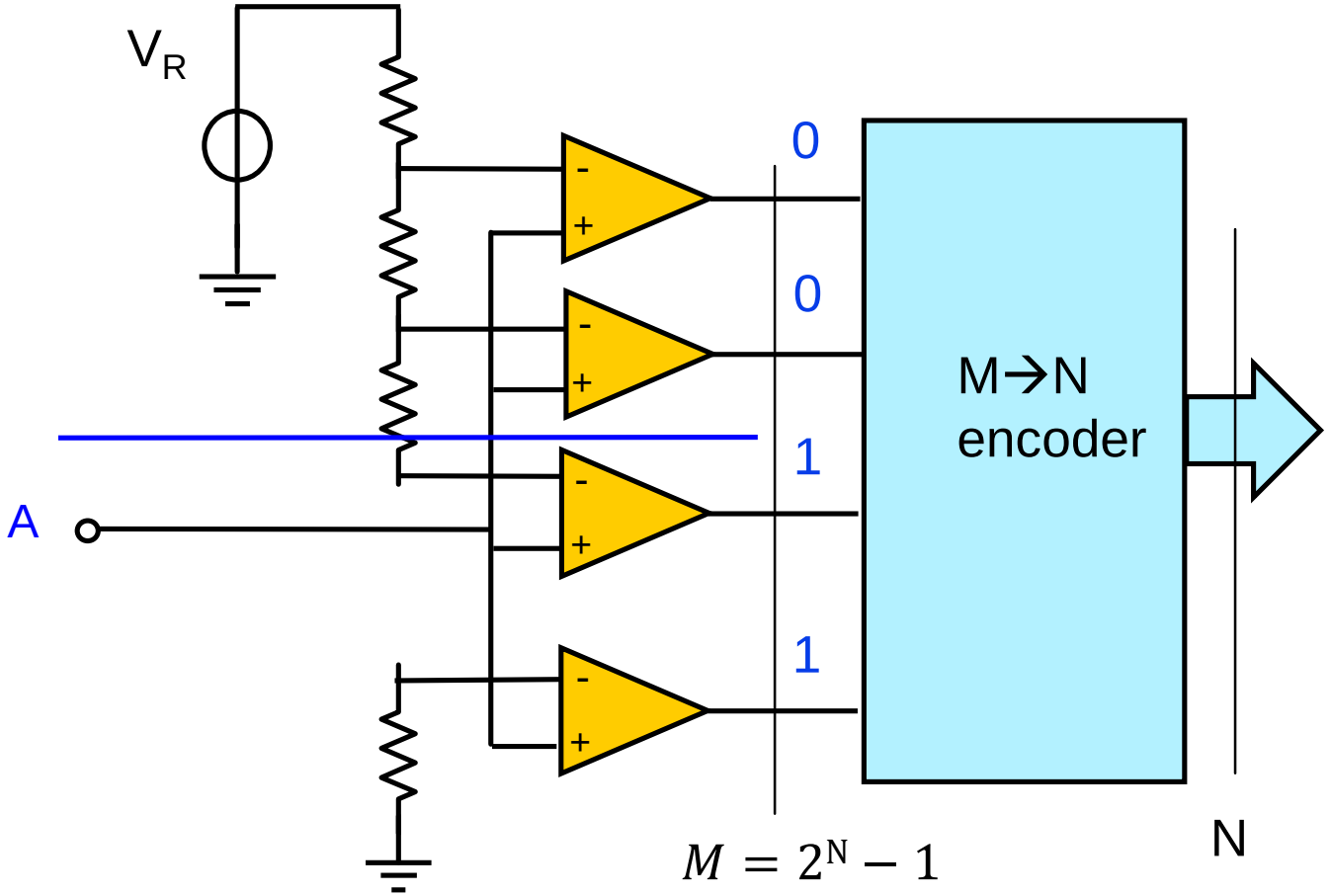
Conversion time: *T*c

Parallel (Flash) ADC

thermometric or linear output coding



Flash ADC with Coded Output

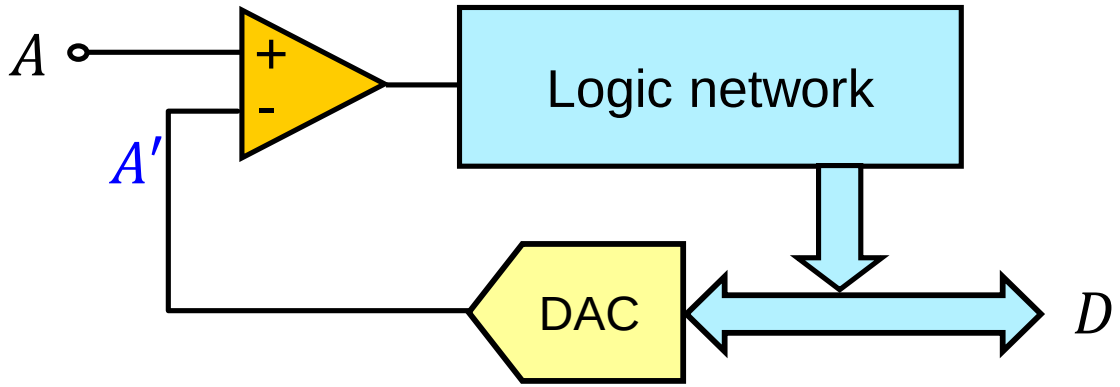


Flash Converter Parameters

- 2^N comparators $(2^N - 1)$
- 1 comparison cycle for N bits
- Fast
  - All comparators operate at the same time
- Complex
  - Requires many comparators

DAC – Feedback Converters

- A logic network builds an approximation A' of the input A using results of $A \leftrightarrow A'$ comparison
  - A' is obtained from D through a DAC
  - D is the numeric representation of A



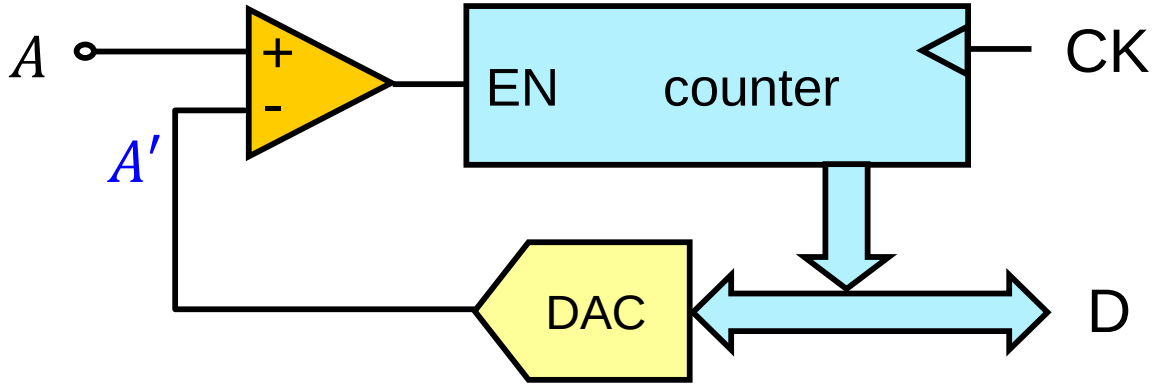
Feedback Converters Algorithms

- Logic network modifies D until A' approximates best A
- Two procedures
- In incremental steps, of one LSB each
  - Tracking converters
  - 2^N steps for a full-scale change
  - Maximum conversion time: $T_{\mathrm{C}} = 2^N \, T_{\mathrm{CK}}$
- One bit at a time, starting from the MSB
  - Successive approximation converters
  - Always N steps, for any conversion: $T_{\mathrm{C}} = N \, T_{\mathrm{CK}}$

LSB Steps: Staircase Converter

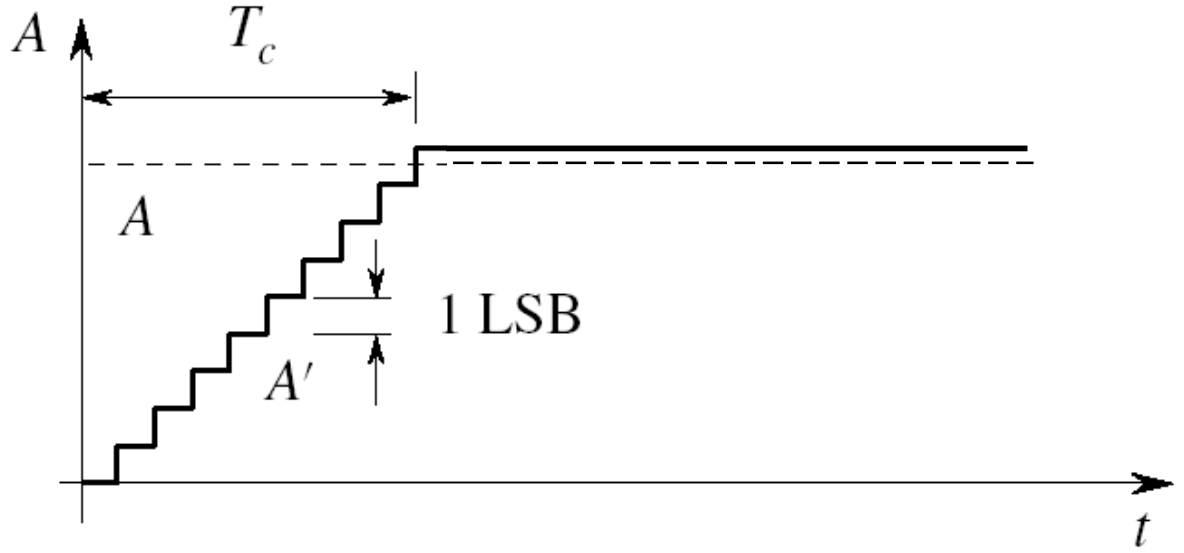
- Counter with enable
  - If A’ < A , EN = 1 (counter enabled)
  - If A’ > A , EN = 0 (counter disabled)

- Max $M = 2^N$ steps to search from 0 to S: $T_C = 2^N T_{CK}$



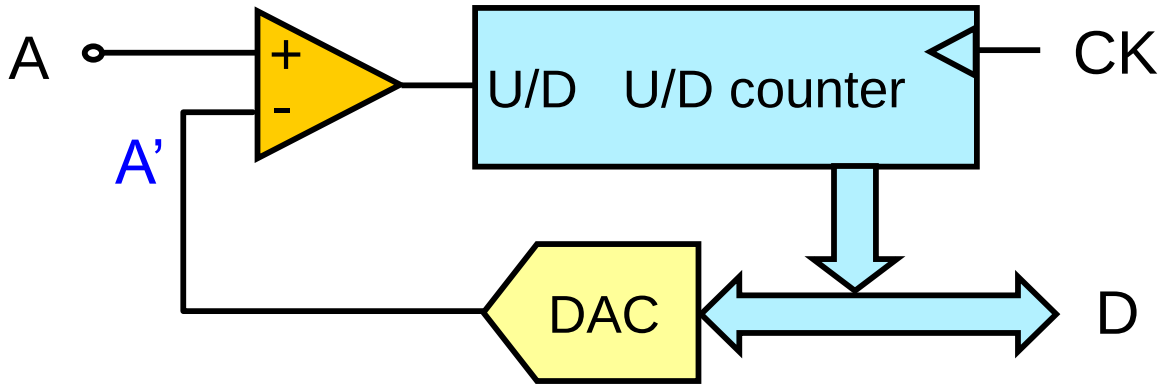
Staircase ADC Operation

- While A' < A, EN = 1 and the counter is enabled
- The feedback signal A' goes up 1 LSB at each T_{CK}
- When A' > A, the comparator disables the counter → A' stops
- Max conversion time: T_{Cmax} (change A' from 0 to S) = $2^N T_{CK}$
- Reset counter to 0 to start a new conversion



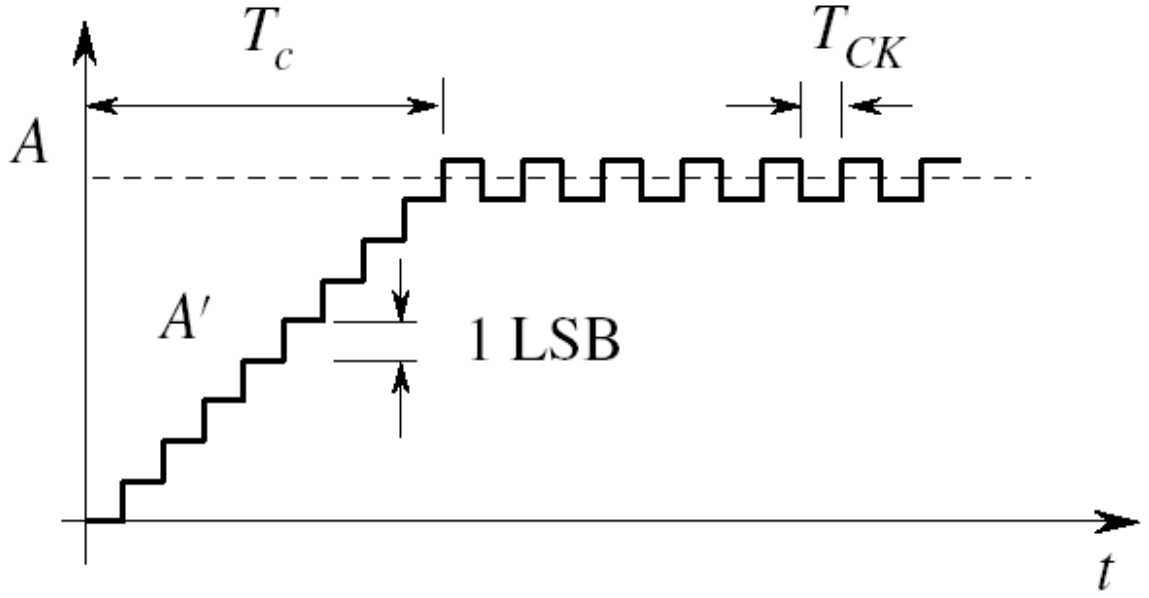
LSB Steps: Tracking Converter

- Up/Down counter
  - If A' < A , D = D + 1
  - If A' > A , D = D – 1
- M = 2^N steps from 0 to S: $T_C = 2^N T_{CK}$



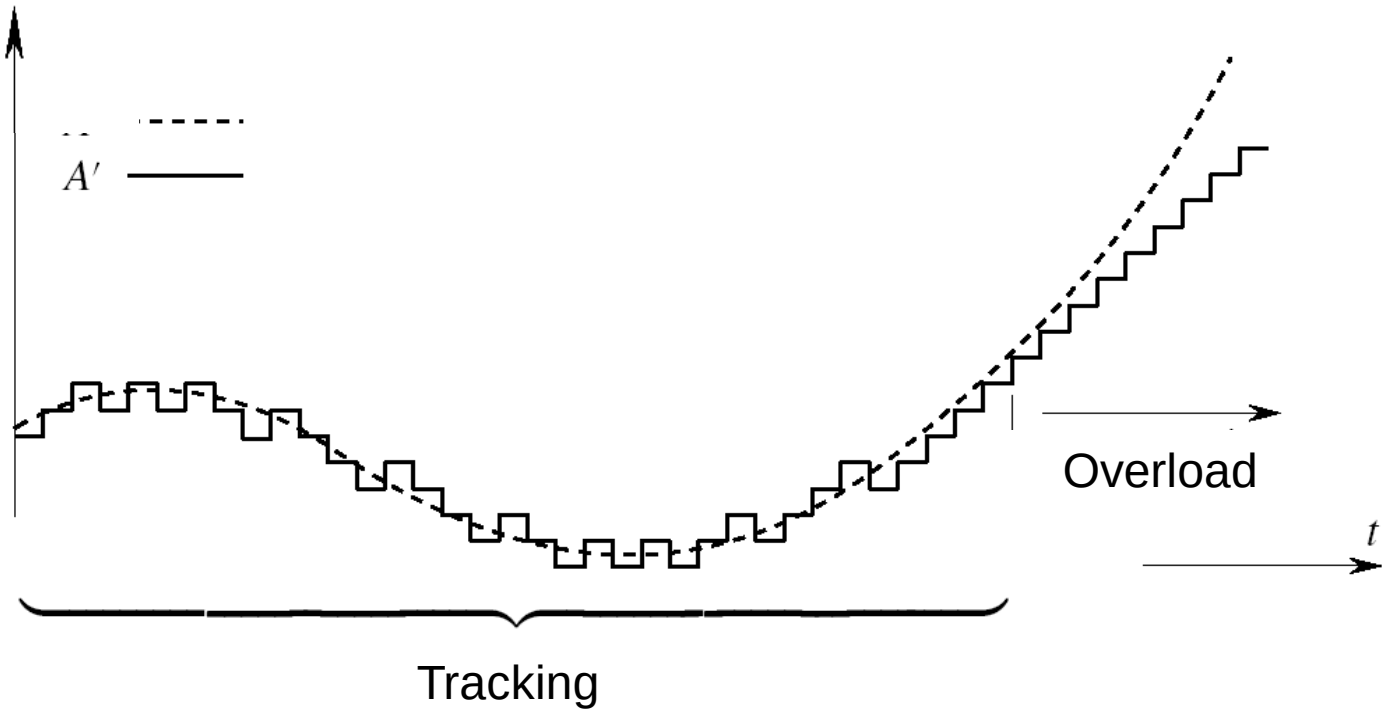
Tracking Converter: Constant Signal

- While A' < A, the counter counts up 1 LSB each CK period
- A' moves 1 LSB up for each T_{CK}
- When A' > A, the counter reverses the counting direction (down)
- Max conversion time: T_{Cmax} (A' from 0 to S) = $2^N T_{CK}$
- No need to reset the counter for a new conversion



Tracking Converter: Changing Signals

- The converter can track signals with $\frac{\mathrm{d}V}{\mathrm{d}t} < \frac{A_\mathrm{D}}{T_\mathrm{CK}}$

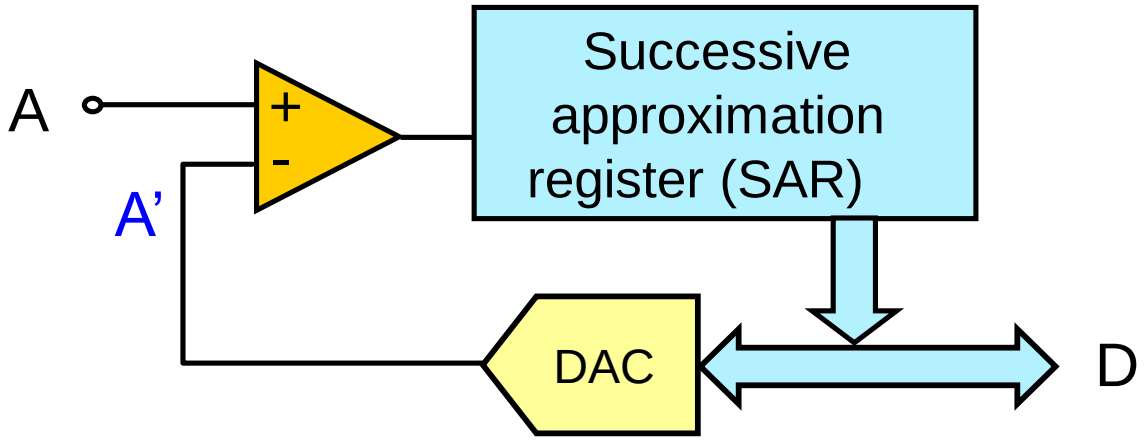


Tracking Converter Main Features

- 1 comparator
- Worst case: 2^N comparison cycles for N output bits
- Slow
  - Fully sequential decisions
  - Limited $\frac{\mathrm{d}V}{\mathrm{d}t}$ tracking capability
- Simple
  - Requires a single comparator

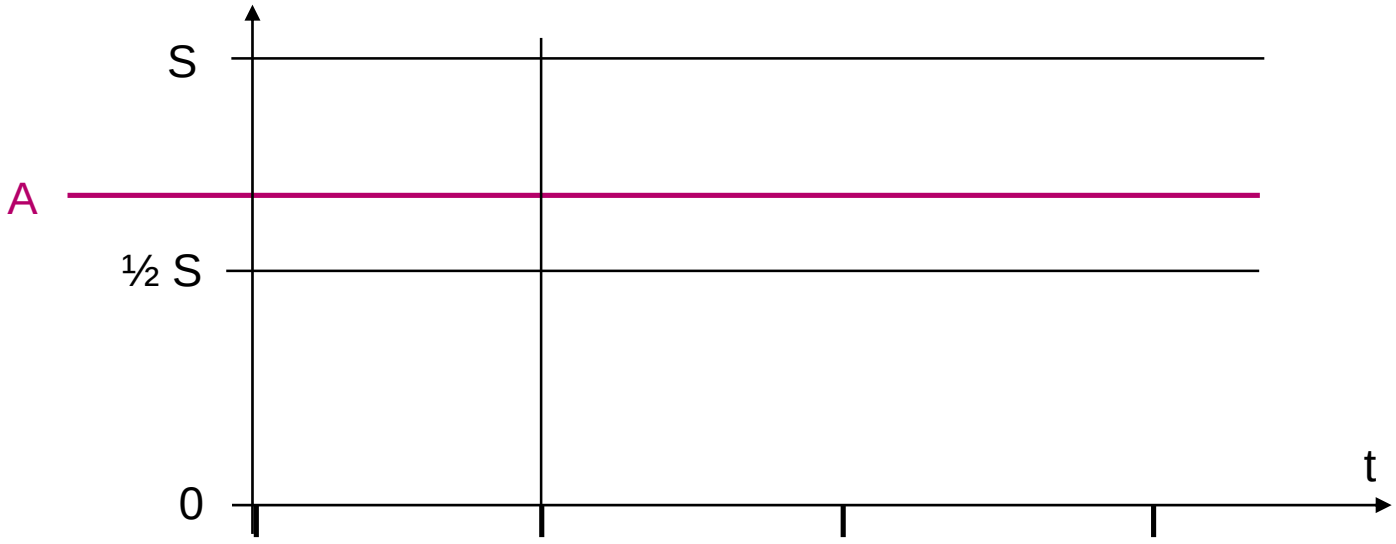
Start With MSB: Successive Approx. ADC

- Input signal compared to *S*/2: result → MSB
  - If MSB = 0: threshold for next comparison = ¼ S
  - If MSB = 1: threshold for next comparison = ¾ S
- Input signal compared to threshold: result → MSB–1
  - …



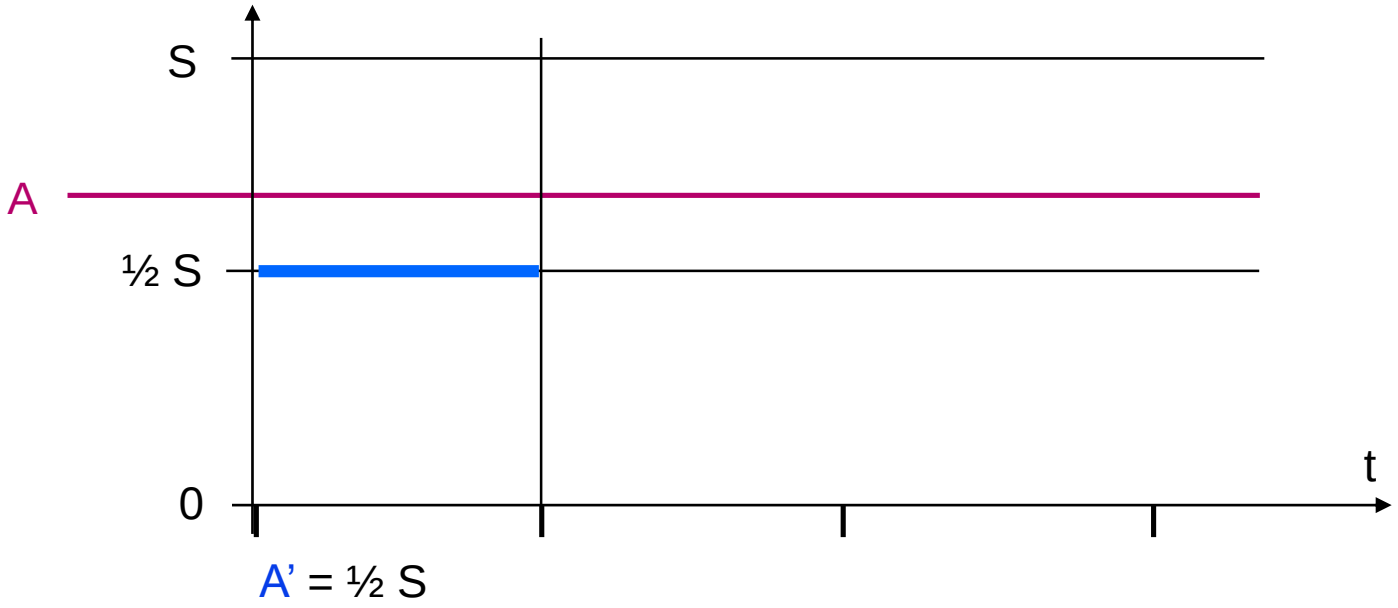
Approximation Sequence

- Input signal A



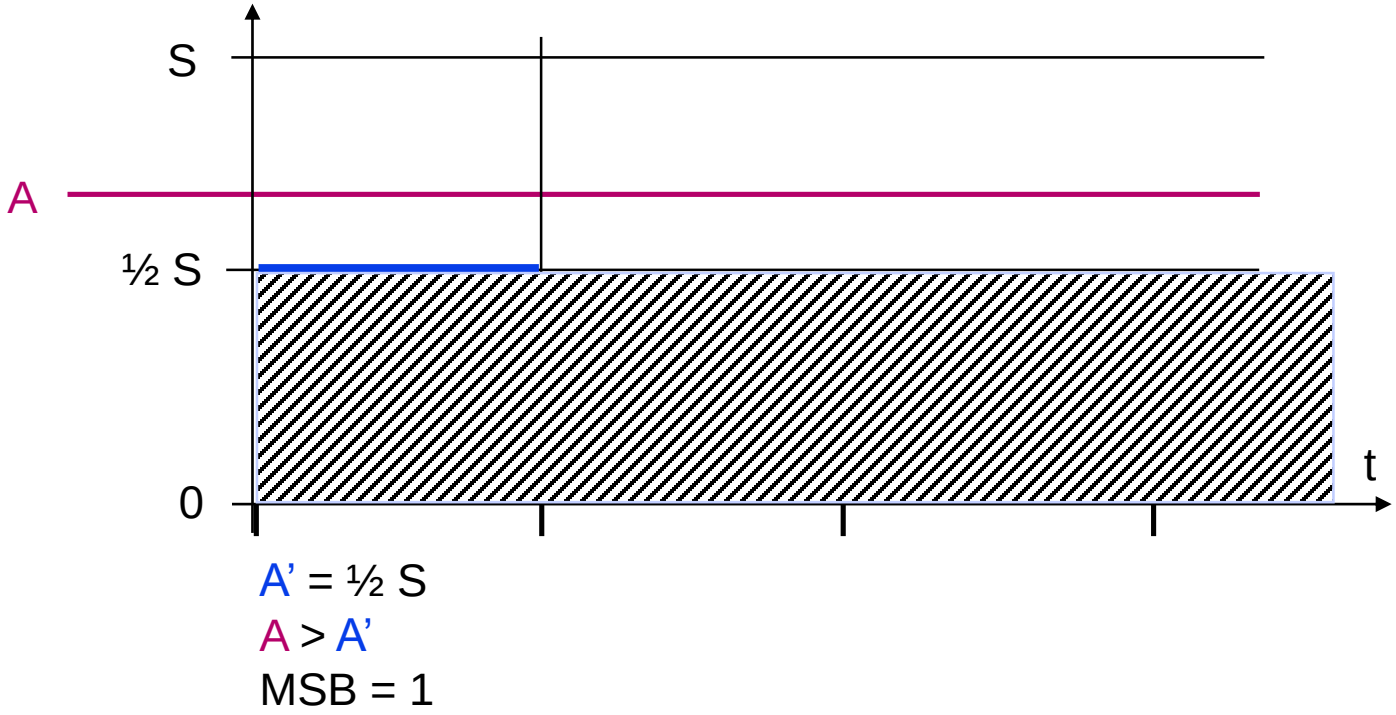
Approximation Sequence

- *A* is compared to *S*/2
  - *A*' becomes ½ *S* by setting MSB = 1



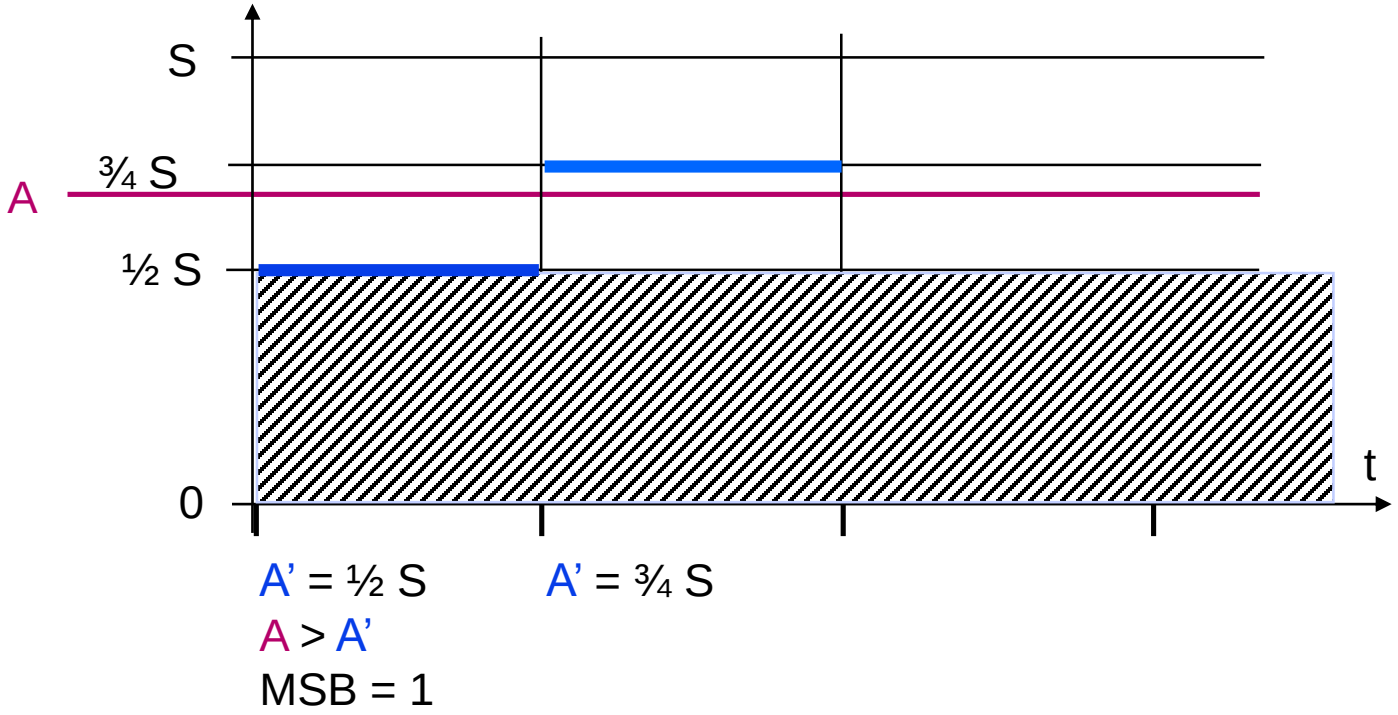
Approximation Sequence

- Since $A > S/2$, MSB = 1
  - Range 0→ ½ S is now excluded from the possible A values



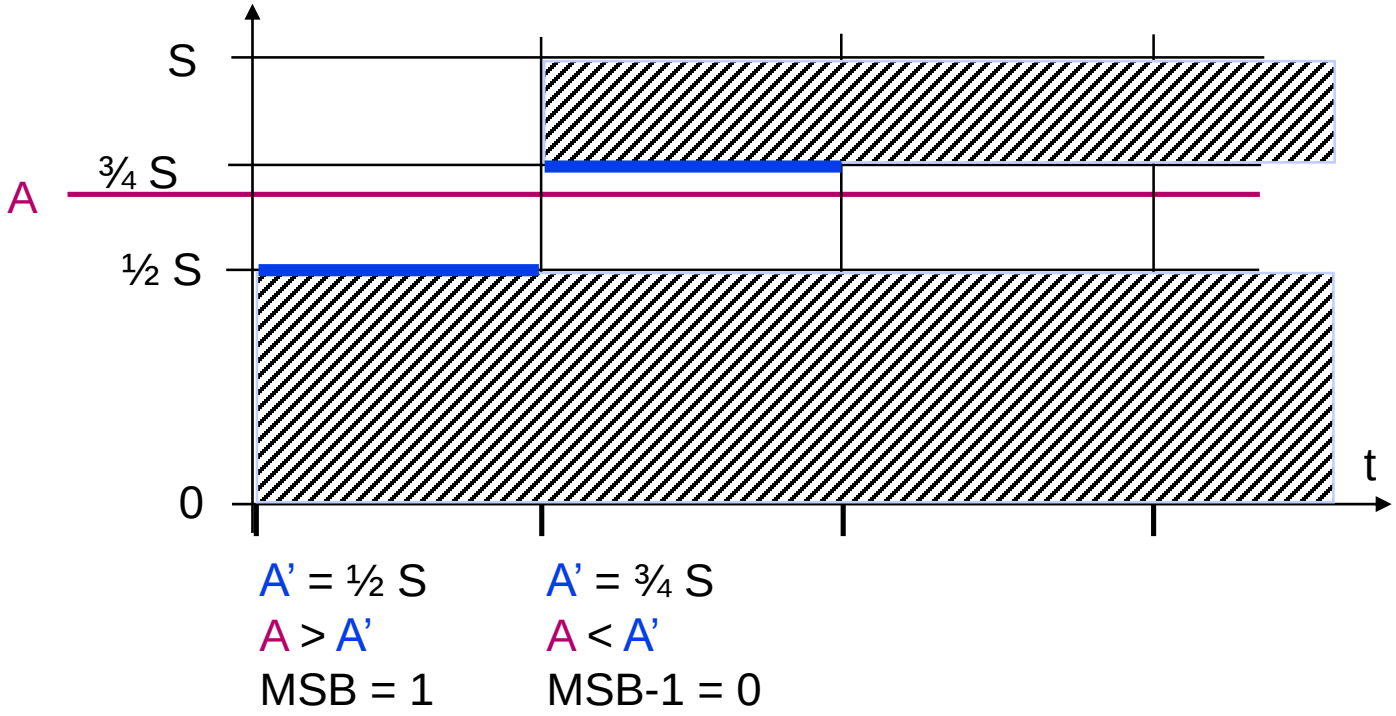
Approximation Sequence

- *A* is compared with mid-value of possible range
  - A’ = ¾ S by setting MSB–1 = 1



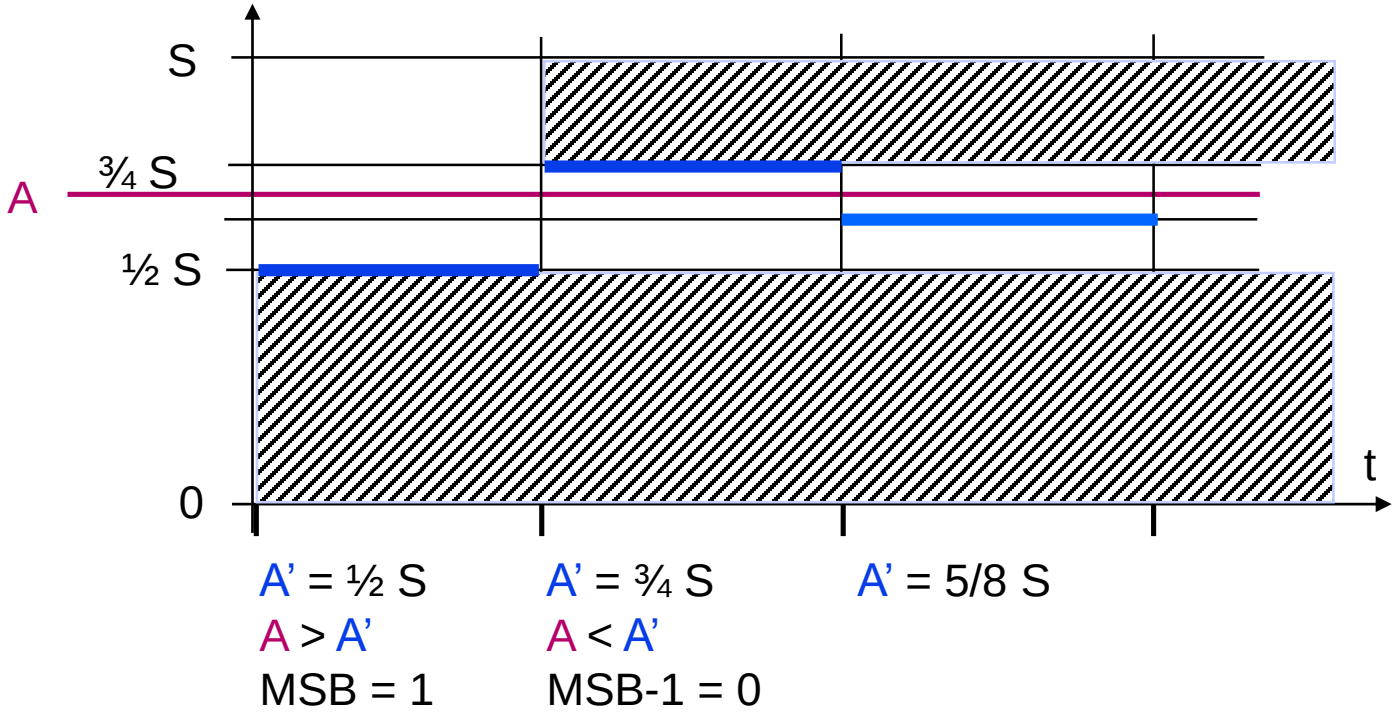
Approximation Sequence

- Since $A < \frac{3}{4} S$, MSB–1 = 0
  - Range $\frac{3}{4} S \rightarrow S$ is now excluded from the possible A values



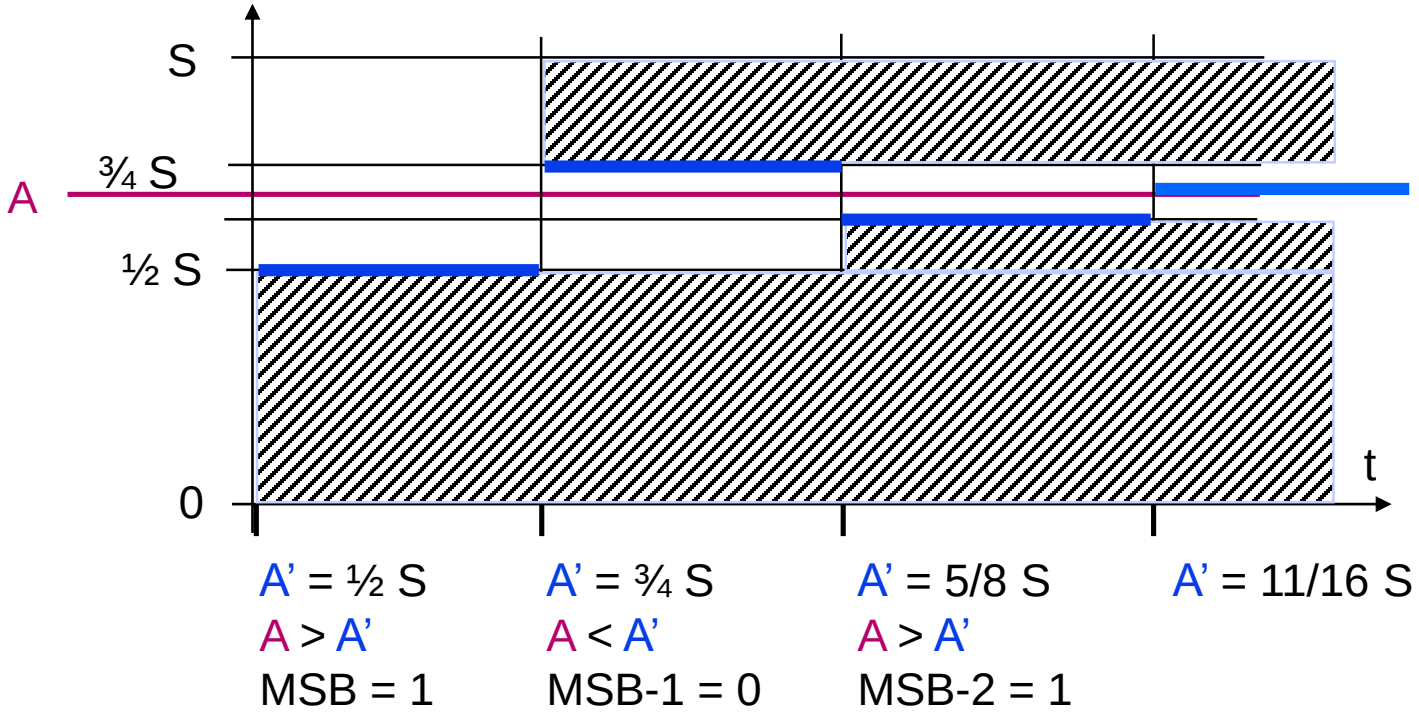
Approximation Sequence

- *A* is compared with mid-value of possible range
  - A’ = 5/8 S by setting MSB–2 = 1



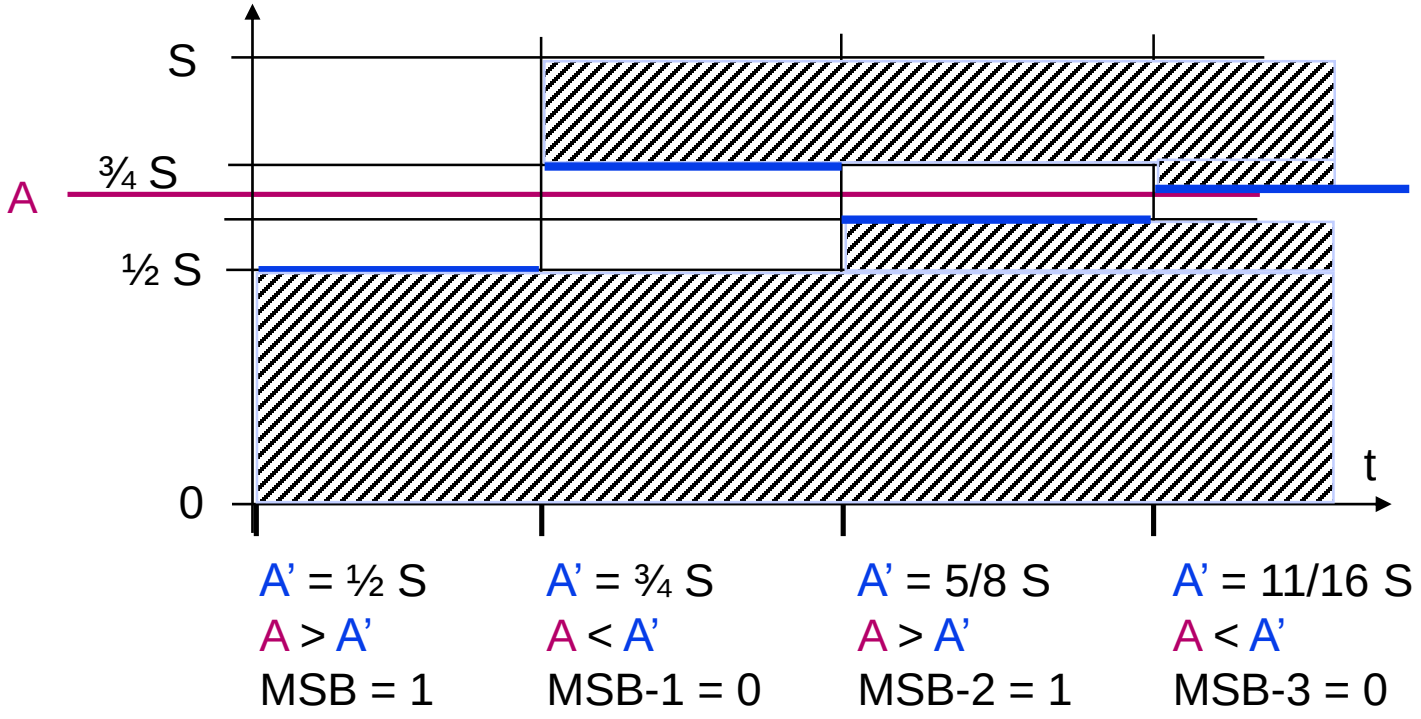
Approximation Sequence

- Since $A < 5/8\ S$, MSB–2 = 1
  - Range ½ S→5/8 S is now excluded from the possible A values



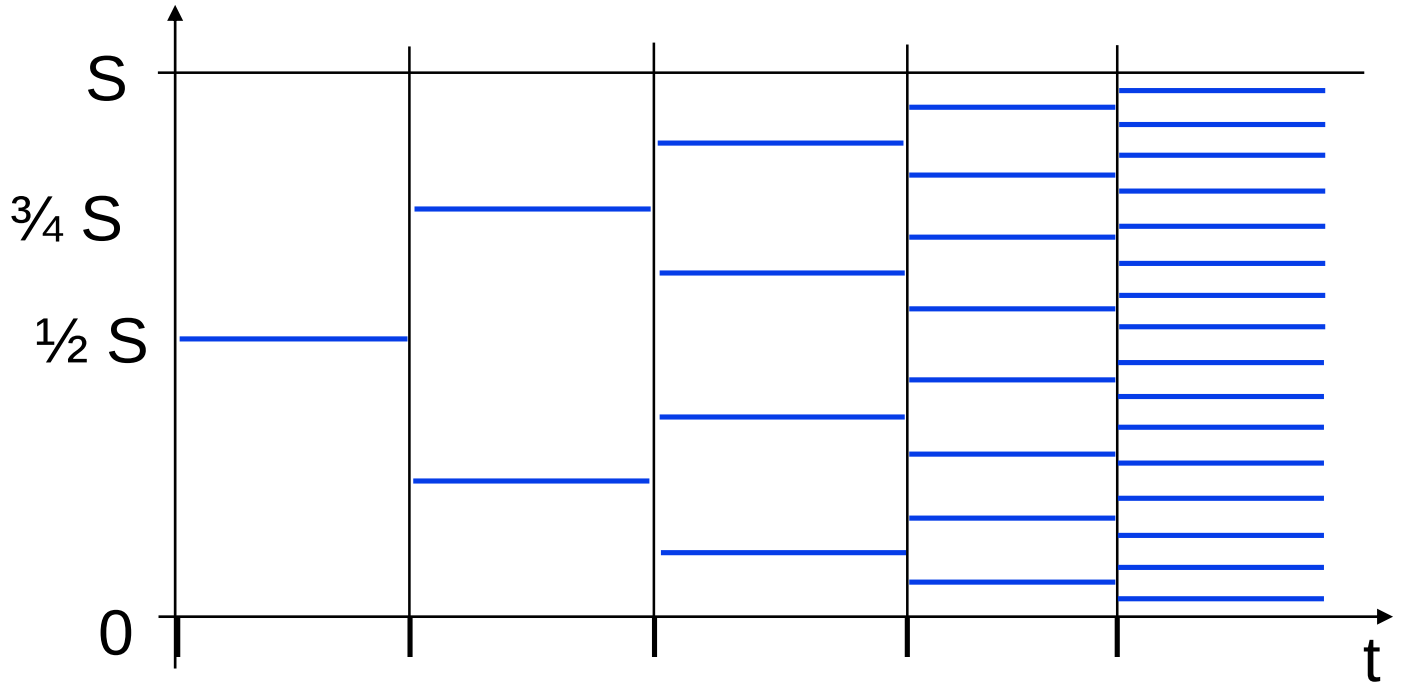
Approximation Sequence

- Since *A* < 11/16 *S*, MSB–3 must be 0
  - Range 11/16 *S*→3/4 *S* is now excluded from possible *A* values



Complete Decision Tree

- Sequence of possible D/A output *A*' which are compared to *A*



Successive Approximation ADC Features

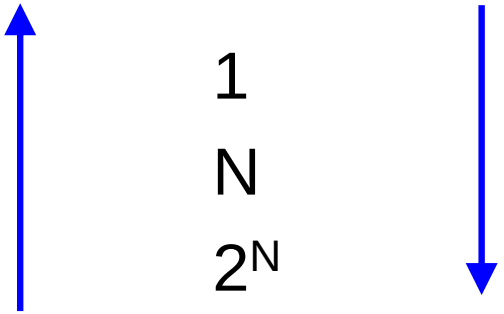
- Single comparator
- Always needs *N* comparison cycles for *N*-bit conversion

- Compared to the flash ADC
  - Simpler: 1 comparator vs 2^N
  - Slower: *N* steps vs 1

- Compared to the tracking ADC
  - Similar complexity: 1 comparator
  - Faster: *N* steps vs 2^N

Speed vs Complexity

	Complexity	Conversion time
Parallel (flash)	2^N	1
Successive Approx.	1	N
Tracking	1	2^N



Complexity: Proportional to the number of comparators.

Conversion time: The maximum number of comparator delays (clock periods) to finish a conversion

Review Questions

- Draw the A/D conversion characteristics which have only one of the basic errors: offset, gain, nonlinearity.
- Draw a conversion characteristic with a 2 LSB integral nonlinearity error. The same for differential nonlinearity.
- What effect has a large differential nonlinearity?
- How many comparators needs an 8-bit flash ADC?
- Draw the schematic of a successive approximation ADC and describe the operations of the SAR.
- What can determine a high nonlinearity error for a successive approximation ADC?

Exercise 1

- An 8-bit tracking ADC receives in input a sinusoidal signal of $1\ \mathrm{V_{pp}}$. The ADC clock is $1\ \mathrm{MHz}$. The DAC of the ADC has $LSB = 10\ \mathrm{mV}$.
  - Calculate the maximum frequency of the input sine wave that avoids the ADC overload.
  - Calculate the max conversion time (for a step signal $0\ \mathrm{V}$ → full scale).

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- $V_{\mathrm{in}} = A \cdot \sin(2\pi f t)\,;\ \ A = 0.5\ \mathrm{V};\ \ f_{\mathrm{CK}} = 1\ \mathrm{MHz}$
- $\left.\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t}\right|_{\mathrm{max}} = 2\pi f A \leq LSB \cdot f_{\mathrm{CK}} \Rightarrow f \leq \frac{LSB \cdot f_{\mathrm{CK}}}{2\pi A}$
- $f \leq \frac{10\ \mathrm{mV} \cdot 1\ \mathrm{MHz}}{2\pi \cdot 0.5\ \mathrm{V}} = 3.18\ \mathrm{kHz}$

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- An 8-bit ADC covers the scale with $2^8 = 256$ levels
- A tracking converter evaluates one level each clock cycle
- $T_{\mathrm{conv}}^{\max} = 2^N \cdot T_{\mathrm{CK}} = \frac{2^8}{1\,\mathrm{MHz}} = 256\,\mu\mathrm{s}$

Exercise 2

- A successive approximation 8-bit ADC receives in input a sinusoidal signal of $1\ \mathrm{V_{pp}}$. The ADC clock is $1\ \mathrm{MHz}$, and the DAC has $LSB = 10\ \mathrm{mV}$.
  - Calculate the maximum conversion time.
  - Calculate the maximum input signal frequency that can be converted without errors (signal amplitude is full scale).

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  - Calculate the maximum conversion time.

- $T_{\mathrm{conv}}^{\mathrm{max}} = N \cdot T_{\mathrm{CK}} = \frac{8}{1\ \mathrm{MHz}} = 8\ \mu\mathrm{s}$

Exercise 2

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  - Calculate the maximum input signal frequency that can be converted without errors (signal amplitude is full scale).
- Must convert before the input signal changes $> 1\ LSB$
- $V_{\mathrm{in}} = A \cdot \sin(2\pi f t)\,; \quad A = \frac{LSB \cdot 2^N}{2} = 1.28\ \mathrm{V}; \quad f_{\mathrm{CK}} = 1\ \mathrm{MHz}$
- $\left.\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t}\right|_{\max} = 2\pi f A \leq LSB \cdot \frac{f_{\mathrm{CK}}}{N} \Rightarrow f \leq \frac{LSB \cdot f_{\mathrm{CK}}}{2\pi A N}$
- $f \leq \frac{10\ \mathrm{mV} \cdot 1\ \mathrm{MHz}}{2\pi \cdot 1.28\ \mathrm{V} \cdot 8\ \mathrm{bit}} = 155\ \mathrm{Hz}$