



# Digital Storage Oscilloscope (DSO)



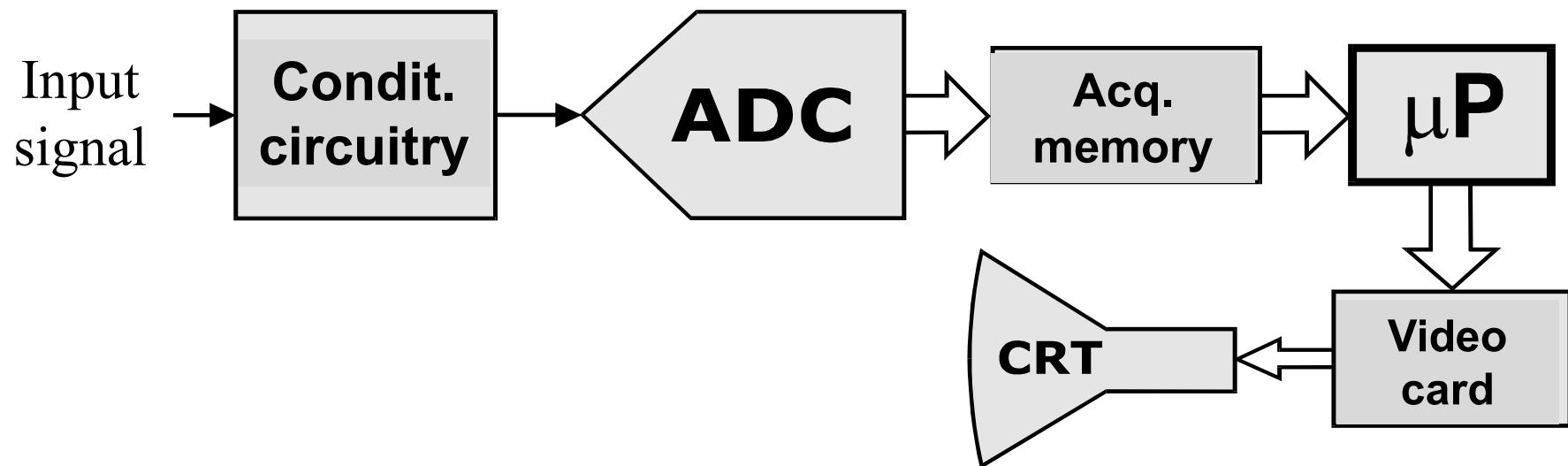
## DSO – basic principle

### Common architecture of a digital instrument

- Processing of the input analogue signal
- Sampling of the signal and conversion in numerical format (Analogue-to-Digital Conversion)
- Storing
- Processing of the numerical samples
- Visualization of the signal waveform (time domain)

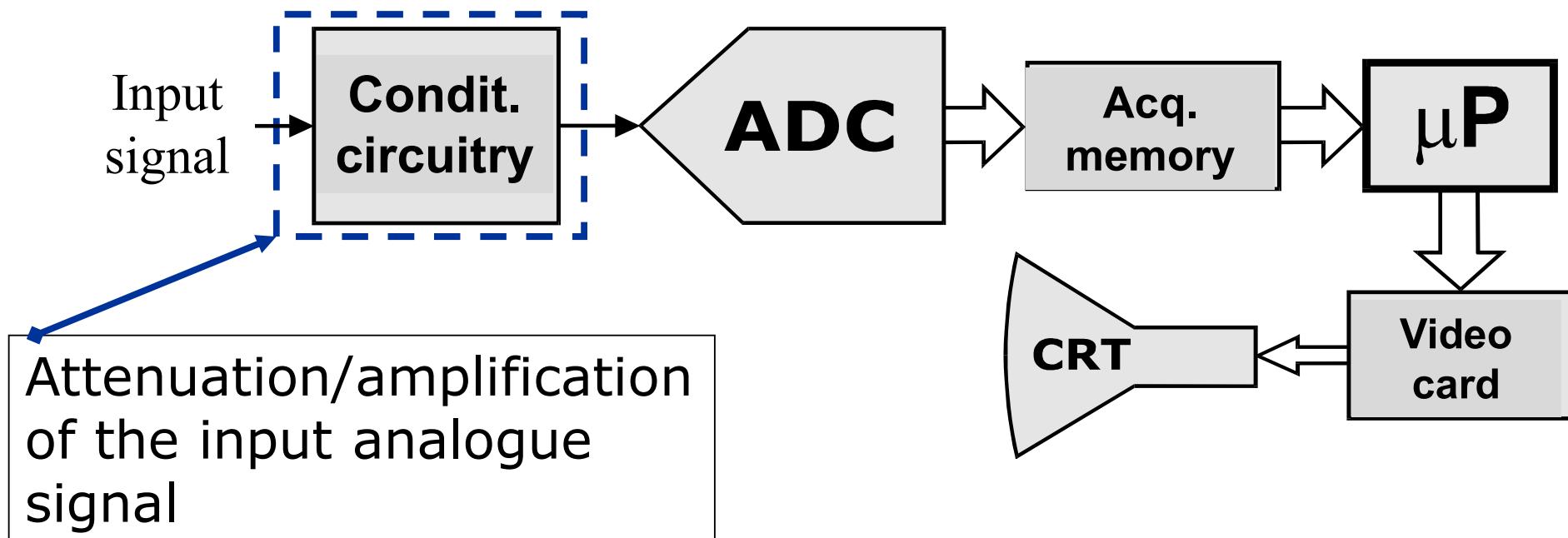
## DSO – basic principle

### *Serial-processing architecture*



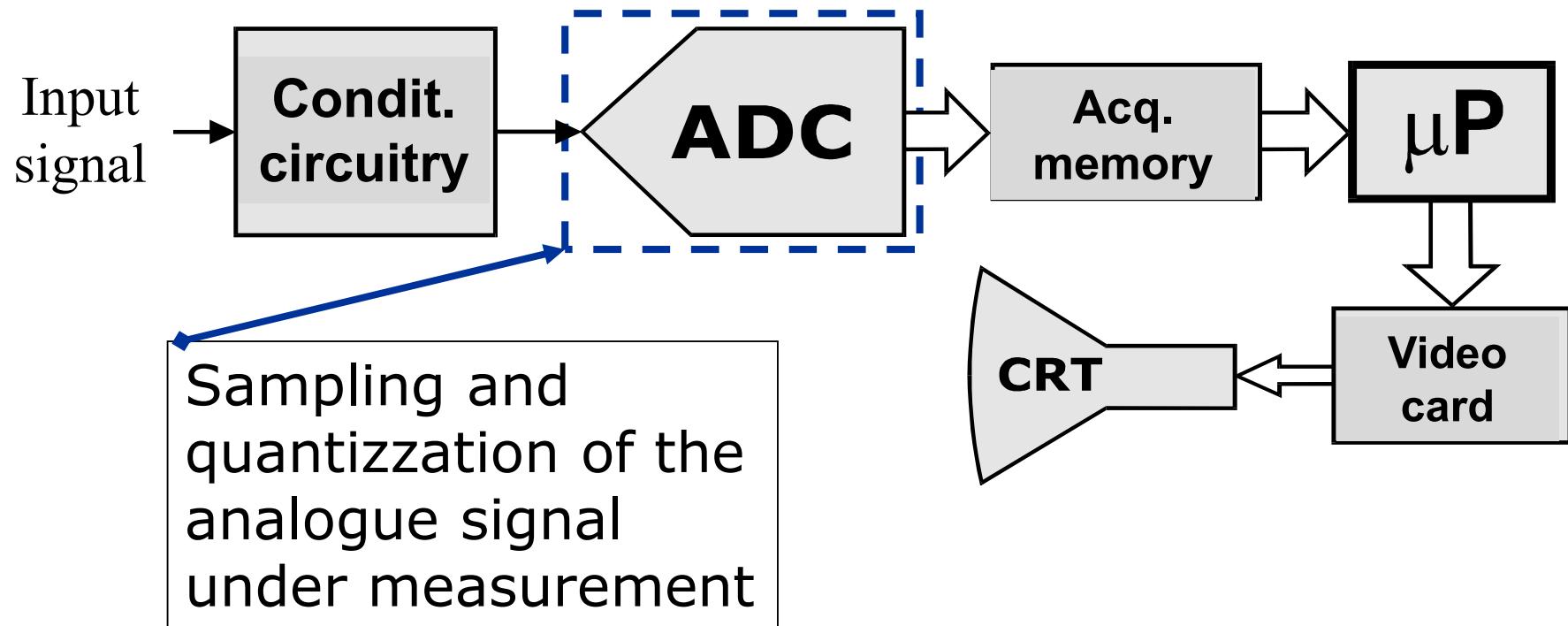
## DSO – basic principle

### *Serial-processing architecture*



## DSO – basic principle

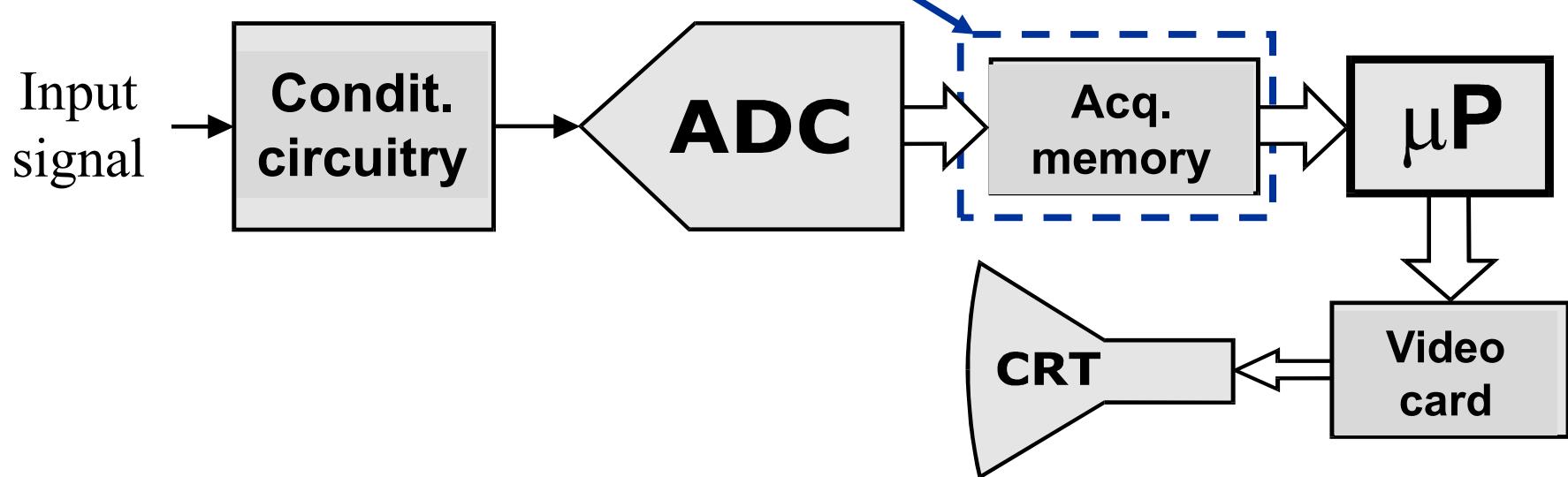
### *Serial-processing architecture*



## DSO – basic principle

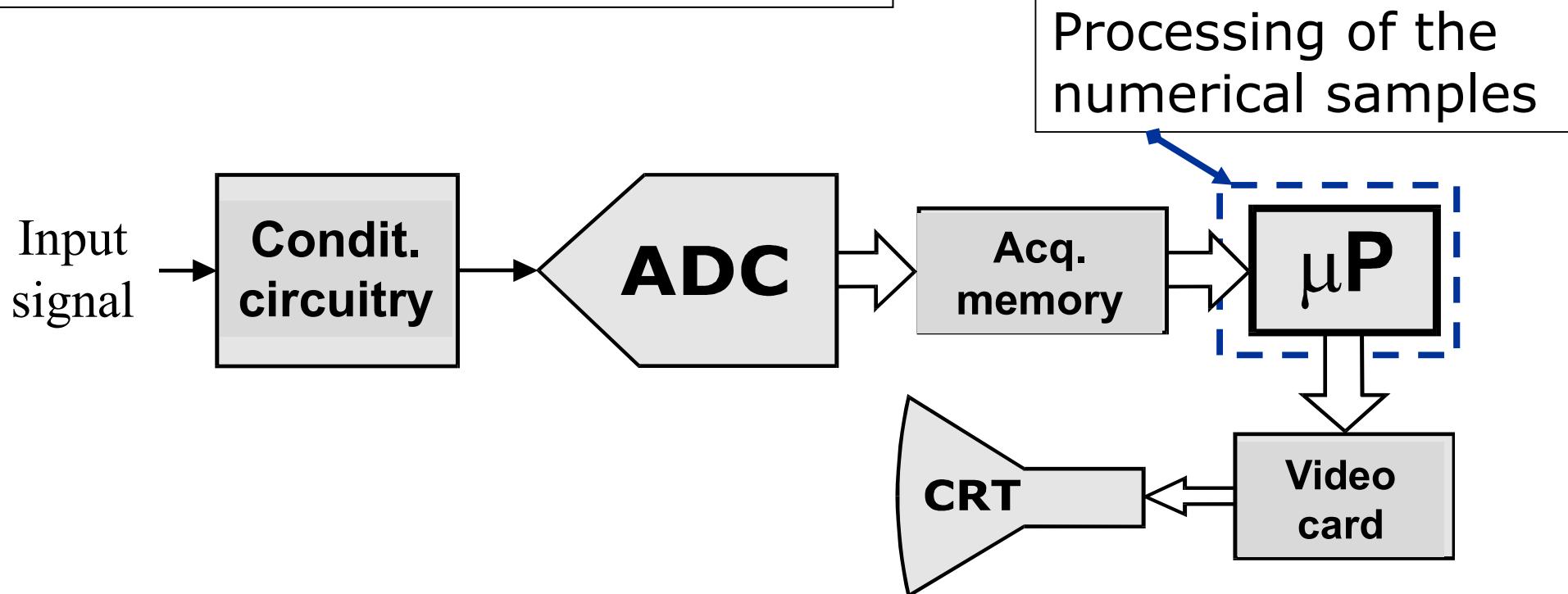
### ***Serial-processing architecture***

Storing of the numerical samples at the output of the ADC



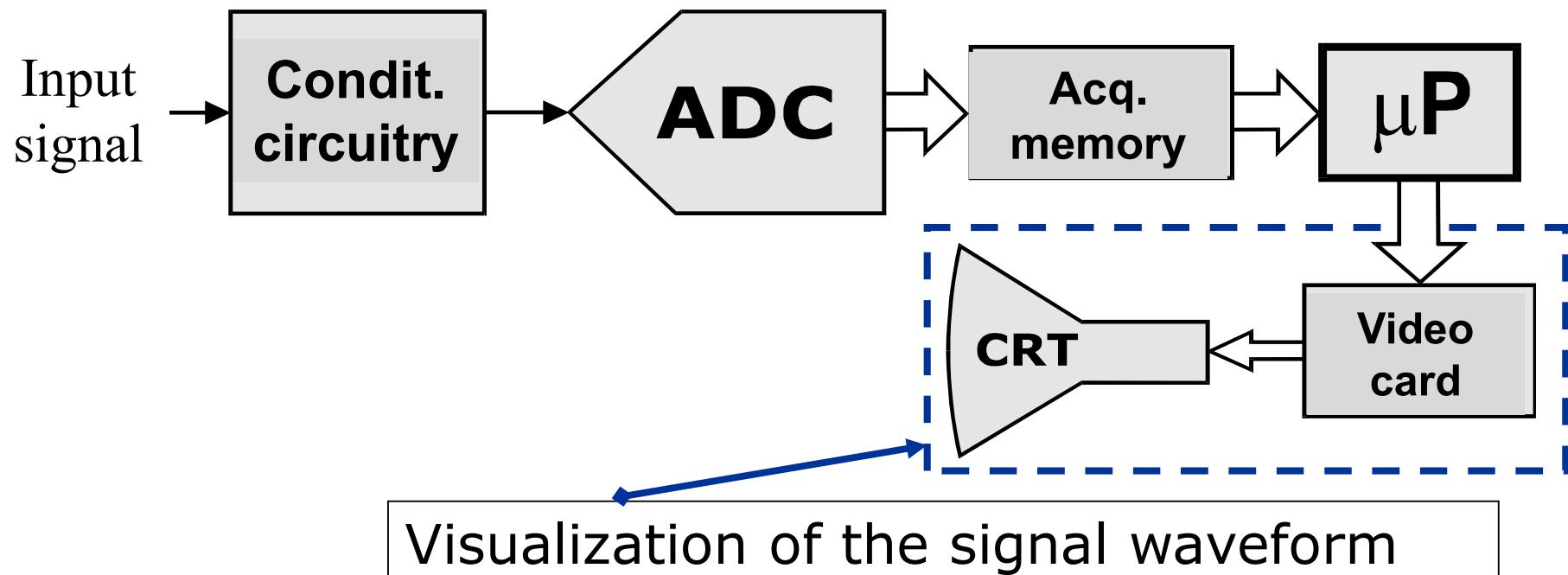
## DSO – basic principle

### *Serial-processing architecture*



## DSO – basic principle

### *Serial-processing architecture*



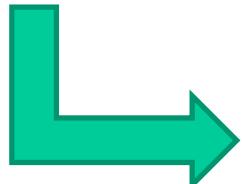


# Digital Storage Oscilloscope

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## DSO – basic principle

### ***Serial-processing architecture***



The DSO “watches” the input signal during some time frames, but is “blind” during others.

The probability to miss part of the signal under measurement decreases as the ***waveform capture rate*** (waveform/s) increases.

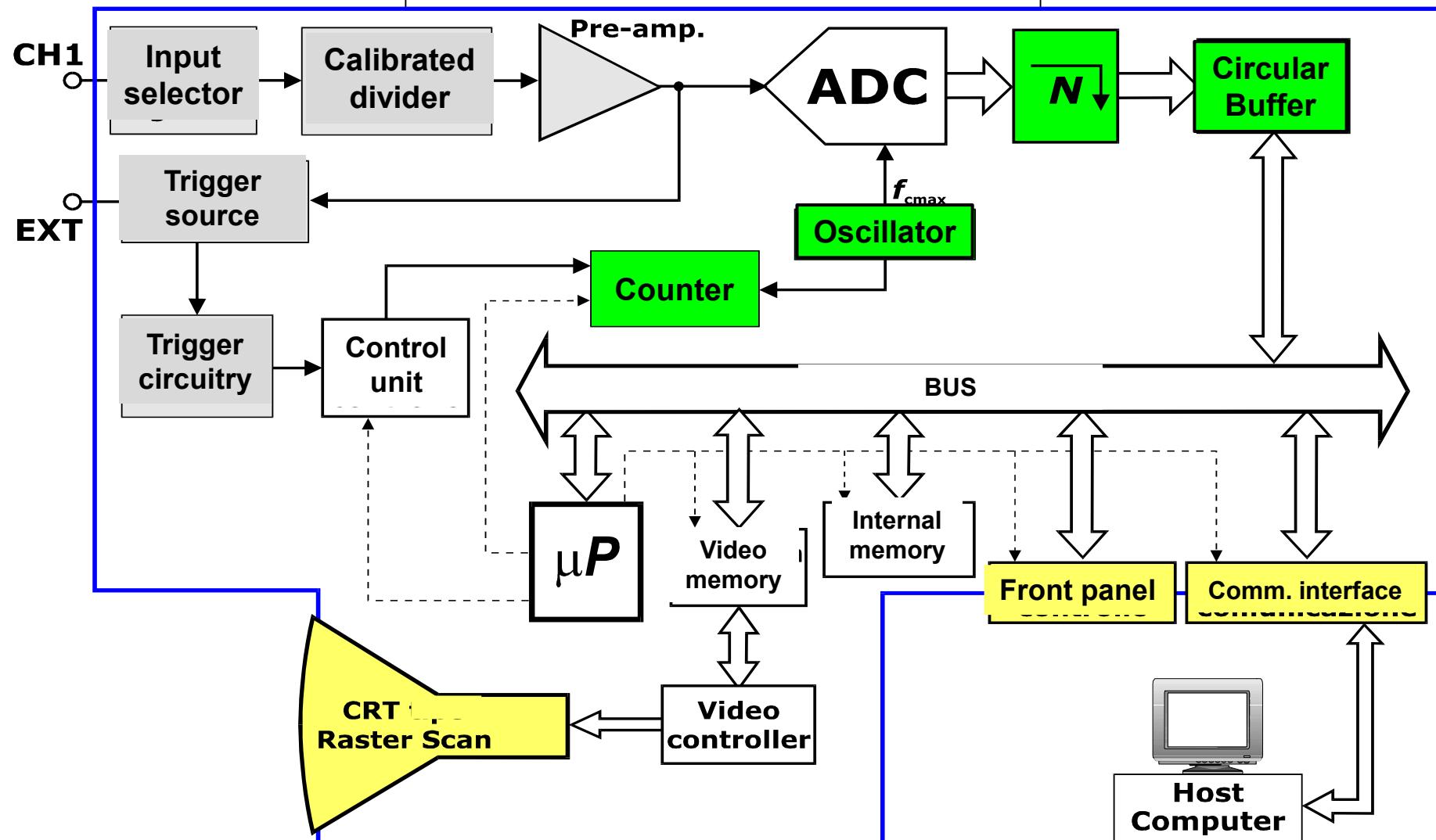


# Digital Storage Oscilloscope

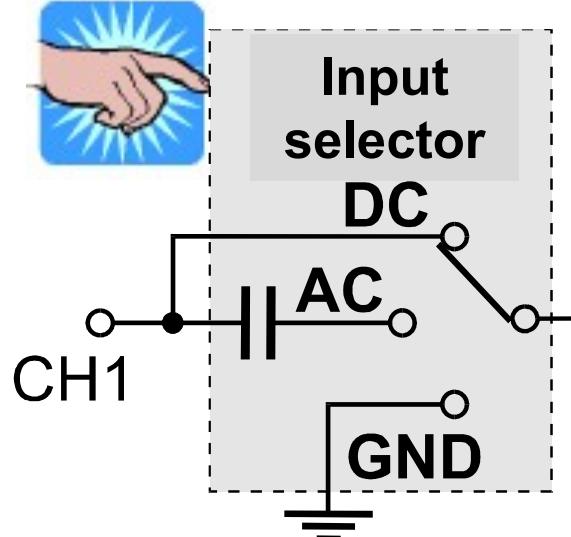
## Block scheme

# Digital Storage Oscilloscope

DSO – block scheme



## DSO – block scheme



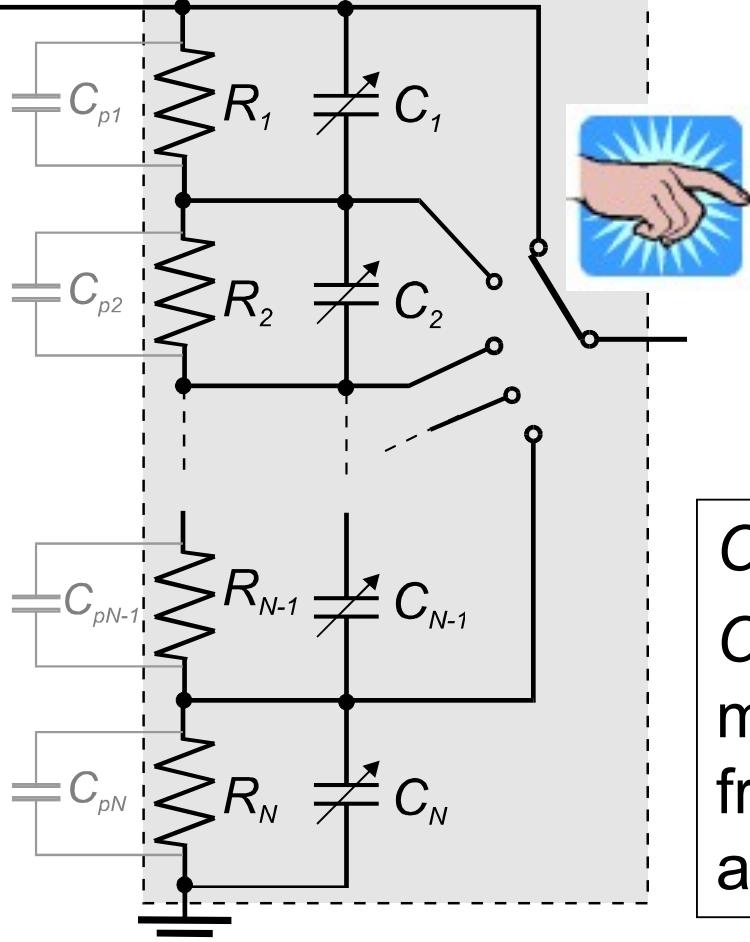
### Input selector

Selection of the input coupling:

- *DC coupling*
  - ↳ Both DC and AC components are sent to the next stages
- *AC coupling*
  - ↳ High-pass filter with a cut-off frequency of few hertz
- *GND*
  - ↳ Input signal set to ground (0 V)

## DSO – block scheme

**Calibrated divider**



### Calibrated divider (V/div)

It allows the amplitude of the signal to be matched to the next stages.

Attenuation steps: 1, 2, 5

$C_{pi}$ : stray capacitances

$C_i$ : compensators (tuned by the manufacturer to obtain a frequency-independent attenuation)

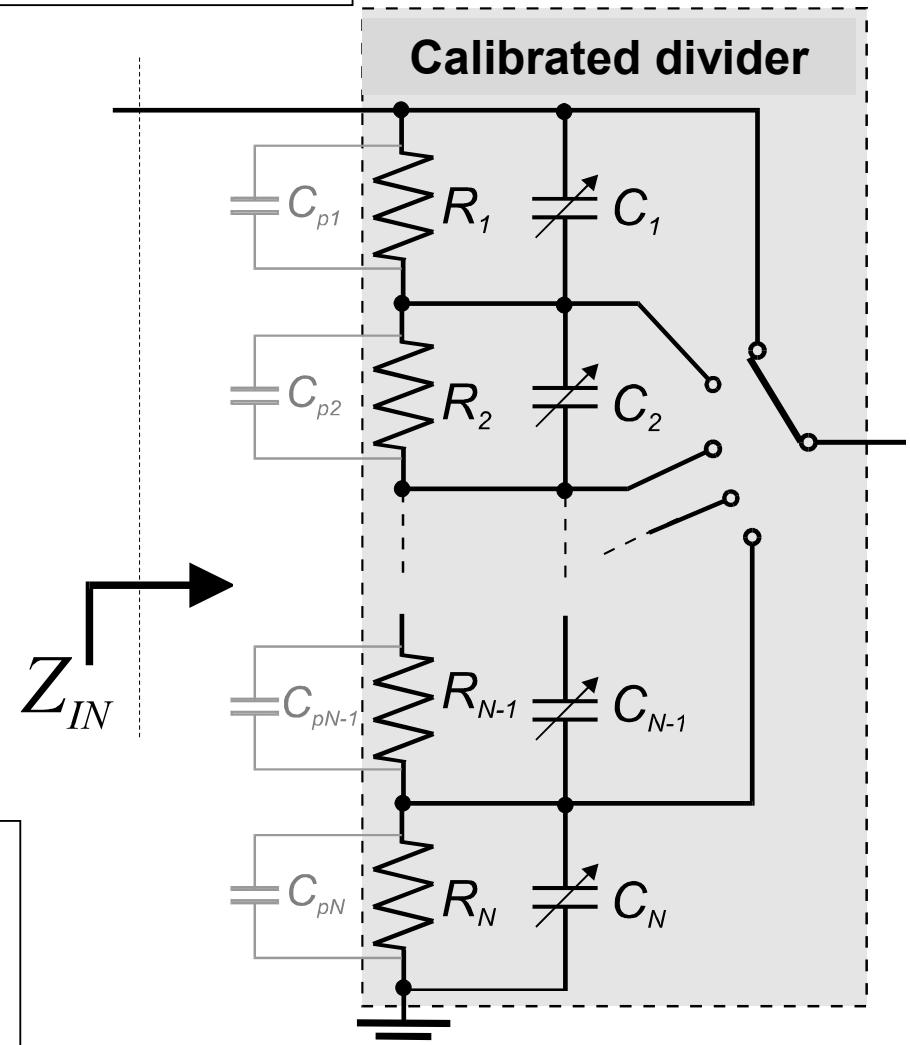
## DSO – block scheme

### Input impedance $Z_{IN}$

Due to the presence of stray and compensation capacitors in the calibrator divider, the input impedance of the DSO is represented by means of a resistance (common value  $1 \text{ M}\Omega$ ) shunted by a capacitance (tens of picofarad).

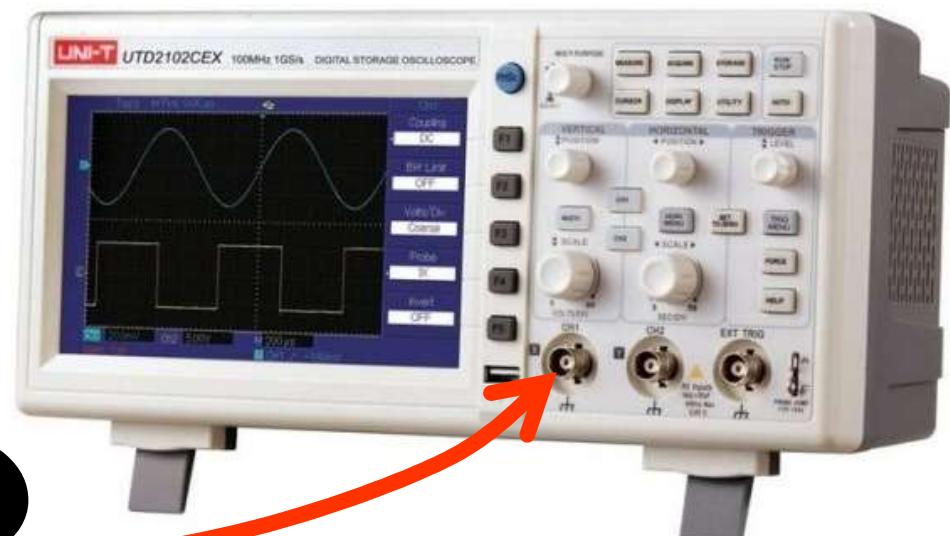
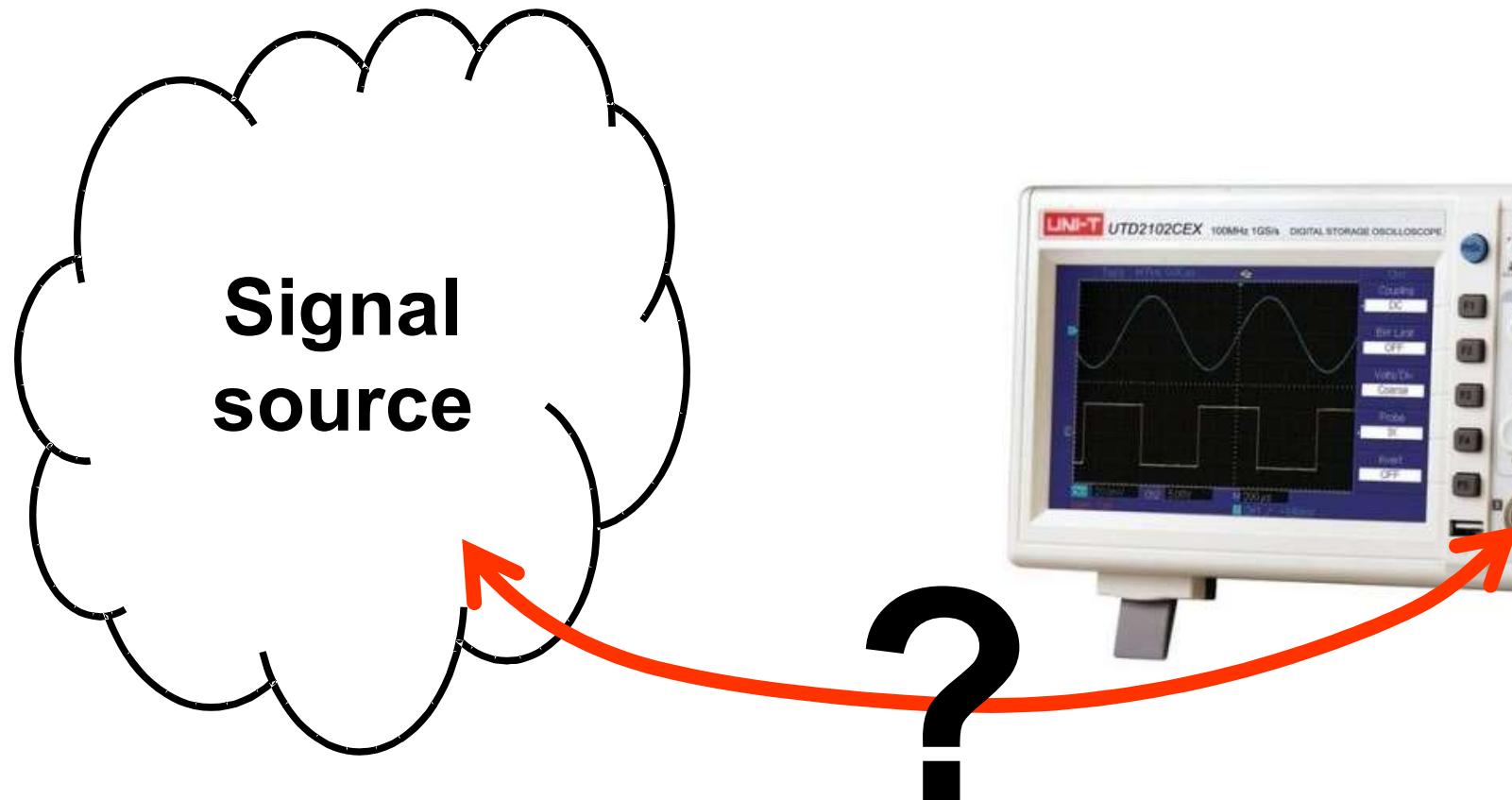


Some instruments give the operator the possibility to select an input resistance of  $50 \Omega$



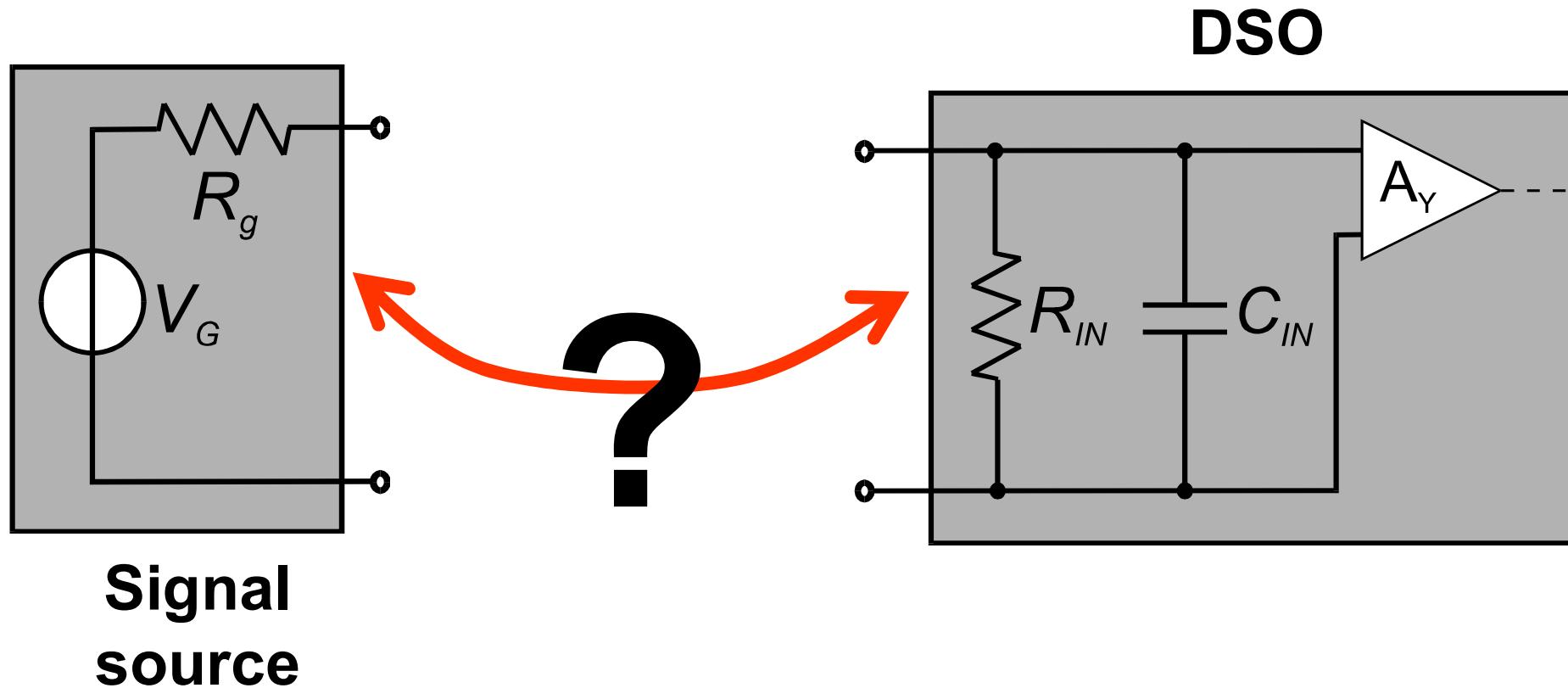
## DSO – block scheme

Connection of the signal to the DSO input



## DSO – block scheme

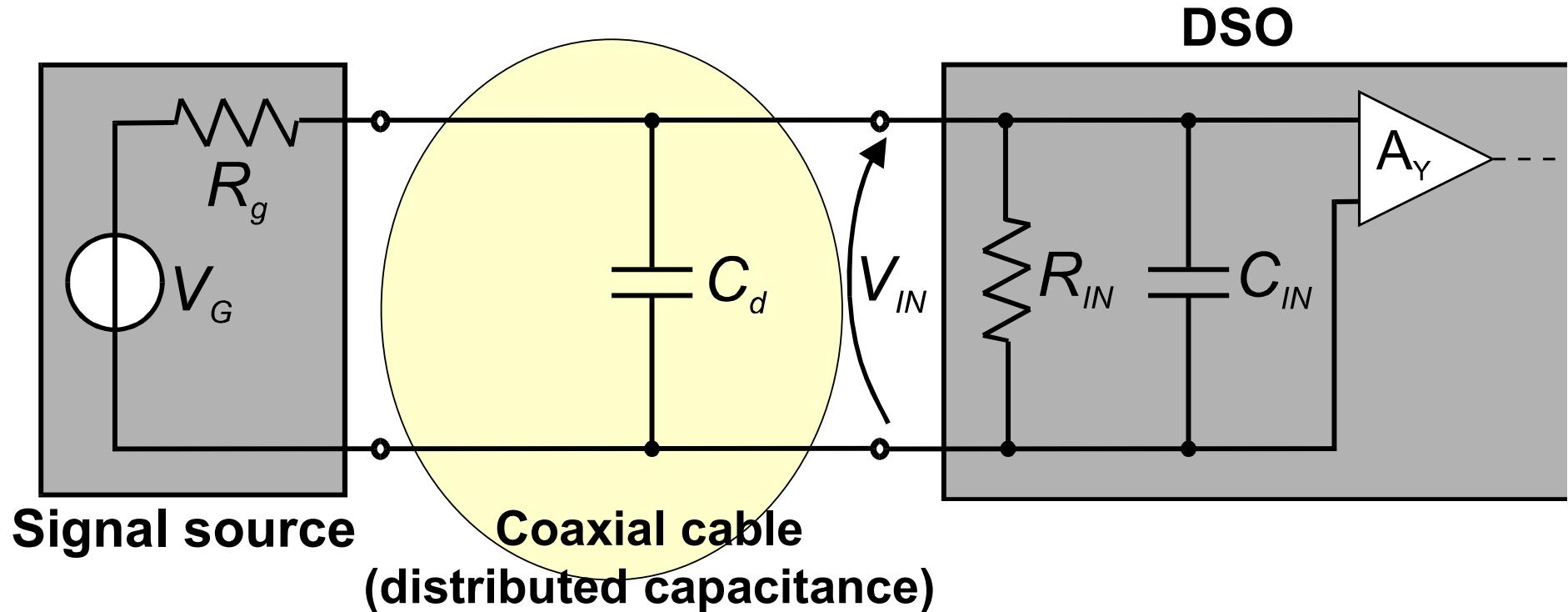
Connection of the signal to the DSO input



## DSO – block scheme

Connection of the signal to the DSO input

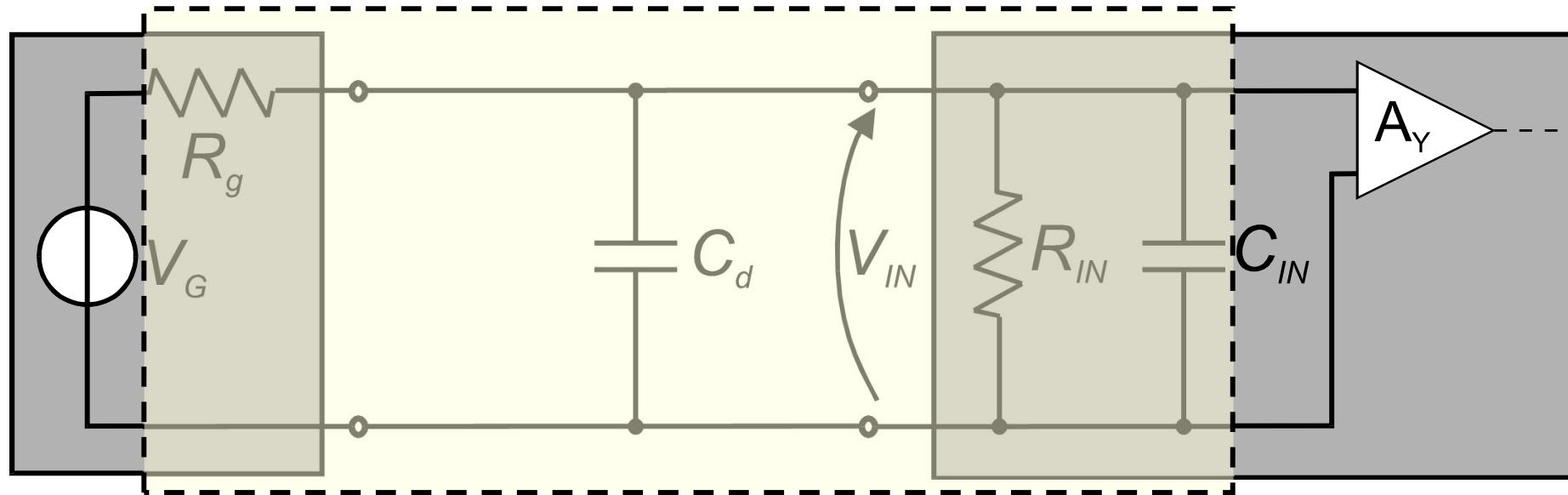
↳ Coaxial cable



## DSO – block scheme

Connection of the signal to the DSO input

↳ Coaxial cable



$$f_{cut} = \frac{1}{2\pi \cdot (R_g // R_{IN}) \cdot (C_d + C_{IN})} \approx \frac{1}{2\pi \cdot R_g \cdot (C_d + C_{IN})}$$



# Digital Storage Oscilloscope

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## DSO – block scheme

Connection of the signal to the DSO input

↳ Coaxial cable

$$f_{cut} = \frac{1}{2\pi \cdot (R_g // R_{IN}) \cdot (C_d + C_{IN})} \approx \frac{1}{2\pi \cdot R_g \cdot (C_d + C_{IN})}$$

### Example

$R_g = 50 \Omega$ ;  $R_{IN} = 1 M\Omega$ ,  $C_{IN} = 10 pF$

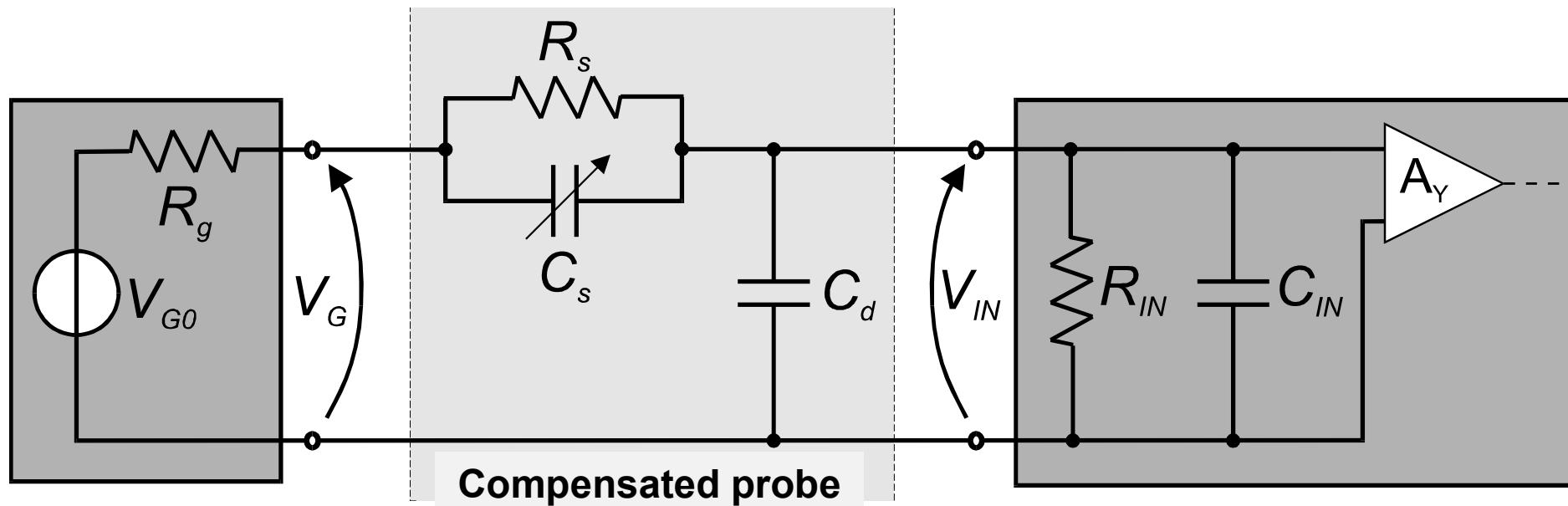
Cable RG-58 (100 pF/m), length = 1 m  $\rightarrow C_d = 100 pF$

$$f_{cut} \approx 28.9 \text{ MHz}$$

**WARNING:** it could be lower than the DSO bandwidth

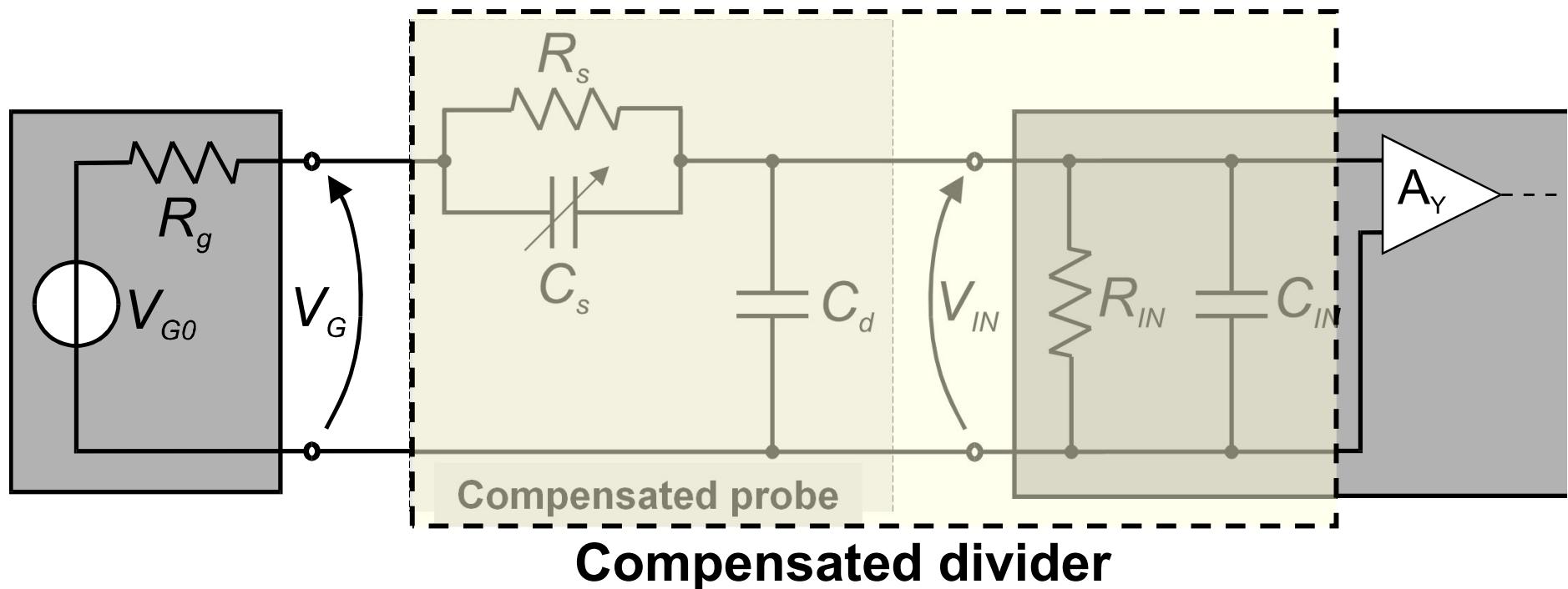
## DSO – block scheme

Connection of the signal to the DSO input  
↳ Compensated probe



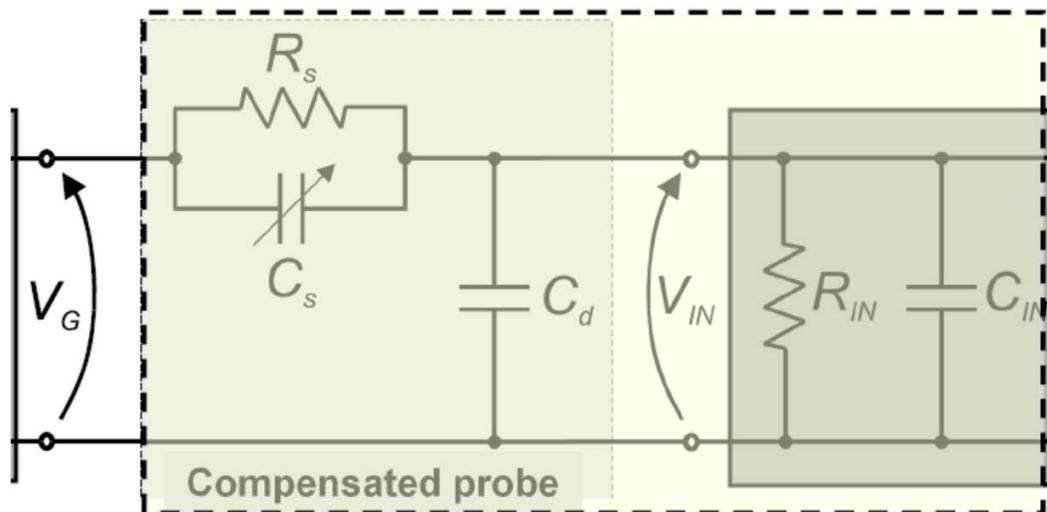
## DSO – block scheme

Connection of the signal to the DSO input  
↳ Compensated probe



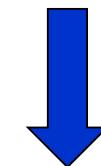
## DSO – block scheme

Connection of the signal to the DSO input  
↳ Compensated probe



**Compensation condition:**

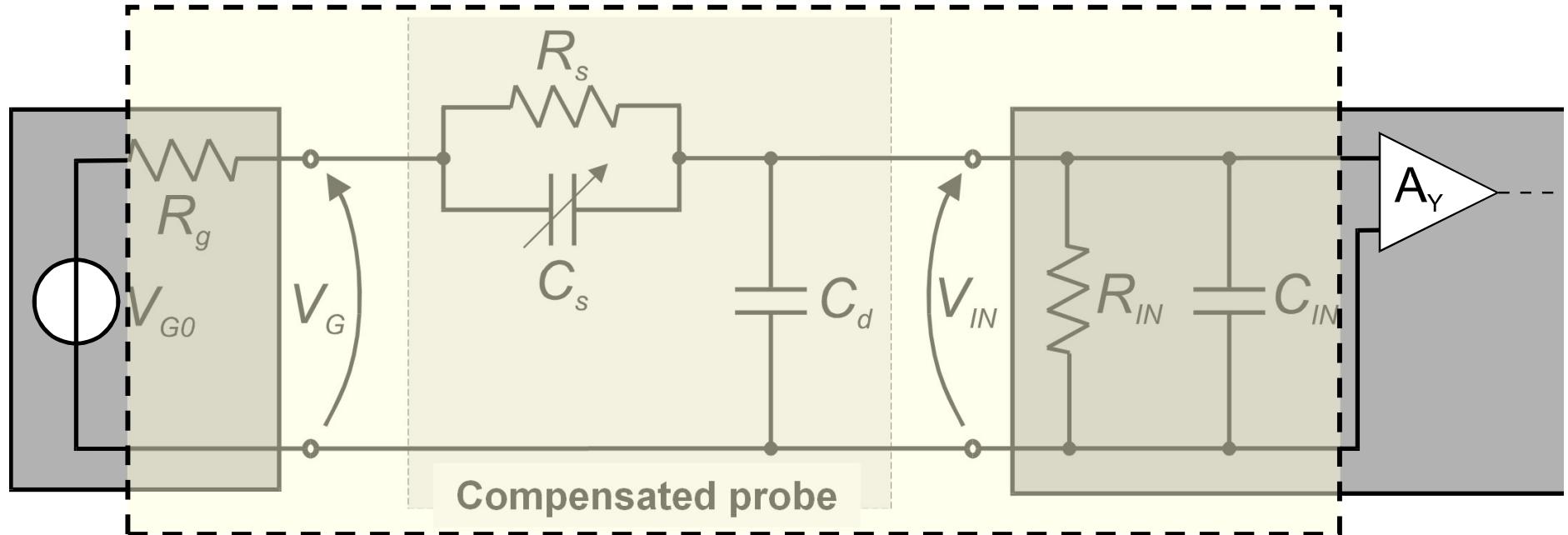
$$R_S \cdot C_S = R_{IN} \cdot (C_d + C_{IN})$$



$$\frac{V_{IN}}{V_G} = \frac{R_{IN}}{R_{IN} + R_S}, \quad \forall f$$

## DSO – block scheme

Connection of the signal to the DSO input  
 ↗ Compensated probe



**Low-pass filter**

$$f_{cut}^P = \frac{1}{2\pi \cdot [R_g // (R_s + R_{IN})] \cdot C_{eq}} \approx \frac{1}{2\pi \cdot R_g \cdot C_{eq}}$$



# Digital Storage Oscilloscope

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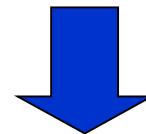
## DSO – block scheme

Connection of the signal to the DSO input

↳ Compensated probe

$$f_{cut}^P = \frac{1}{2\pi \cdot [R_g // (R_S + R_{IN})] \cdot C_{eq}} \approx \frac{1}{2\pi \cdot R_g \cdot C_{eq}}$$

$$C_{eq} = \frac{C_S \cdot (C_d + C_{IN})}{C_S + C_d + C_{IN}} < (C_d + C_{IN})$$



$$f_{cut}^P > f_{cut}$$

## DSO – block scheme

Connection of the signal to the DSO input  
↳ Compensated probe

Example:  $\times 10$  compensated probe

Attenuation = 10:1

$$\frac{V_{IN}}{V_G} = \frac{R_{IN}}{R_{IN} + R_S} = \frac{1}{10} \Rightarrow R_S = 9 \cdot R_{IN}$$

Compensation condition:

$$R_S \cdot C_S = R_{IN} \cdot (C_d + C_{IN}) \Rightarrow 9 \cdot R_{IN} \cdot C_S = R_{IN} \cdot (C_d + C_{IN}) \Rightarrow C_S = \frac{(C_d + C_{IN})}{9}$$

$$C_{eq} = \frac{C_S \cdot (C_d + C_{IN})}{C_S + C_d + C_{IN}} = \frac{(C_d + C_{IN})}{10} \quad \rightarrow \quad f_{cut}^P = \frac{1}{2\pi \cdot R_g \cdot C_{eq}} = 10 \cdot f_{cut}$$

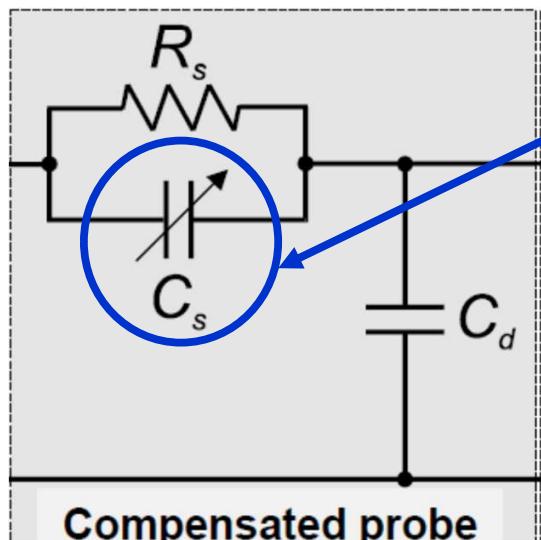
## DSO – block scheme

Connection of the signal to the DSO input

↳ Compensated probe

Compensation condition:  $R_S \cdot C_S = R_{IN} \cdot (C_d + C_{IN})$

↳ It is obtained tuning the variable capacitance  $C_S$  while a square wave is present at the probe input



Exceeding compensation



Correct compensation



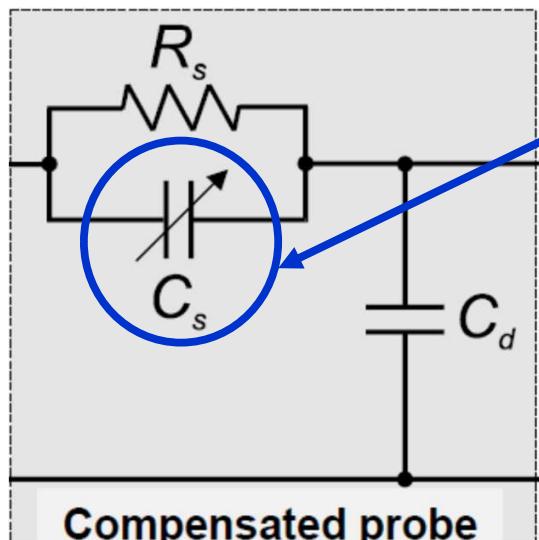
Insufficient

## DSO – block scheme

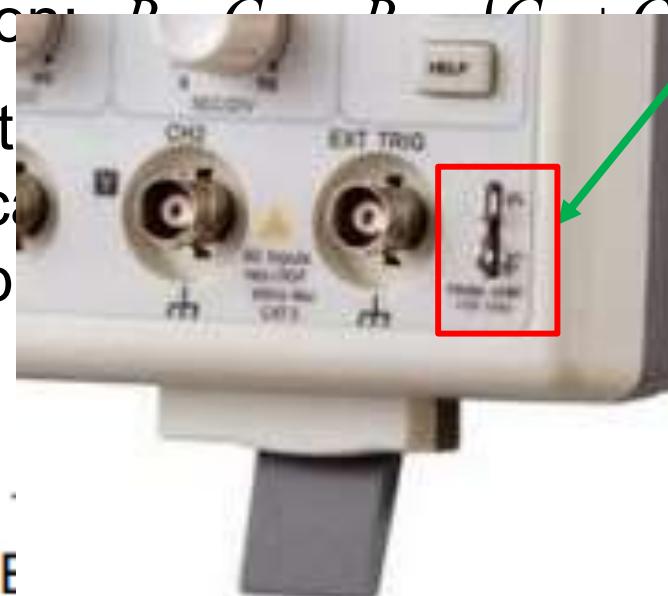
Connection of the signal to the DSO input  
↳ Compensated probe

Square quave available at the front-panel connector

Compensation conditions:  $R_s < C_d \cdot (C_s + C_N)$



↳ It can be seen that



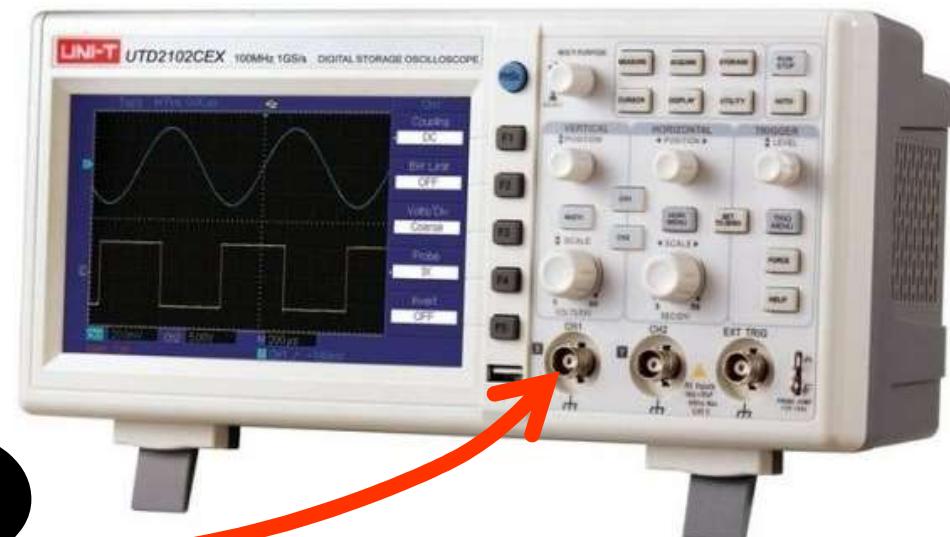
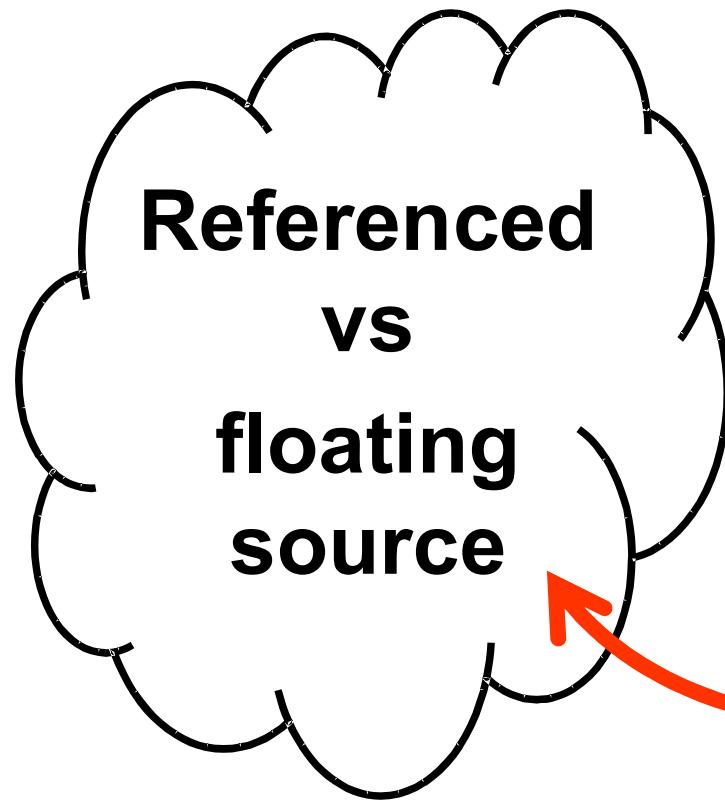
variable square wave is obtained



Insufficient

## DSO – block scheme

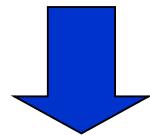
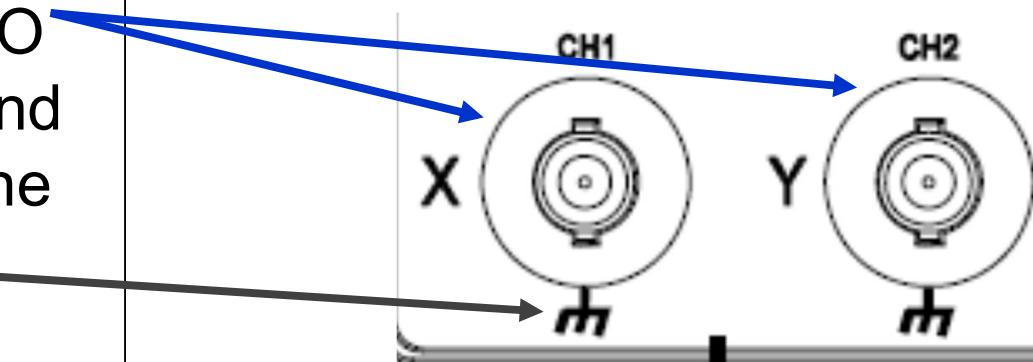
Connection of the signal to the DSO input



## DSO – block scheme

### Connection of the signal to the DSO input

The input channels of a DSO are usually referred to ground through the connection to the Protecting Earth (PE) of the mains

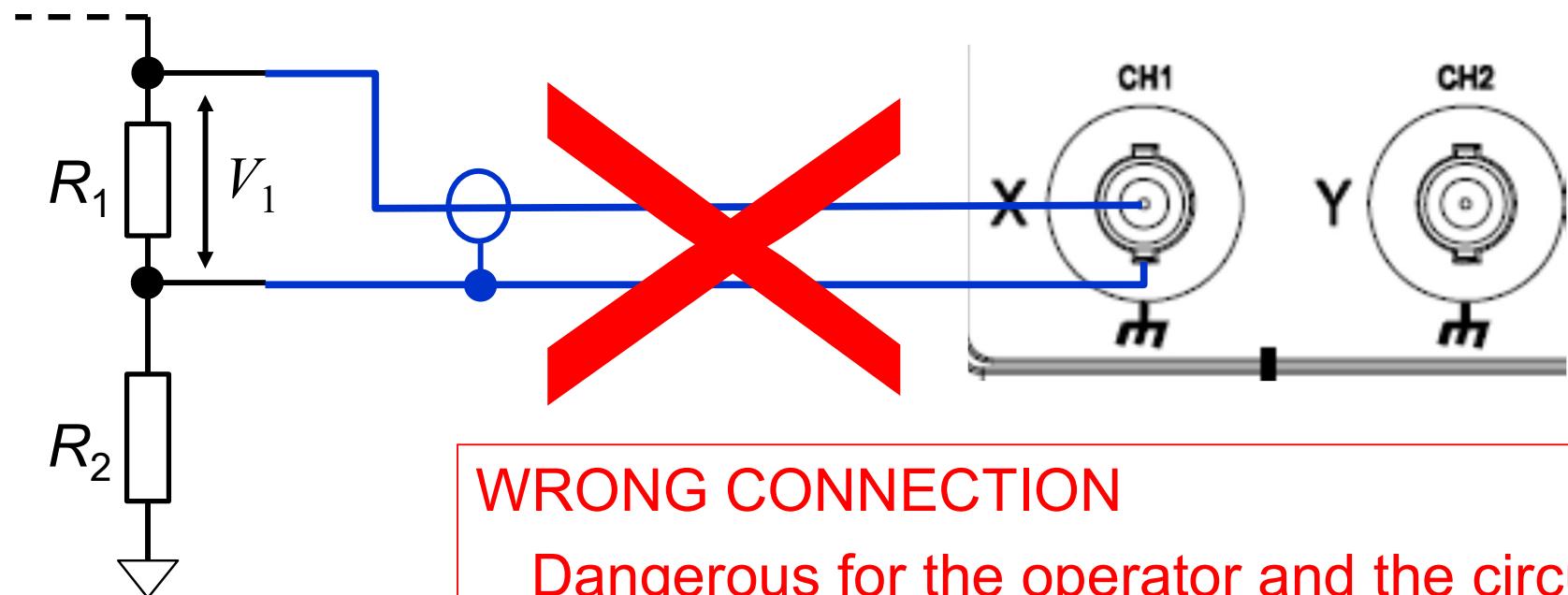


Attention has to be paid towards the type of voltage source, above all when a floating source has to be connected.

## DSO – block scheme

Connection of the signal to the DSO input

Measurement of a differential signal



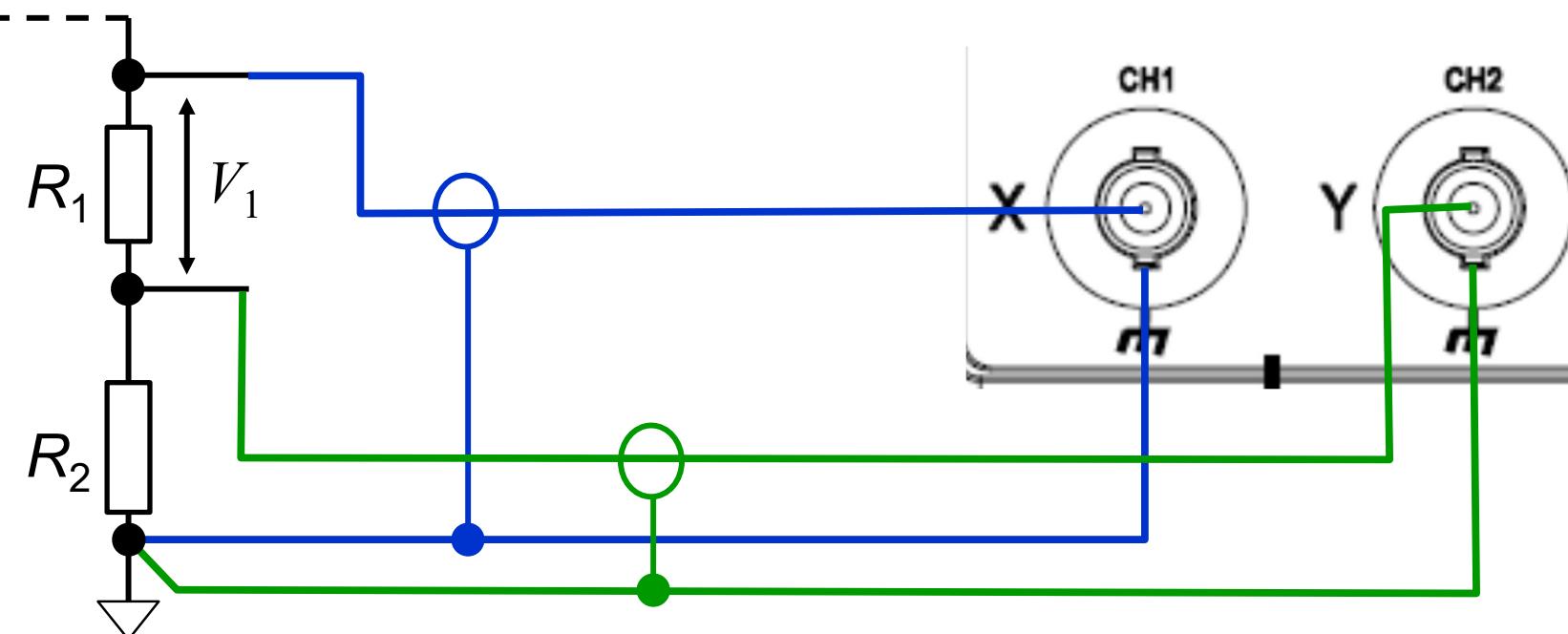
## DSO – block scheme

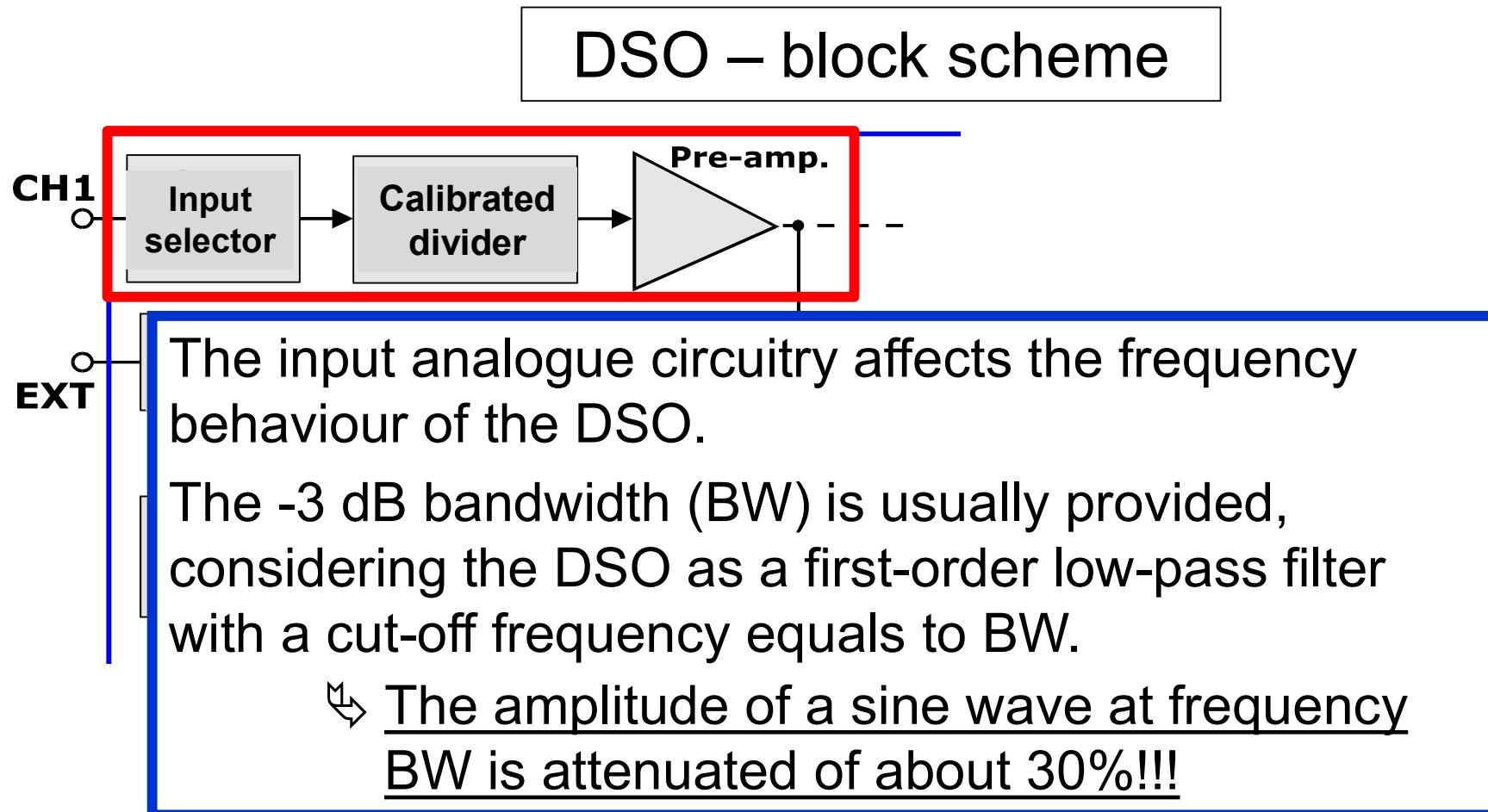
Connection of the signal to the DSO input

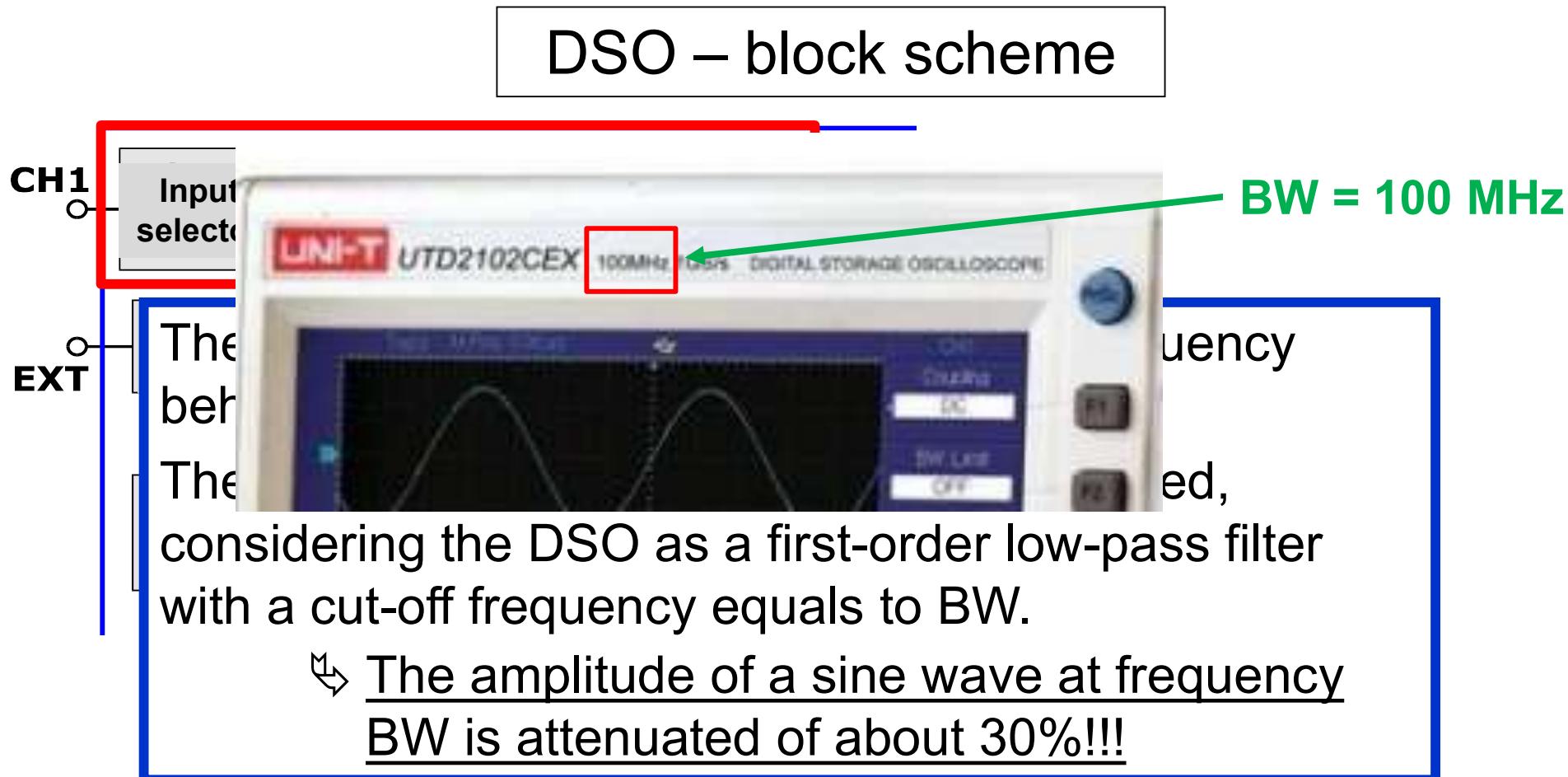


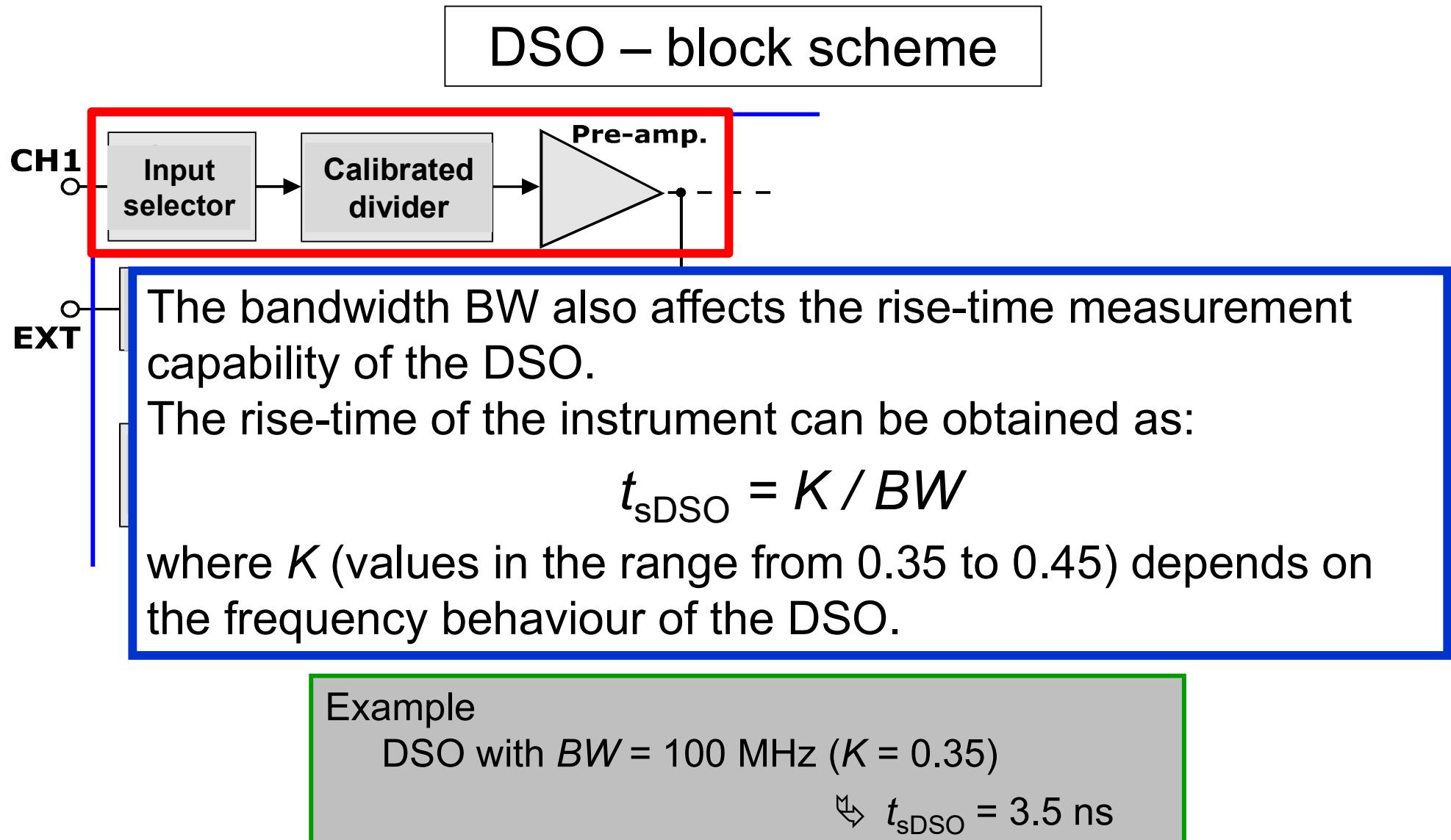
Measurement of a differential signal

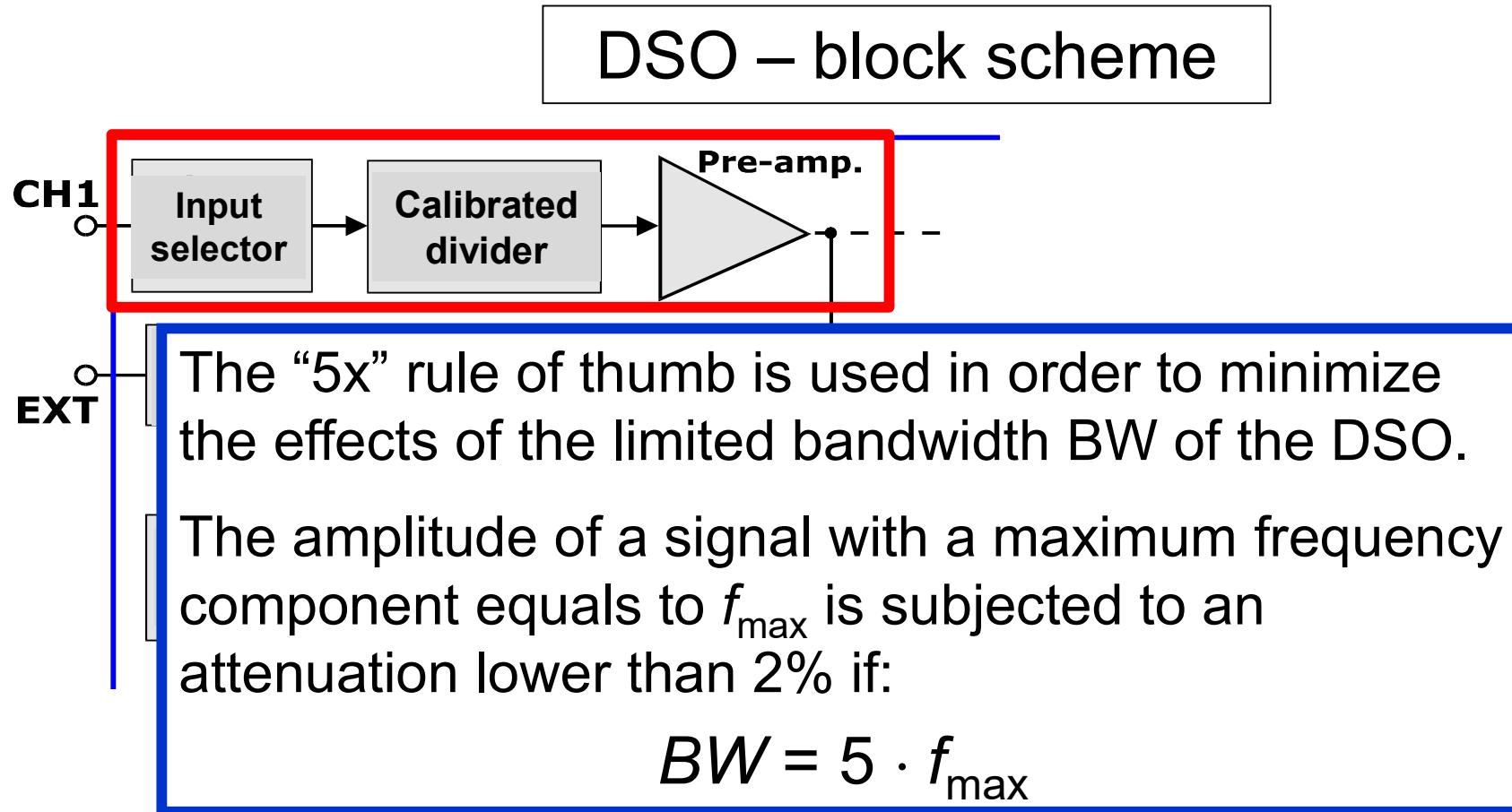
↳ DSO configured to measure (CH1-CH2) in the MATH menu



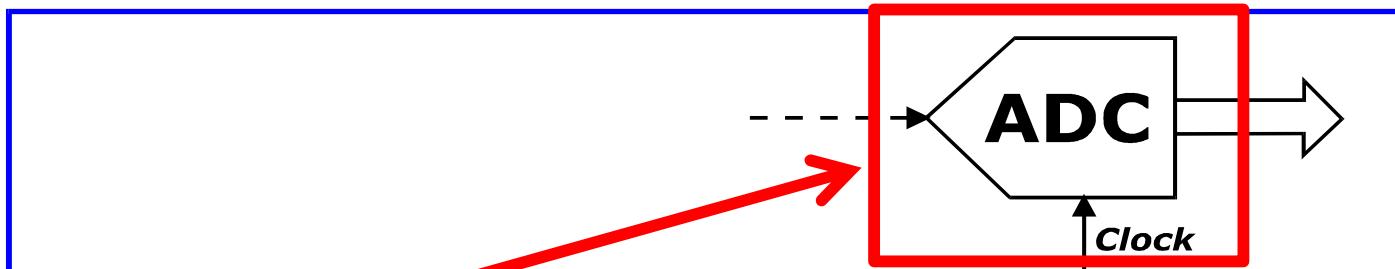








## DSO – block scheme



**The Analog-to-Digital Converter returns a sequence of numerical codes that represent the samples of the input analog signal**

The main parameter of interest is the sampling rate  $f_s$ , which is expressed in sample per second (Sa/s) or in Hertz (Hz). The «sampling theorem» has to be met in order to correctly rebuild the signal waveform on the display of the DSO:

$$f_s > 2 \cdot f_{\max}$$

## DSO – block scheme



WARNING: often one ADC for n channels

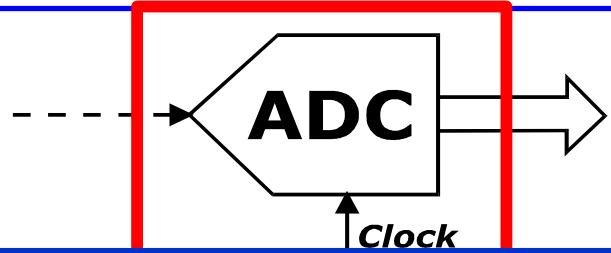
The A/D converter sequentially samples the samples of the input analog signal

The main parameter of interest is the sampling rate  $f_s$ , which is expressed in sample per second (Sa/s) or in Hertz (Hz).

The «sampling theorem» has to be met in order to correctly rebuild the signal waveform on the display of the DSO:

$$f_s > 2 \cdot f_{\max}$$

## DSO – block scheme

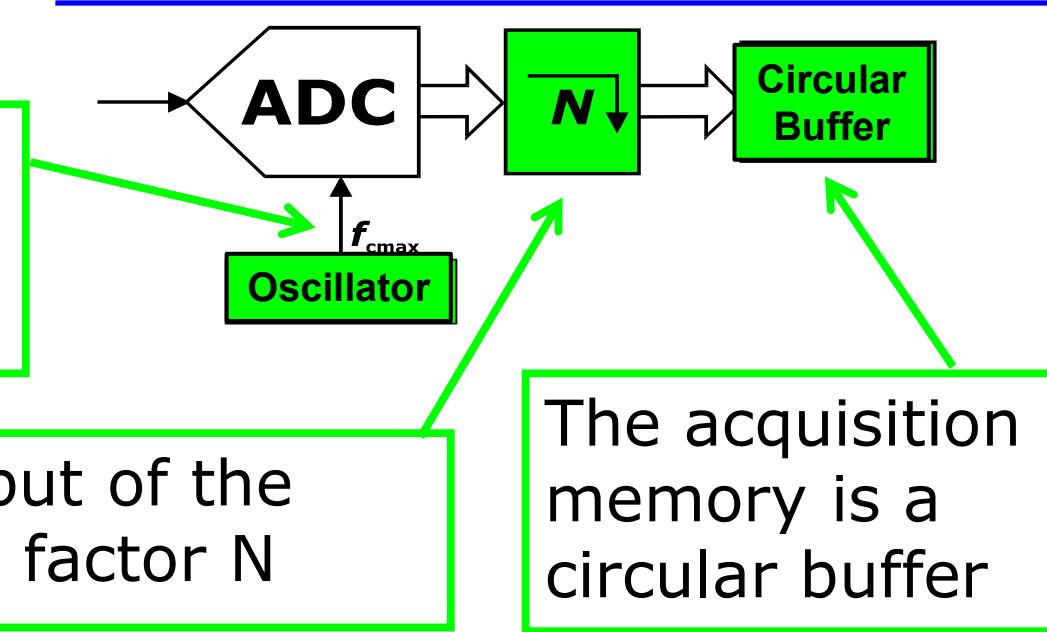


### Example

$$f_s = 1 \text{ GSa/s}$$

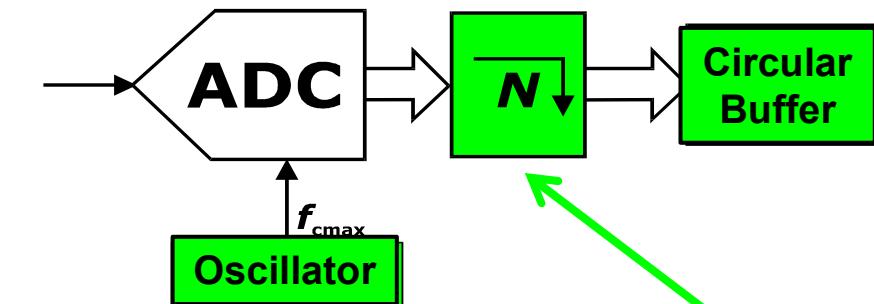
- ↳ Signals with frequency content up to about  $f_s / 2.5 = 400 \text{ MHz}$  can be correctly rebuilt.
- ↳ Otherwise, a waveform different than the input signal is shown on the display **(ALIASING)**

## DSO – block scheme



**The ADC continuously samples the input signal**  
↳ **The trigger event does not start the acquisition process**

## DSO – block scheme



This block allows the number of sample points to be reduced when the signal is oversampled

### Example

$f_{Smax} = 1 \text{ GSa/s}$ ; periodical input signal with  $f_0 = 1 \text{ kHz}$

Time/div set to 0.1 ms/div  $\rightarrow$  Display time-interval  $D_t = 1 \text{ ms}$

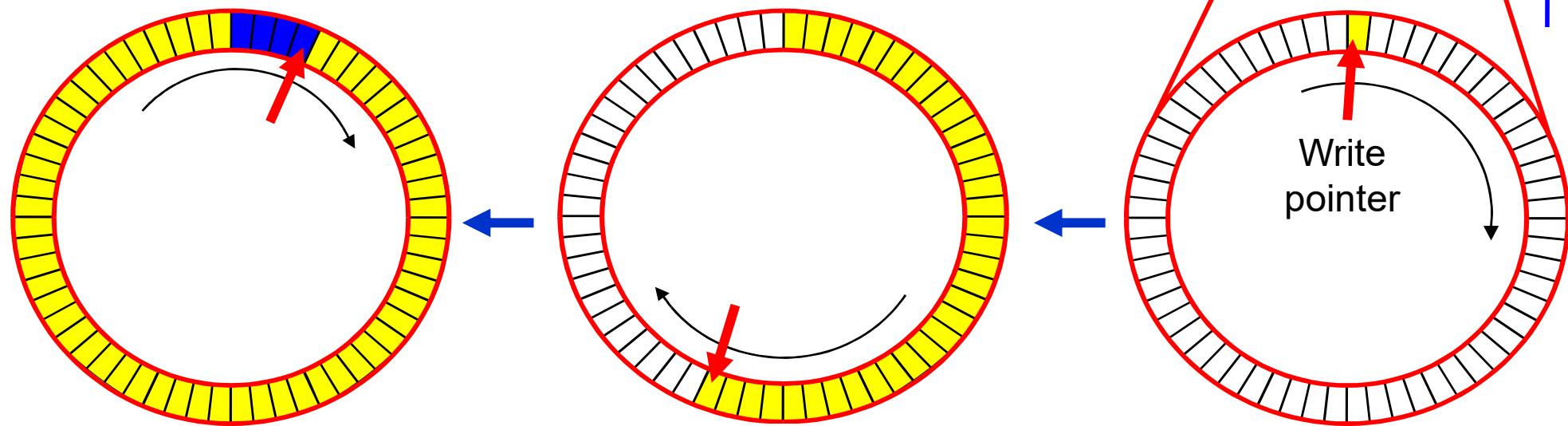
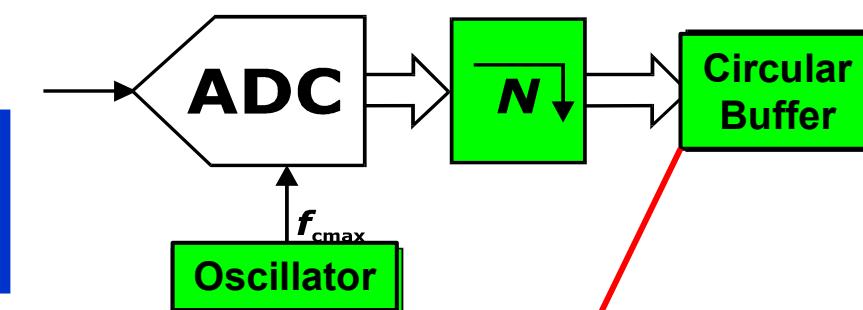
    ⇒ Number of samples at the output of the ADC: 1 MSa!!!

The decimation factor depends on the Time/div setting

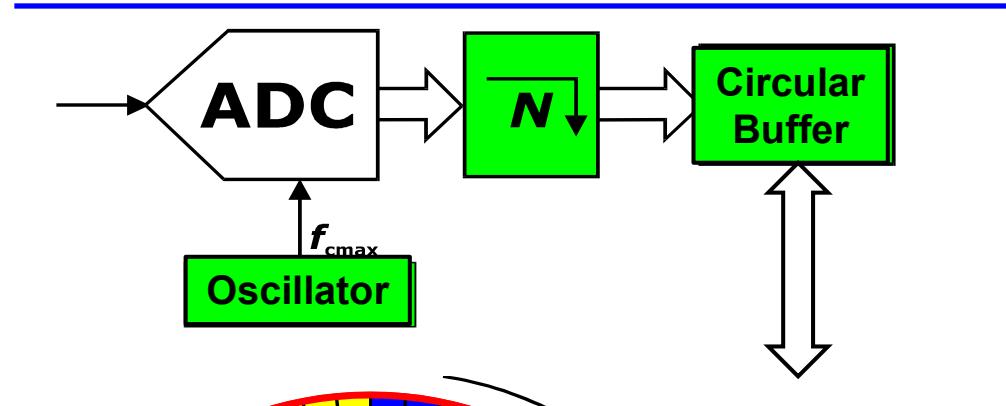
# Digital Storage Oscilloscope

## DSO – block scheme

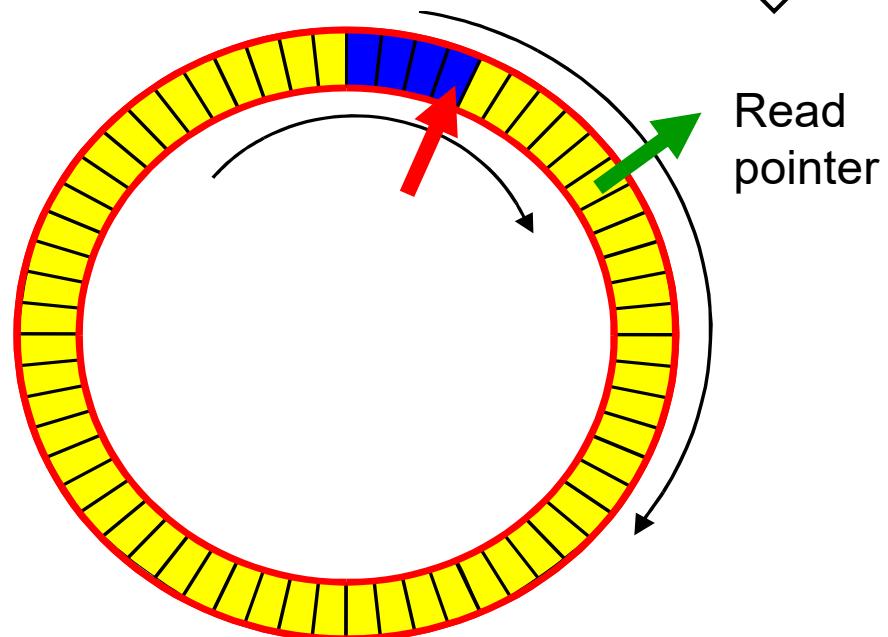
The write pointer has a rate that is  $f_{S\max}/N$



## DSO – block scheme

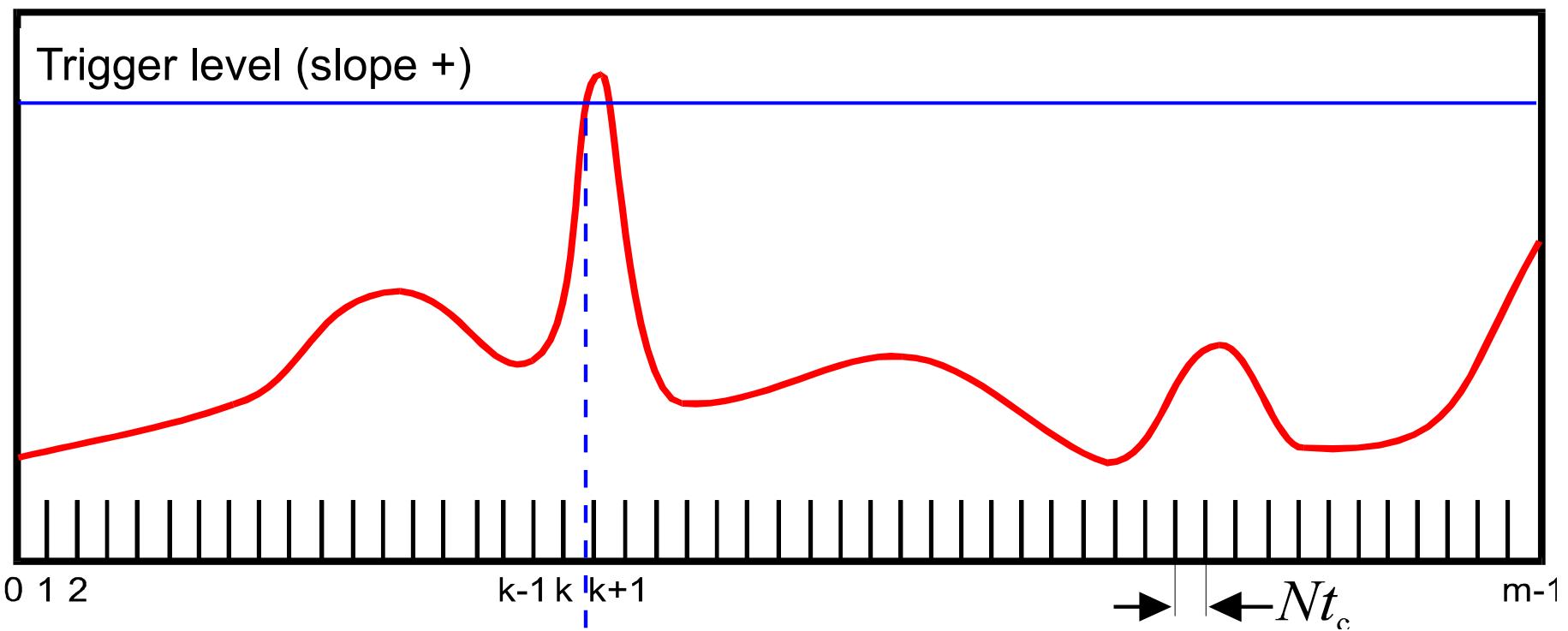


The read pointer scans the memory block that is transferred to the internal memory



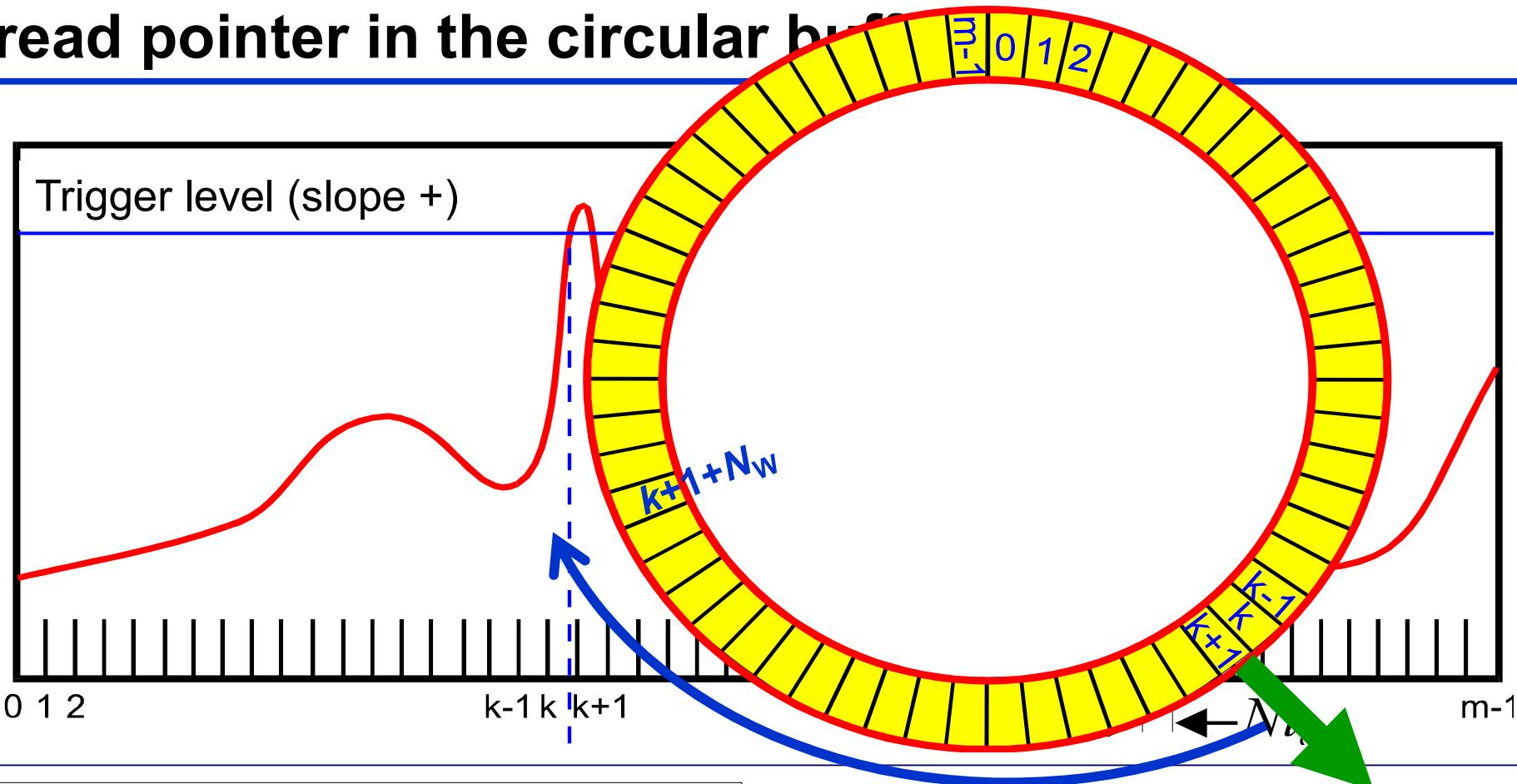
## DSO – block scheme

The *trigger event* set the starting position of the read pointer in the circular buffer



## DSO – block scheme

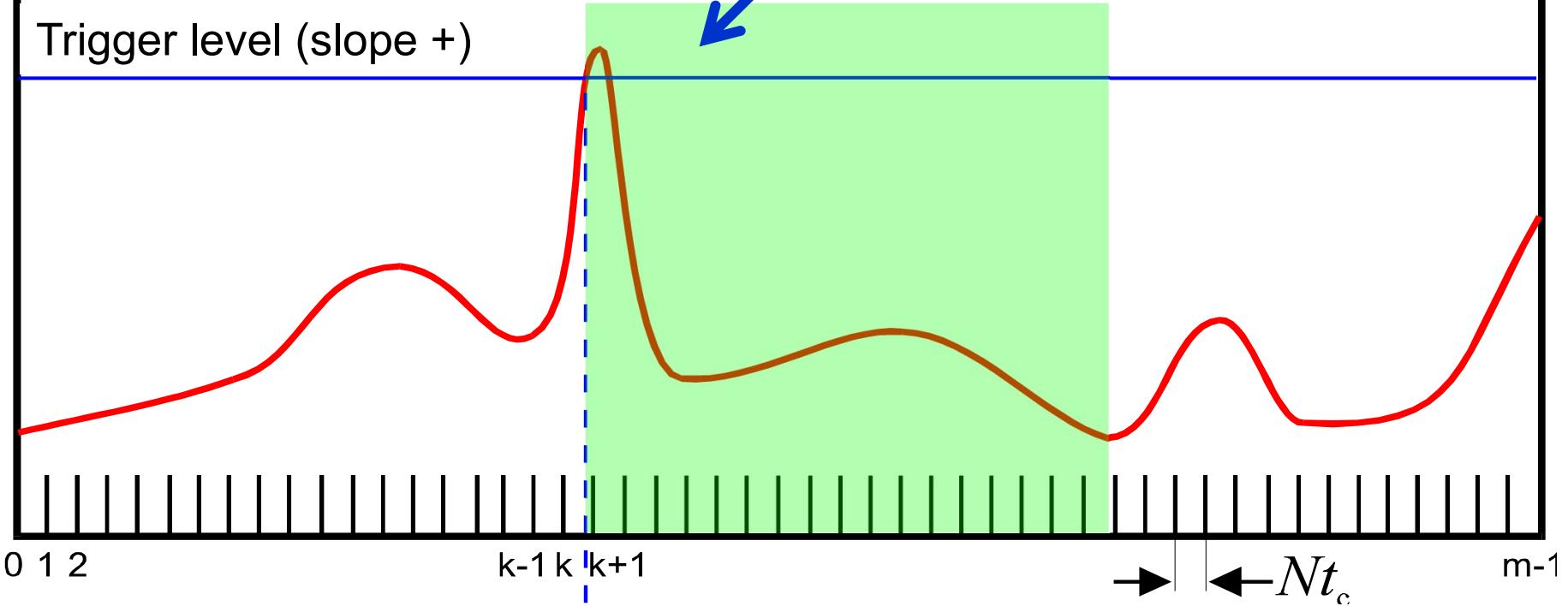
The *trigger event* set the starting position of the read pointer in the circular buffer.



## DSO – block scheme

Part of the signal that is shown on the display of the DSO

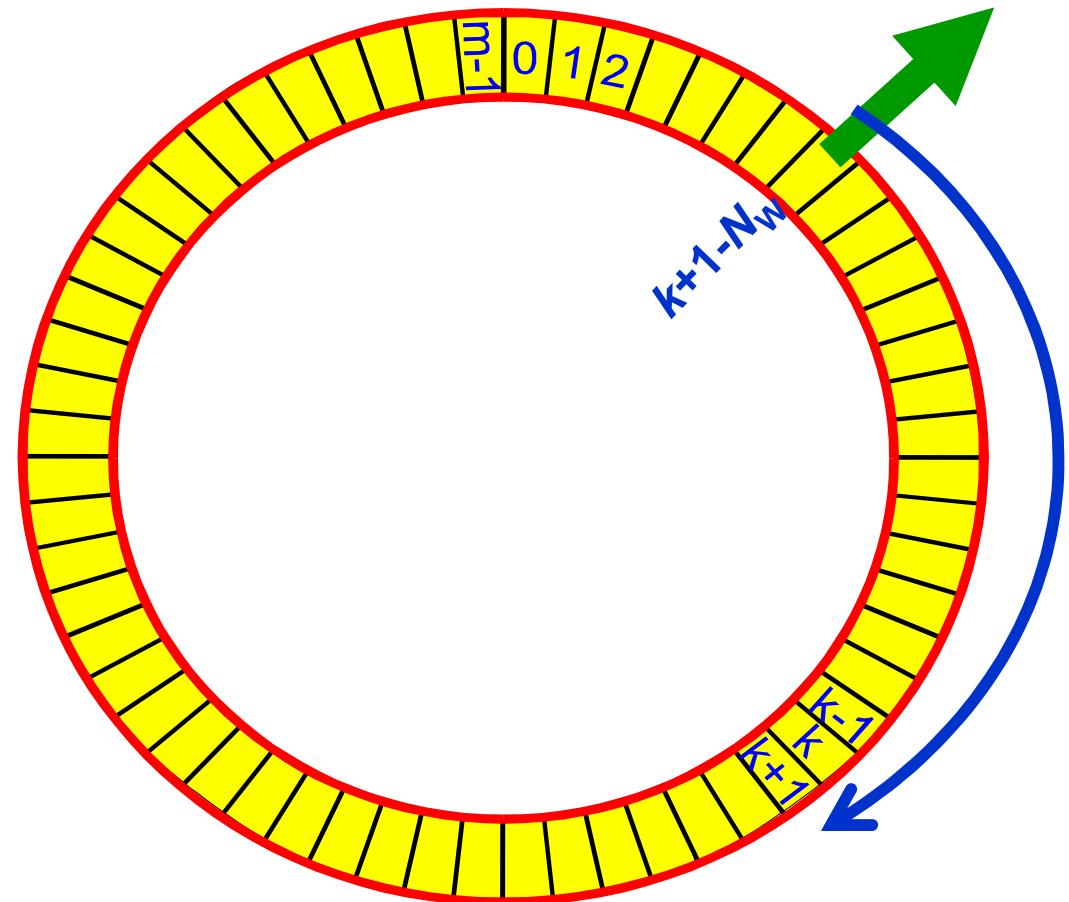
👉 *post-trigger*



## DSO – block scheme

The circular buffer also includes the samples that precede the trigger event

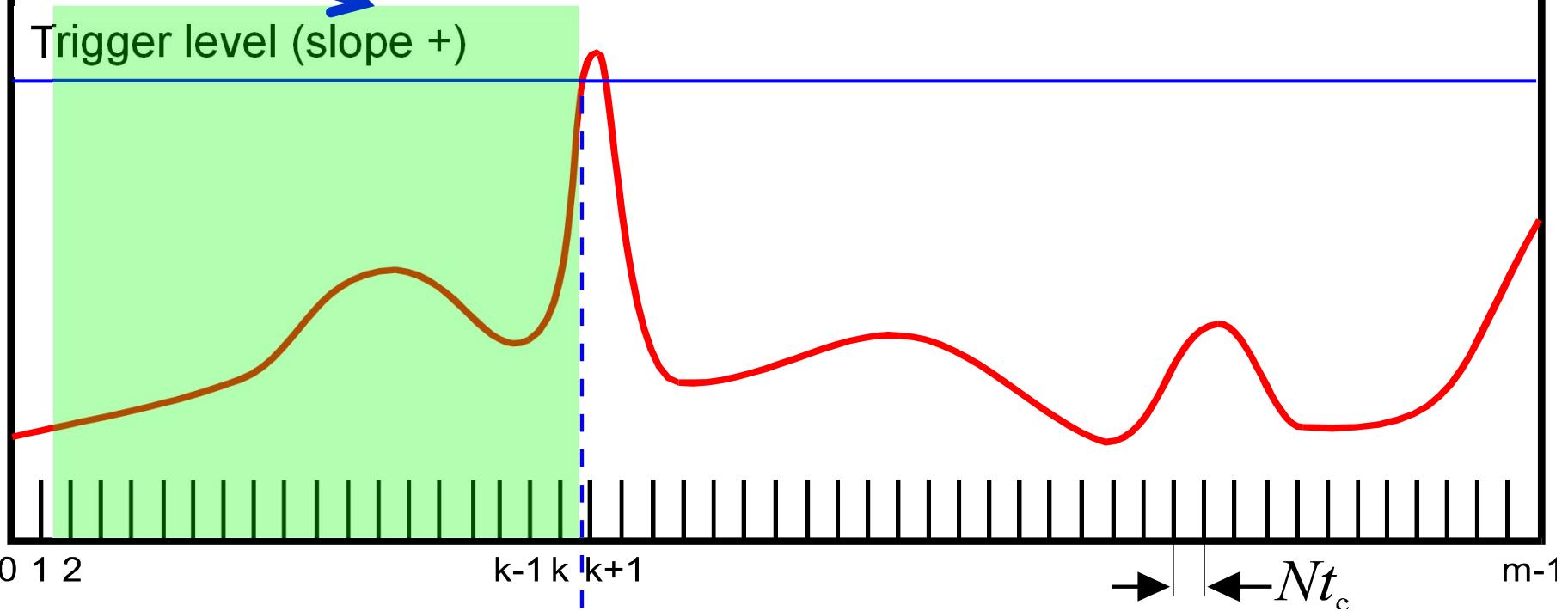
- They can be transferred to the internal memory through a suitable position of the read pointer



## DSO – block scheme

Part of the signal that is shown on  
the display of the DSO

➡ *pre-trigger*

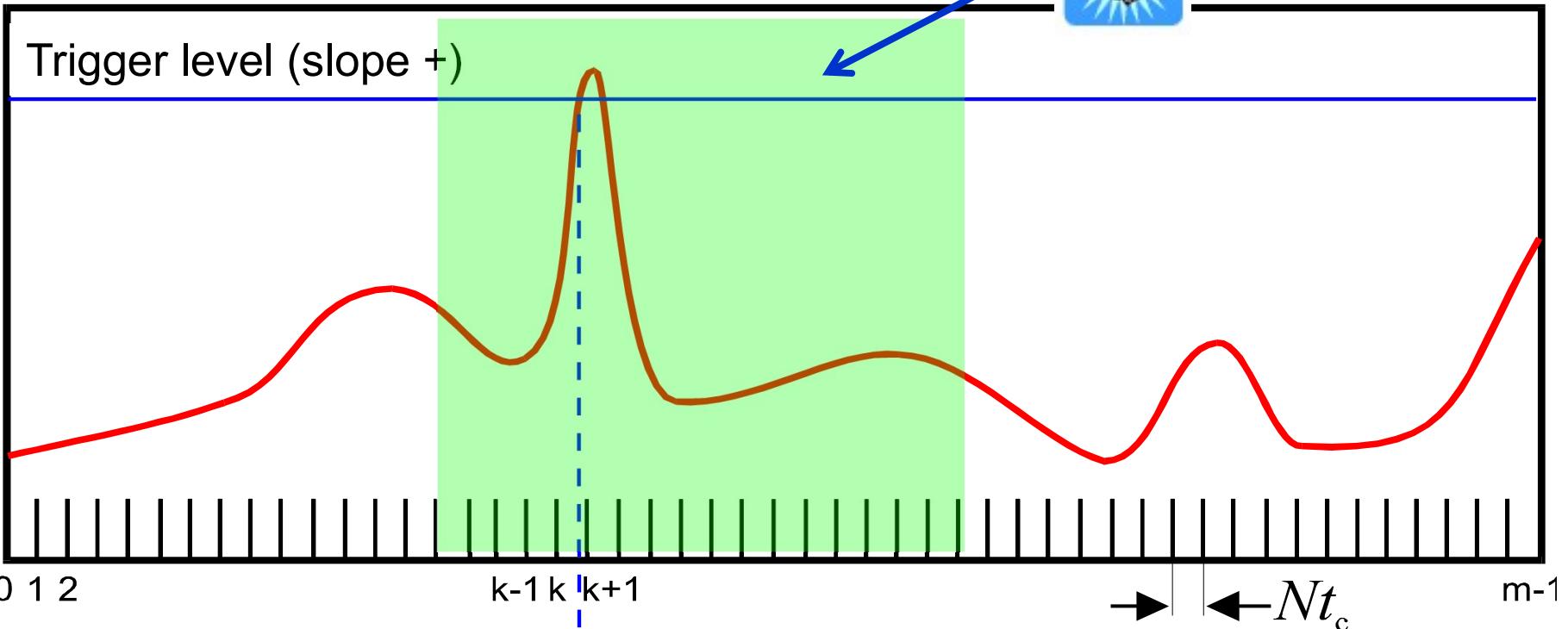


## DSO – block scheme

It is also possible to transfer to the internal memory a part of samples before and after the trigger



***pre/post-trigger***





## DSO – block scheme

### Management of the acquisition process

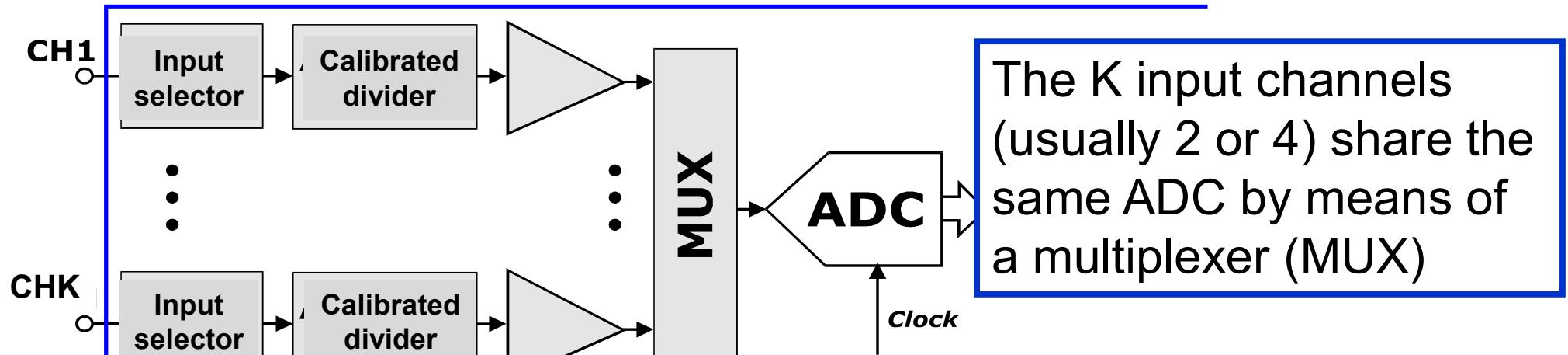
Once the samples have been transferred to the internal memory, they can be stored until another trigger event occurs

**The display of the DSO can be continuously updated both for repetitive signals and transient signals**

- ➡ **This is one of the main advantage of the DSO if compared to the analogue oscilloscope**

## DSO – block scheme

### Multi-channel DSO – low-cost solution

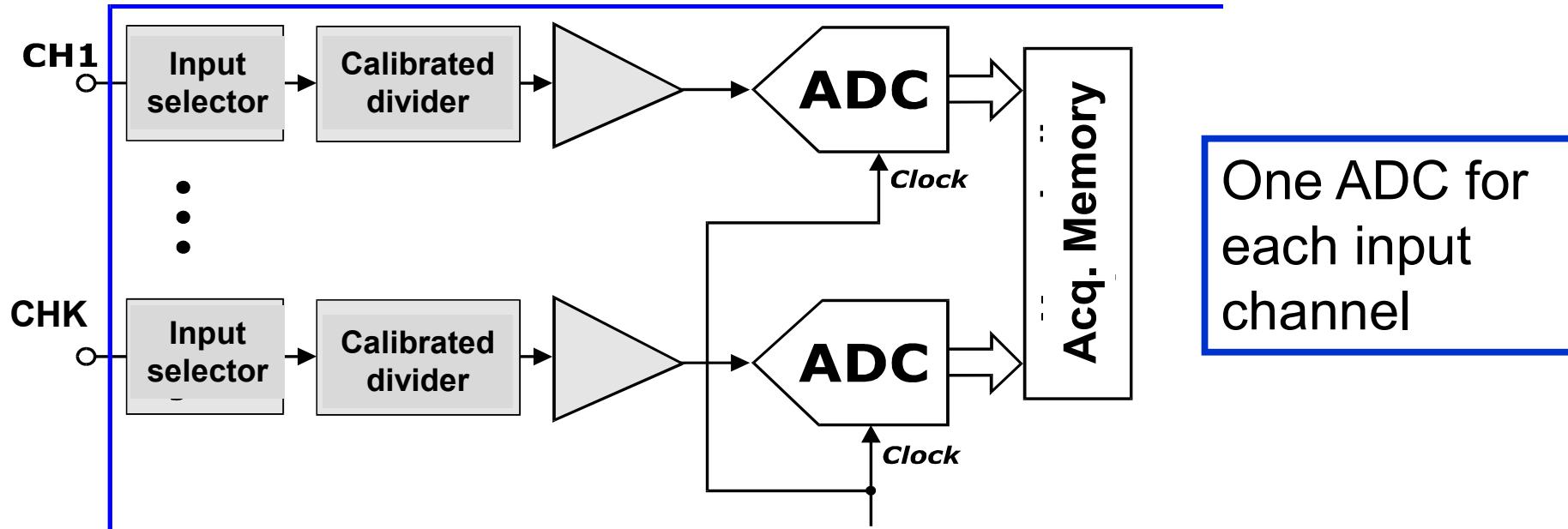


#### Main drawbacks

- ↳ Each channel is sampled at the frequency  $f_{\text{Smax}}/K$  (or lower)
- ↳ The samples of the different channels are not simultaneous
- ↳ The *cross-talk* between the MUX input channels is not negligible

## DSO – block scheme

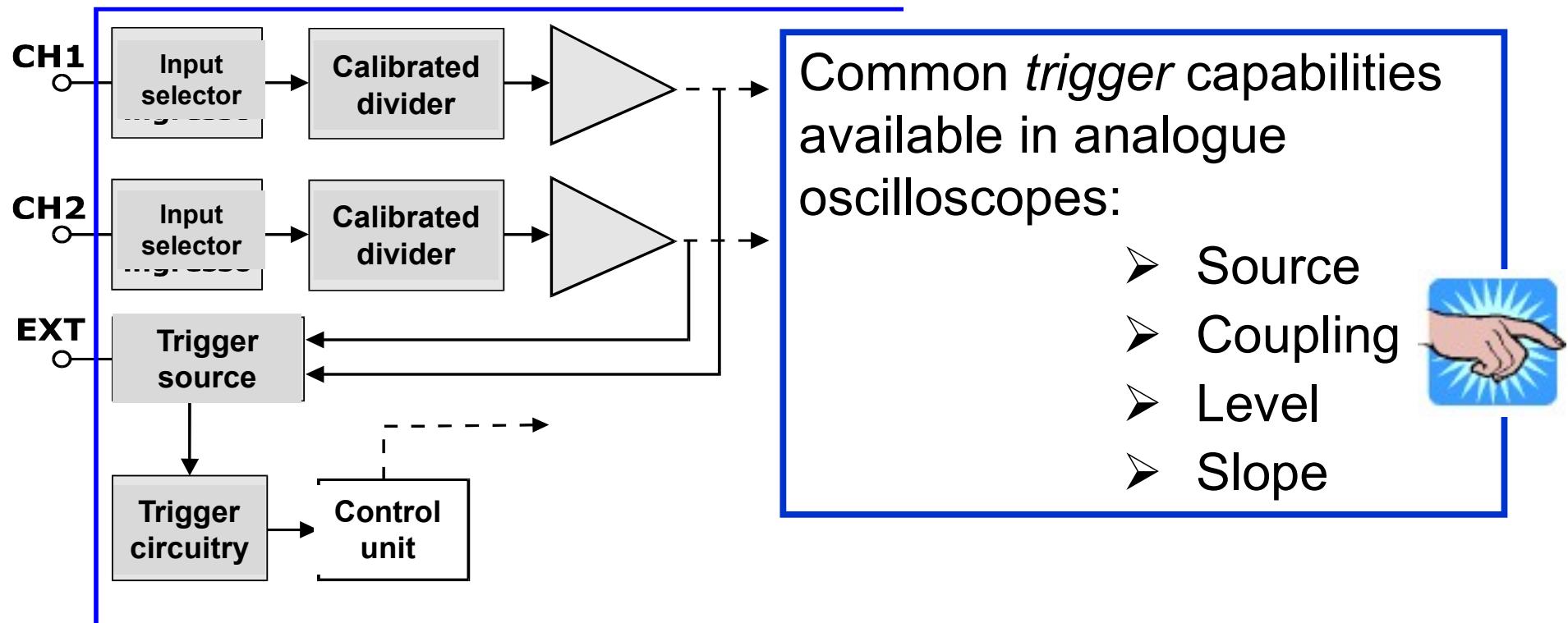
### Multi-channel DSO – high-performance solution



The previous problems are avoided, but ...  
:( Expensive solution

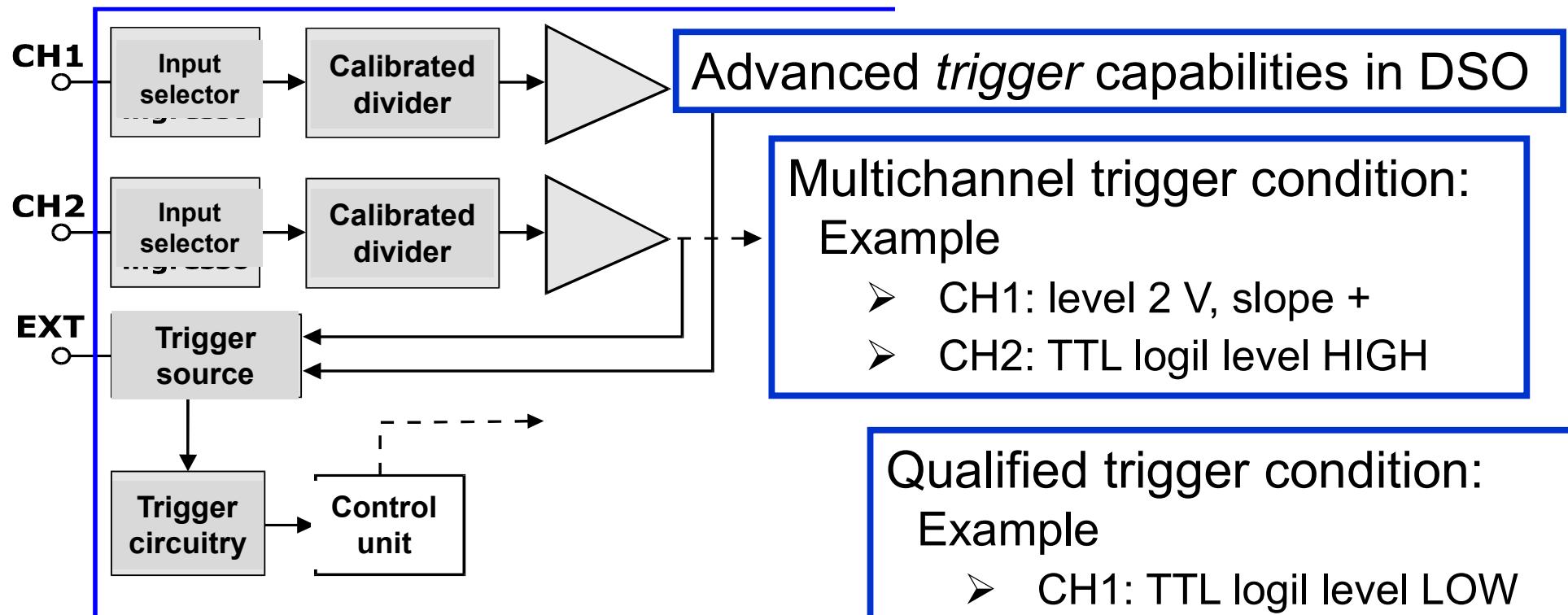
## DSO – block scheme

### Trigger capabilities



## DSO – block scheme

### Trigger capabilities



## DSO – block scheme

### Trigger capabilities



#### EXAMPLE

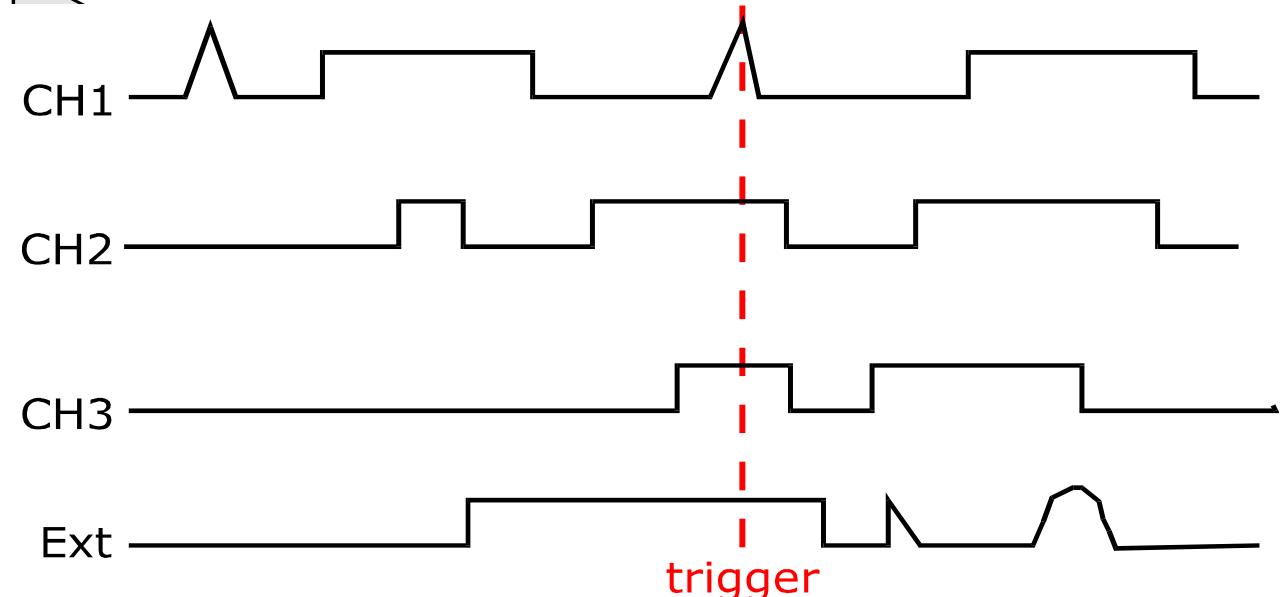
Trigger condition:

CH1: H per  $t < 10$  ns

CH2: X

CH3: H

External: X



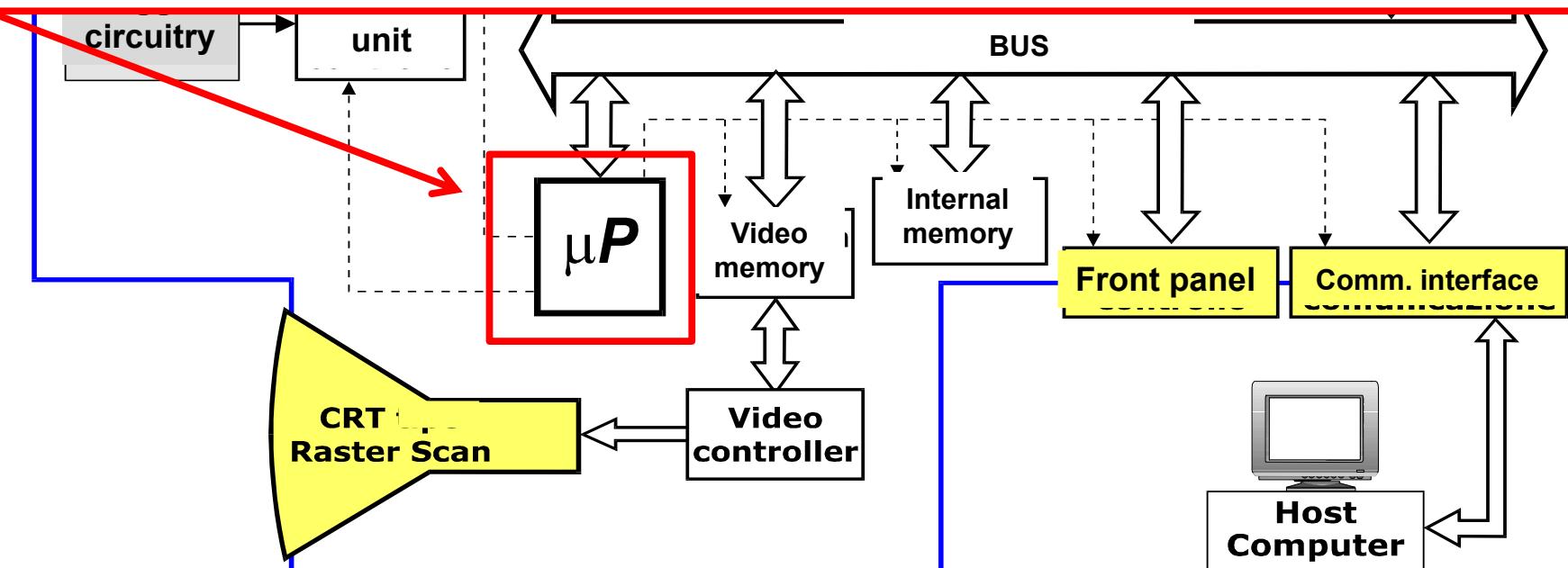
circuitry

unit

## DSO – block scheme

**The micro-processor manages the whole system and processes the samples in the internal memory**

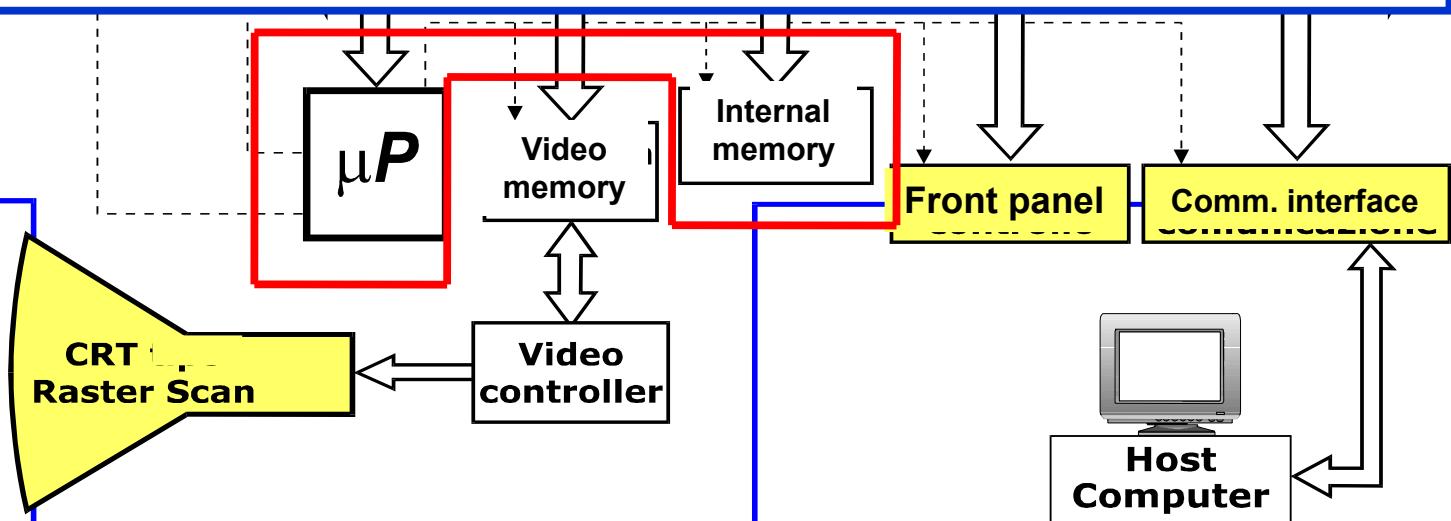
- In modern DSOs more than one  $\mu P$  are used, each one dedicated to a specific function (acquisition, processing, visualization, ...)



## DSO – block scheme

The samples in the internal memory can be processed according to different algorithms:

- ↳ Interpolation
- ↳ Evaluation of amplitude ( $V_{pp}$ ,  $V_{mean}$ ,  $V_{rms}$ , ...) and time ( $T$ , PW,  $t_s$ , ...) parameters
- ↳ Spectral analysis (Fast Fourier Transform)

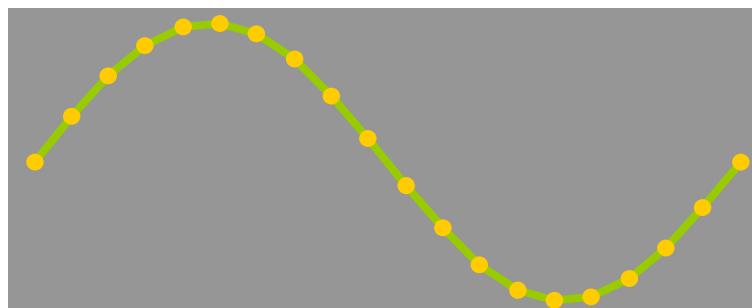


## DSO – Configuration problems

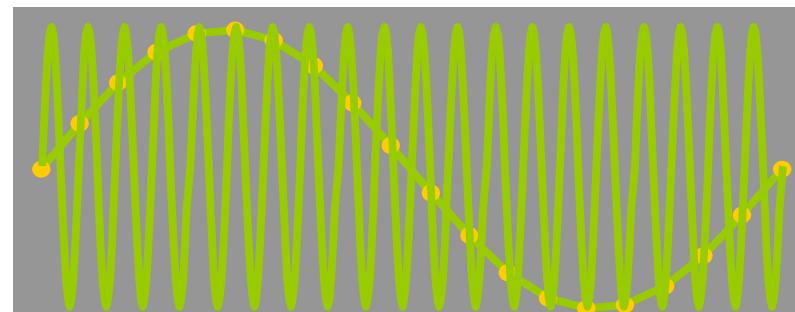
If the sampling rate (set by the Time/div configuration) is not suitable for the input analogue signal

- ↳ Aliasing phenomena
- ↳ The waveform on the display of the DSO is different than the input signal

It seems a correct signal ...



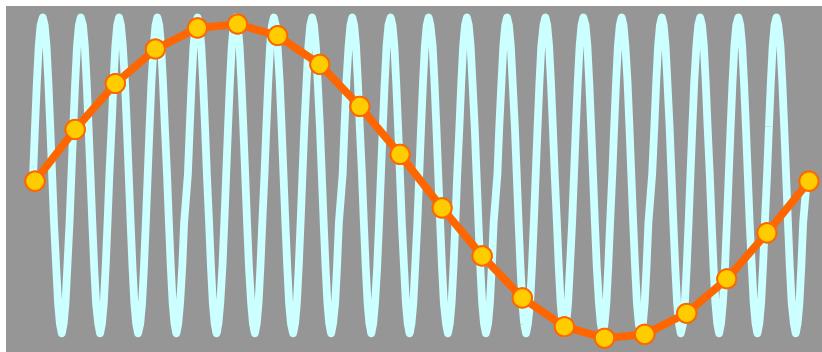
... but in true it is a subsampled signal



## DSO – Configuration problems

Aliasing phenomena can be highlighted by inconsistent waveforms at different Time/div configurations

Configuration 1



Configuration 2

