Applied Electronics

Logic, Comparator, Oscillator Exercises

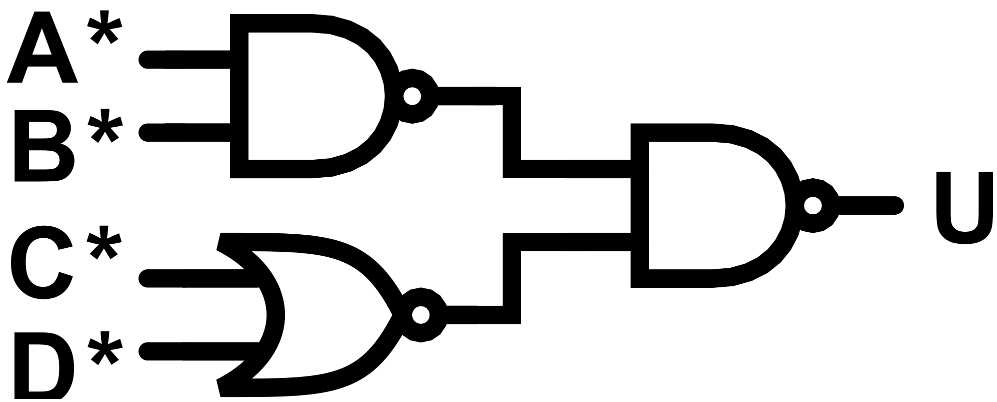
E1: CMOS Logic Gates

- Implement through CMOS logic gates the following logic function: $U = \bar{A} \cdot \bar{B} + \overline{C \cdot D}$

- $U = \bar{A} \cdot \bar{B} + \overline{C \cdot D} = \overline{\overline{\bar{A} \cdot \bar{B} + \overline{C \cdot D}}} = \overline{\left(\overline{\bar{A} \cdot \bar{B}}\right) \cdot \left(\overline{\bar{C} + \bar{D}}\right)}$

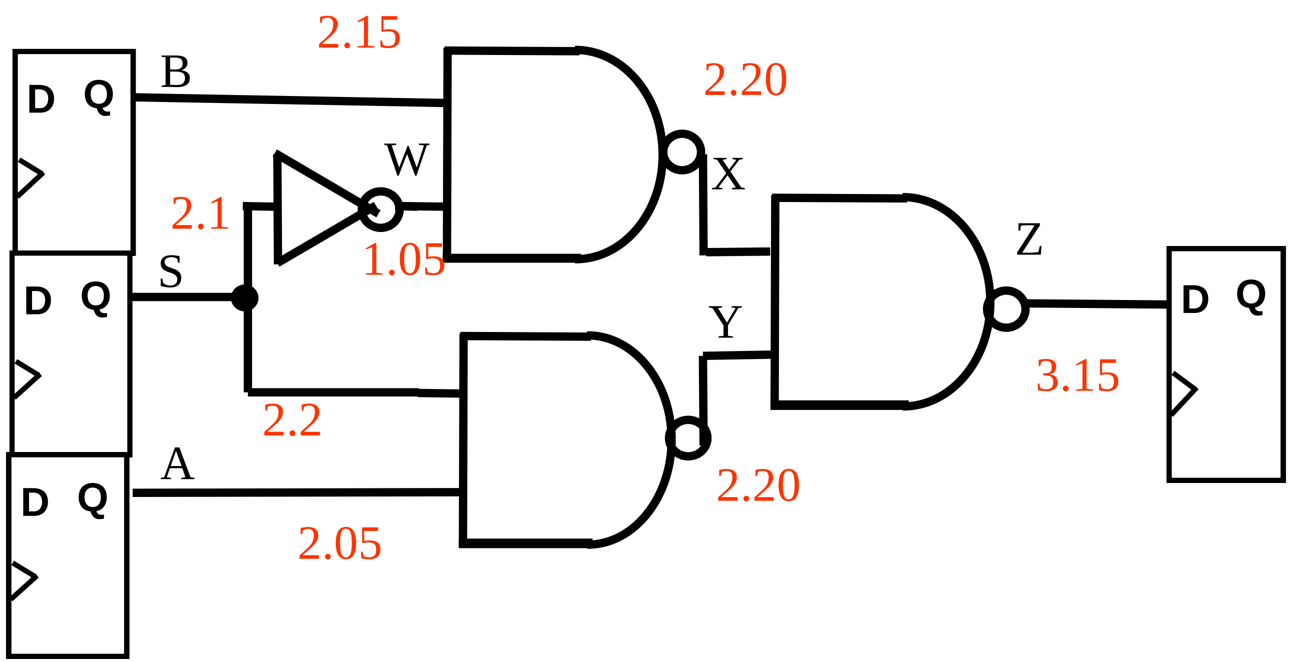
E1: CMOS Logic Gates – Design

- $U = \bar{A} \cdot \bar{B} + \overline{C \cdot D} = \overline{\overline{\bar{A} \cdot \bar{B} + \overline{C \cdot D}}} = \overline{\left(\overline{\bar{A} \cdot \bar{B}}\right) \cdot \left(\overline{\bar{C} + \bar{D}}\right)}$



E2: Calculation of delays and $F_{\mathbf{max}}$

- Analyze the delay of this circuit (delays in ns)
- Evaluate F_{max} of the clock signal if:
  $T_{\mathrm{SU}} = 1.5\ \mathrm{ns}$; $T_{\mathrm{H}} = 0.5\ \mathrm{ns}$



E2: Calculation of delays and $F_{\mathbf{max}}$

- Delays include t_{CKQ}

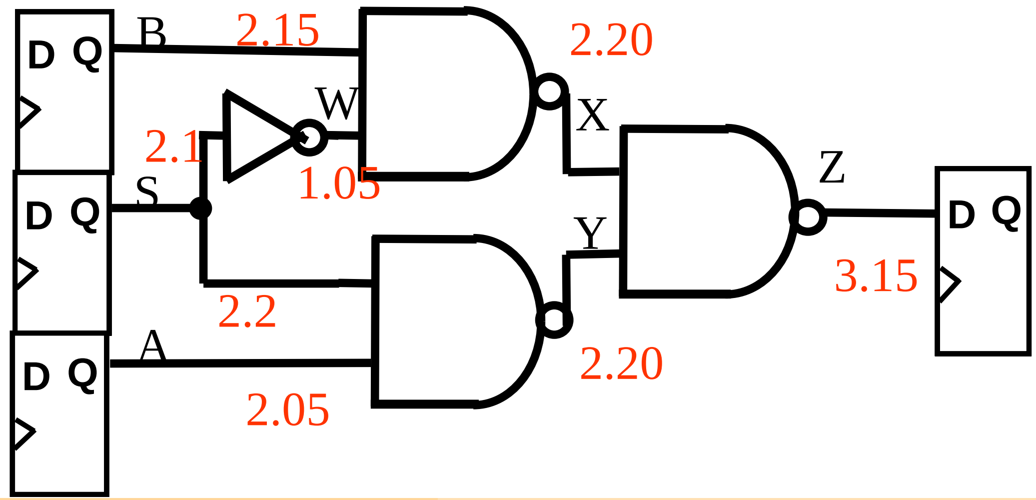
$$t_{\mathrm{B}\to\mathrm{D}} = 2.15\ \mathrm{ns} + 2.2\ \mathrm{ns} + 3.15\ \mathrm{ns} = 7.5\ \mathrm{ns}$$

$$t^1_{\mathrm{S}\to\mathrm{D}} = 2.1\ \mathrm{ns} + 1.05\ \mathrm{ns} + 2.2\ \mathrm{ns} + 3.15\ \mathrm{ns} = \mathbf{8.5\ ns} \leftarrow \text{max}$$

$$t^2_{\mathrm{S}\to\mathrm{D}} = 2.2\ \mathrm{ns} + 2.2\ \mathrm{ns} + 3.15\ \mathrm{ns} = 7.55\ \mathrm{ns}$$

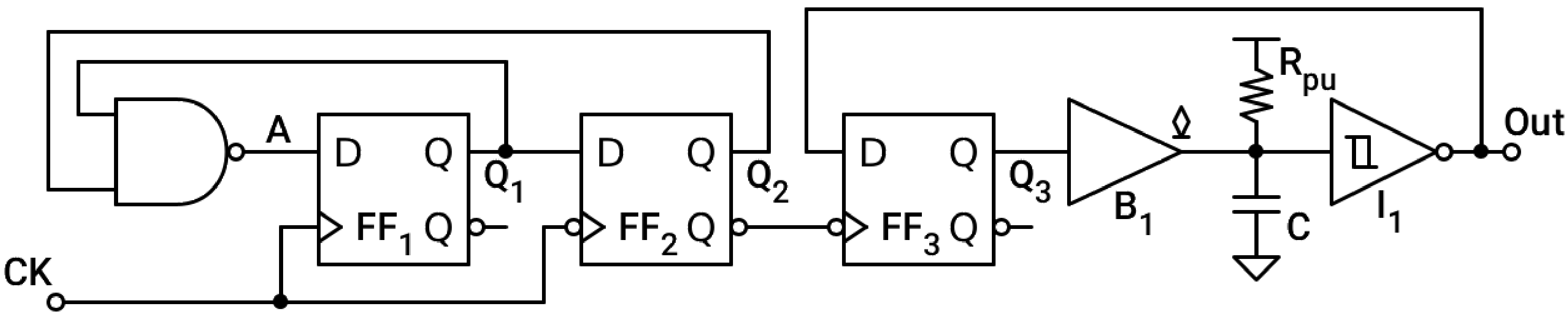
$$t_{\mathrm{A}\to\mathrm{D}} = 2.05\ \mathrm{ns} + 2.2\ \mathrm{ns} + 3.15\ \mathrm{ns} = \mathbf{7.4\ ns} \leftarrow \text{min}$$

$$\boldsymbol{F}_{\mathbf{max}} = \frac{1}{t^1_{\mathrm{S}\to\mathrm{D}} + t_{\mathrm{SU}}} = \frac{1}{8.5\ \mathrm{ns} + 1.5\ \mathrm{ns}} = \mathbf{100\ MHz}$$



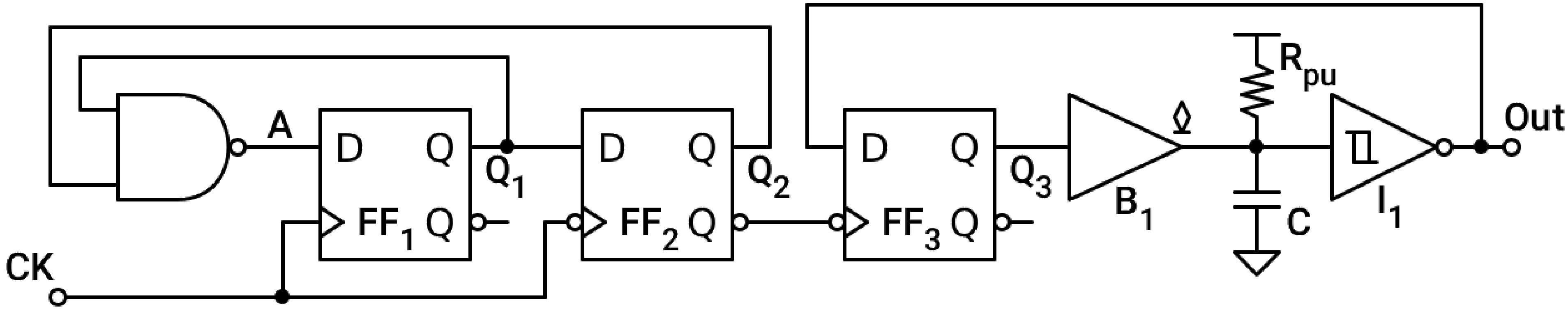
E3: Sequential Circuit

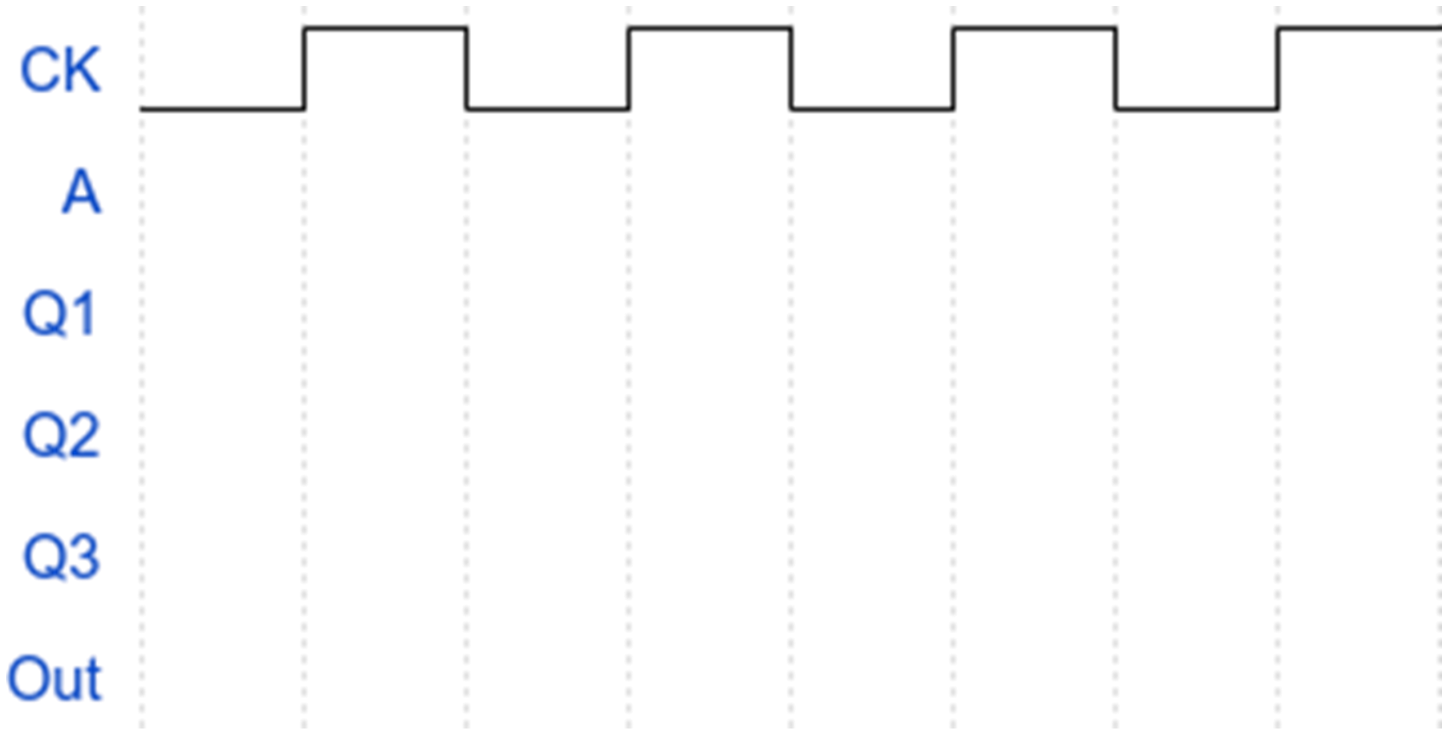
- The Q outputs are preset to 0. The clock has $50\ \%$ duty cycle. The open-drain buffer B_1 has $R_{\mathrm{ON}} = 40\ \Omega, I_{\mathrm{OH}} = 200\ \mu\mathrm{A}$. I_1 is a Schmitt trigger inverter with $V_{S_1} = 3\ \mathrm{V}$ and $V_{S_2} = 2\ \mathrm{V}$. Supply voltage: $5\ \mathrm{V}$.



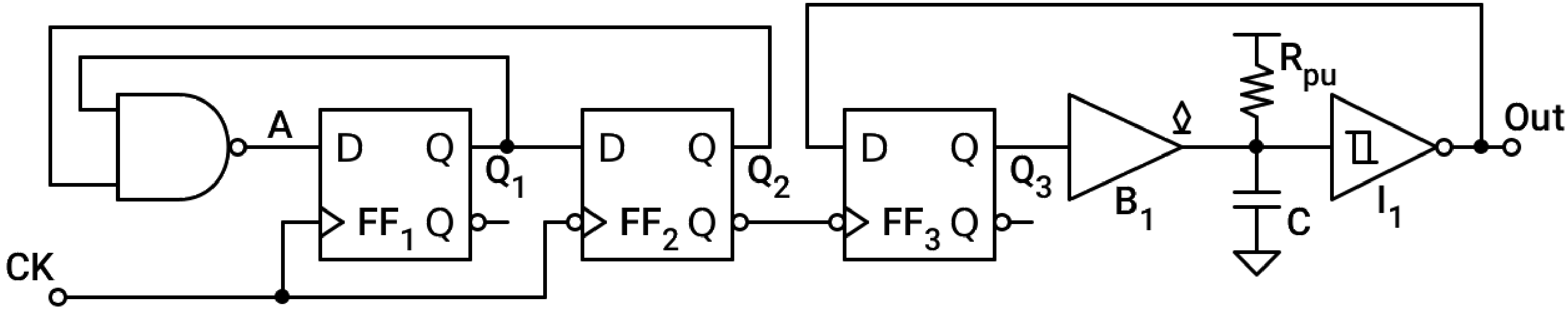
- Draw the waveforms at nodes A, Q_1, Q_2, Q_3 ,and Out for the first three periods of CK clock considering $C = 0\ \mathrm{F}$ and zero propagation delay for all components.

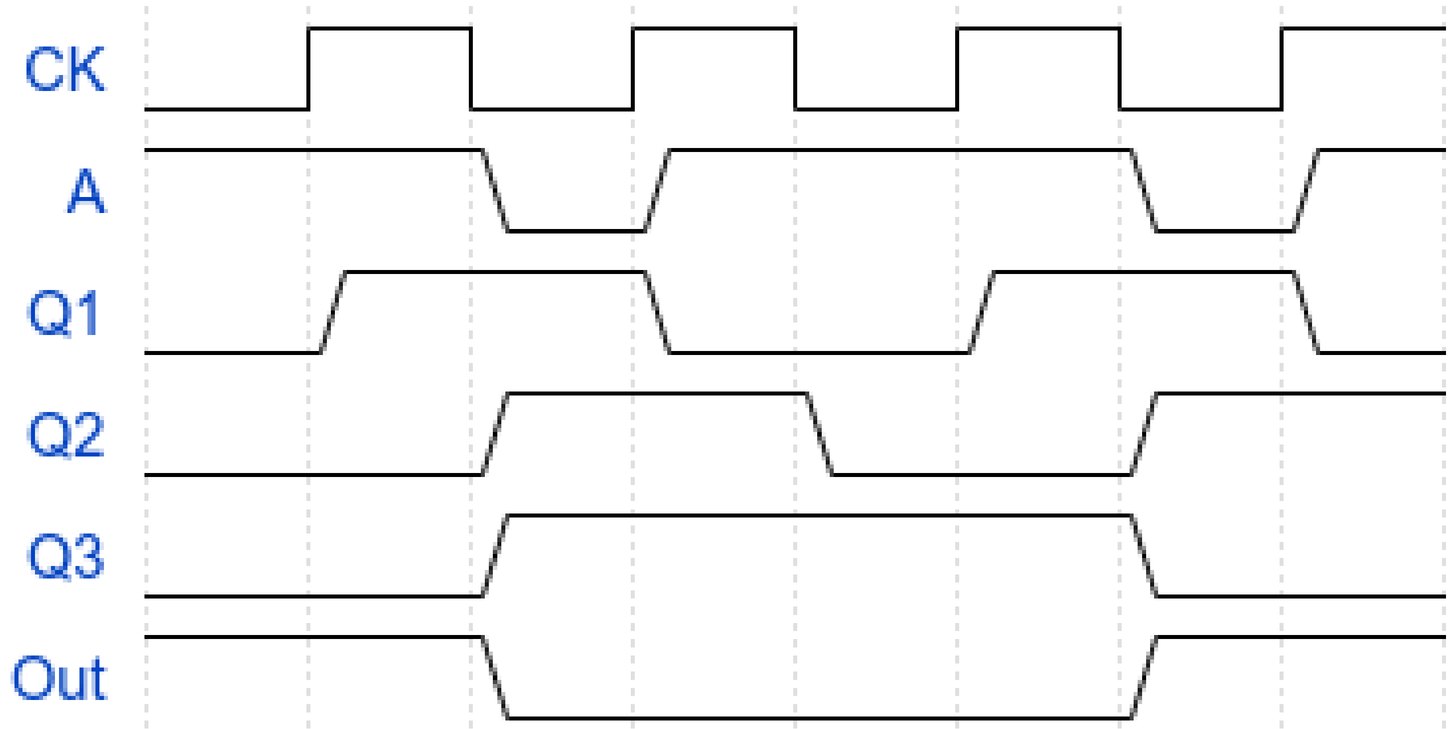
E3: Sequential Circuit: Signals and States



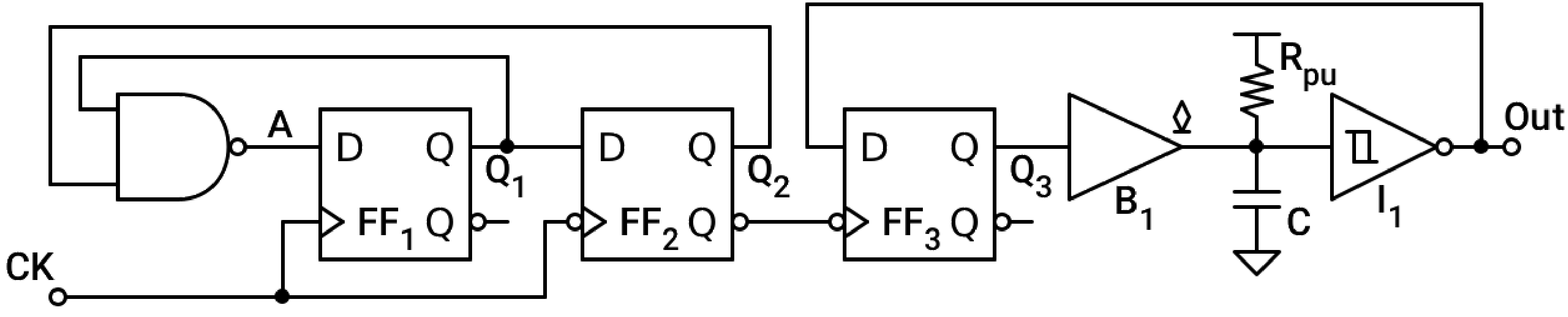


E3: Sequential Circuit: Signals and States



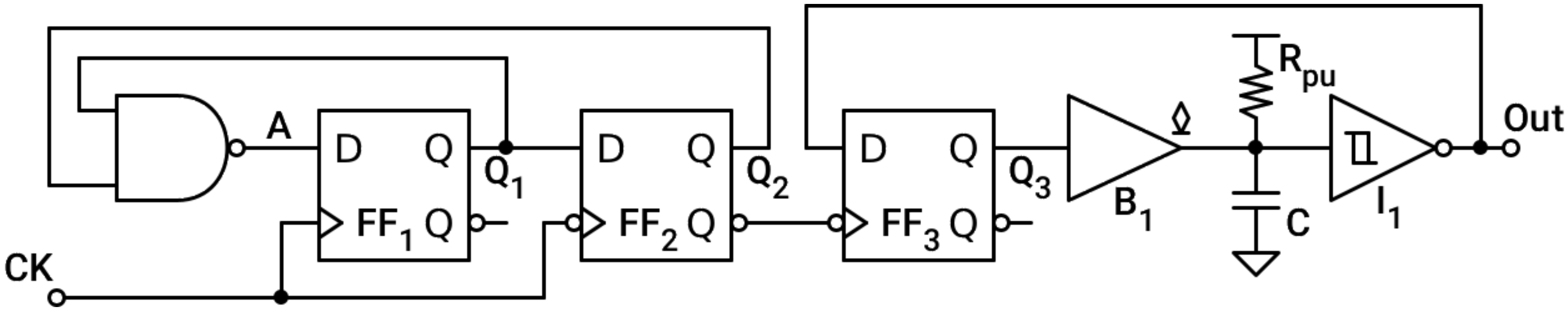


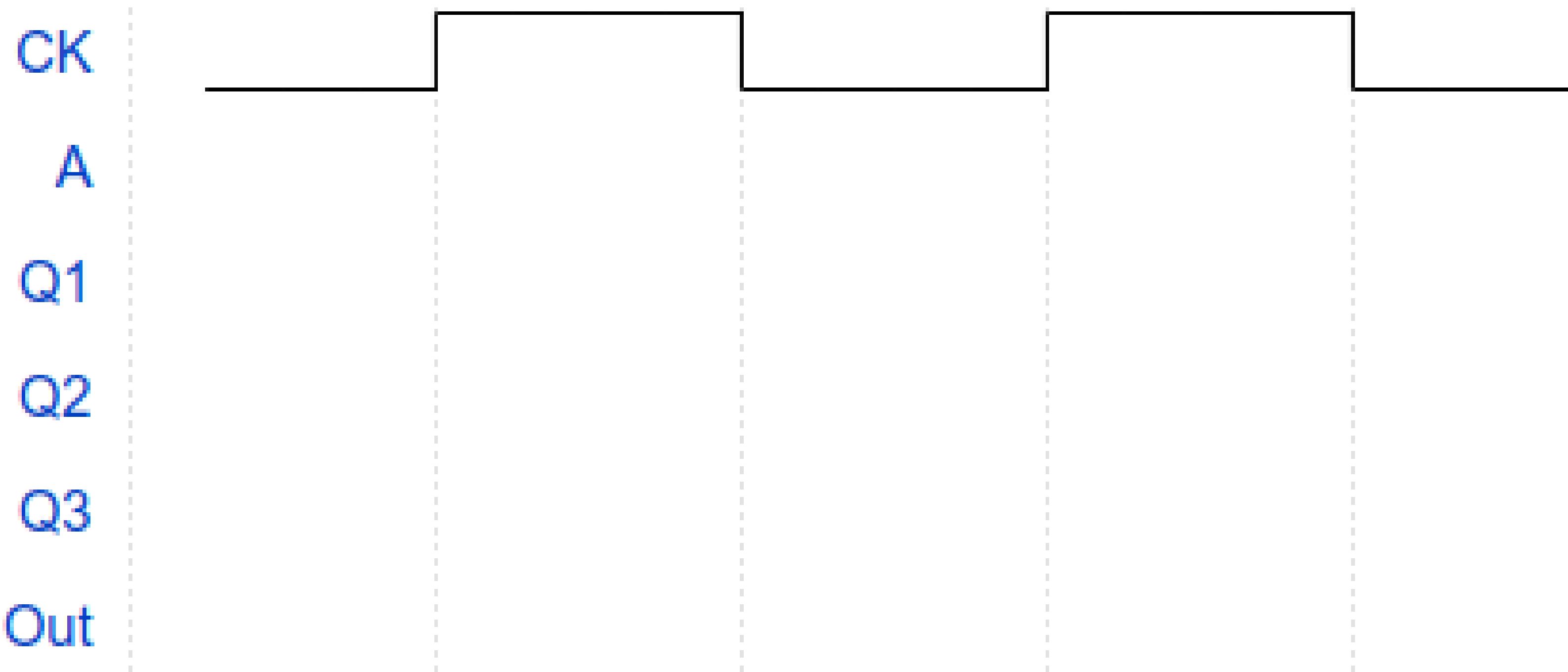
- Draw the waveforms for 2 clock periods on nodes A, Q_1, Q_2, Q_3 and Out for
  - $C = 0\,\mathrm{F}$
  - All FFs: $t_{\mathrm{SU}} = 3\,\mathrm{ns},\ t_{\mathrm{H}} = 2\,\mathrm{ns},\ t_{\mathrm{CKQ}} = 5\,\mathrm{ns}$
  - NAND and I_1: $t_{\mathrm{LH}} = 3\,\mathrm{ns},\ t_{\mathrm{HL}} = 4\,\mathrm{ns}$
  - B_1: $t_{\mathrm{P}} = 6\,\mathrm{ns}$ for both transitions $\mathrm{L} \rightarrow \mathrm{H}$ and $\mathrm{H} \rightarrow \mathrm{L}$



E3: Sequential Circuit: Delays

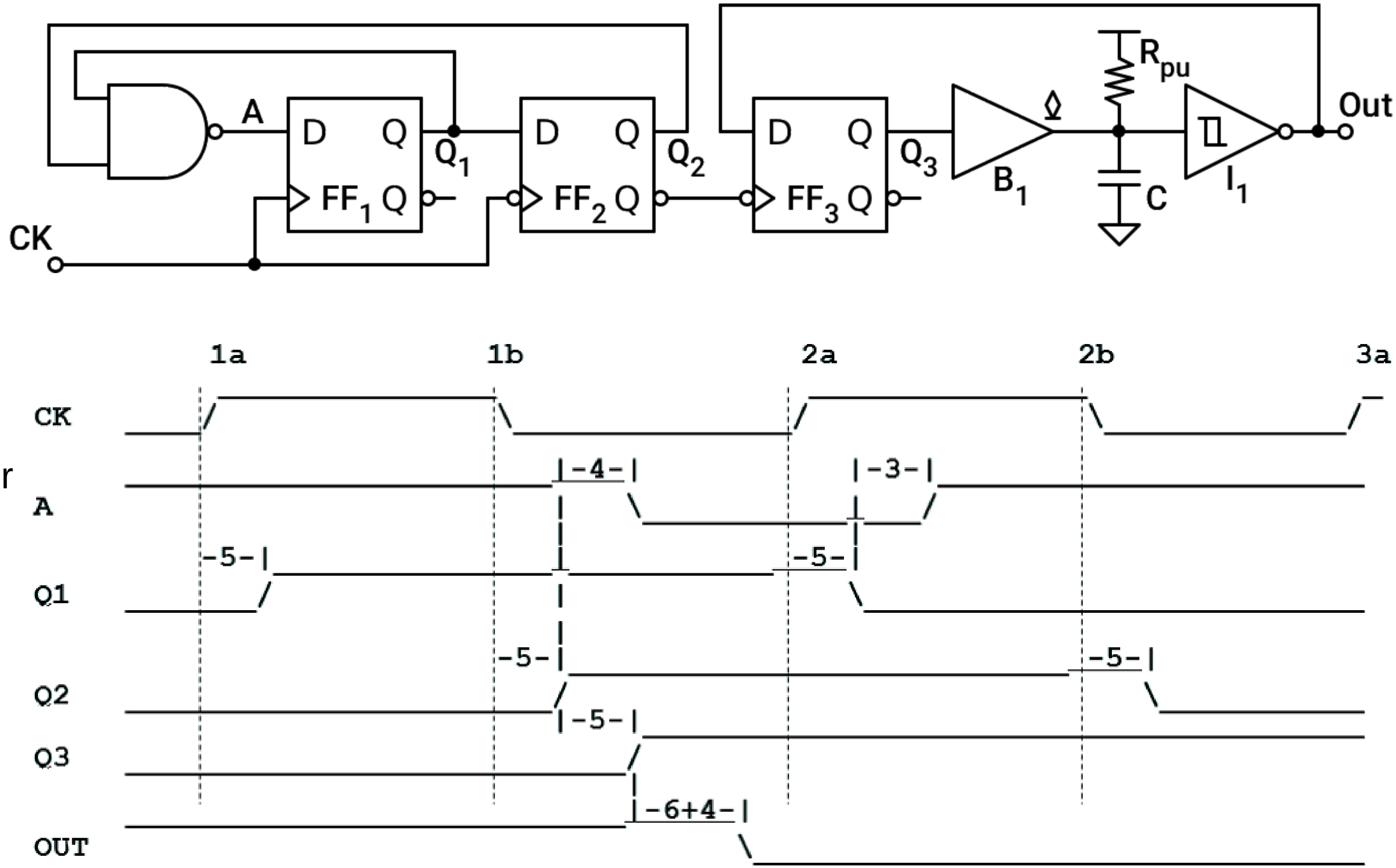
- $C = 0$ F
- FFs
  - $t_{SU} = 3\,\mathrm{ns}$
  - $t_{H} = 2\,\mathrm{ns}$
  - $t_{CKQ} = 5\,\mathrm{ns}$
- NAND and I_1
  - $t_{LH} = 3\,\mathrm{ns}$
  - $t_{HL} = 4\,\mathrm{ns}$
- B_1
  - $t_{P} = 6\,\mathrm{ns}$ for both $\mathrm{L} \rightarrow \mathrm{H}$ and $\mathrm{H} \rightarrow \mathrm{L}$ transitions

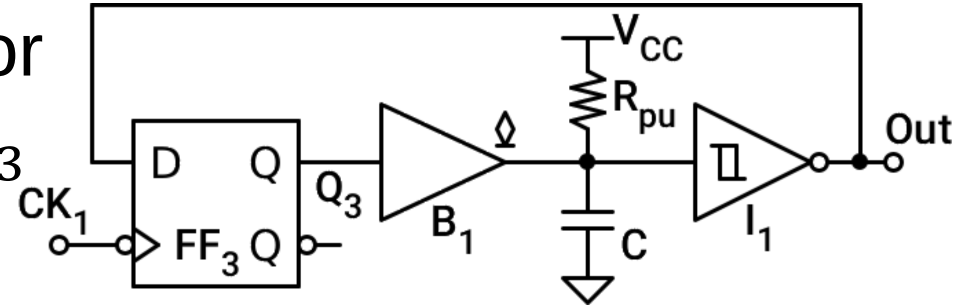




E3: Sequential Circuit: Delay Evaluation

- $C = 0\,\mathrm{F}$
- FFs
  - $t_{SU} = 3\,\mathrm{ns}$
  - $t_{H} = 2\,\mathrm{ns}$
  - $t_{CKQ} = 5\,\mathrm{ns}$
- NAND and I_1
  - $t_{LH} = 3\,\mathrm{ns}$
  - $t_{HL} = 4\,\mathrm{ns}$
- B_1
  - $t_P = 6\,\mathrm{ns}$ for both $\mathrm{L} \rightarrow \mathrm{H}$ and $\mathrm{H} \rightarrow \mathrm{L}$ transitions



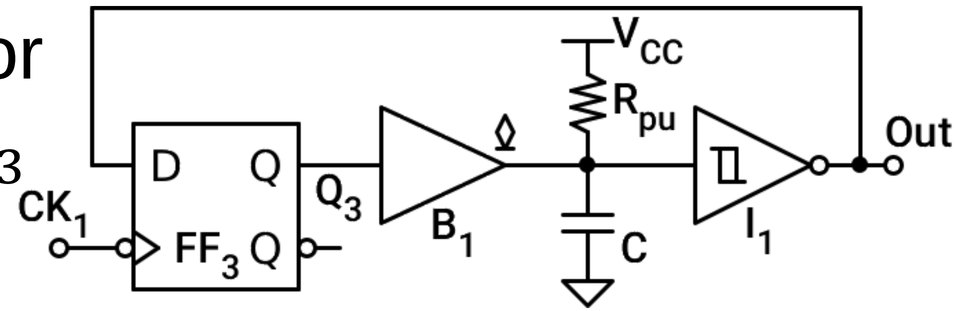


- Analyze the dynamic behavior of the loop $\mathrm{B_1} \to C \to \mathrm{I_1} \to \mathrm{FF_3}$

1. Draw qualitatively the signals Q_3, V_C, and Out
2. Determine maximum $f_{\mathrm{CK_1}}$ for
   - ♦ $R_\mathrm{PU} = 1\,\mathrm{k\Omega},\ C = 25\,\mathrm{pF},\ V_\mathrm{CC} = 5\,\mathrm{V}$
   - ♦ $V_{\mathrm{S_1}} = 3\,\mathrm{V},\ V_{\mathrm{S_2}} = 2\,\mathrm{V}$

E3: Sequential Circuit: V_{C} and V_{Out}

- Analyze the dynamic behavior of the loop $\mathrm{B}_1 \rightarrow C \rightarrow \mathrm{I}_1 \rightarrow \mathrm{FF}_3$



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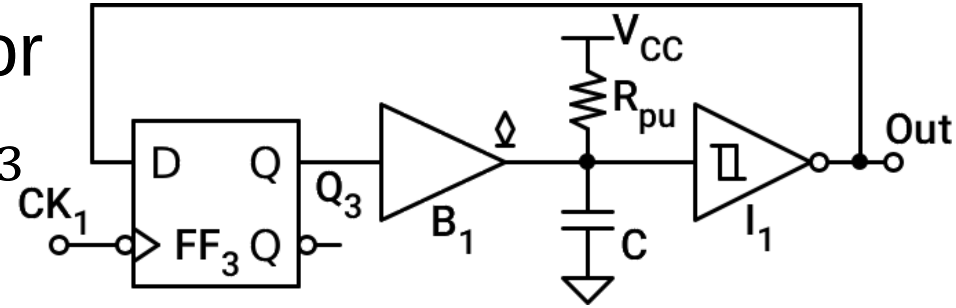

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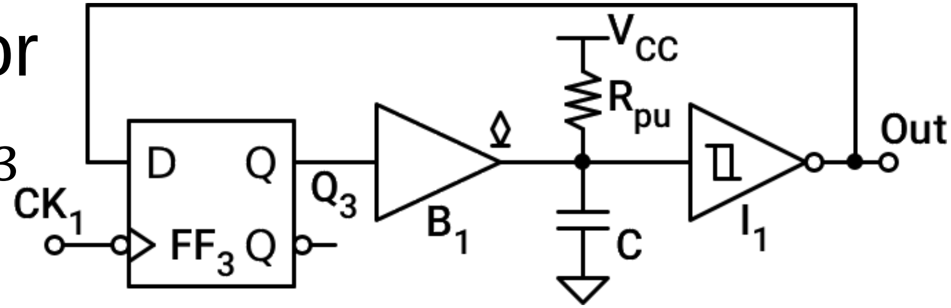

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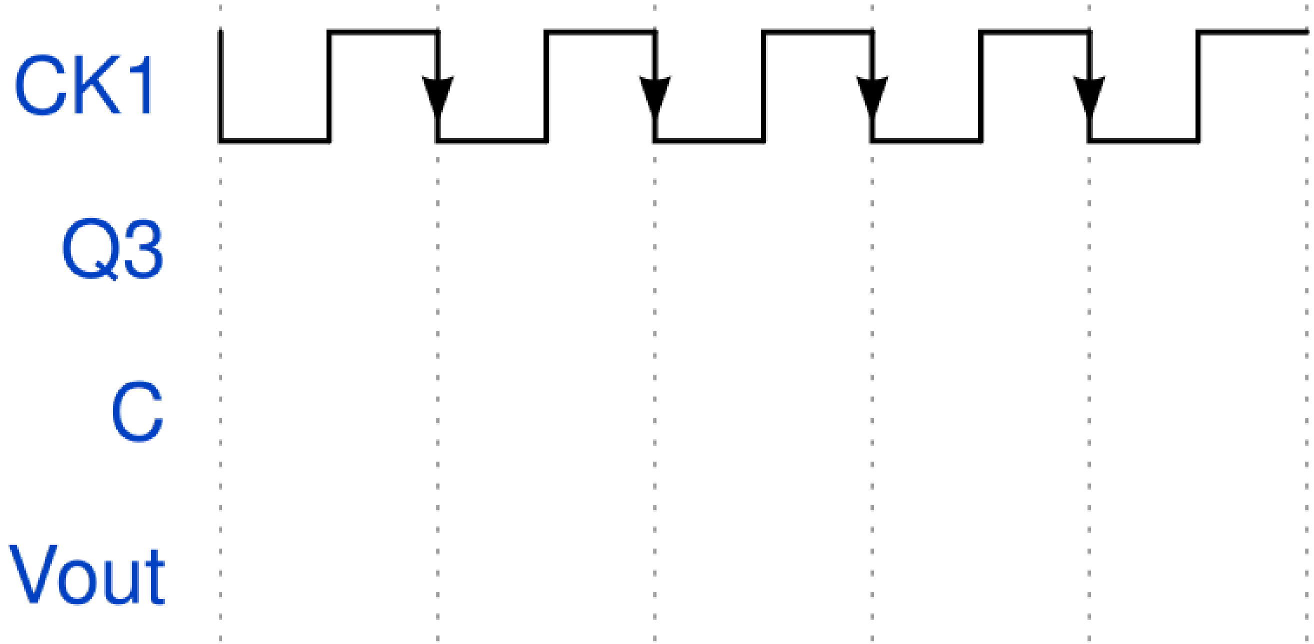

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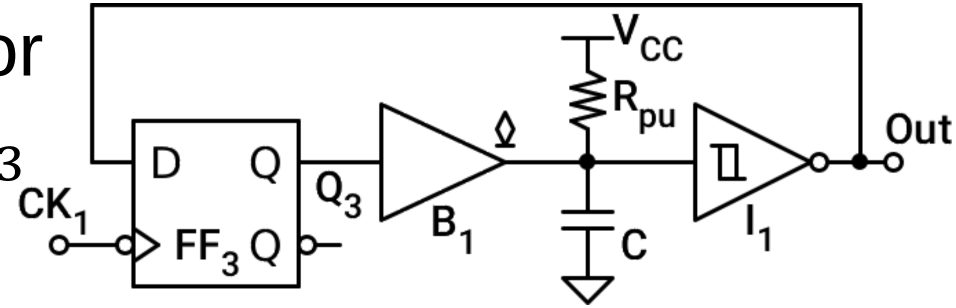

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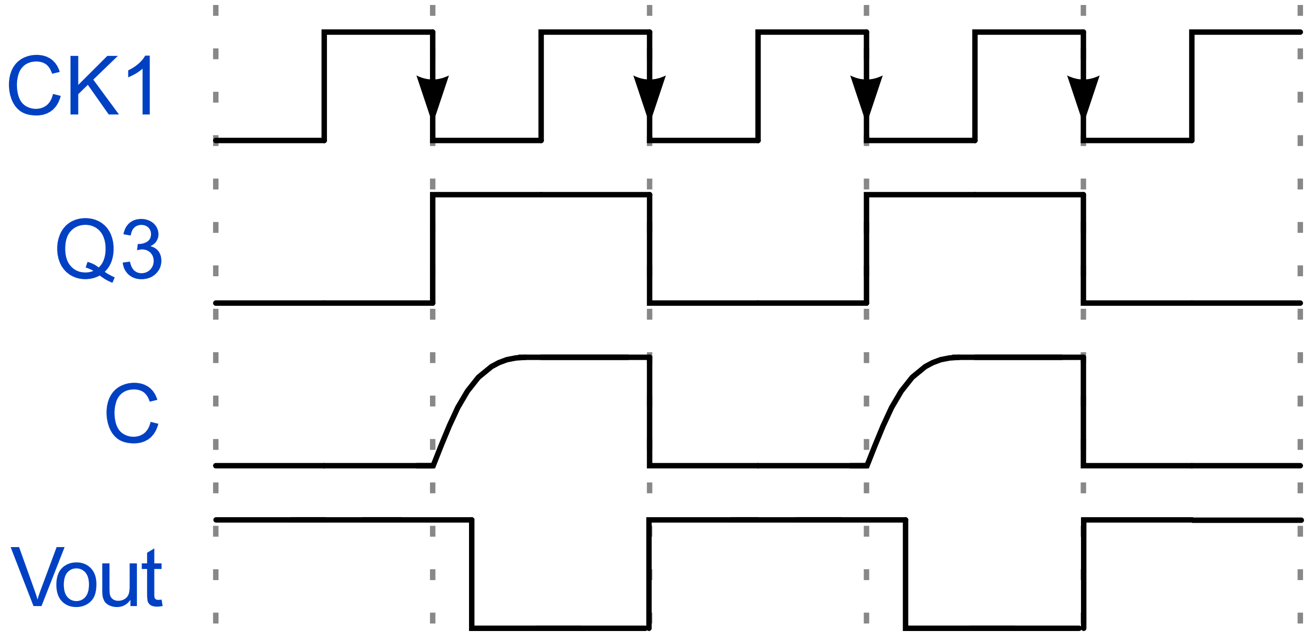
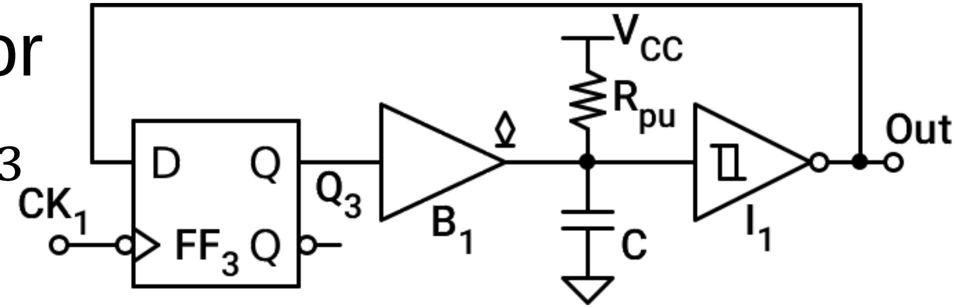


E3: Sequential Circuit: V_{C} and V_{Out}



- Analyze the dynamic behavior of the loop $\mathrm{B}_1 \rightarrow C \rightarrow \mathrm{I}_1 \rightarrow \mathrm{FF}_3$

2. Determine max f_{CK_1} for
   - $R_{\mathrm{PU}} = 1\,\mathrm{k}\Omega,\ C = 25\,\mathrm{pF},\ V_{\mathrm{CC}} = 5\,\mathrm{V}$
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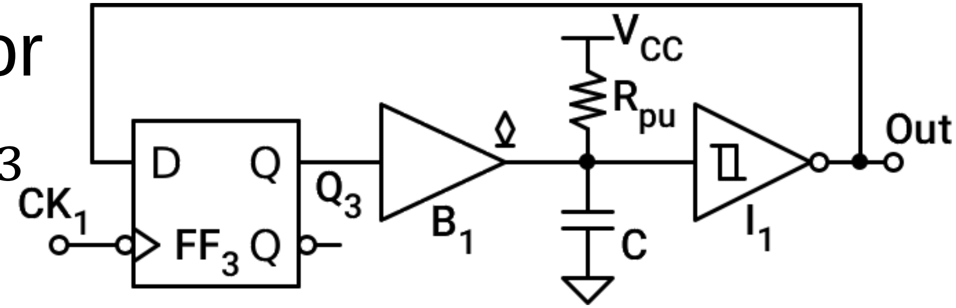
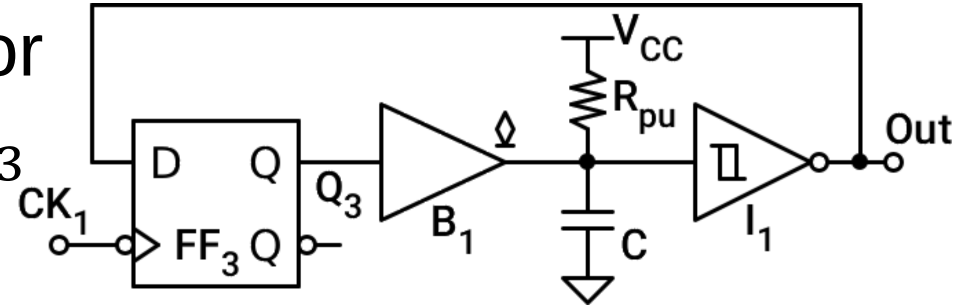


Worst: $V_{\mathrm{C_{LH}}} \to V_{Out_{\mathrm{HL}}}: V_{\mathrm{C}}(t_{\mathrm{LH}}) = V_{\mathrm{S1}} = (V_{\mathrm{GND}} - V_{\mathrm{CC}})e^{-\frac{t_{\mathrm{LH}}}{R_{\mathrm{pu}}C}} + V_{\mathrm{CC}}$

$$\boldsymbol{t_{\mathrm{C_{LH}}}} = R_{\mathrm{pu}}C \ln \frac{V_{\mathrm{CC}} - V_{\mathrm{GND}}}{V_{\mathrm{CC}} - V_{\mathrm{S1}}} = 1\,\mathrm{k\Omega} \cdot 25\,\mathrm{pF} \cdot \ln \frac{5\,\mathrm{V} - 0\,\mathrm{V}}{5\,\mathrm{V} - 3\,\mathrm{V}} = \mathbf{22.91\,ns}$$



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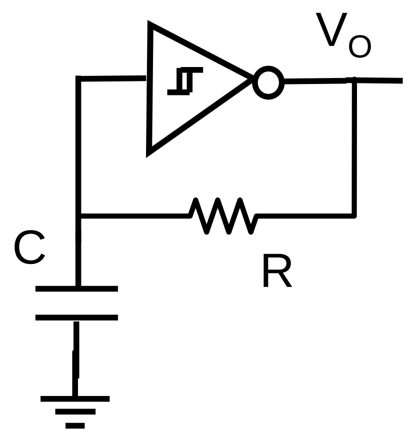
$$\boldsymbol{t_{\mathrm{C_{LH}}}} = R_\mathrm{pu}C\ln\frac{V_\mathrm{CC} - V_\mathrm{GND}}{V_\mathrm{CC} - V_\mathrm{S1}} = 1\,\mathrm{k\Omega}\cdot 25\,\mathrm{pF}\cdot\ln\frac{5\,\mathrm{V} - 0\,\mathrm{V}}{5\,\mathrm{V} - 3\,\mathrm{V}} = \mathbf{22.91\,ns}$$

$$\boldsymbol{T_{\mathrm{CK_{min}}}} = \underbrace{t_{\mathrm{CKQ_{LH}}}}_{\mathrm{FF_3}} + \underbrace{t_{\mathrm{p_{LH}}}}_{\mathrm{B_1}} + \underbrace{t_{\mathrm{C_{LH}}}}_{R_\mathrm{pu},C} + \underbrace{t_\mathrm{HL}}_{\mathrm{I_1}} + \underbrace{t_\mathrm{SU}}_{\mathrm{FF_3}}$$

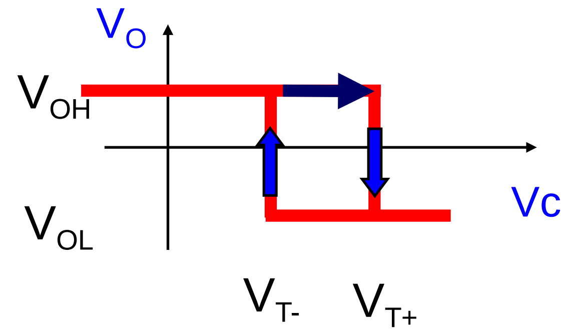
$$= 5\,\mathrm{ns} + 6\,\mathrm{ns} + 22.91\,\mathrm{ns} + 4\,\mathrm{ns} + 3\,\mathrm{ns} = 40.91\,\mathrm{ns} \Longrightarrow F_{\mathrm{CK_{max}}} = \mathbf{24.4\,MHz}$$

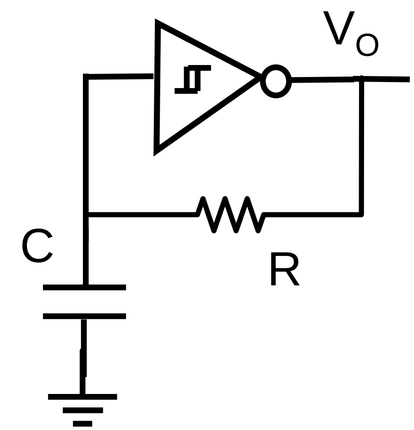
E4: Clock Generator

- Calculate the frequency of the V_O square wave
- Comparator parameters
  - $V_{T+} = 2\ \mathrm{V}$
  - $V_{T-} = 1.2\ \mathrm{V}$
  - $V_{OH} = 4.7\ \mathrm{V}$
  - $V_{OL} = 0.3\ \mathrm{V}$
- Components
  - $R = 1\ \mathrm{k\Omega}$
  - $C = 10\ \mathrm{nF}$



E4: Clock Generator: Half Period *T'*





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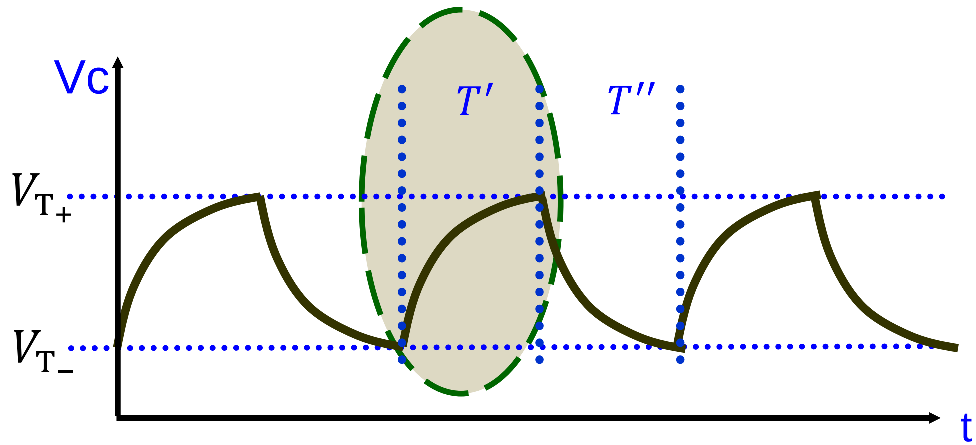
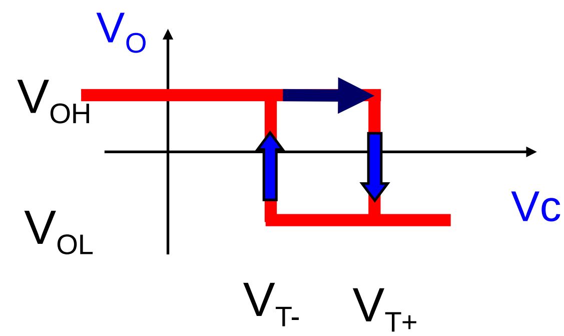
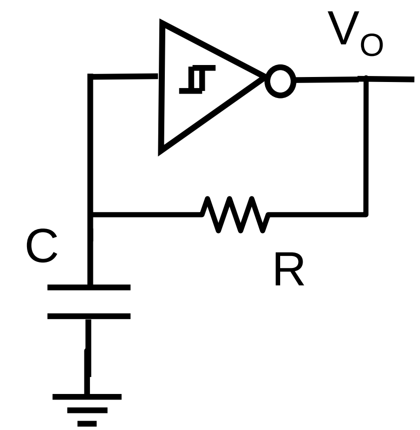




- V_O: switches between V_{OH} and V_{OL}
- V_C: exponentials between V_{T-} and V_{T+}



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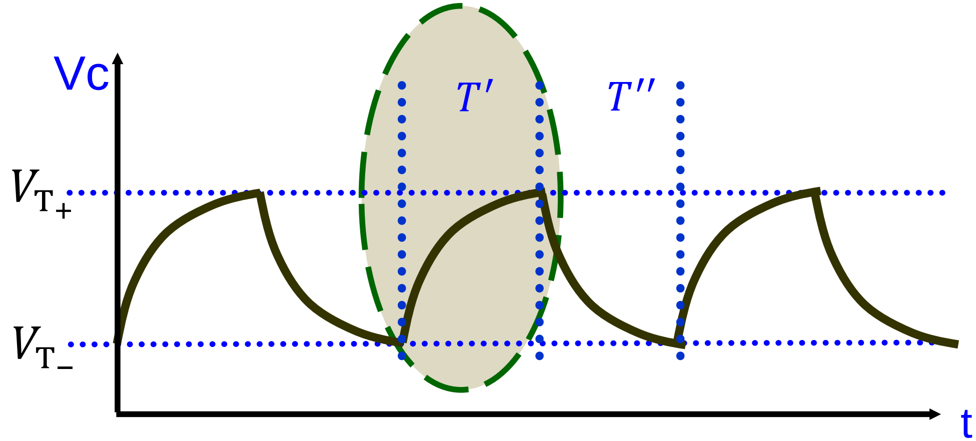
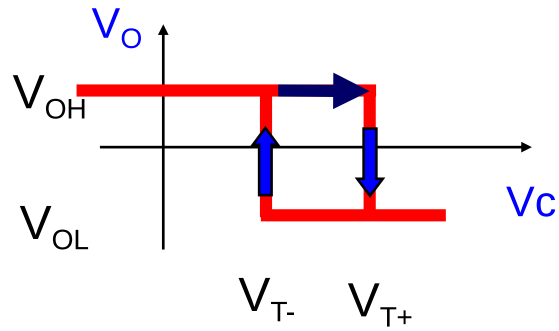
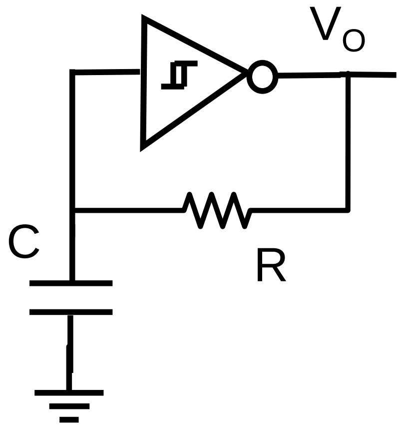


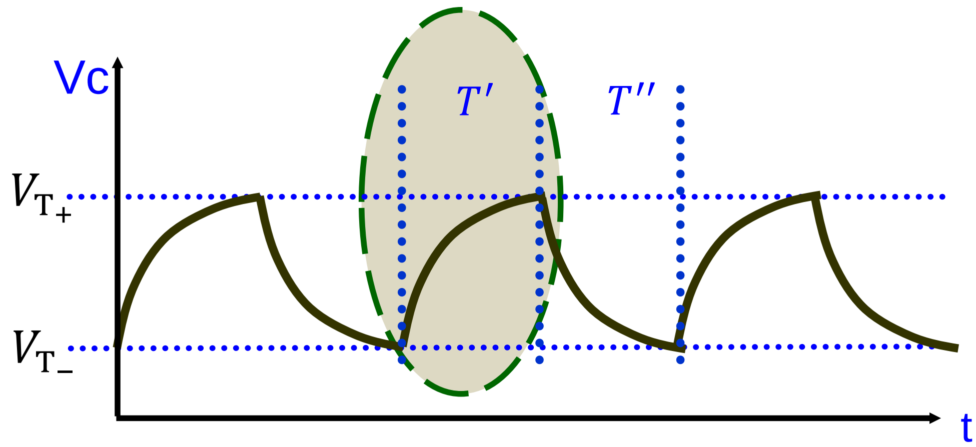


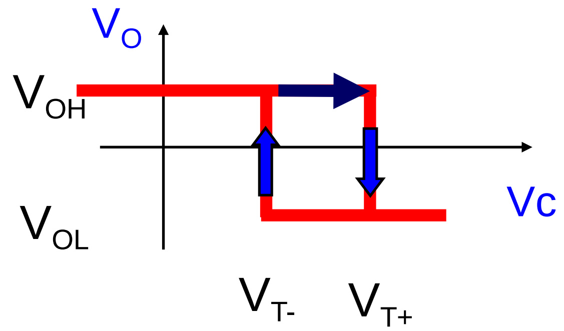
- V_O: switches between V_{OH} and V_{OL}
- V_C: exponentials between V_{T-} and V_{T+}

$$T': V_C(t) = V_{OH} + (V_{T-} - V_{OH})\mathrm{e}^{-\frac{t}{RC}}$$



E4: Clock Generator: Half Period T'





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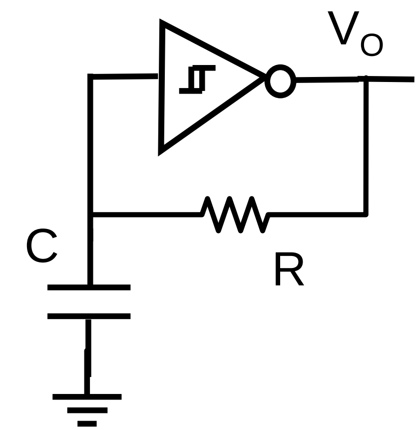
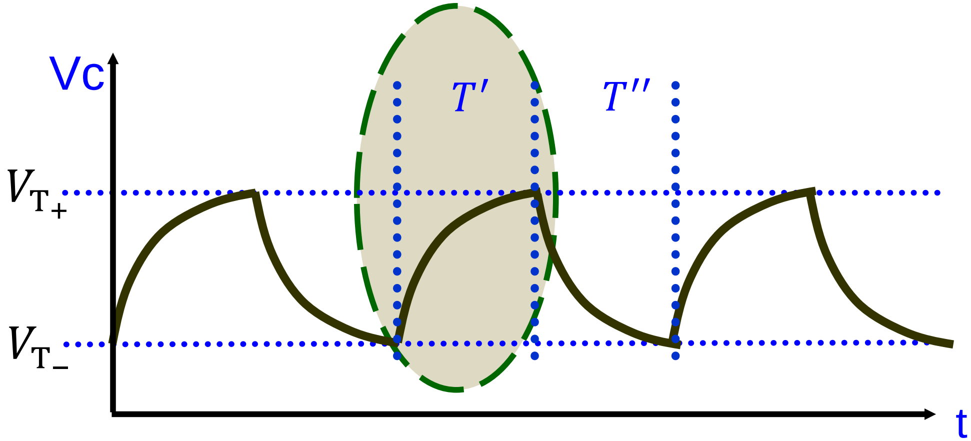
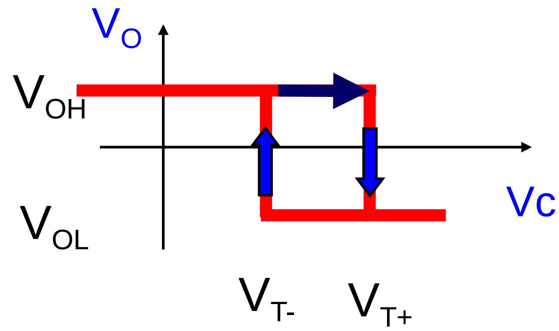


$$T': V_C(t) = V_{OH} + (V_{T-} - V_{OH})e^{-\frac{t}{RC}}$$

When $t = T' \rightarrow V_C(T') = V_{T+}$





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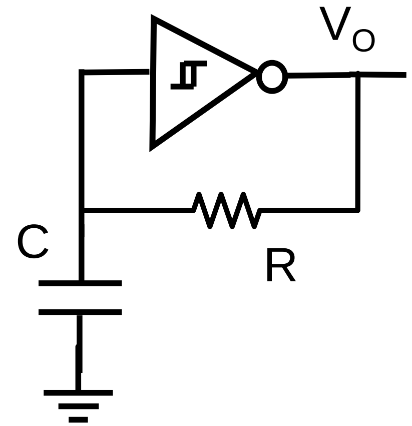
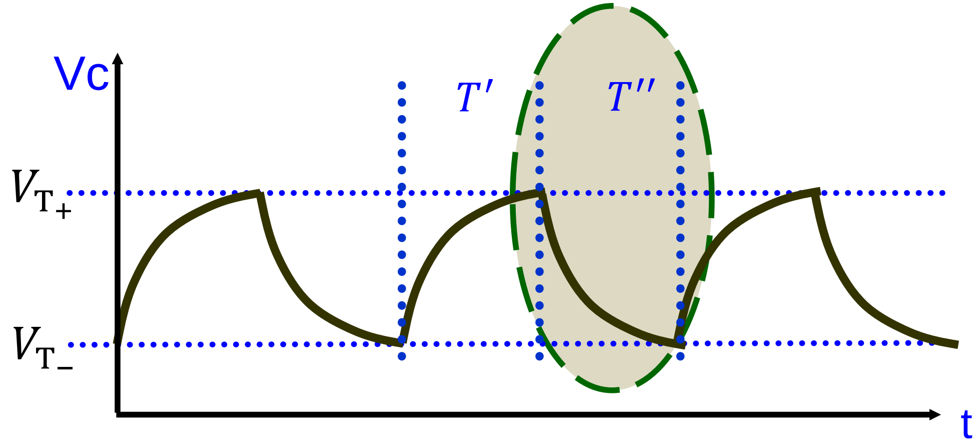


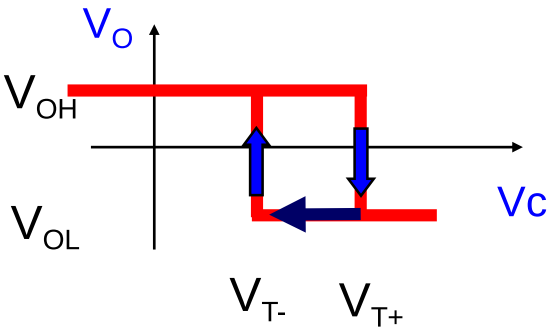
$$T': V_C(t) = V_{OH} + (V_{T-} - V_{OH})\mathrm{e}^{-\frac{t}{RC}}$$

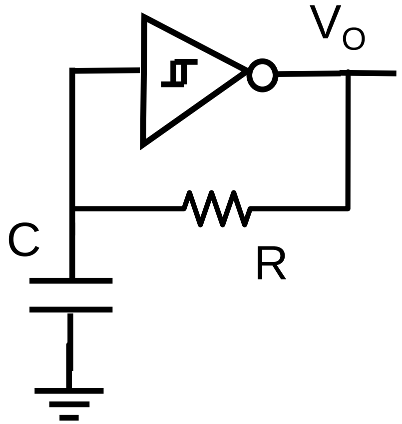
When $t = T' \rightarrow V_C(T') = V_{T+}$

$$T' = RC \ln\left[\frac{V_{OH} - V_{T-}}{V_{OH} - V_{T+}}\right] = 1\,\mathrm{k\Omega} \cdot 10\,\mathrm{nF} \cdot \ln\left[\frac{4.7\,\mathrm{V} - 1.2\,V}{4.7\,\mathrm{V} - 2\,\mathrm{V}}\right] = 2.6\,\mathrm{\mu s}$$

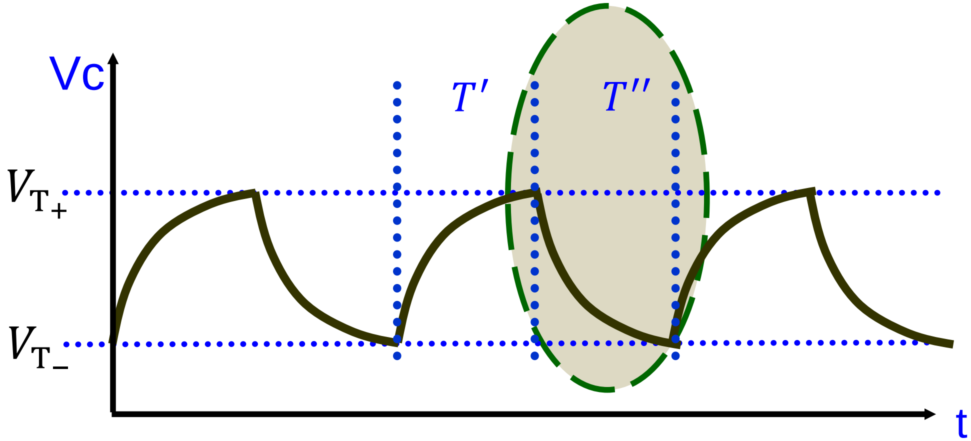
E4: Clock Generator: Half Period T'

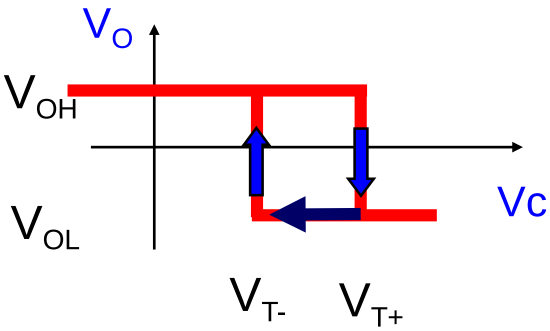


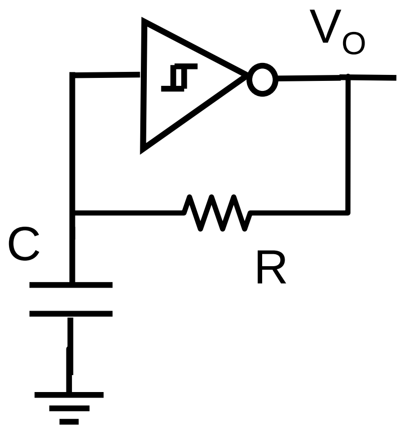




$$T'': V_C(t) = V_{OL} + (V_{T+} - V_{OL})e^{-\frac{t}{RC}}$$







$$T'': V_C(t) = V_{OL} + (V_{T+} - V_{OL})e^{-\frac{t}{RC}}$$

When $t = T'' \rightarrow V_C(T'') = V_{T-}$

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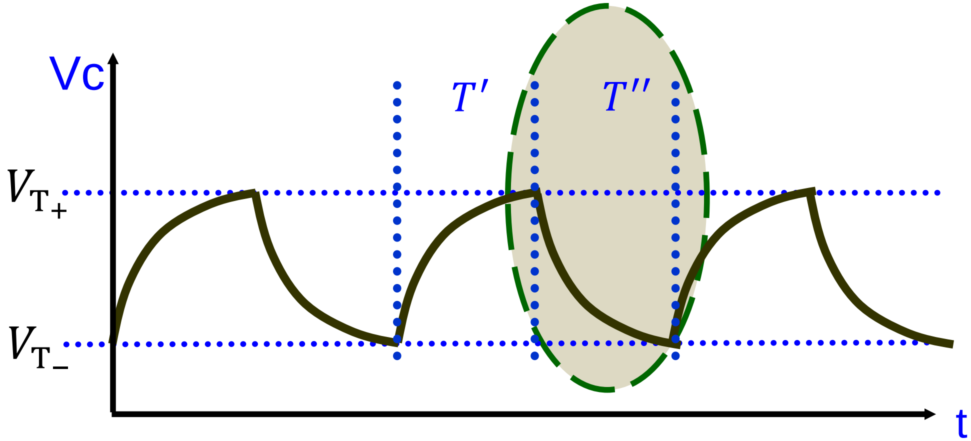

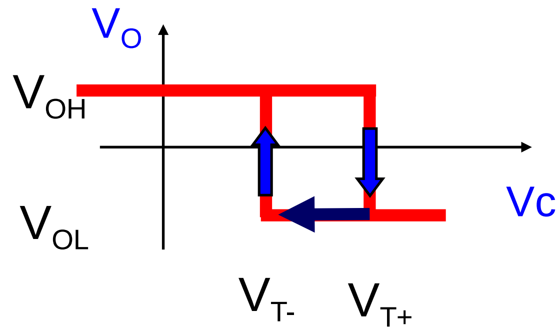

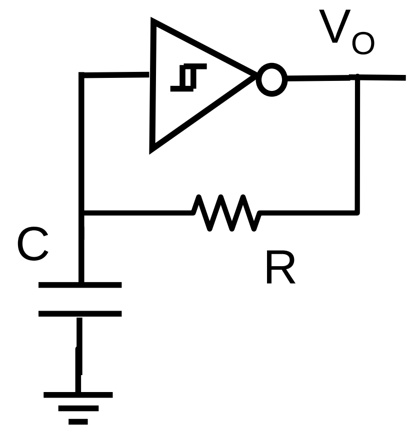

$$T'': V_C(t) = V_{OL} + (V_{T+} - V_{OL})e^{-\frac{t}{RC}}$$

When $t = T'' \rightarrow V_C(T'') = V_{T-}$

$$T'' = RC \ln\left[\frac{V_{OL} - V_{T+}}{V_{OL} - V_{T-}}\right] = 1\,\mathrm{k\Omega} \cdot 10\,\mathrm{nF} \cdot \ln\left[\frac{2\,\mathrm{V} - 0.3\,V}{1.2\,\mathrm{V} - 0.3\,\mathrm{V}}\right] = 6.4\,\mathrm{\mu s}$$

$$T = T' + T'' = 2.6\,\mathrm{\mu s} + 6.4\,\mathrm{\mu s} = 9\,\mathrm{\mu s} \Rightarrow f = \frac{1}{T} = 111\,\mathrm{kHz}$$