Applied Electronics

C5 – Bus Protocols

- Addressing
- Arbitrage
- Performance parameters
- Source sync transfers
- DDR transfers

Lecture C5: bus protocols

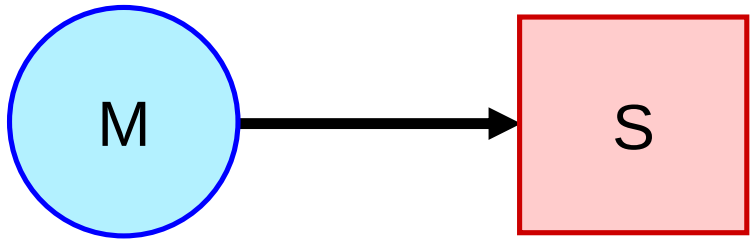
- Addressing techniques (single-Master systems)
- Channel allocation (multi-Master systems)
  - Basic allocation mechanisms and techniques
  - Priority, starvation, fairness
- Analysis and improvement of the performance of a bus
  - Source-Synchronous Transfers
  - Doble Data Rate (DDR) Transfers
- References:
  - D. Del Corso: Telecommunication Electronics: Ch. 5.4

Services provided by the cycle level

- Transfer of information units (byte, word, ...), respecting the time specifications of the destination register
  - Independent of the information TYPE (address, data, …)
- There is one source of information and one destination
  - Extended protocols support asynchronous 1-to-N and N-to-M transfers (N-partner protocols)
- Cycle level operations can be read or write
- They need power and time to provide the services.

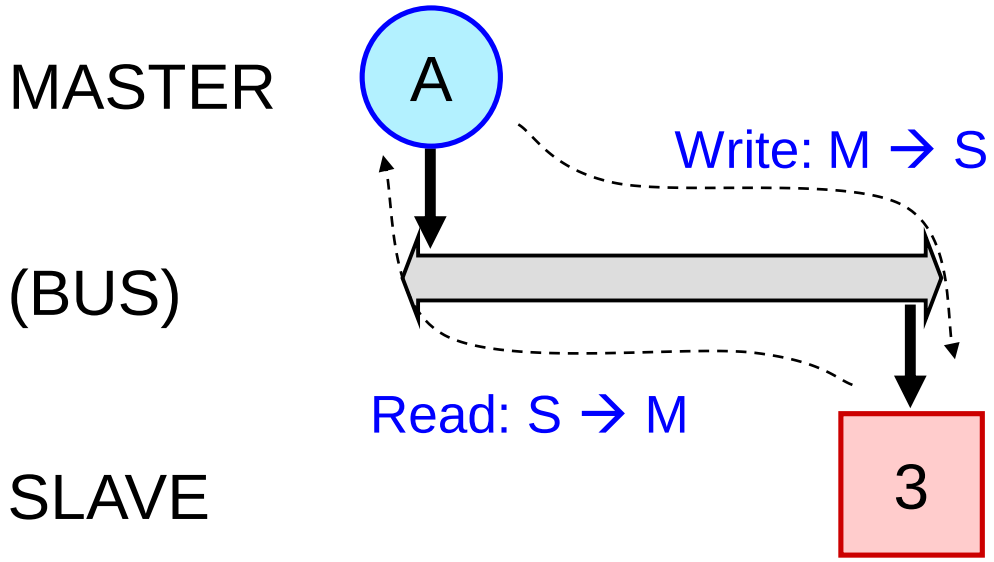
Definition of transaction

- Sequence of one or more cycles, which transfer elements of information with a definite meaning (addresses, data, priority vector, ...)
- Transaction-level items
  - MASTER: activates the operations
  - SLAVE: responds to Master commands



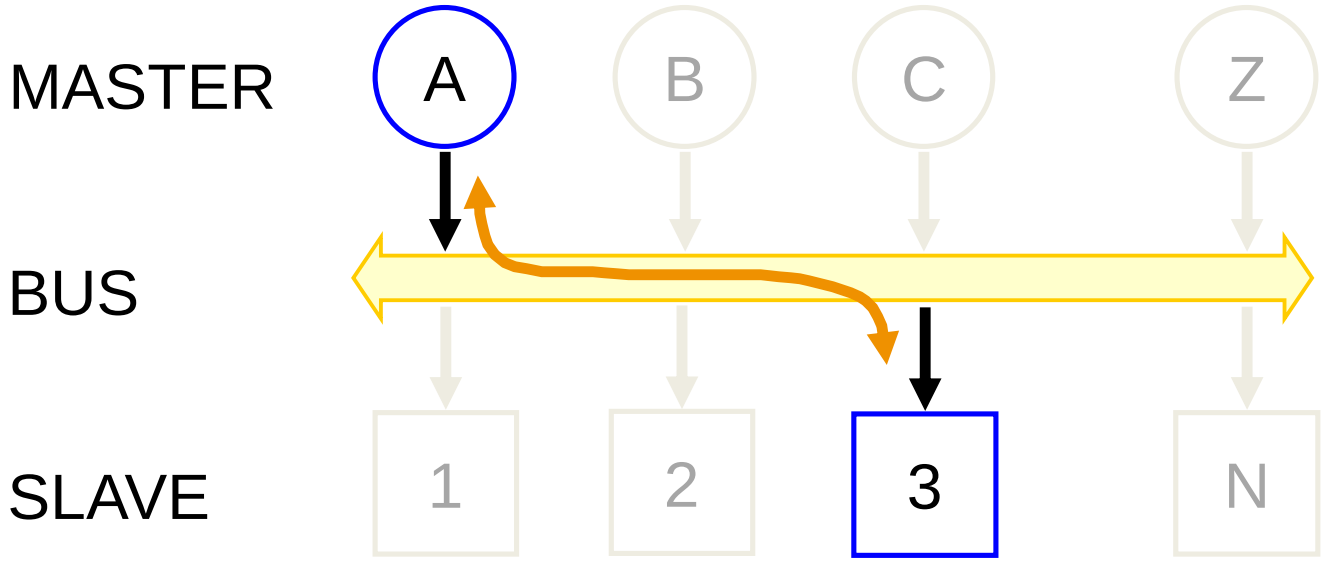
Point-to-point systems

- Transfer point-to-point
  - The two elements between which the information is transferred are defined beforehand



Multi-point systems (bus)

- More units use the same physical channel: the BUS
  - Step 1: Select the units participating in the transfer
  - Step 2: perform the transfer



Bus systems

- Systems with bus: one can change the configuration by removing/adding modules
  - MODULAR OPEN system
- All units must follow the same rules for transferring information
  - PROTOCOL
- Parameters of a bus interface
  - Physical-electrical structure (connector, formats, levels, ..)
  - Transaction type, speed, and width (protocol)
  - ….

Comparison of bus and point-to-point

- Point-to-point connections
  - Multiple connection ports required on each module
  - Independent physical channels; well-defined op. conditions
  - Requires routing for communication between various unit pairs
  - Can reach higher speeds
- Multi-point / bus connections
  - One port on each unit, one physical channel
  - Variable electrical conditions (depending on board number)
  - Requires choice of who controls the channel (arbitrage)
  - Requires partner selection mechanism (addressing)
  - Maximum modularity

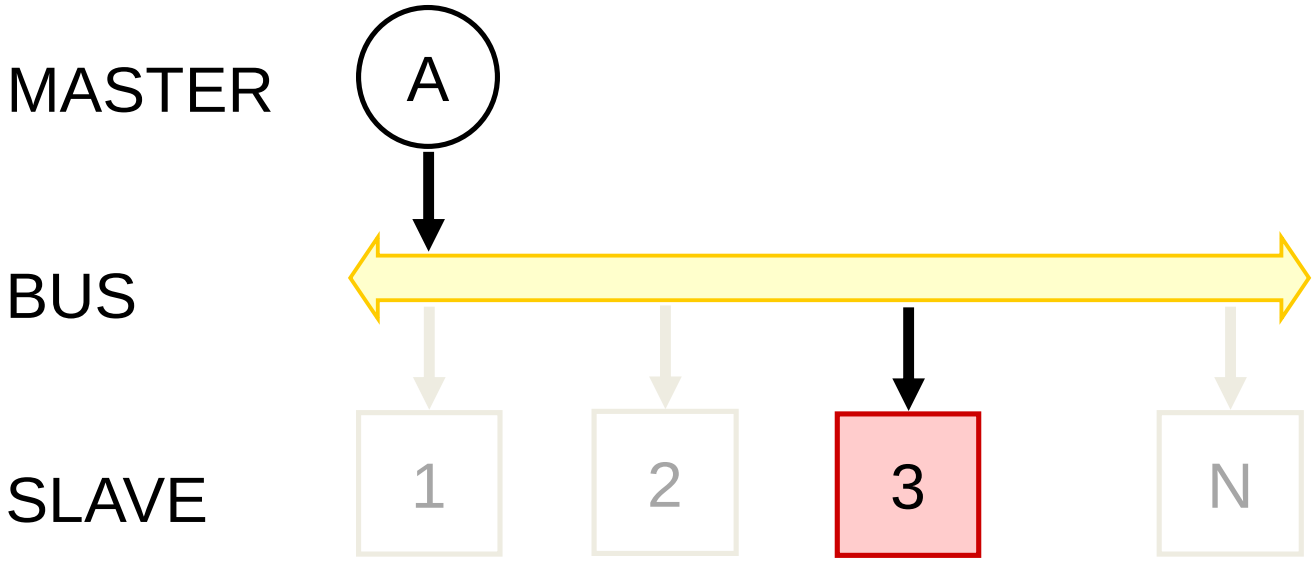
Transaction protocols

- In multipoint (bus) systems, specific cycles are required to select the participating units
  - Master selection → **Allocation** (of the channel)
  - Slave selection → **Addressing**
- Only after the transfer can be performed

cycle 1 cycle 2 cycle 3

Single master - multislave systems

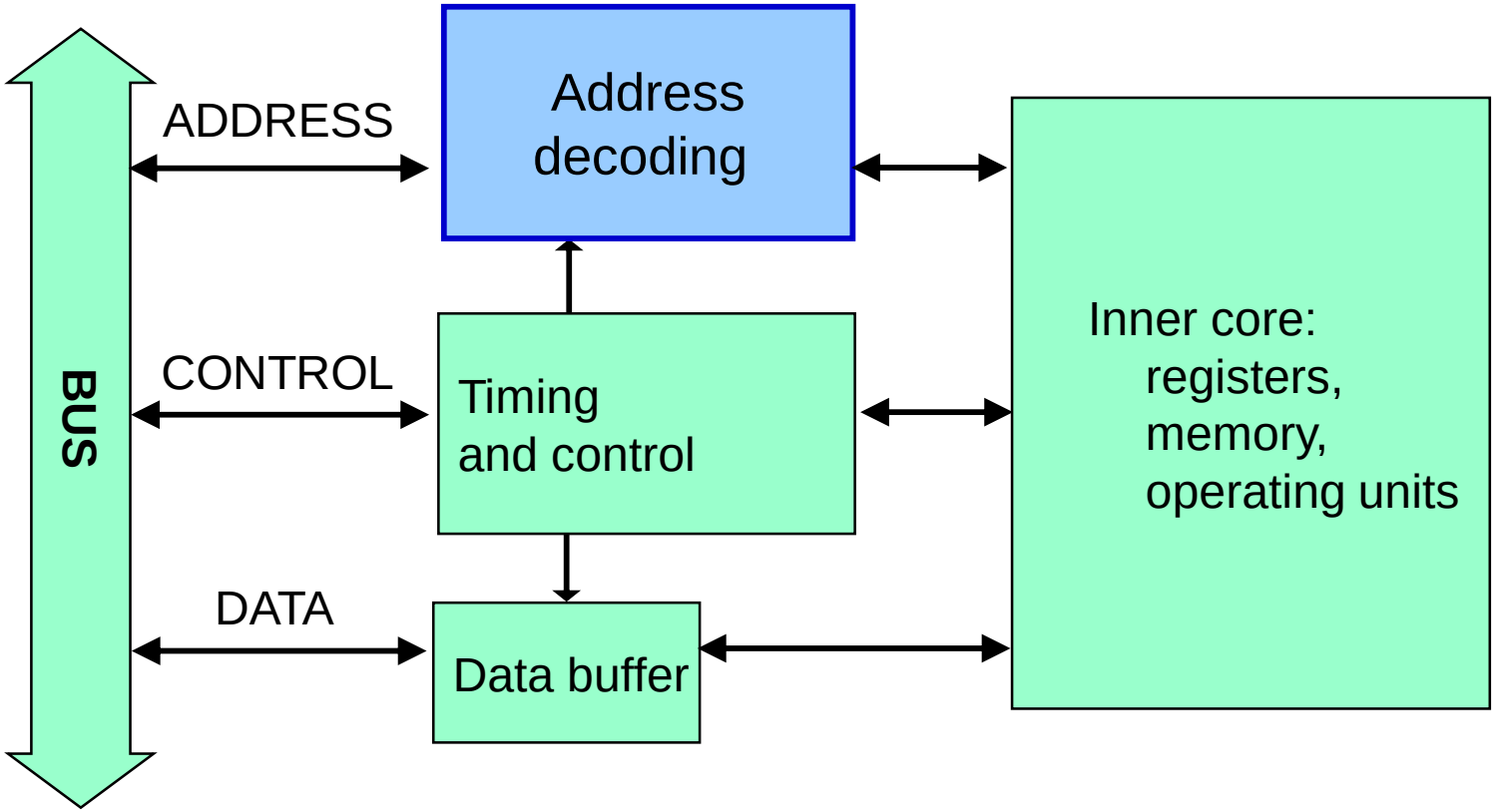
- The master is predefined (unique)
- The slave is selected with an operation of ADDRESSING



Structure of the Slave units

- Address decoding
  - Recognizes the address issued by the Master
  - Uses comparators, decoders, gate logic, ….
- Timing and control
  - Generates internal command signals
  - Manages synchronization (handshake) and data buffers
- Inner core
  - Registers, memory, operating units, ...
- Data buffer
  - Adequate for driver and receiver, monolithic transfer to the bus

Block diagram of the Slave units



Addressing techniques

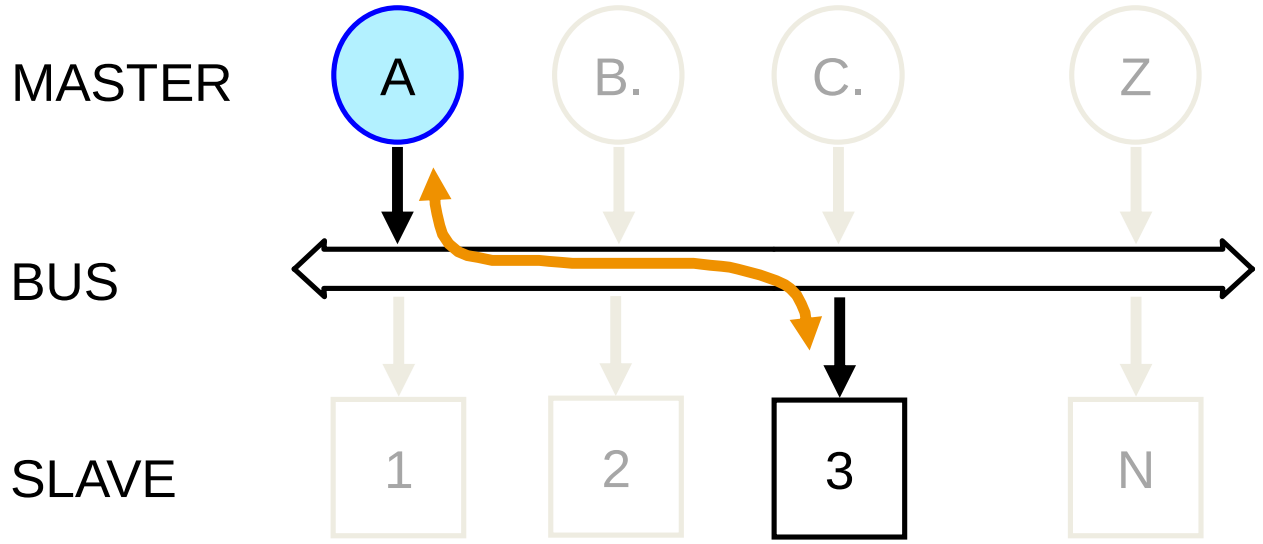
- Coded / Decoded Selection
  - Encoded: N bits select 1 element out of 2^N
    - Selection of memory and peripheral cells (with address)
  - Decoded: M bits select 1 (or more) of M elements
    - Direct selection of registers
    - Selection of memory cells after the address decoder
- Logical / Geographic Addressing (position)
  - Logical: Selection depends on the "name" of the Slave (logical)
    - Memory, registers, ...
  - Geographic: Selection depends on location (connector)
    - Used to determine configuration and identify cards at system startup

Lecture C5: bus protocols

- Addressing techniques for Single-Master systems
- Channel allocation for Multi-Master systems
  - Basic allocation mechanisms and techniques
  - Priority, starvation, fairness
- Performance analysis of a bus
- Techniques to improve the performance
  - Source-Synchronous transfers
  - Double Data Rate (DDR) transfers

Multimaster systems: who uses the bus?

- Multimaster / multislave systems
  - Must identify the couple Master / Slave for transfers
  - Operation of ALLOCATION (ARBITRATION)



Allocation techniques

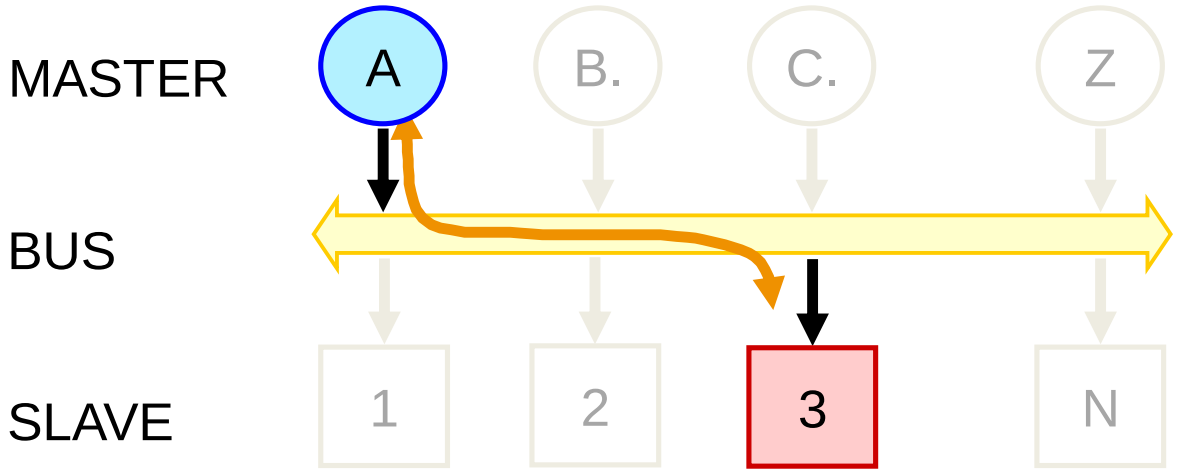
- Collision: simultaneous access of two users
  - It must be avoided → allocation of the channel before use
- Allocation mechanisms
  - Token passing
    - Single token, moved between masters (without evaluating requests)
  - Collision detector for collision detection
    - GRANT to all those who ask for access → collision
    - Collision detection mechanisms and retry
  - Arbitration
    - Evaluation of REQUESTS, issue a single GRANT
    - No collision
    - Deterministic access, controllable parameters

Arbitration policies

- Time-based priority: FCFS (First-Come, First-Served)
  - Limited time resolution
  - May not order all events → need another mechanism
- Logic priority
  - Define a "rank" of the requests (priority level)
  - High-priority request sequences can block low priority ones
    - Starvation
  - Must guarantee servicing in a limited time
    - Fairness
- Next slides: examples of requested / grant sequences:
  - FCFS referee and priority
  - Starvation and fairness

Complete sequence summary

- Op. 1: Master selection (arbitration)
- Op. 2: Slave selection (addressing)
  - Master and Slave form a Point-to-Point “virtual channel”
- Op. 3: M-S pair transfers the information as point-to-point



Lecture C5: bus protocols

- Addressing techniques (single Master systems)
- Channel allocation (multi-master systems)
  - Basic allocation mechanisms and techniques
  - Priority, starvation, fairness
- Performance evaluation of a bus
- Techniques for improving performance
  - Source-Synchronous Transfers
  - DDR transfers

Performance of a bus

- The amount of information transferred in a unit of time is THROUGHPUT (T)
- T = W x S
  - W: bus width
  - S: bus speed (cycles/second)
    if the cycle has duration t_C, S = 1 / t_C
- The duration of the cycle t_C depends on
  - Electrical parameters: t_{TX}, t_K
  - Module parameters: t_{SU}, t_H, t_{WR}, t_{EN}, ...
  - Protocol (number of transitions/cycle, type of protocol, ...)

Performance of protocols

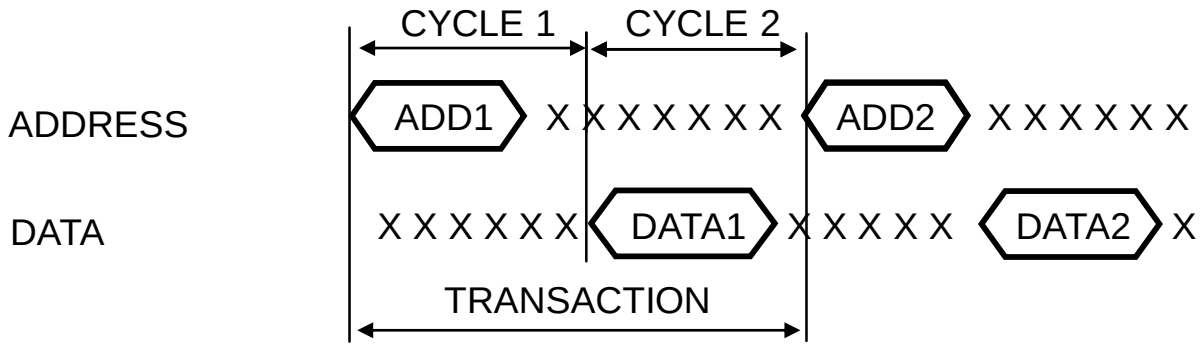
- Synchronous protocol (READ/WRITE)
  - Fixed speed, limited by the slowest device
  - Write cycle time: depends on t_K
  - Reading cycle time: depends on t_{TX} (without pipeline)
- Asynchronous protocol
  - Variable speed, adaptable to the involved devices
  - Cycle time: depends on t_{TX}, for both READ and WRITE
- Best protocol: Source Synchronous
  - Control signals managed by both units
    - Only the necessary delays

Multiplexed buses

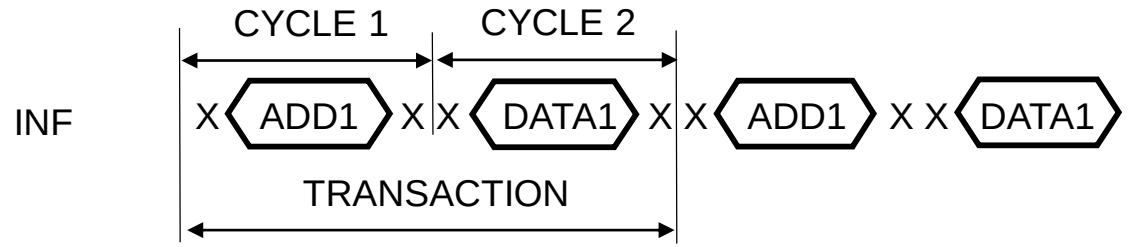
- Basic structure of parallel buses
  - Addresses and data use different conductors/tracks
  - Driver/receiver, tracks on the backplane, connector pins are expensive resources (require space, use energy, ...)
- Objective
  - Reduce the number of (physical) conductors
- Solution
  - Use the same conductor for multiple signals
- Multiple, MULTIPLEXED, bus
  - Addresses, data, other information use the same conductors, but at different times

Comparison of parallel/multiplexed buses

- Parallel: separate conductors for addresses and data



- Multiplates (multiplexed): addresses, data, other information use same conductors

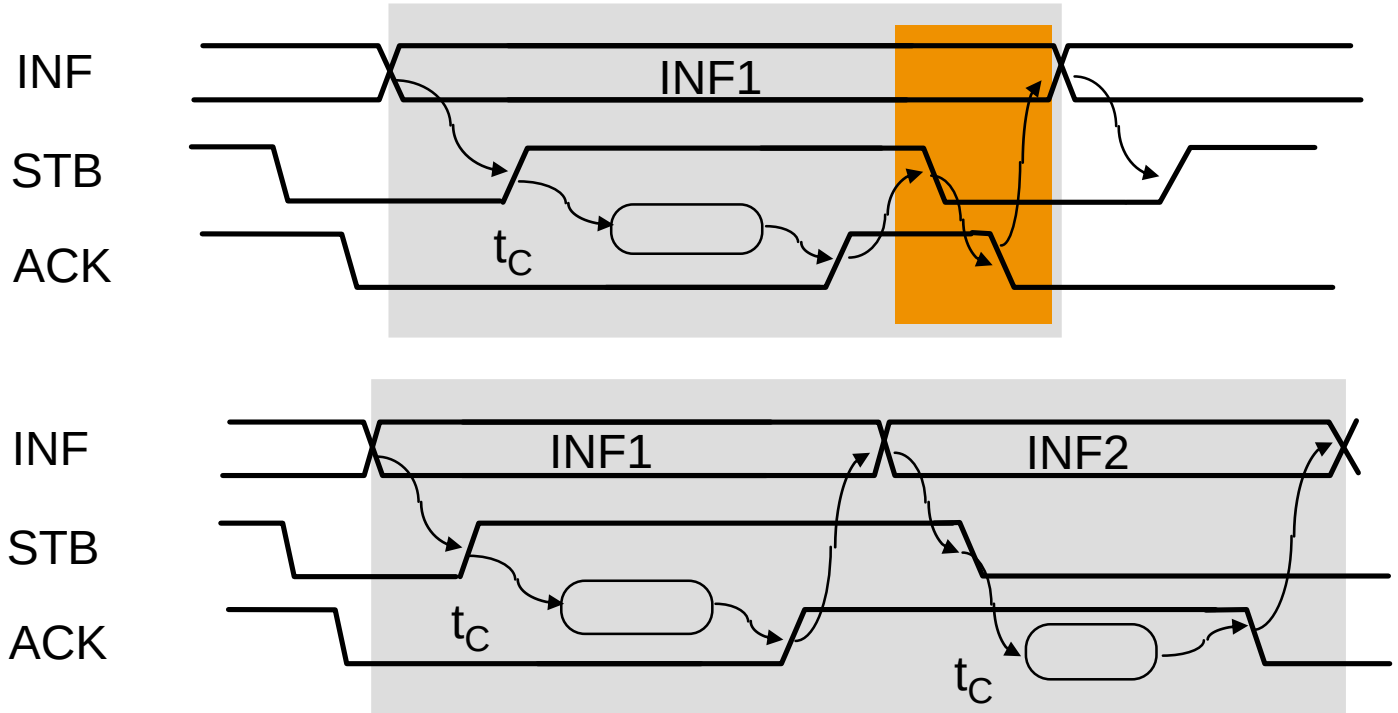


Performance improvement

- Improving performance for the same power consumption?
- Standard Read/Write cycle
  - Two transitions/cycle for control signals (but *one* used for timing)
  - Bandwidth and consumption are linked to number of transitions
  - Data bandwidth lower than control signal bandwidth
    - One transition/cycle compared to two
- DDR, Double Data Rate, cycle
  - Uses both transitions of the control signals STB/ACK
  - Lower consumption
  - Higher speed
  - Higher complexity

Two-edge cycles (Dual-edge): DDR

- Removes the unused transitions
- Reduces the consumption / increases the speed

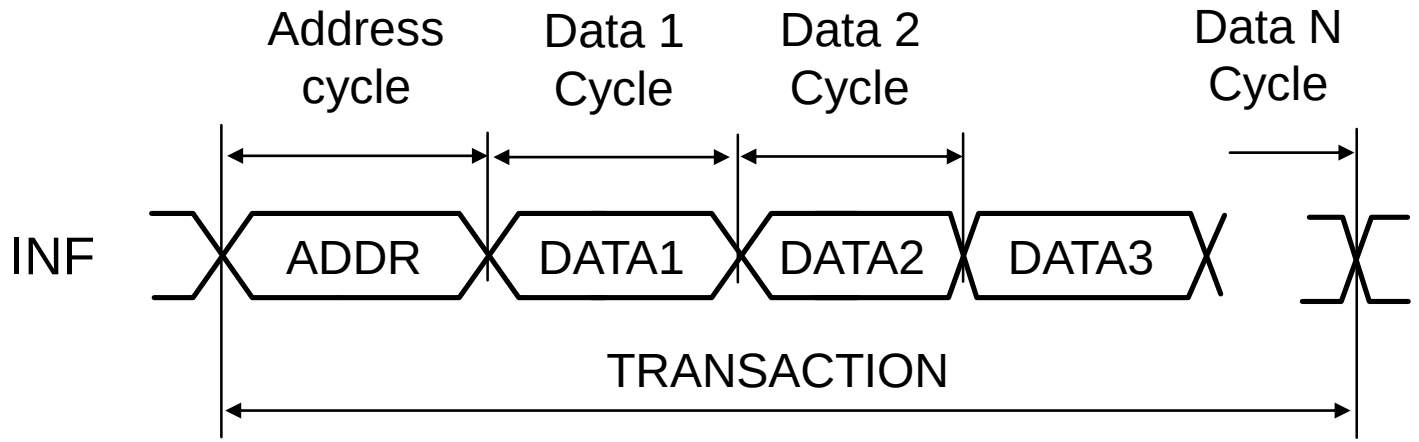


Source Synchronous cycles

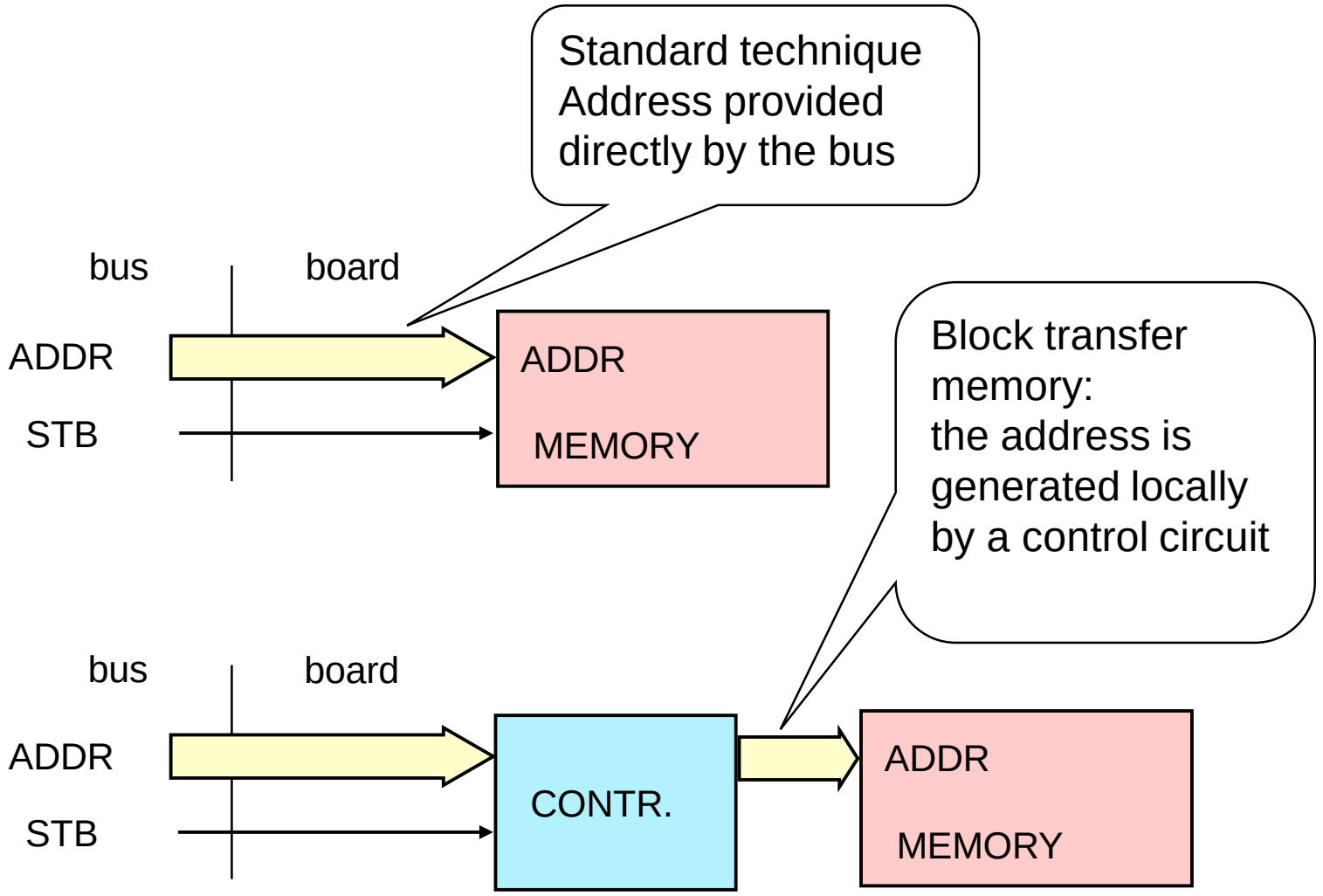
- In the writing cycles, INF and STB move in the same direction, Master → Slave
- Two timing parameters
  - Cycle duration, t_C, or cadence in cycles/s f_C ($t_C = 1 / f_C$)
    - Depends on skew t_K , not on t_{TX}
  - Data latency, t_L, how long to wait to get the data
    - Depends on t_{TX} and on skew t_K
- A new transfer can start before the previous one is over
  - Pipeline technique applied to transfers
  - Pipeline example: Source Synchronous protocols
    - Used for high-speed RAM (SSTL-2 and later)

Block Transfers (Burst)

- Most transfers in program execution involve sequences of successive memory cells
  - Send only the first address
  - Double the INF amount for long packages transferred per time
    - Skips the address transfer

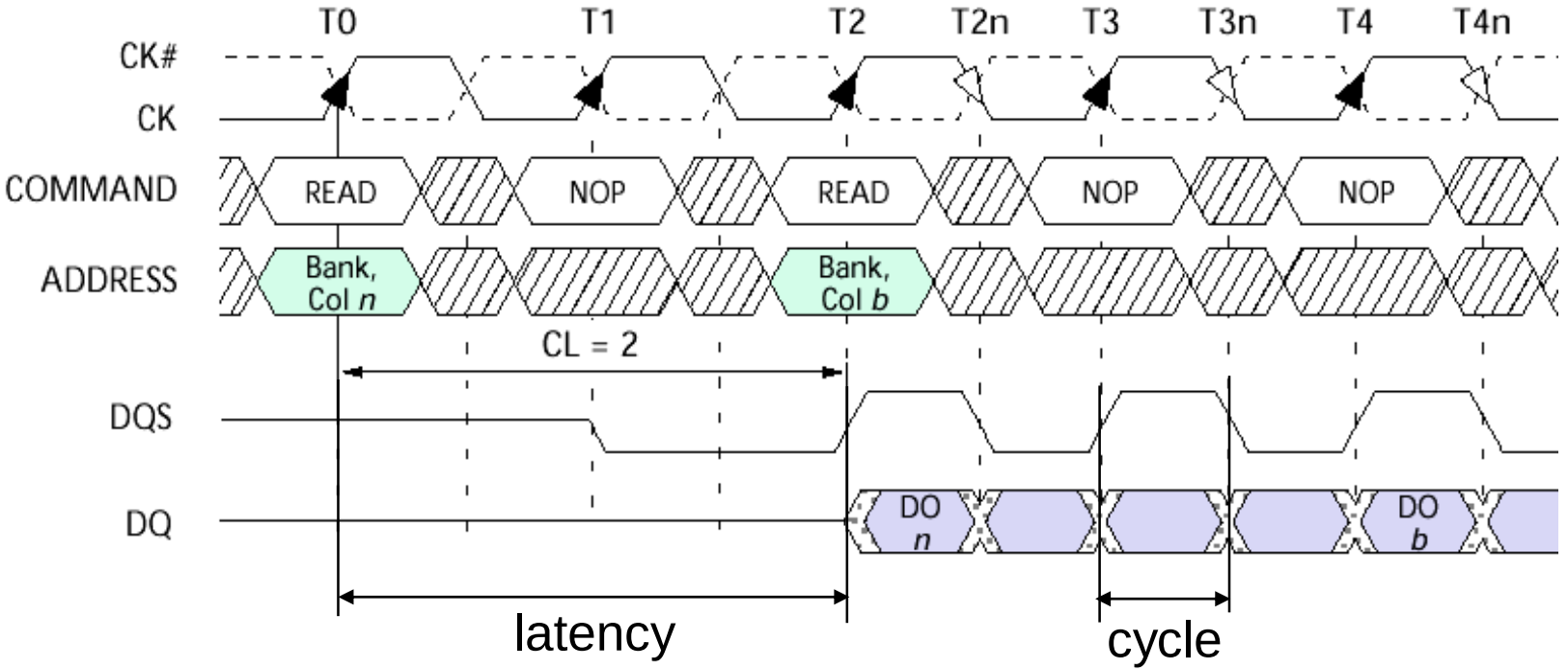


Block transfer interface



Burst transfers: DDR memories

- Source Synchronous DDR Block transfer
  - DQS (Data Strobe) driven by the memory (double edge)
  - Latency of two clock periods



Beyond Source Synchronous

- With a Source Synchronous (SS) protocol
  - An SS read requires Slave-controlled STBs
  - Access time delays are still present
  - Pipeline for even better performance
- Skew t_K is the key parameter for speed
  - t_K due to INF and STB using different physical channels (wires)
  - How to eliminate the skew? Use only one wire!
- Modulations with embedded clock or self-synchronizing
  - Timing and INF on the same physical signal
  - Convert parallel transfers into multiple serial channels

Lecture C5 – final test

- When and why must there be an addressing operation?
- In which systems is an arbitration operation necessary?
- Describe the operation of a bus arbiter.
- What is meant by “performance” of a bus?
- What parameters determine the performance of a bus?
- What does the minimum cycle time depend on?
- Compare min cycle times for synch. and asynch. protocol.
- Describe the benefits of DDR protocols.
- What are the advantages of multiplexed buses?
- Describe the benefits of block transfer transactions.