

Student ID		Version	A	Date	..2018
Given name		Family name	CORRECTION		

**GENERAL WARNING:**

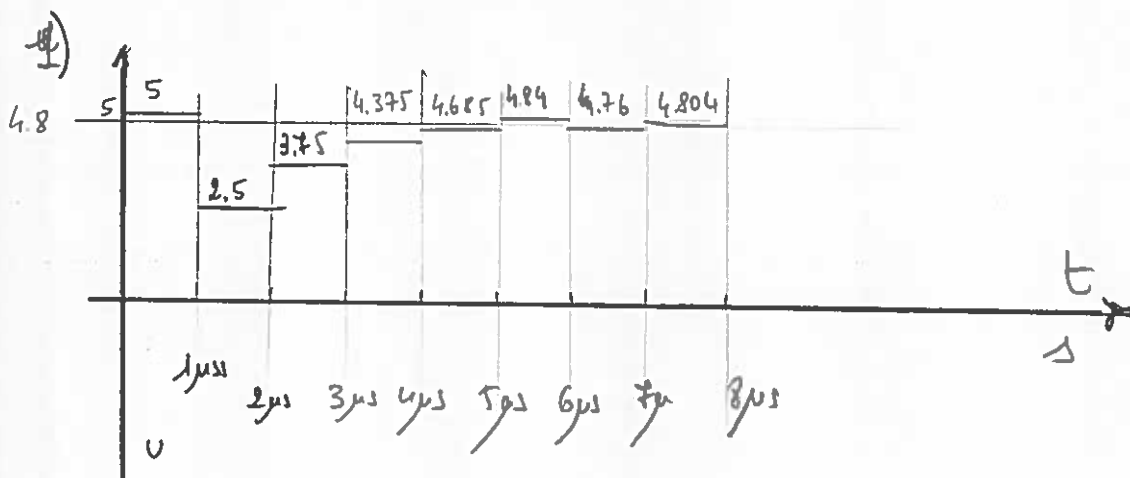
ANSWER THE QUESTIONS WHICH ARE ASKED AND NOT OTHER ONES. ANY COMMENT WHICH IS NOT RELEVANT TO WHAT ASKED **WILL NOT BE CONSIDERED.**

**Exercise 1) ( max 9 points)**

A successive approximations 8 bit A/D converter has a clock of 1 MHz and an input range of 10 V.

If at the input there is a voltage of 4.8V and a conversion is started compute:

- 1) The sequence of values at the output of the internal D/A converter as a function of the time (7 points)
- 2) The number of cycles required for the conversion (1 point)
- 3) The final digital output voltage (1 point)



2) 8 cycles

3) 0111 1011      OUTPUT VALUE

Student ID		Version	A	Date	..2018
Given name		Family name			

**Exercise 2) ( 5 points)**

A triangular signal with 5kHz frequency is digitalized with a 12 bit AD converter, with an input range of 5 V.

1. Find the SNR when the input signal has peak to peak amplitude of 2.5 V (2 points)
2. If the spectrum of the signal may be considered 0 after the 8<sup>th</sup> harmonic which is the minimum sampling frequency (3 points)

$$1) \text{ SNR}_{dB} = 6N - 6 = 6 \cdot 12 - 6 = 66 \text{ dB}$$

$$2) f_{\text{min}} \geq \underbrace{(5 \text{ kHz} \cdot 8)}_B \cdot 2 = 80 \text{ kHz}$$

Student ID		Version	A	Date	..2018
Given name		Family name			

**Exercise 3) (8 points)**

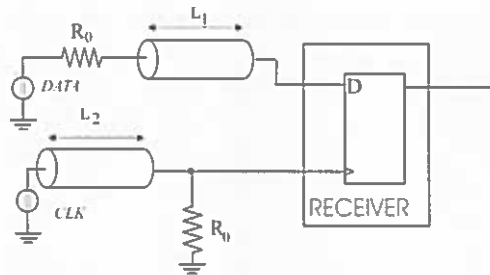
Given the schematic of the figure, where the parameters of the transmission lines are:

$L_1 = 35 \text{ cm}$

$L_2 = 20 \text{ cm}$

$v = c/3$  (  $c$  is the speed of the light).

where the input signals are  $\text{DATA} = 3.3 \text{ u(t)}$  and  $\text{CLK} = 3.3 \text{ u(t-t}_0\text{)}$  and the parameters of the flip-flops are the threshold voltage  $V_T = 1.7 \text{ V}$  and set-up time  $= 2 \text{ ns}$  determine the minimum value of  $t_0$  which will guarantee the correct transmission of the data.



$$t_{\text{DATA}} = \frac{35 \text{ cm}}{c/3} = \frac{35 \cdot 10^{-2} \text{ m}}{100 \cdot 10^6 \text{ m/s}} = 3.5 \text{ ns}$$

$$t_{\text{CLK}} = 2 \text{ ns}$$

$$t_{\text{CLK}} + t_0 \geq t_{\text{DATA}} + t_{\text{setup}}$$

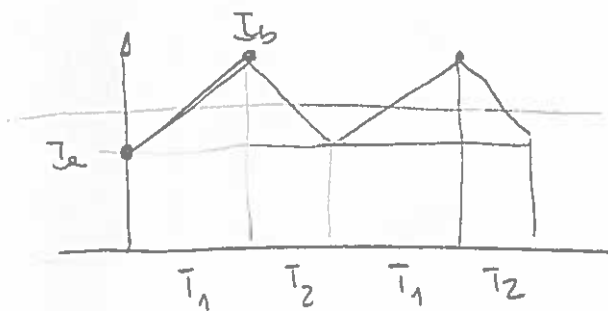
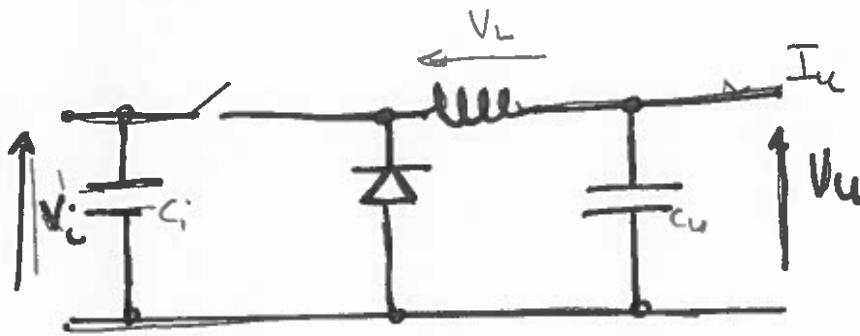
$$t_0 \geq t_{\text{DATA}} + t_{\text{setup}} - t_{\text{CLK}} = 3.5 \text{ ns} + 2 \text{ ns} - 2 \text{ ns} = 3.5 \text{ ns}$$

Student ID		Version	A	Date	..2018
Given name			Family name		

**Exercise 4 (8 points)**

Draw the schematic of a buck (step-down) power converter (5 points)

Compute the the value of the output voltage as a function of the switching frequency, duty cycle and input voltage. (3 points)



During  $T_1$   $V_L = V_i - V_u$   
 During  $T_2$   $V_L = -V_u$

$$\frac{V_i - V_u}{L} T_1 = \frac{V_u}{L} T_2$$

$$V_i T_1 = V_u (T_1 + T_2)$$

$$V_u = V_i \frac{T_1}{T_1 + T_2} = V_i D$$

$V_u$  does not depend on the frequency