
# Applied Electronics

## C1 – Interconnections

- Signal integrity, EMI
- Static and dynamic interfacing
- RC models of interconnection
- Definition of parameters

# The real bottleneck

- Currently more than $10^9$ transistors/chip (Intel i9), but…
  - How to transfer the information – distribution of signals?
  - How to transfer the energy – power supply system?
  - How to remove the heat – thermal circuits?
- The distribution of signals and power is the main performance bottleneck of IC, SoC, PCB
  - Digital circuits use **0 and 1** (binary symbols), but ...
    - The real quantities are Voltages and Currents (V and I)
  - Needed analog electronics and microwaves knowledge
    - Behaviors related to the physical structure (layout)
    - Consider the effects of propagation (transmission lines)
    - Always useful analysis, necessary for high-speed systems

# Unit C: interconnections – objectives

- Problems of interconnection systems for:
  - Signals (transport of information)
  - Power (transport of energy)
- Main point: the conductors are not single nodes
- Problems are known as **SIGNAL INTEGRITY**
- Objective: understand and apply *basic techniques* for
  - Transfer of digital signals
    - Bus and communication protocols
  - Energy distribution for power supply
    - Bypass capacitors, layout criteria, ...

# Unit C: organization and contents

- C1: Signal integrity, problems, RC models.
- C2: Transmission line models
- C3: Interconnections with transmission lines
- C4: Basic transfer operations
- C5: Bus protocols
- C6: Serial communications
- C7: Signal integrity, power distribution

# Unit C: reference texts

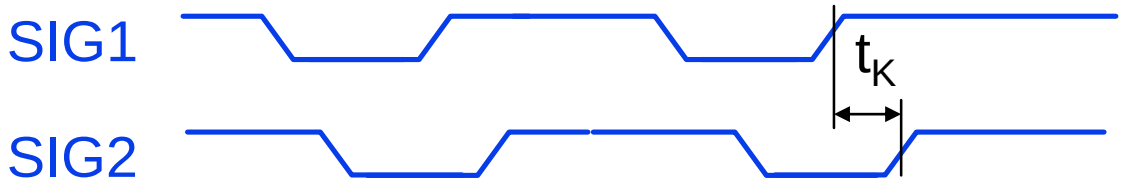
- D. Del Corso: "Interconnections for high-speed digital circuits", 2 parts, MindSigInt1.pdf and MindSigInt2.pdf
  - PDFs are available in the Applied Electronics → Course materials folder in the “Materials” tab in the course site

# Lecture C1: Interconnections

- Signal integrity and interferences (EMI)
- Limits due to interconnections
  - Problem identification
  - Static and dynamic interfacing
- Models of the interconnection system
  - RC model
  - Definition of parameters
- References
  - D. Del Corso: Interconnections for High Speed ..: lectures 1, 2

# Time-domain noise: Jitter and Skew

- Difference between delays: skew $t_K$
  - Skew is defined for ***one transition*** simultaneous for two signals

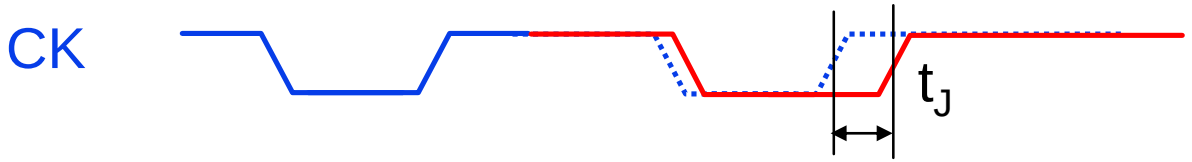



- Variation from period to period: jitter $t_J$
  - Jitter is measured on ***two transitions*** of a single signal

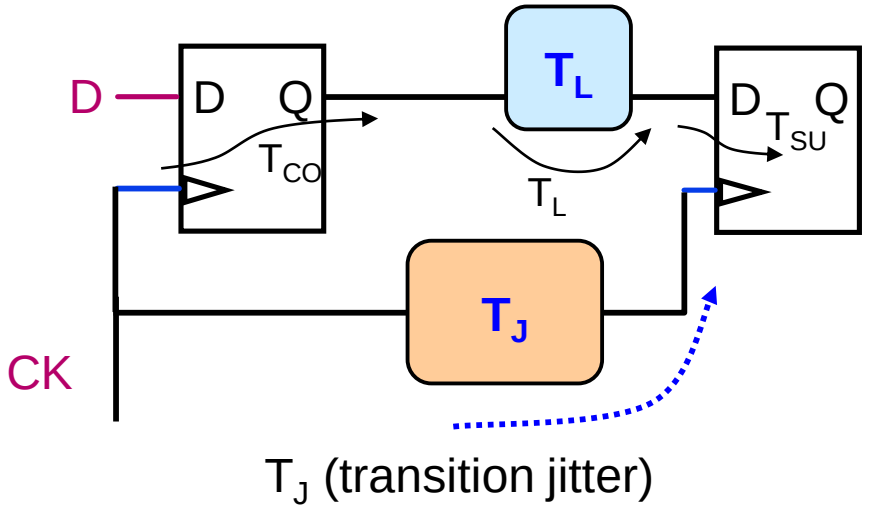

- Skew and Jitter change temporal relationships
  - Change the timing margins, hence the synchronization!
  - Are random variables, usually defined by the maximum (min = 0)

# $F_{max}$: effect of the clock jitter

- Consider the clock jitter $T_J$ (changes of the period)
  - "Temporal noise" over the clock period




- Max operating frequency
  - $T_{CKmin} = T_{CO} + T_L + T_{SU} + T_J$
  - $F_{max} = 1 / T_{CKmin}$
  - $F_{max}$ ($T_{CO}$, $T_L$, $T_J$, $T_{SU}$)




$T_J$ (transition jitter)

# $F_{max}$: effect of interconnections

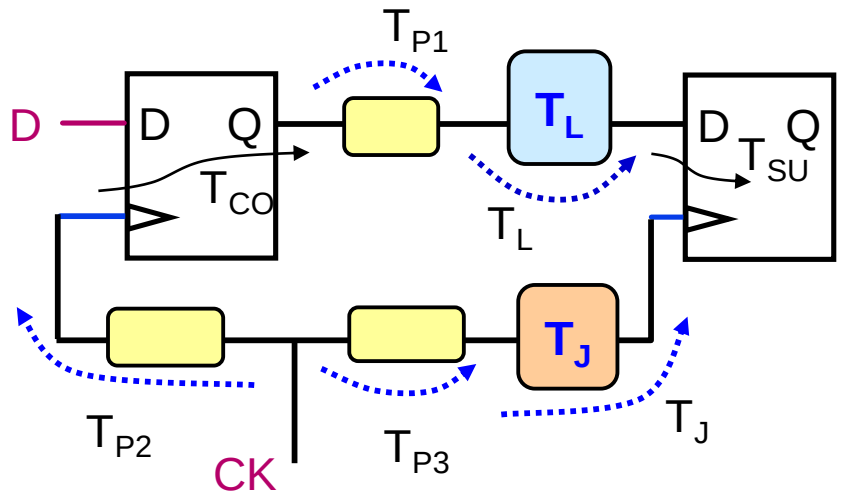
- The interconnections introduce propagation delays $T_P$
  - The OUT and IN nodes are separated (transmission delays $T_{Pn}$)
  - The delays are partly unknown

- Max operating frequency

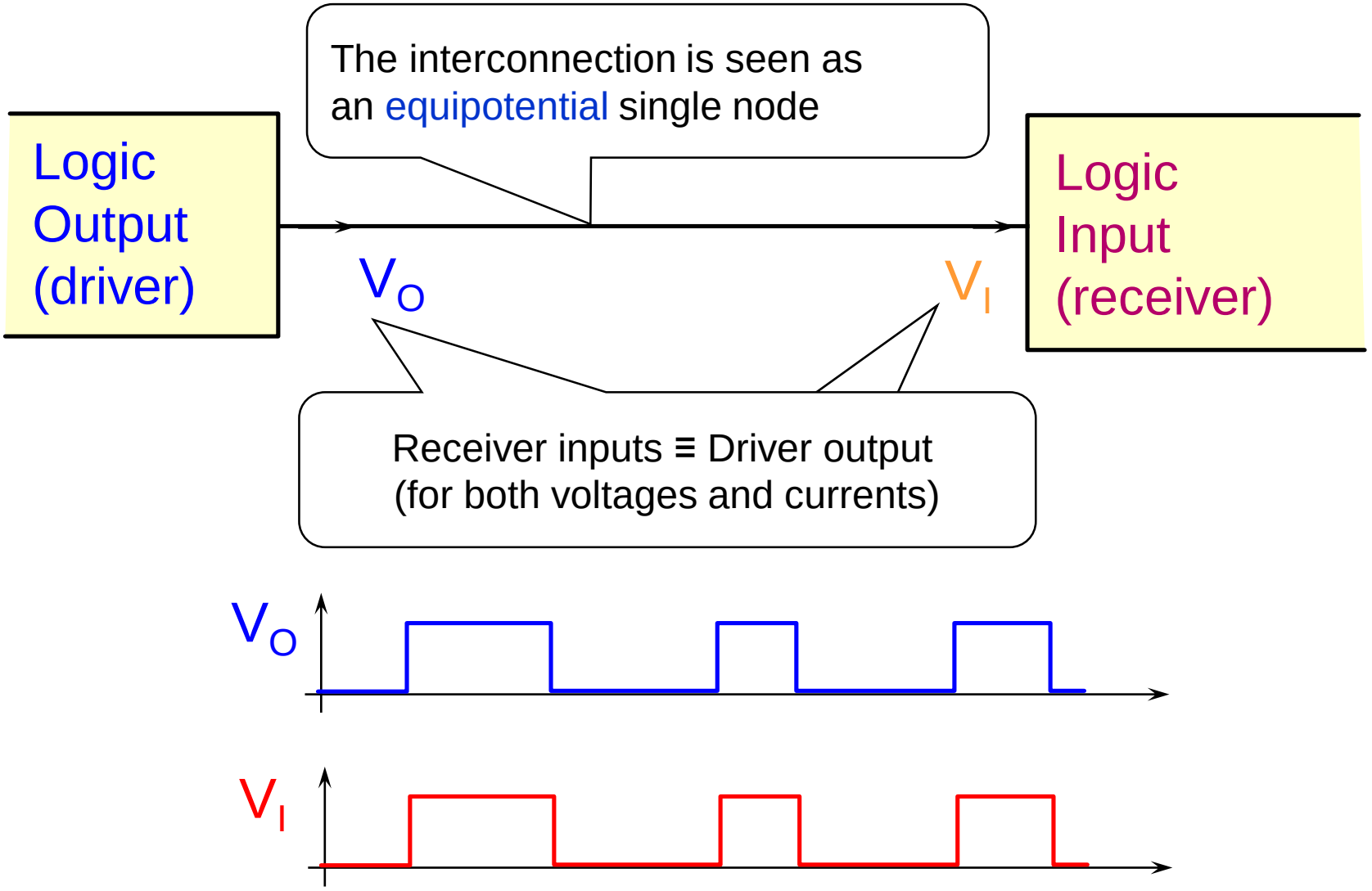
$$T_{CKmin} = T_{CO} + T_L + T_{SU} + T_J + \\ + f(T_{P1}, T_{P2}, T_{P3})$$

$$F_{max} = 1 / T_{CKmin}$$

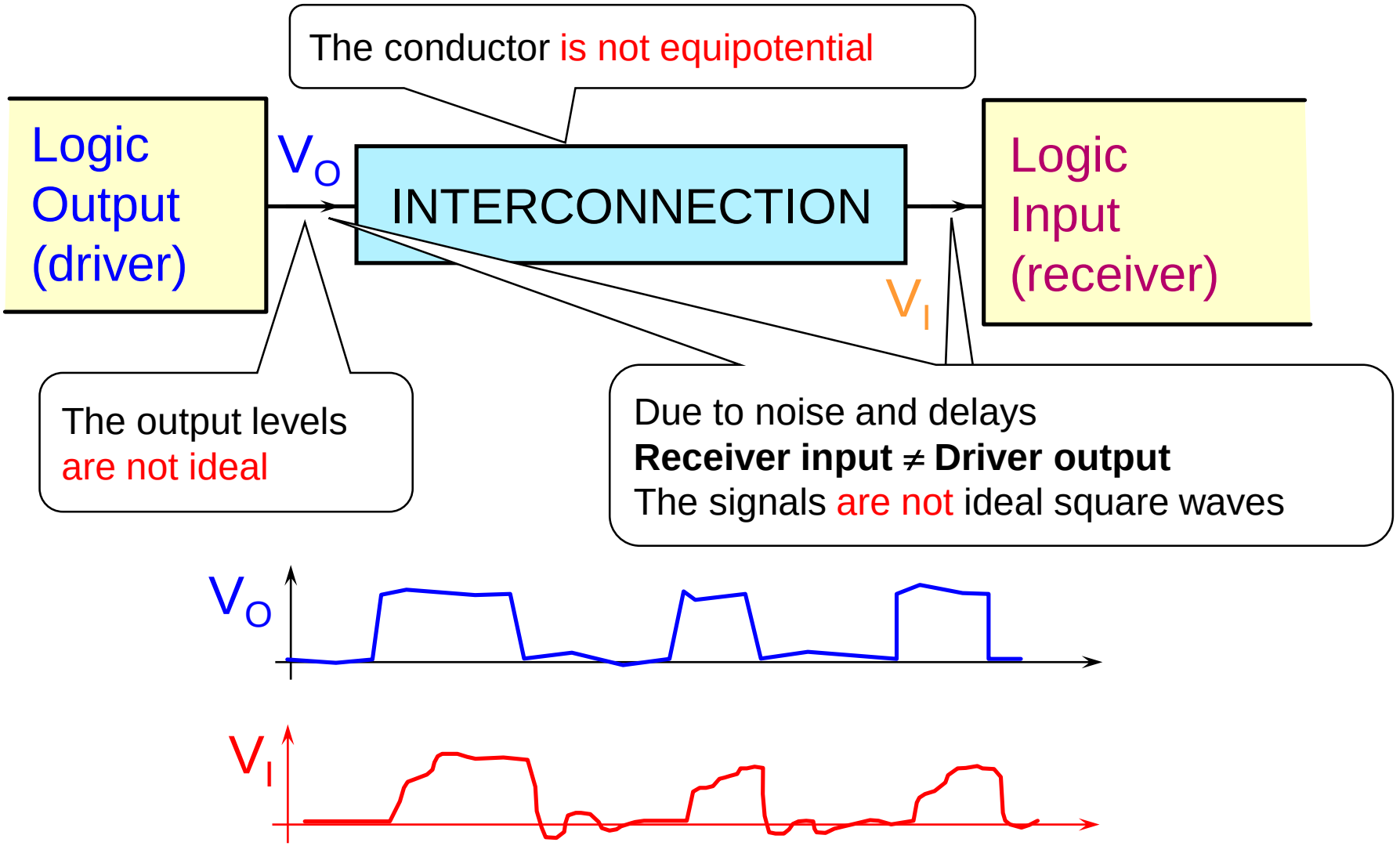
$$F_{max}\,(T_{CO}, T_L, T_{P1}, T_{P2}, T_{P3}, T_J, T_{SU})$$



# Ideal interconnection



# Real interconnection



# Interconnection models

- How to analyze the exchange of digital information?
  - Use a layered pattern (ISO-OSI type)
  - Define services and interfaces for each layer
    - Highest level: application
    - …
    - Lowest level: physical variables (V, I, R, ...)
- These lectures cover the **lower levels**
  - **Physical**: transfer of single bits
  - **Cycle**: transfer of groups of bits
  - **Transaction**: reading instructions/data, writing, ...
- Objectives: correctness, speed, low power

# References to the ISO-OSI Model

- 7 APPLICATION
- 6 PRESENTATION
- 5 SESSION
- 4 TRANSPORT
- 3 NETWORK
- 2 DATA LINK
- 1 PHYSICAL

In lectures of group C

# Signal integrity and protocols

TRANSACTION

Data transfer,
instructions, ...

| CYCLE 1 | CYCLE 2 | CYCLE 3 | | CYCLE N |
|---|---|---|---|---|

CYCLE

Transfer of bit groups

Time margins,
synchronization

Lectures
C3, C4
(protocols)

ELECTRIC level

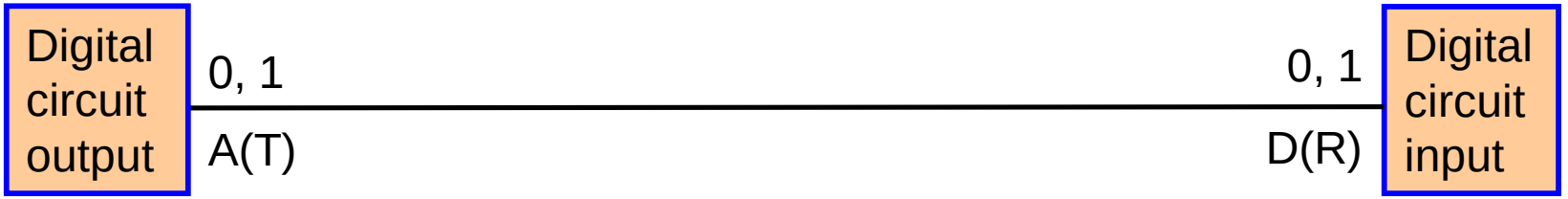
Single bit transfer

Voltages,
Currents,
R, C, Z, ...

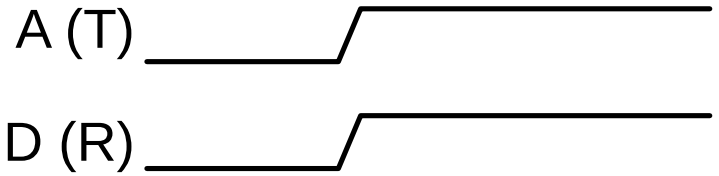
Lectures
C1, C2
(signal
integrity)

# Ideal interconnection (IT)

What happens in a conductor (wire)? → "minimum" model



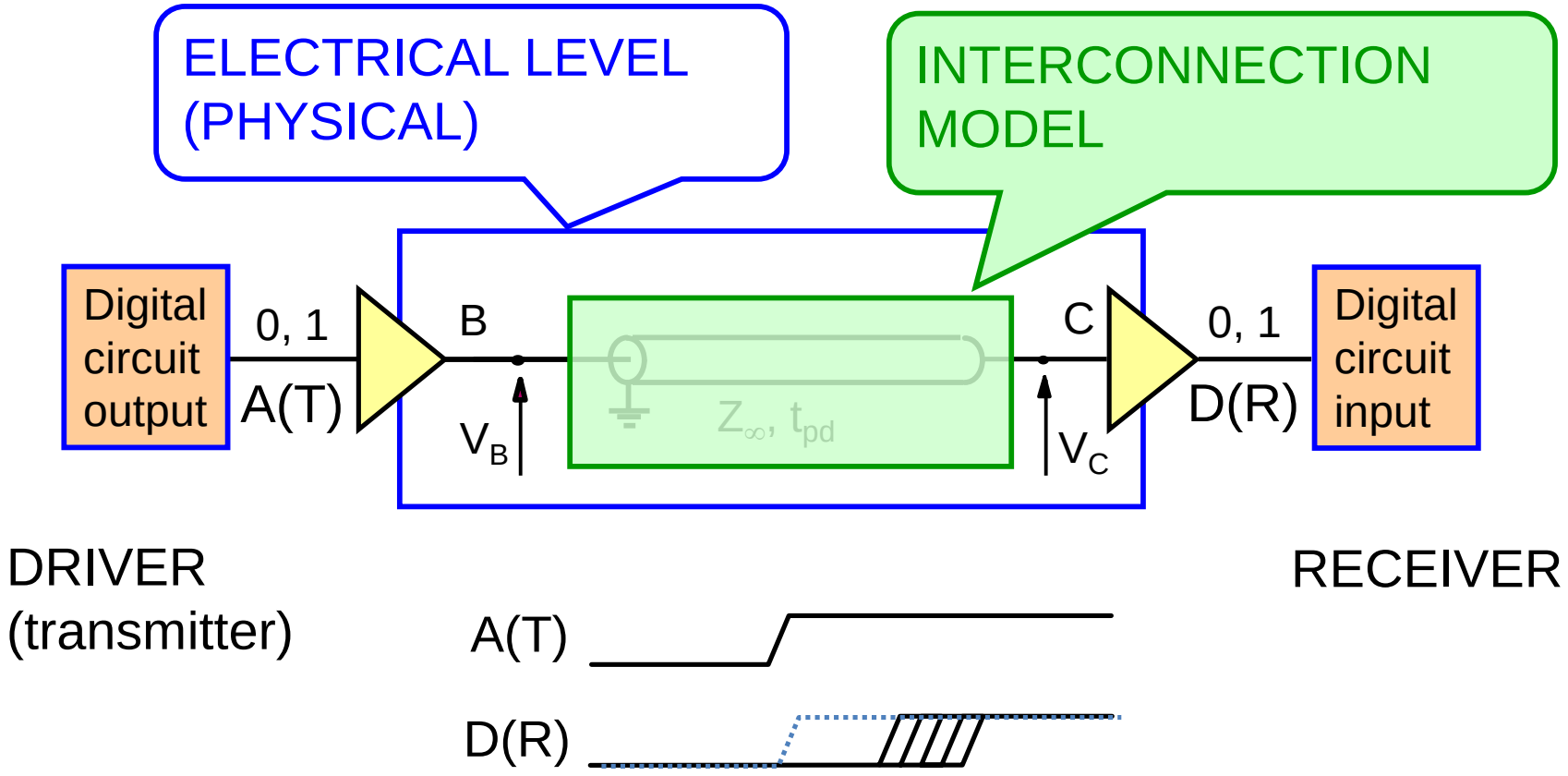

DRIVER (transmitter)




RECEIVER

Same signal at points A and D

# Real interconnection (electronics)




**Analog** effects from B to C: additive noise, delay, ...
**Digital** effects from A to D: delay, skew.

# Analysis sequence

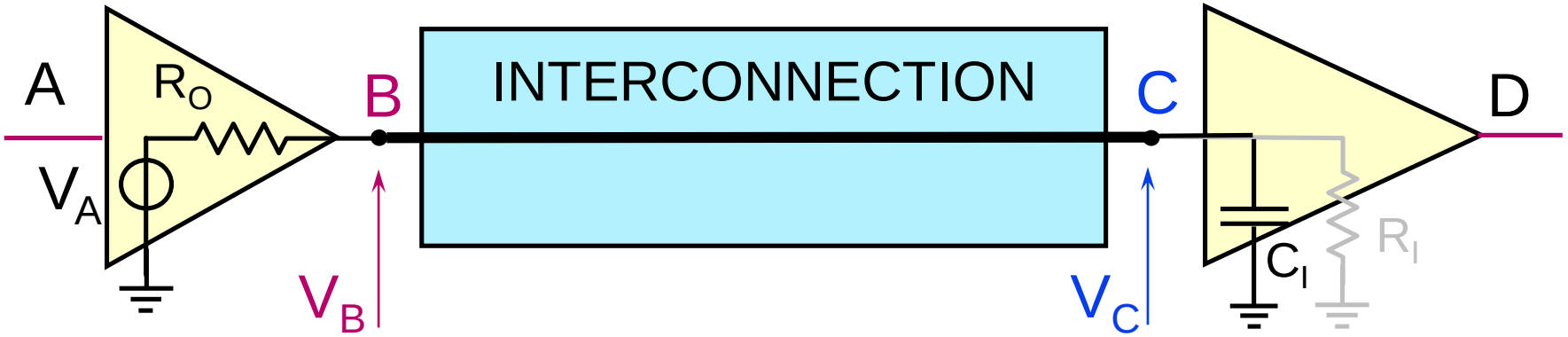
- OBJECTIVES: maximum speed, no errors
  - How to distribute energy and signals to maximize clock freq. $F_{CK}$
    - Limits from structure and physical parameters
  - How to preserve the information correctness
    - Ensure compliance with static and dynamic specifications
- Models and procedures are needed for
  - Static and dynamic interfacing of logic circuits
  - Behavior of interconnections (delays, noise, ...)
  - → Signal integrity
- Correct distribution of power supply is important
  - → Power integrity

# Models for Driver and Receiver

- Linear model for driver and receiver
  - A, D input/output Boolean variables (0, 1)
  - $R_O$ equivalent driver output resistance
  - $R_I$ equivalent input resistance of the receiver ($\rightarrow \infty$)
  - $C_I$ equivalent input capacitance of the receiver

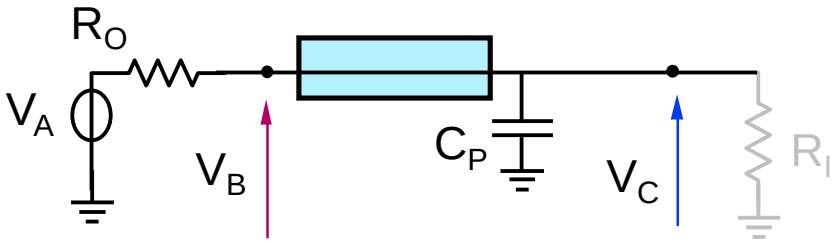
# Single equipotential node

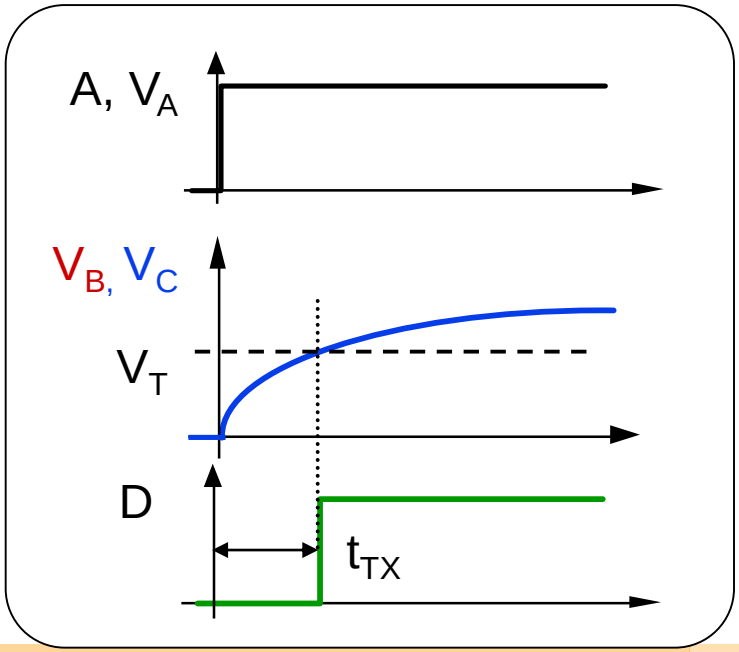
- The simplest interconnection model
  - Interconnection modeled as single node (B ≡ C) (no loss, no delay)
  - One can define the parameters
    - Transmission time: $T_{TX}$
    - Skew (misalignment): $T_K$



# RC model

- Driver-receiver connection modeled as low-pass RC cell
- Voltage step on $V_A$
- Exponential evolution
  - Time constant (tau)
    $\tau = R\,C$
  - Logical state change detected when $V_C$ crosses the threshold $V_T$
- Delay $t_{TX}$ in the reception



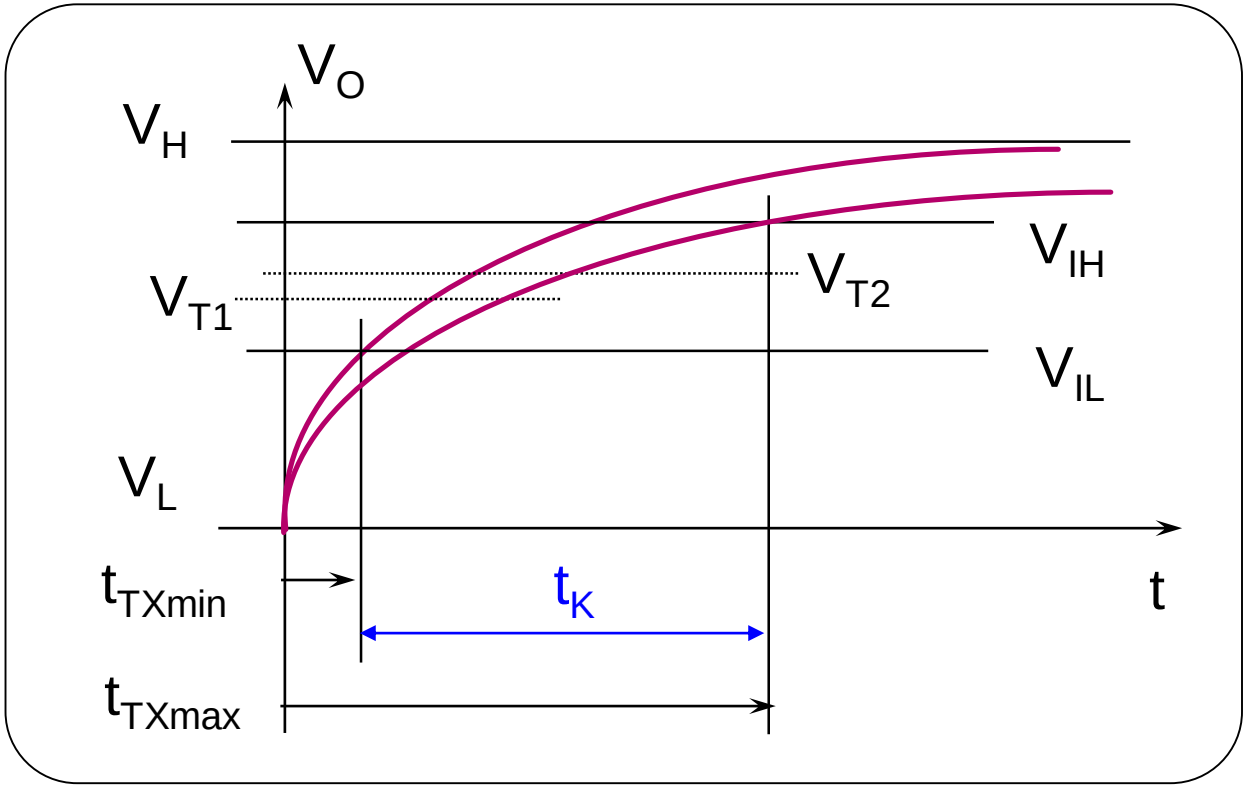



# Transmit Time and Skew

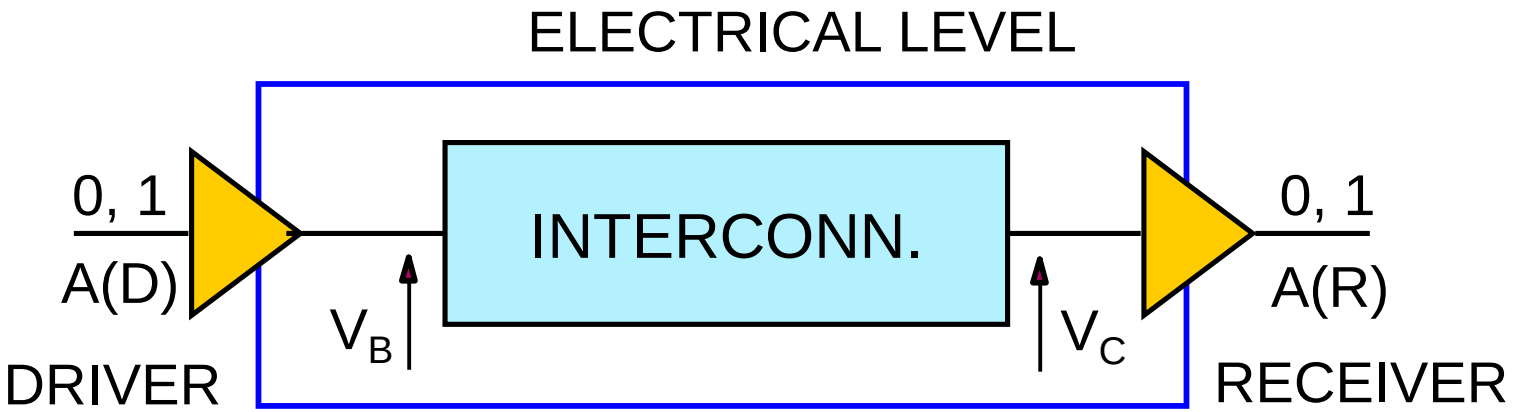
- Delay with which a change in logic state is detected
  - TRANSMISSION TIME ($t_{TX}$)
  - Called also $t_P$ (propagation time)
  - Called $t_{TX}$ here to emphasize the interconnection
- $t_{TX}$ mainly depends on
  - Initial and final levels at the driver output ($V_H$, $V_L$)
  - Threshold of the receiver ($V_T$)
  - Driver output resistance ($R_O$)
  - Receiver input capacitance ($C_I$)
- These parameters can have wide variations
  - $t_{TX}$ depends on interconnection, even with identical components

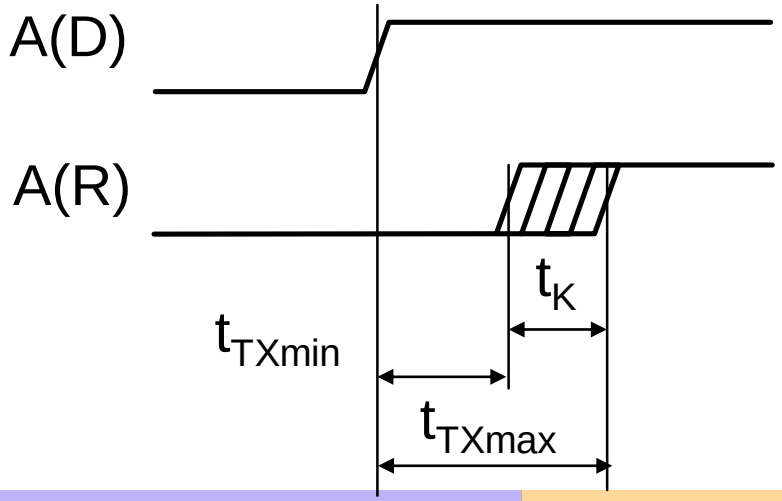
# Variations of $t_{TX}$ and Skew $t_K$

- The difference $t_{TXmax} - t_{TXmin}$ is the SKEW $t_K$
  - The skew (misalignment) to a receiver depends on the dispersion of the parameters that determine $t_{TX}$
    - $\Delta R_O$
    - $\Delta C_I$
    - $\Delta V_{H/L}$
    - $\Delta V_T$
    - ...



# Parameters of an interconnection



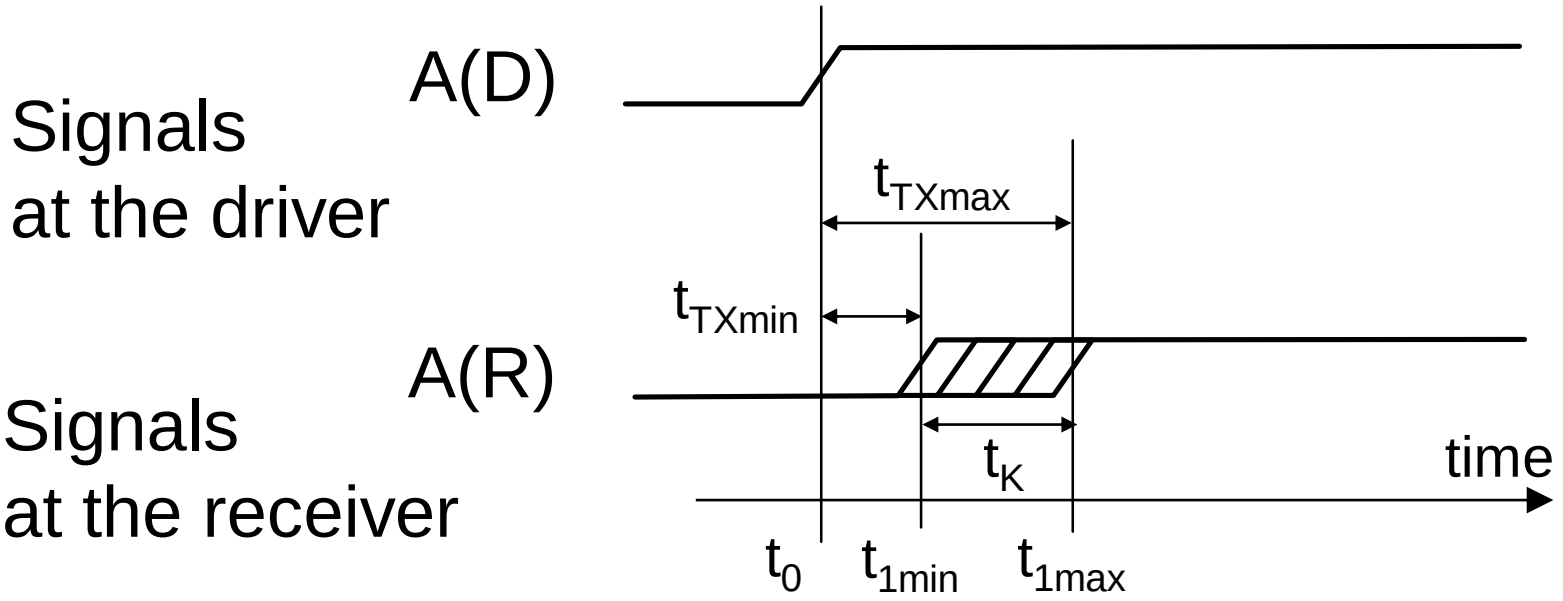

$t_{TX}$ → transmission time
$t_{TXmax}$ → transmission time max
$t_{TXmin}$ → transmission time min
$t_K = t_{TXmax} - t_{TXmin}$ → SKEW

# Exercise C1.1: RC model delays

- A CMOS driver and receiver are connected using an equipotential conductor with the parameters
  - Driver: $V_{DD}$ = 5 V, $R_O$ = 120 Ω
  - Receiver: $R_I \rightarrow \infty$, $V_{IH}$ = 3 V, $V_{IL}$ = 1 V
  - Total equivalent capacitance: C = 80 pF
- For a transition L→H plot the signals on
  - Driver input
  - Driver output – conductor – receiver input
  - Receiver output
- Calculate the transmission time $t_{TX}$ and the skew $t_K$

# Effects of skew – single signal

- The skew is the indetermination of the time position of the signal at the receiver – example only for signal A
  - $t_{1min} = t_{TXmin}$
  - $t_{1max} = t_{TXmax} = t_{TXmin} + t_K$



# Effects of skew – pair of signals

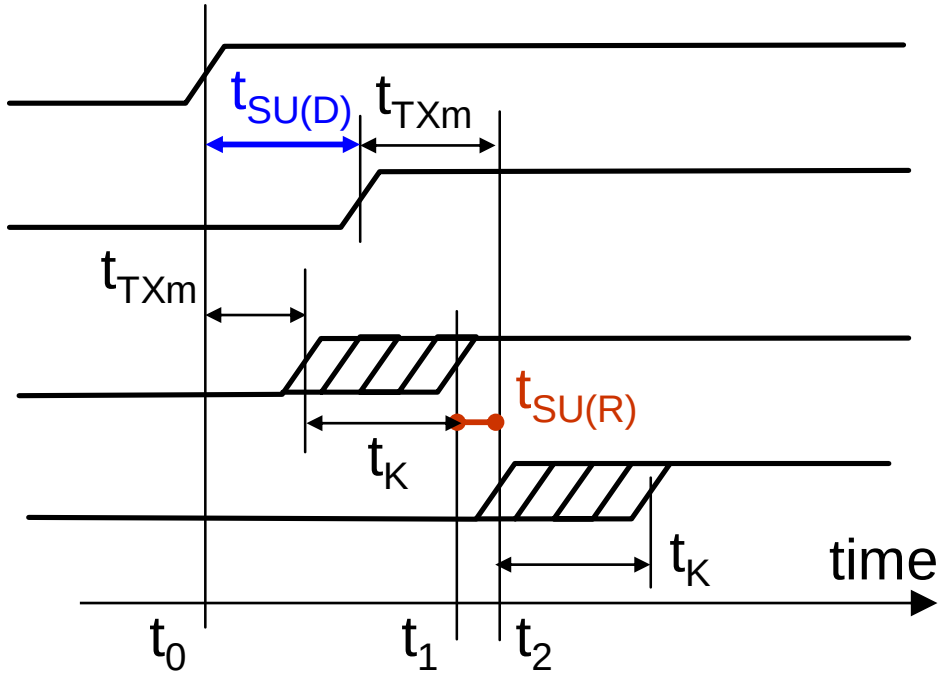
- Skew changes temporal relationships between signals
  - The set-up time $t_{SU}$ is reduced by $t_K$

$t_1 = t_0 + t_{TXm} + t_K$ $\quad$ $t_2 = t_0 + t_{SU(D)} + t_{TXm}$

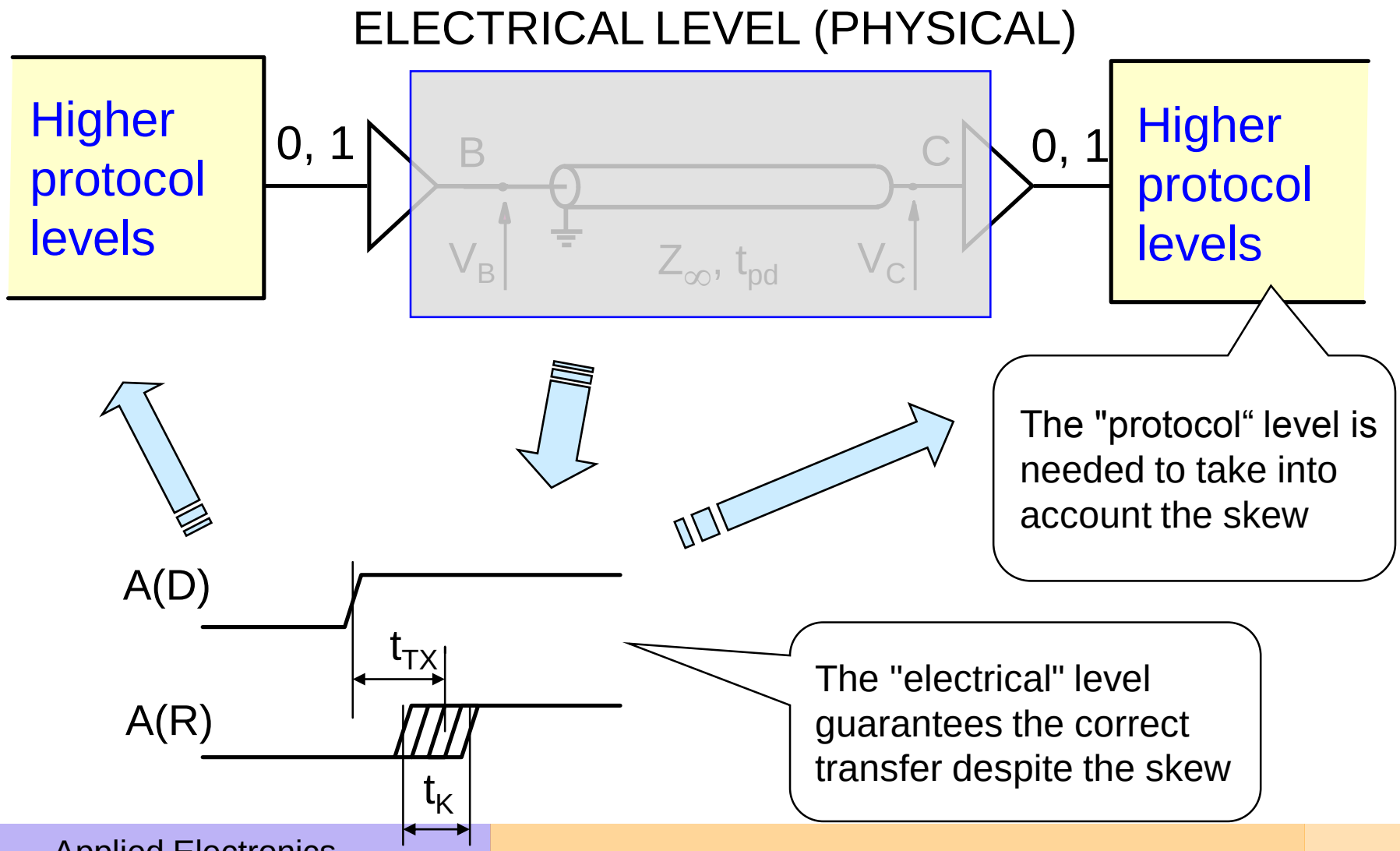
$t_{SU(R)} = t_2 - t_1 = t_{SU(D)} - t_K$

Signals at the driver

Signals at the receiver



# Model of the lower layers



# Lecture C1 – final test

- Why is the analysis of interconnections important?
- Describe the structure and advantages of a layered model.
- Explain the meaning of “signal integrity”.
- What is the logic state at the output of an inverter with input voltage $V_I$, where $V_{IL} < V_I < V_{IH}$?
- Define the propagation time and skew.
- For a CMOS driver-receiver pair, does a change in the supply voltage change the transmission time (as a first approximation)?