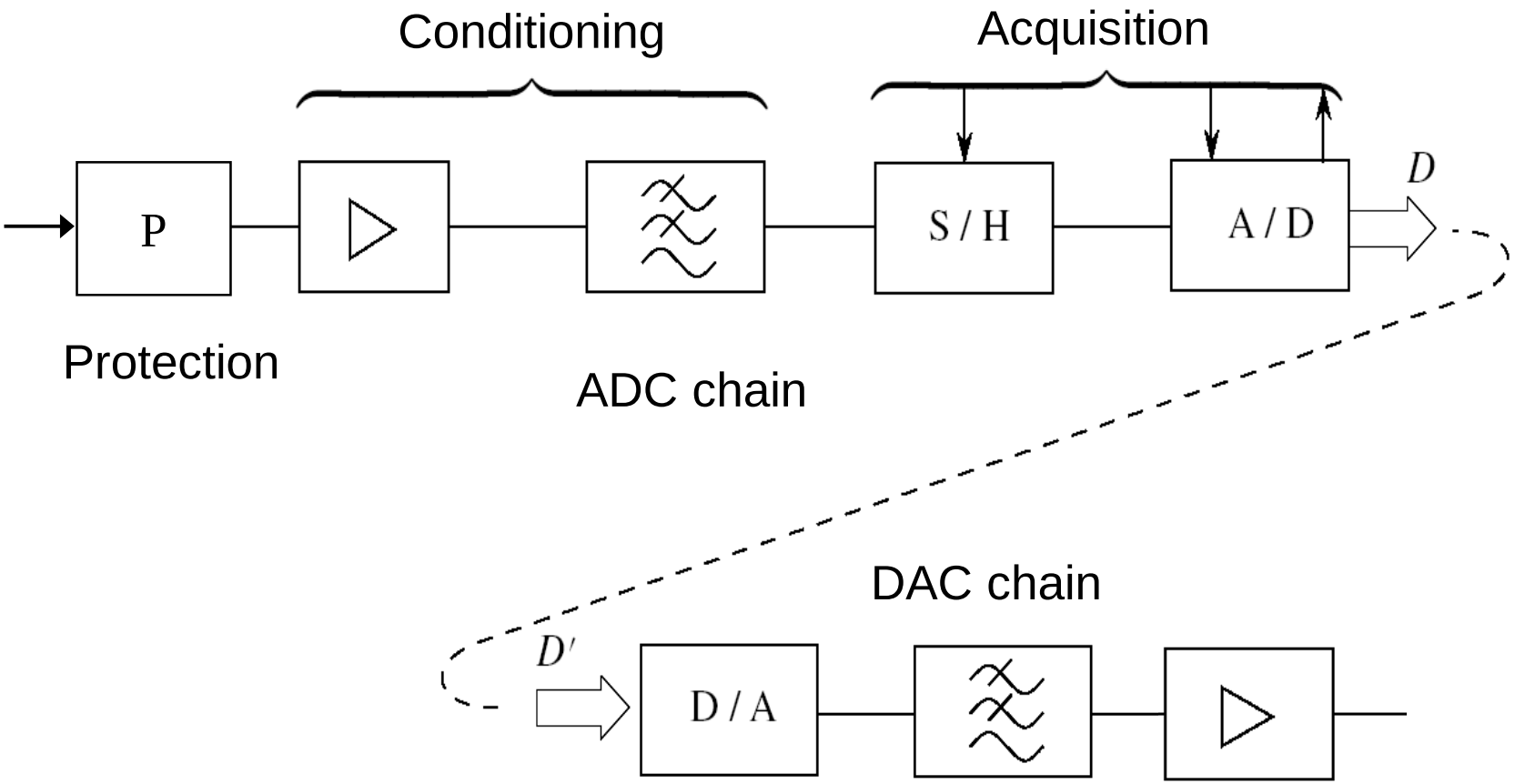
Applied Electronics

Signal Conditioning and Sampling

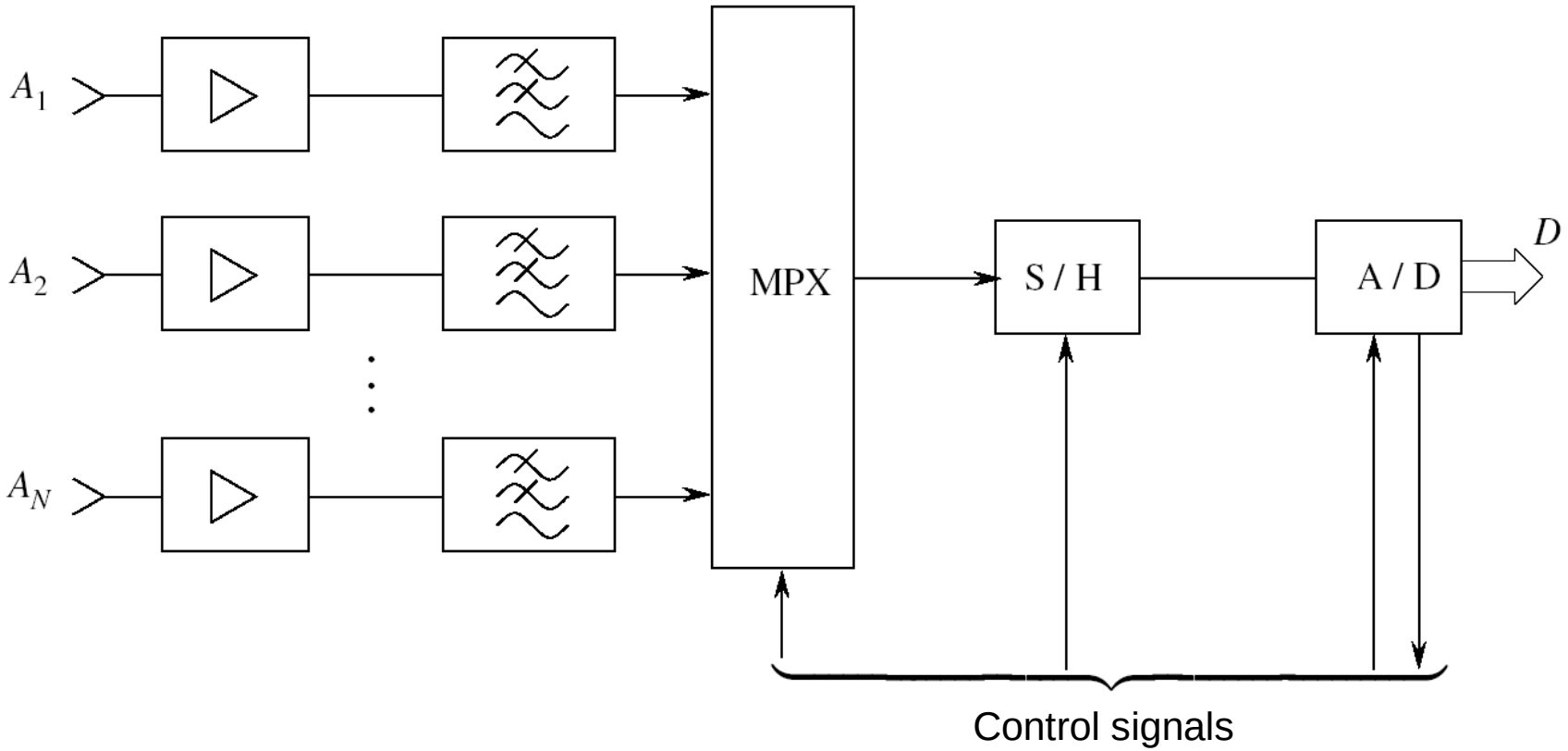
A/D–D/A system block diagram



Complete ADC chain

- Input protection circuits
  - Block signals which may damage the other circuits
- Amplifier
  - Make signal level compatible with ADC input range
  - Optimize SNRq
- Anti-alias filter
  - Makes signal bandwidth compatible with sampling rate
- Multiplexer (for multiple channel systems)
- Sample/Hold or Track Hold
  - Sampling (discretize in the time axis)
- A/D Converter
  - Quantization (discretize in the amplitude axis)

Multiple channel system

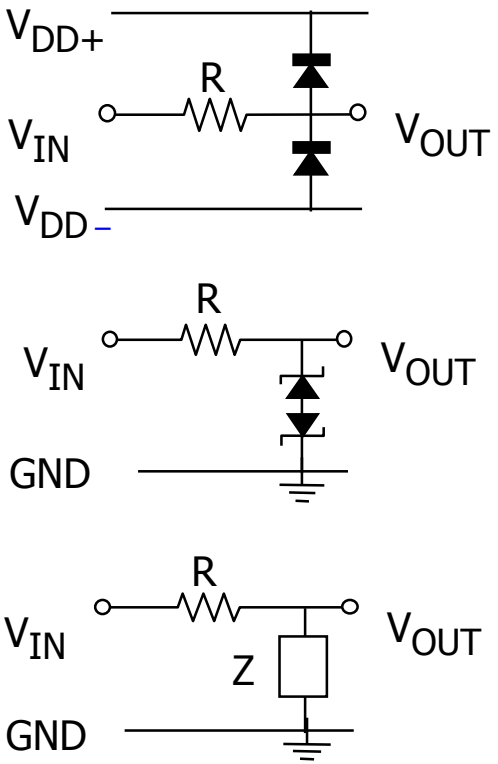


Input protection circuits

- Signal from the field
  - Electrostatic charges
  - EMI, noise
  - Direct contacts (unplanned)
- Need to limit input voltage within safe limits, to avoid damage to the system
- Usual limits (non-damaging)
  - Inputs between supply voltage, but V_{DD} = 0 V when powered off!
- Input protection circuits
  - Diode clamp
  - Special devices (Zener diodes, varistor, …)

Amplitude limiting circuit

- Clamp towards power supply
  - V_{OUT} limited between V_{DD+} and V_{DD-}
- Zener diodes to GND
  - V_{OUT} limited to Zener voltage + V_γ
- Specific devices
  - V_{OUT} limited by characteristic $V(I)$ of Z



- In all circuits, the series resistance *R* limits the input current when the protection is active

ADC input dynamic

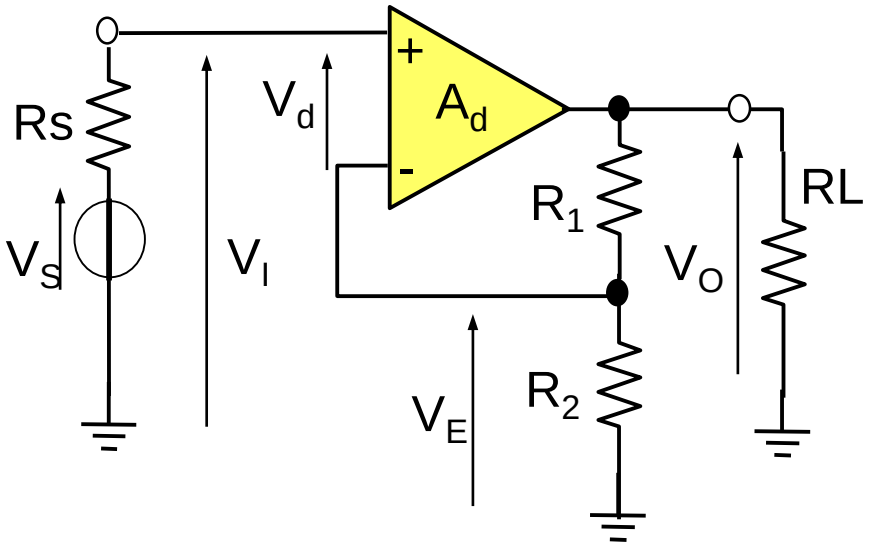
- The A/D converter has an input dynamic range
  - Unipolar: 0 ... S, 0 … 5 V, 0 … 10 V
  - Bipolar: –S/2 … + S/2, –5 … + 5 V, –10 … +10 V
- For max SNRq the signal must match the dynamic range
  - Amplifier (or attenuator)
  - Level shifter (bipolar/unipolar)
  - Signal level must match the system (ADC) dynamic range

Signal types

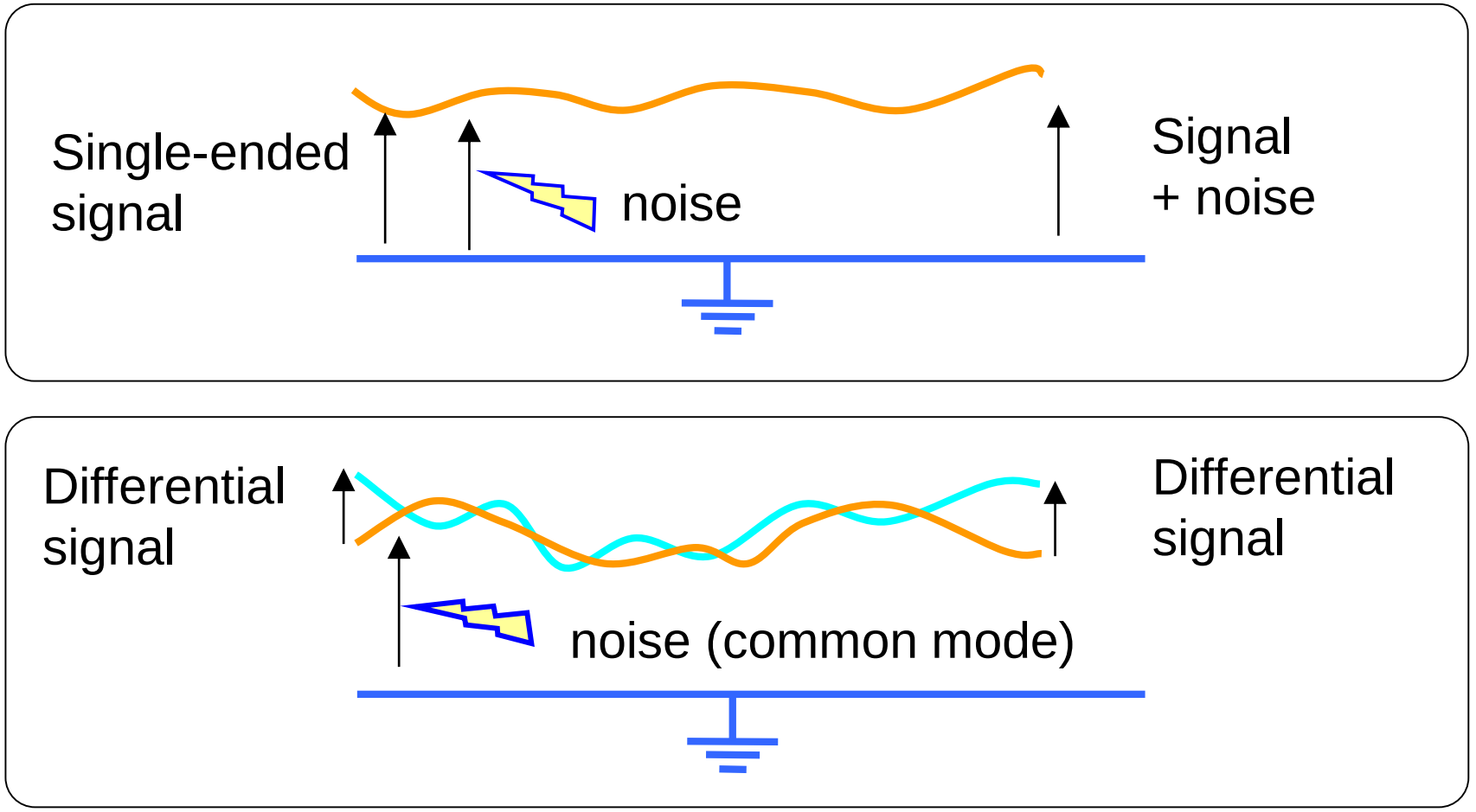
- The ADC accepts specific signal types
  - Voltage or current (V/I)
  - Single-ended or differential (S/D)
- The unit that matches the dynamic range is the conditioning amplifier
- Many configurations
  - V→V, V→I, I→I, I→V
  - S→S, S→D, D→S, D→D
  - 16 combinations + the offset and gain

Voltage amplifier

- Single-ended voltage amplifier
  - Operational amplifier with feedback
  - $A_V = \frac{V_O}{V_I} = \frac{R_1}{R_2} + 1$
  - High Z_I
    - R_S does not affect A_V
  - Low R_O
    - R_L does not affect A_V



Single-ended and differential signals

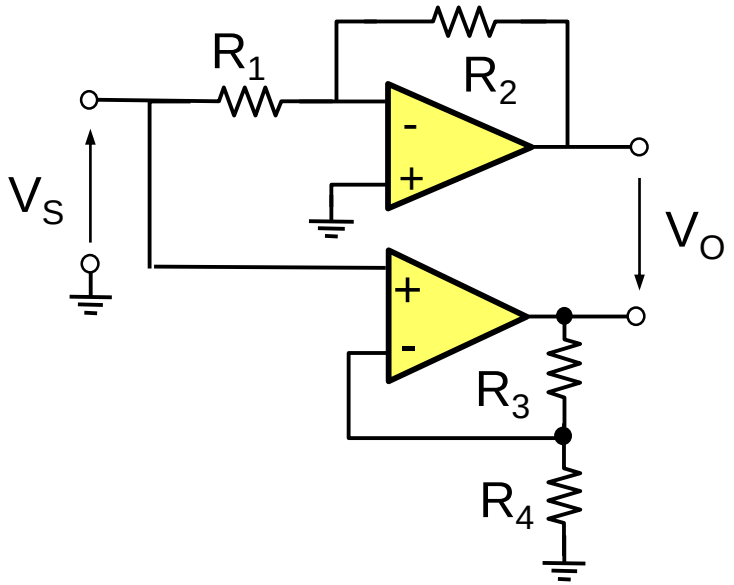


Differential signals

- Differential signals are insensitive to common mode noise
- Differential signals do not emit noise
- Some transducers have differential outputs
- Fast and accurate A/D converters use differential signals
- To handle differential signals
  - Single-ended ⇔ differential converters
  - Differential amplifiers
  - Instrumentation amplifiers

From single-ended to differential

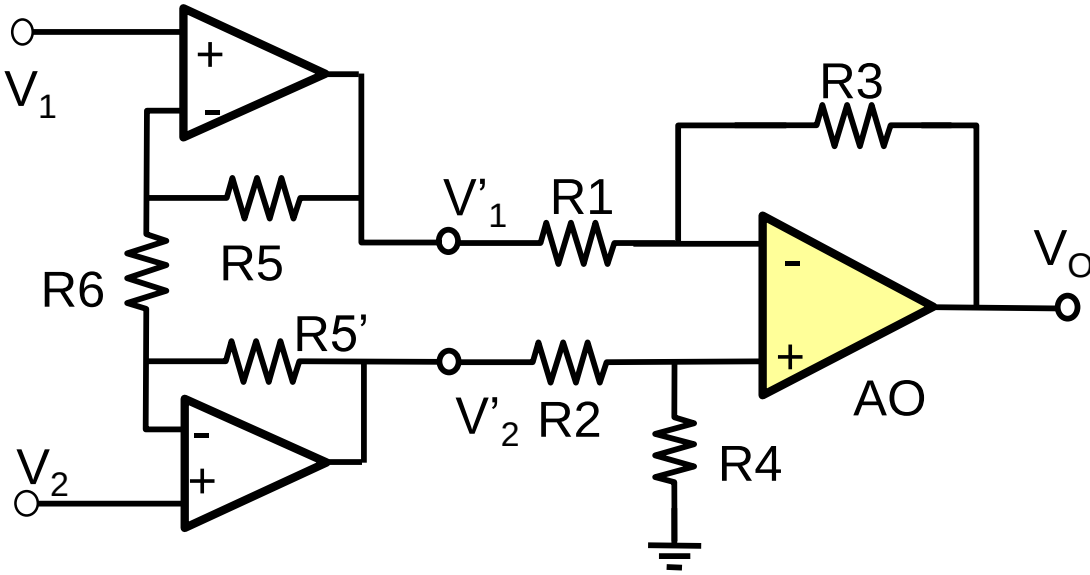
- Two amplifiers with the same $|A_V|$
  - Inverting
    - $A_V = -\frac{R_2}{R_1}$
  - Noninverting
    - $A_V = \frac{R_3}{R_4} + 1$
    - $V_O = V_S\left(\frac{R_3}{R_4} + 1 + \frac{R_2}{R_1}\right)$
- Operational amplifiers with differential output
- Fully differential circuits



Instrumentation amplifier

- Voltage followers on inputs
- AO rejects common mode signals (noise)
- If $R_5' = R_5 \Rightarrow V_2' - V_1' = (V_2 - V_1)\left(2\frac{R_5}{R_6} + 1\right)$
- If then $\frac{R_3}{R_1} = \frac{R_4}{R_2}$

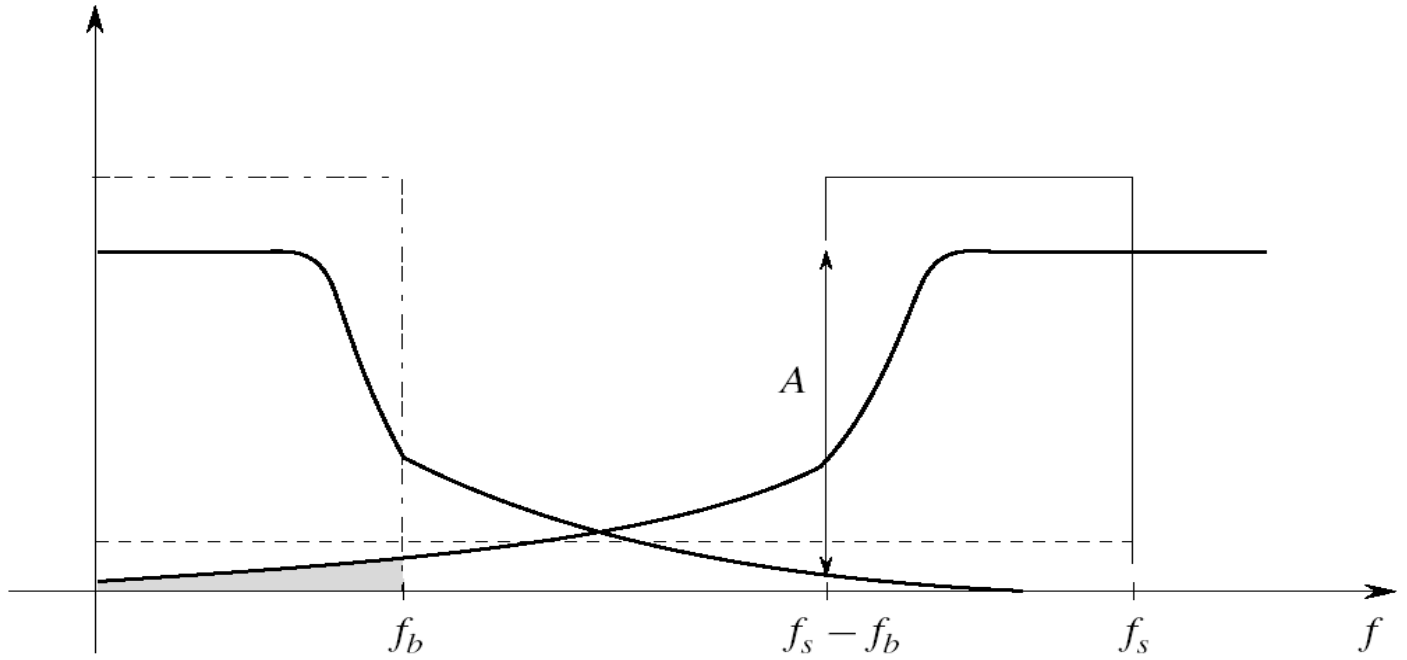
$$V_O = (V_2 - V_1)\left(2\frac{R_5}{R_6} + 1\right)\frac{R_3}{R_1}$$



Anti-alias filter

- Signals have a nominal bandwidth
  - Contains useful information
- Signals include also outband components
  - Noise, distortion, …
- Upon sampling, outband components are folded within the signal bandwidth
  - Aliasing noise
- Aliasing noise depends on two parameters
  - Shape of the outband spectrum
  - Sampling rate

Inband folding of signal spectrum



Outband signal folded by sampling into the useful band

Quantization noise

Reconstruction filter mask

Reducing aliasing noise

- Lower outband signal level
  - Steeper input filter (more expensive)
- Increase sampling rate F_S (oversampling)
  - Moves alias spectra away from baseband
  - Higher sample rate is more expensive
- Oversampling A/D chain
  - Anti-alias input filter (analog, simple)
  - High-rate sampling
  - Fast A/D conversion → high bit rate
  - Bit rate reduction with digital filter (decimation)
  - Move complexity from analog to digital domain

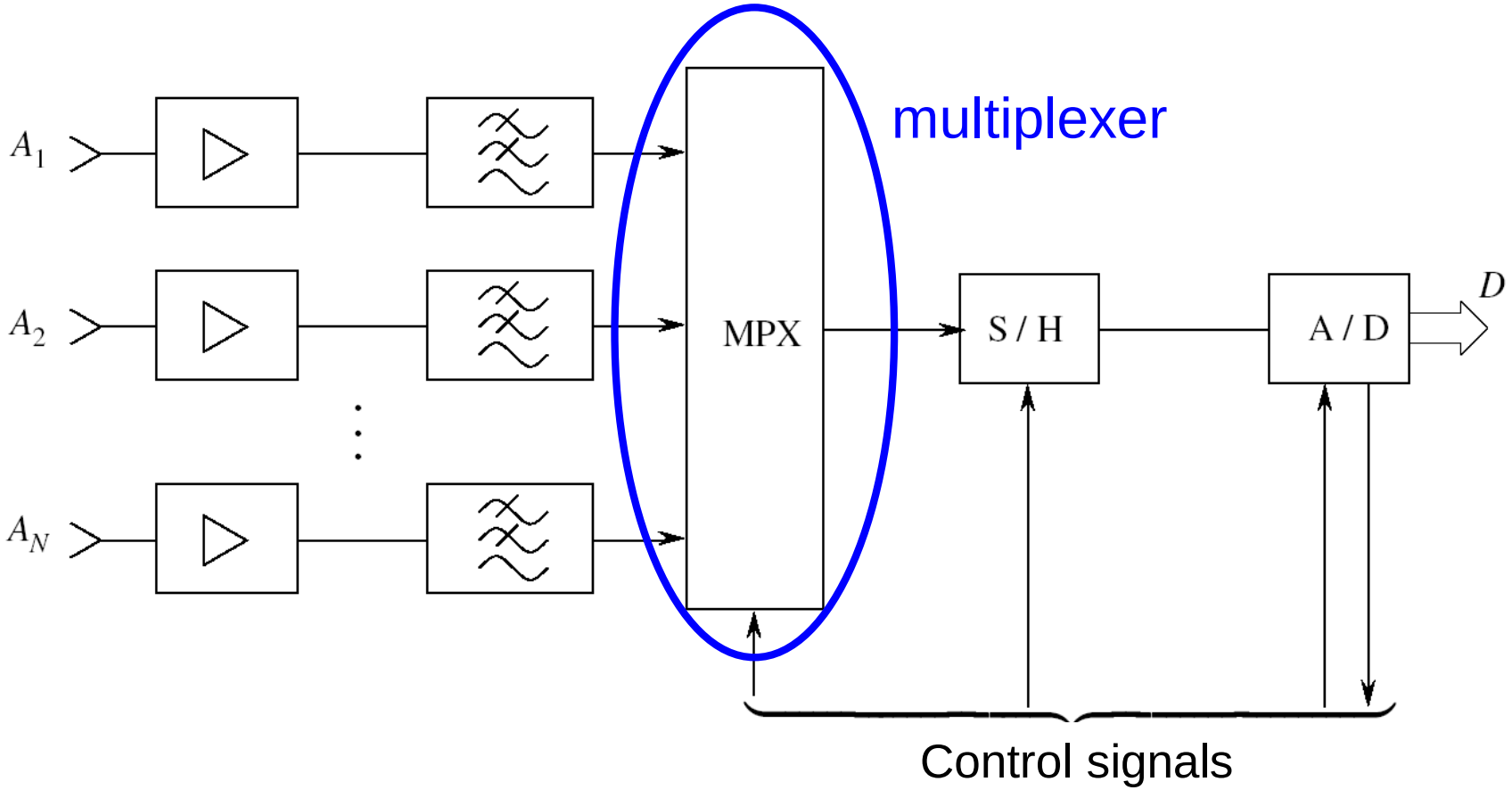
Anti-aliasing filter parameters

- Signal-to-noise ratio is SNR_{A}
  - Signal amplitude outside signal bandwidth is S
  - Anti-aliasing filter specifications
    - No attenuation up to f_{B}
    - Attenuation by SNR_{A} dB at $f_{\mathrm{S}} - f_{\mathrm{B}}$
- From f_{B} to $f_S - f_{\mathrm{B}}$ is a relative frequency range $\frac{f_{\mathrm{S}} - f_{\mathrm{B}}}{f_{\mathrm{B}}}$
  - Each filter pole attenuates 6 dB per octave
  - One pole attenuates from f_{B} to $f_{\mathrm{S}} - f_{\mathrm{B}}$
  - $A_{\mathrm{P}} = 6 \log_2 \left(\frac{f_{\mathrm{S}} - f_{\mathrm{B}}}{f_{\mathrm{B}}} \right)$ dB or $A_{\mathrm{P}} = 20 \log_{10} \left(\frac{f_{\mathrm{S}} - f_{\mathrm{B}}}{f_{\mathrm{B}}} \right)$ dB
- Number of necessary poles: $P = \frac{SNR_{\mathrm{A}}}{A_{\mathrm{P}}}$
  - Conservative estimation, depends on filter type

Exercise: anti-aliasing filter dimensioning

- Signal bandwidth: $f_B = 12$ kHz
- Sampling frequency: $f_S = 50$ ks/s
- 12-bit conversion: $SNR_q = 6N + 1.76 = 73.8$ dB
- Aliasing noise equal to quantization noise
  - $SNR_a = SNR_q = 73.8$ dB
- Calculate the number of poles of the anti-aliasing filter
  - $A_P = 6 \log_2\left(\frac{f_S - f_B}{f_B}\right) = 20 \log_{10}\left(\frac{f_S - f_B}{f_B}\right) = 20 \lg\left(\frac{50-12}{12}\right) = 10$ dB
  - $P = \frac{SNR_A}{A_P} = \frac{73.8}{10} = 7.4$ poles ➔ 8 poles

Multiple channels system

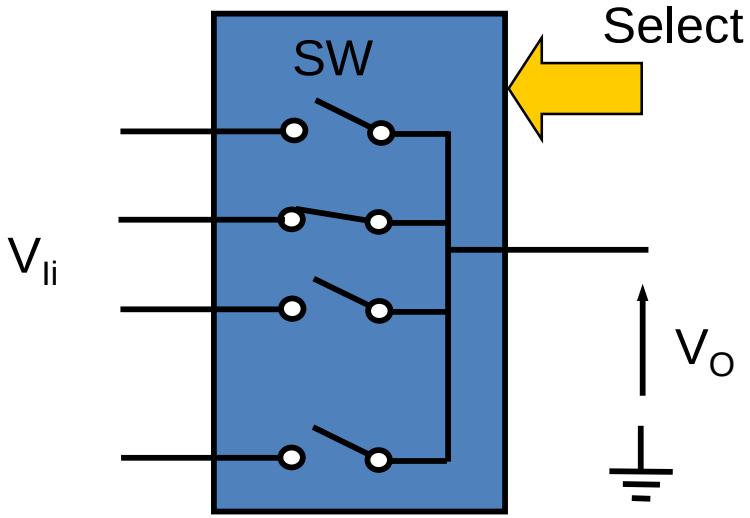


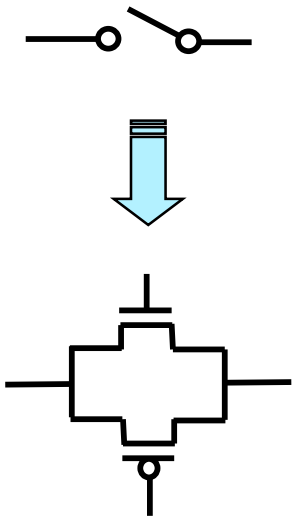
Multiplexer

- Allows to use the same functional units (S/H and A/D) for several channels
- Must select one channel among N
  - Must not modify the selected signal
  - Must block other channels
- Multiplexer parameters
  - Equivalent series resistance R_{ON}
  - Leakage current I_{OFF}
  - Insulation/feedthrough
  - Settling time
  - Input range, …

Multiplexer structure

- Switches built with MOS (or CMOS) transistors
- Decoding and command circuits

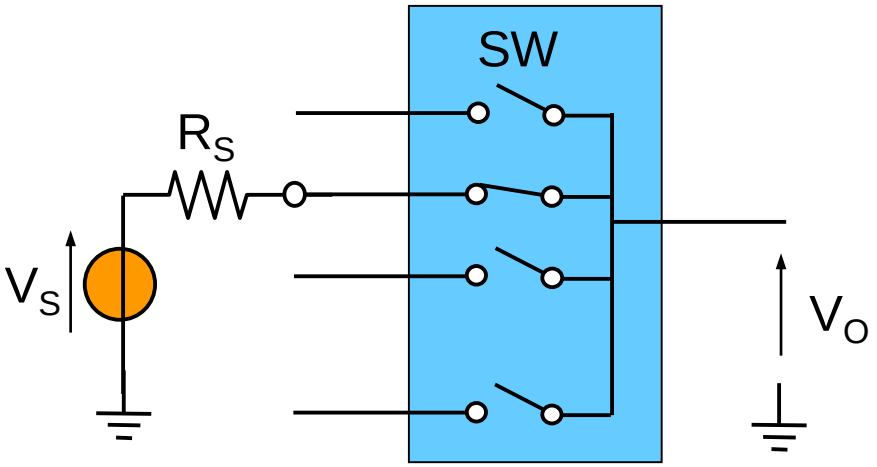




Multiplexer error sources

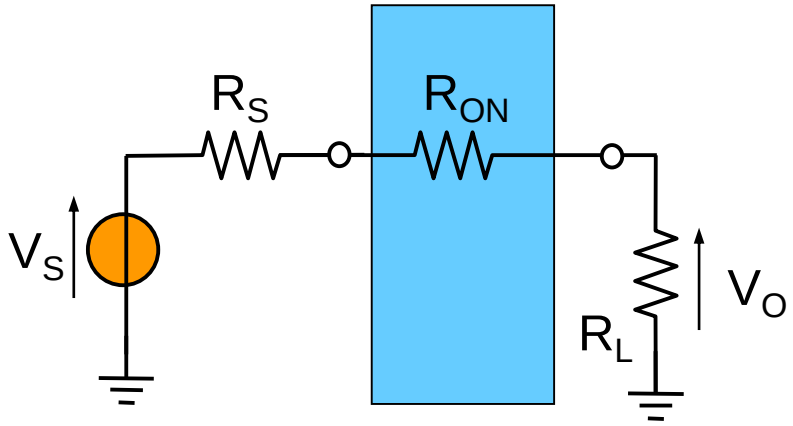
- MOS switch model
  - ON: resistor R_{ON}
  - OFF: leakage current I_{OFF} + parallel capacitor C_{DS}
- Partition from V_I to V_O caused by R_{ON}
- Offset caused by leakage currents of open switches
- Feedthrough from other channels (through C_{DS})
- Dynamic parameters
  - Switching delay
  - Bandwidth (RC low-pass cells)

Ron error

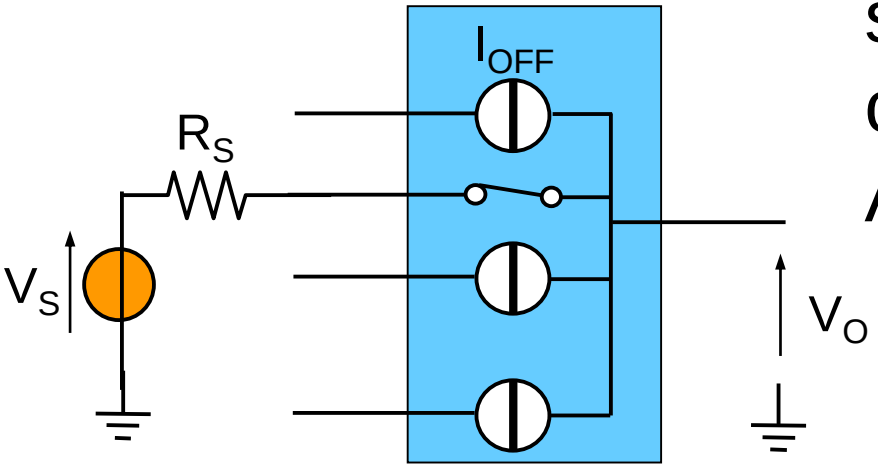


Only one switch is closed (ON) to select the input channel V_S connected to V_O ouput.

An ON switch has an equivalent resistance R_{ON}. Gain from V_S to V_O is < 1 due to voltage divider made by R_{ON} with the load resistance R_L.

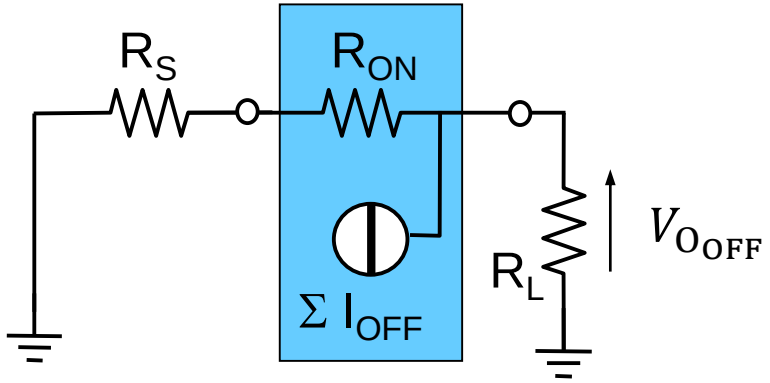


I_{off} error

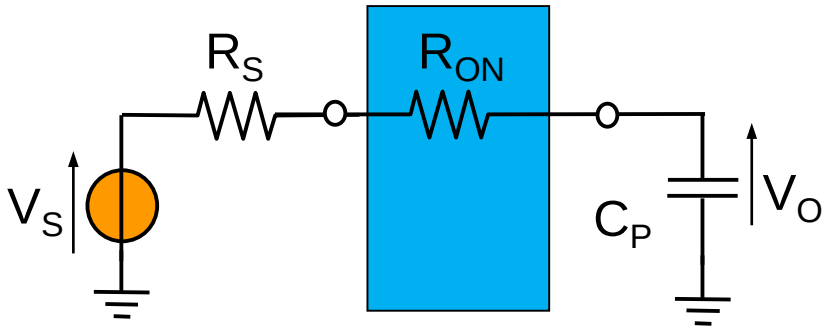


Only one switch is closed (ON) to select the input channel V_S connected to V_O ouput.
All other switches are open (OFF).

Any OFF switch has a leakage current I_{off}.
The sum of all I_{off} causes an offset voltage V_{Ooff} on the output.



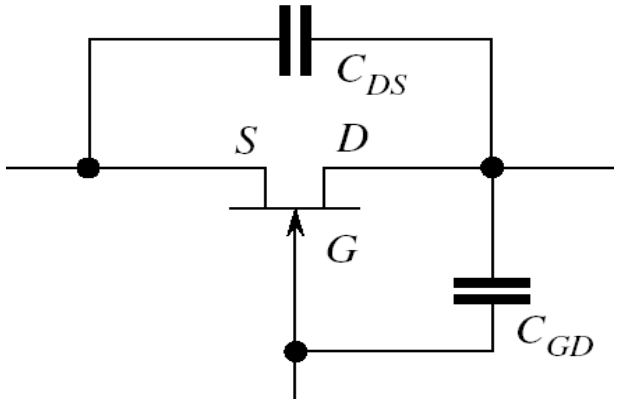
Frequency limit



The parasitic capacitance of multiplexer and load limit the transferred signal bandwidth.

The signal path includes the lowpass cell R_{ON} / C_P .

The C_{GD} and C_{DS} paritic capacitances generate respectively pedestal and feedthrough errors (as in S/H circuits).



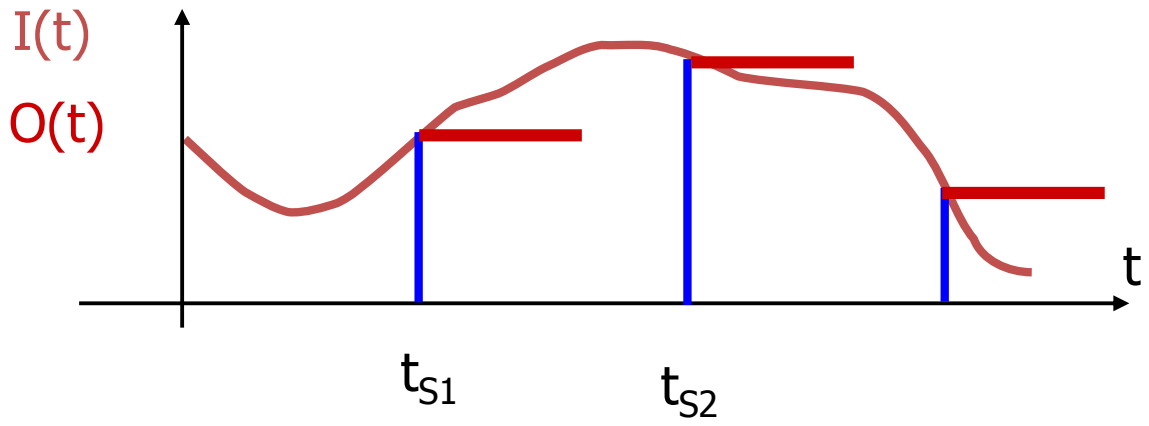
Where to place the multiplexer

- The multiplexing operation changes the signal spectrum
  - For example, two dc signals become a square wave
- The mux must be placed *after* the filter
- S/H and ADC can be used on many channels
  - IF each sampling and conversion is independent from the previous values (e.g., do not use tracking ADCs)
- The filter *cannot* be used on multiple channels
  - It keeps track (memory) of the previous signal values

→Crosstalk between channels

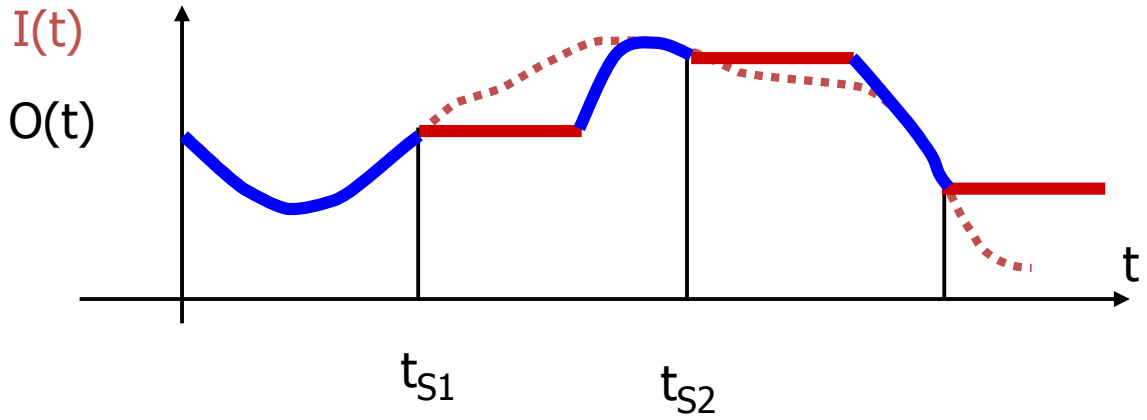
Sample-Hold unit

- Function: sample the input analog signal I(t)
  - Sampling at $t = t_s$ → multiply input signal by $\delta(t_s)$
  - Keep stable the sample value at the output (O) as long as it is required for the A/D conversion
    - HOLD operation



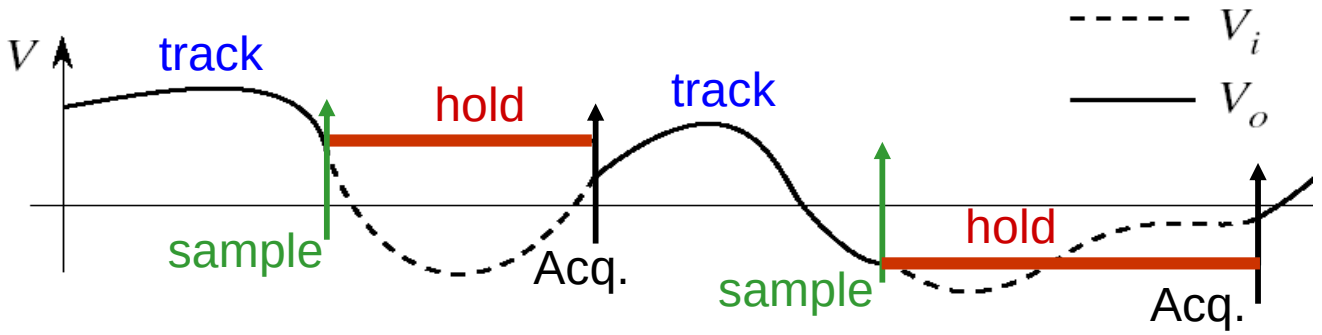
Track-Hold operation

- Before the next sampling operation, the circuit must acquire the new value
- The complete sequence is
  - Tracking: $O(t) = I(t)$
  - Sampling: $O = I(t_s)$
  - Hold: $O(t) = I(t_s)$
  - New tracking



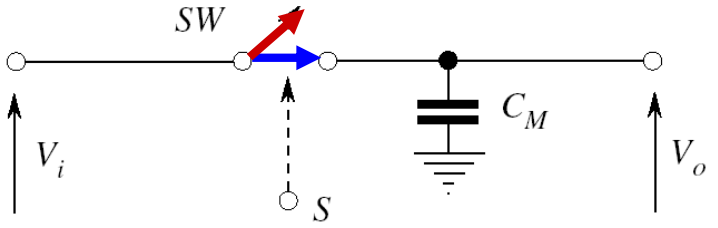
Track-Hold operation sequence

- Track
  - output = input
- Sample
  - reading the analog signal value
  - transition from Track to Hold
- Hold
  - constant output, corresponding to sampled value
- Acquisition
  - the ADC operates during this phase

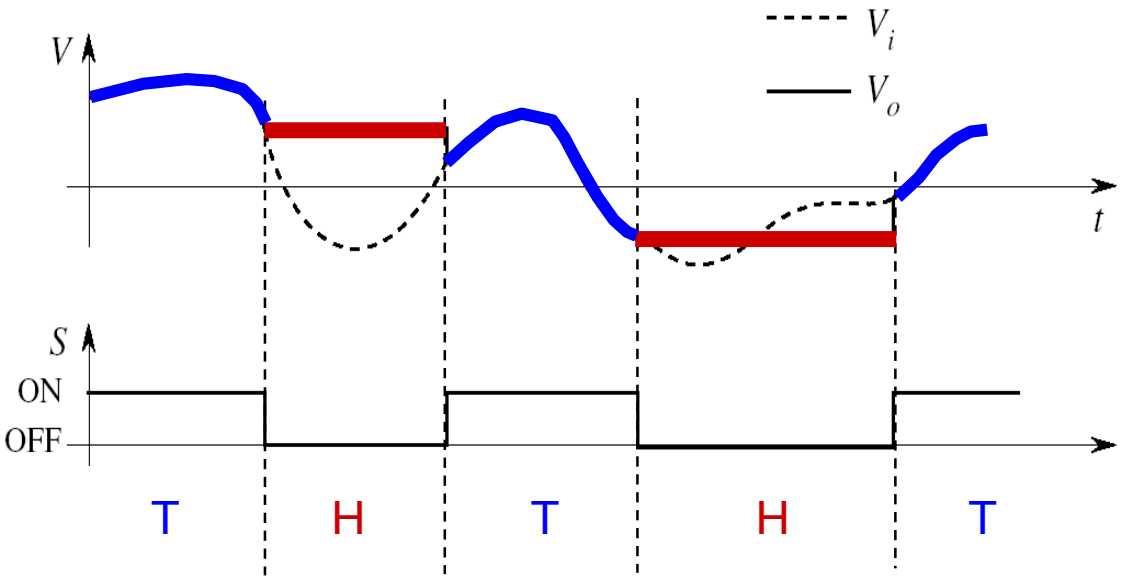


Basic Circuit: Track and Hold state

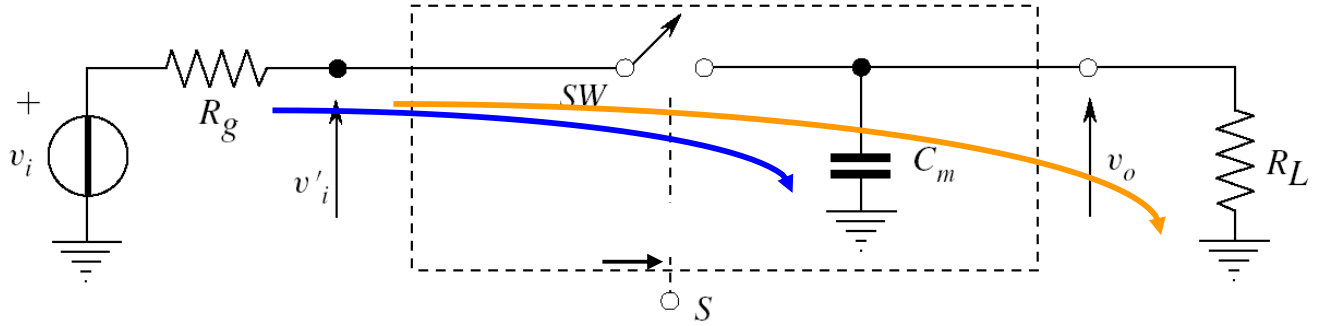
- The Sample/Hold is an analog memory
  - Capacitor
  - Switch



- Track:
  SW ON
- Hold:
  SW OFF



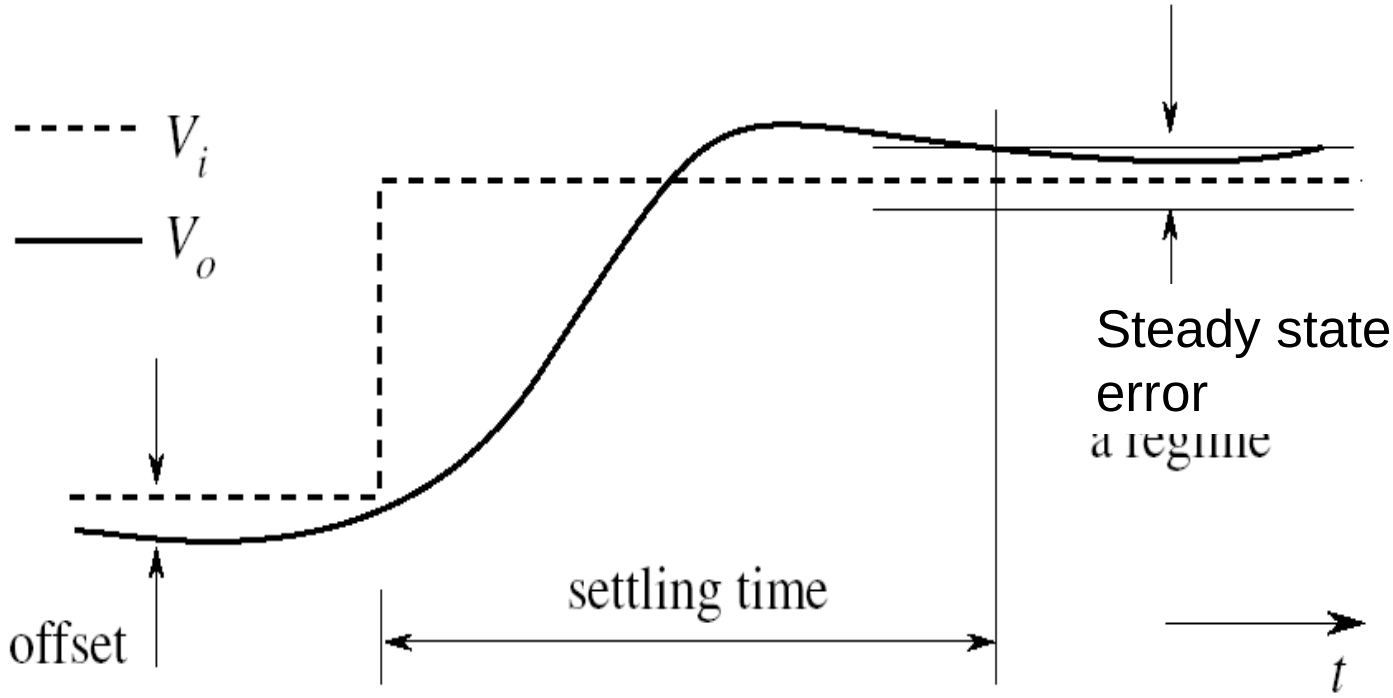
Tracking: gain error



- Partition of Vi between Rg and R_L
  - Gain error
- Lowpass RC cell
  - Bandwidth limit
  - Settling time for transient response
  - Offset, nonlinearity, …

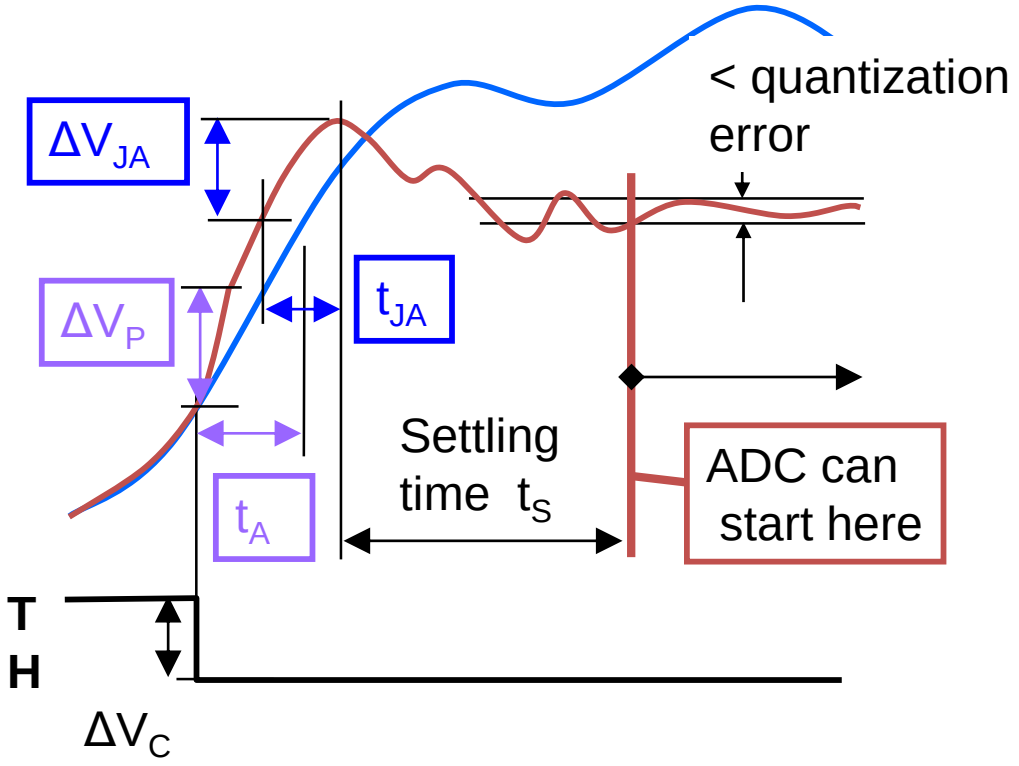
Tracking: step response

- Step Vi input
- Output Vo with II order transient: it means that the output cannot follow very fast variations of the input

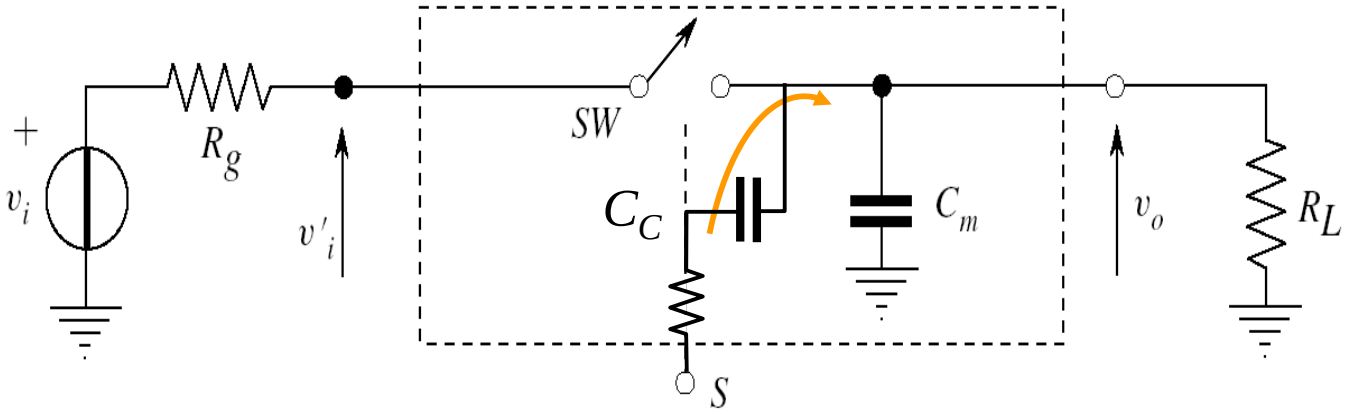


Sampling

- Time error
  - Delay in SW opening → aperture delay
  - Delay variations → aperture jitter
  - Errors due to aperture jitter
    $\Delta V_{\mathrm{JA}} = t_{\mathrm{JA}} \cdot SR_{\max}$
  - T→H in t_S: settling time
- Amplitude error
  - Pedestal ΔV_{J}
    charge injection through SW
- Transient
  - T→H settling time

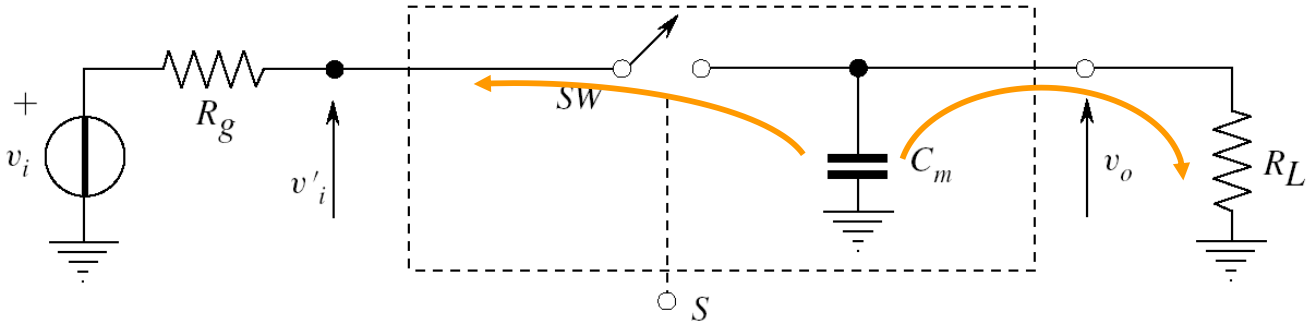


Sampling: pedestal error



- Partition of the Gate command signal between Cc and Cm
  - Pedestal error

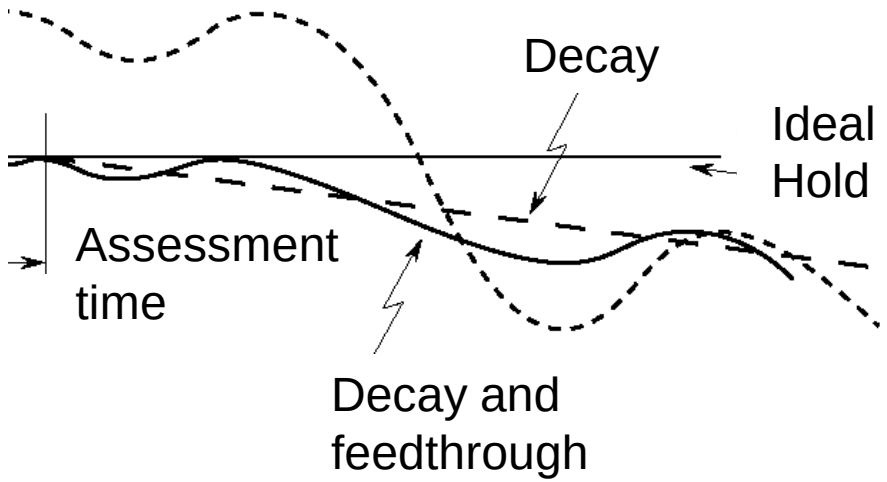
Hold state: decay error



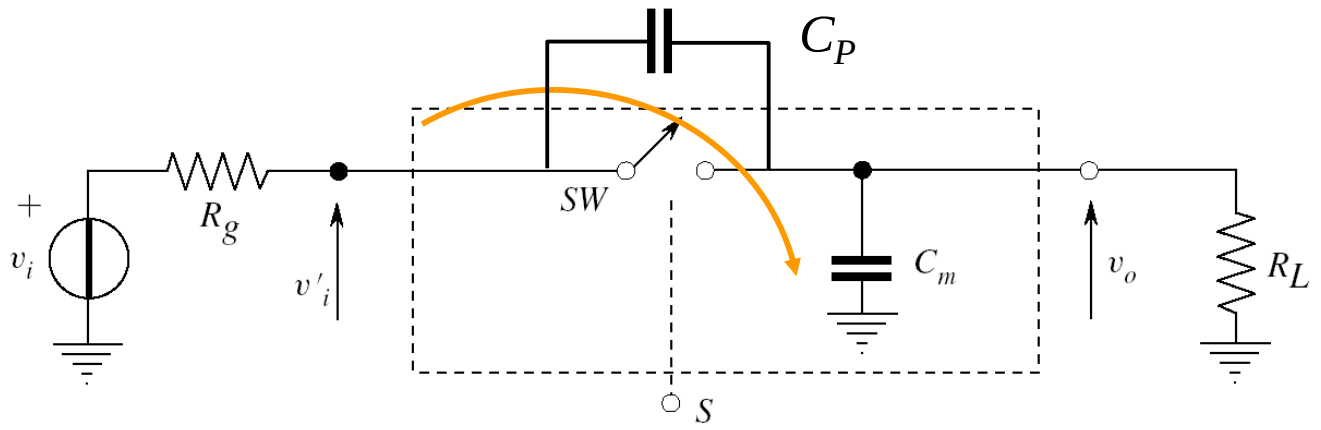
- Switch OFF: Vo(t) = V'i(ts)
  - Output = voltage previously stored on the capacitor
- The capacitor discharges through R_L and I_{OFF} (leakage)
  - Decay error

Basic circuit: hold error

- The charge stored on the capacitor changes
  - Decay error
- Poor isolation of input signal
  - Feedthrough error
- Dielectric polarization
  - Slow reduction of capacitor voltage (capacitance increases)



Basic circuit: feedthrough error



- Switch OFF: Vo(t) = V'i(ts)
  - Output = voltage previously stored on the capacitor
- Input signal partitioned between Cp and Cm
  - Feedthrough error

Total error

- Each unit introduces errors and noise
  - Amplifier: Gain, offset, nonlinearity, band limits
  - Filter: Out of band signals
  - Sample/Hold: Sampling jitter
  - A/D converter: Quantization

- Actual accuracy depends on *all* these elements
  - Not just the bit number N of the A/D

Total SNR

- Ratio of signal-to-total noise, from all sources: SNR_t
  - Quantization noise (given by bit number)
  - Aliasing noise (given by sampling frequency and filter)
  - Jitter error (S&H aperture jitter and signal slew rate)
  - Conditioning chain noise (component noise, EMC noise, …)
- Independent noise components
- Total noise power
  - Sum the powers of components
  - Compute SNR_t

$$SNR_i = 10 \lg\left(\frac{P_S}{P_{N_i}}\right) = 20 \lg\left(\frac{V_S}{V_{N_i}}\right)$$

$$SNR_{tot} = -10 \lg\left(\sum_i 10^{-\frac{SNR_i}{10}}\right)$$

$$SNR_{tot} = -10 \lg\left(\frac{\sum_i P_{N_i}}{P_S}\right)$$

$$SNR_{tot} = -20 \lg\left(\frac{\sqrt{\sum_i V_{N_i}^2}}{V_S}\right)$$

Effective Number of Bits: ENOB

- SNR_t can also be expressed as the equivalent number of bits for a full-scale sine wave signal
- Calculated including all noise/error sources (quantization, aliasing, S&H aperture jitter, …)

- $ENOB = \frac{SNR_t - 1.76}{6} = \frac{SNR_t}{6} - 0.3$

- Represents the number of the actually useful bits of the A/D conversion system

Review Questions

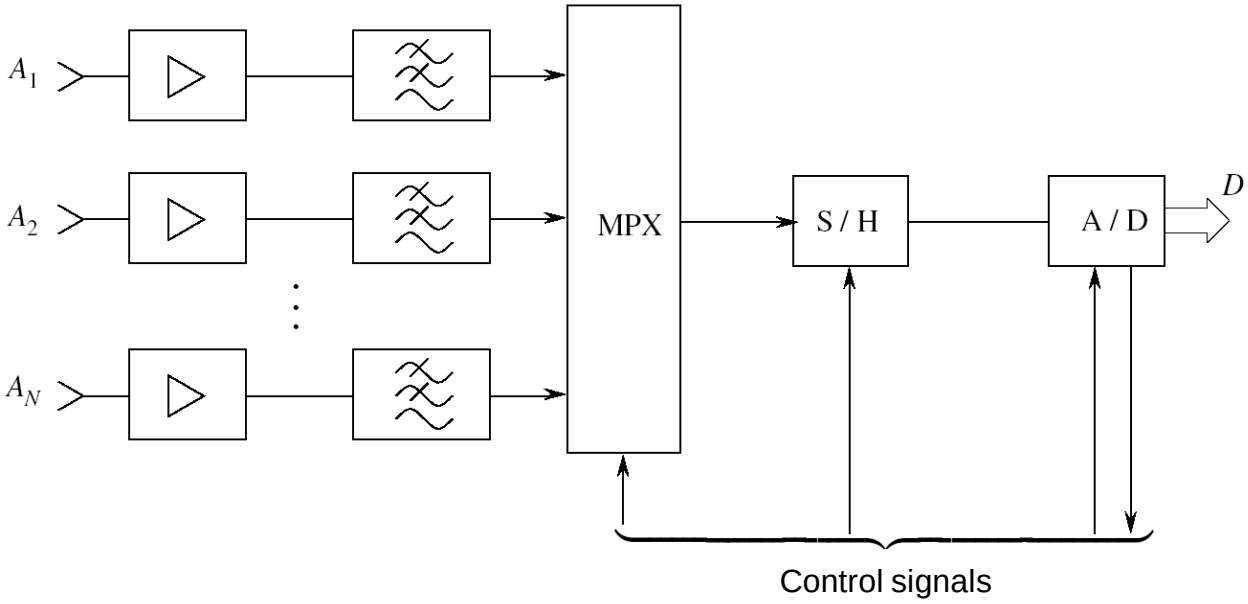
- What is needed to adapt a 10 V_{pp} bipolar signal to an A/D converter with input dynamic 0 V – 5 V?
- Why are preferred the differential signals?
- What errors are introduced by multiplexers?
- What multiplexer parameters limit the signal bandwidth?
- List the main errors in an A/D conversion system.
- What are the errors introduced by the sample-and-hold?
- What S&H parameters define the signal bandwidth?
- What are the advantages and disadvantages of increasing the hold (memory) capacitance of a S&H?

Exercise 1

- Draw the block schematic of a 4-channel A/D conversion system with
  - Unipolar input signals from 1 V to 2 V, freq. band 0 Hz – 15 kHz
  - A/D converter with input scale 0 V – 5 V and T_C = 1 µs
  - Sample-and-hold with acquisition time T_a = 700 ns
- For the conditioning amplifier
  - Provide the specifications
  - Draw the schematic of the amplifier
  - Indicate the parameters that define the values of its resistors

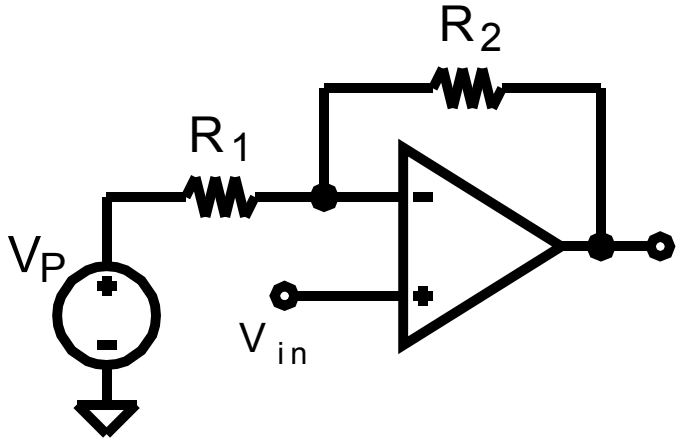
Exercise 1

- $T_c + T_a = 1\ \mu s + 0.7\ \mu s = 1.7\ \mu s,\ F_s < \frac{1}{1.7\ \mu s} = 588\ kHz$
- For each channel: $F_s^{ch} < \frac{588\ kHz}{4\ ch} = 147\ \frac{kHz}{channel}$
- Nyquist sampling: $F_s > 2\ F_{max} = 2 \cdot 15\ kHz = 30\ kHz \Rightarrow OK$
- Maximum oversampling factor: $K = \frac{147\ kHz}{30\ kHz} = 4.9$



Exercise 1

- Conditioning amplifier gain
  - $G = \frac{\Delta V_{\mathrm{o}}}{\Delta V_{\mathrm{i}}} = \frac{5\ \mathrm{V}}{1\ \mathrm{V}} = 5$
- Output offset
  - $V_{\mathrm{os_o}} = V_{\mathrm{average}}^{\mathrm{ADC}} - G \cdot V_{\mathrm{average}}^{\mathrm{in}} = 2.5\ \mathrm{V} - 5 \cdot 1.5\ \mathrm{V} = -5\ \mathrm{V}$
- Input offset
  - $V_{\mathrm{os_i}} = \frac{V_{\mathrm{os_O}}}{G} = -\frac{5\ \mathrm{V}}{5} = -1\ \mathrm{V}$
- Amplifier biasing
  - $G = 1 + \frac{R2}{R1} = 5 \Rightarrow \frac{\mathrm{R2}}{\mathrm{R1}} = 4$
  - $-V_{\mathrm{p}} \frac{R2}{R1} = -5\ \mathrm{V} \Rightarrow V_{\mathrm{p}} = \frac{5\ \mathrm{V}}{4} = 1.25\ \mathrm{V}$



Exercise 2

- For the system in exercise 1
  - Determine the possible sampling frequency range
  - Indicate the anti-aliasing filter characteristics for $SNR_a \geq 60$ dB
  - Indicate the maximum aperture jitter T_{JAmax} for an error due only to aperture jitter $E_{JA} < 0.1$ %
  - Indicate the minimum number of bits to obtain a quantization error E_q at most equal to aliasing error

Exercise 2

- For the system in exercise 1
  - Determine the possible sampling frequency range

- The number of poles depends on the oversampling ratio
  - $F_s \geq 2\,F_{max} = 30\ \text{kHz}$ and $F_S \leq F_s^{ch} = 147\ \text{kHz}$
  - For $F_s = 2\,F_{max} = 30\ \text{kHz}$, $N_{decades} = \log_{10}\left(\frac{30\ \text{kHz} - 15\ \text{kHz}}{15\ \text{kHz}}\right) = 0$
    - We would need an infinity of poles

Exercise 2

- For the system in exercise 1
  - Indicate the anti-aliasing filter characteristics for $SNR_a \geq 60$ dB
- With $F_s = 147\ \text{kHz}$ we have
  - $F_s - F_{max} = 147\ \text{kHz} - 15\ \text{kHz} = 132\ \text{kHz}$
  - $N_{dec} = \log_{10} \frac{132\ \text{kHz}}{15\ \text{kHz}} = 0.94$ decades
- Attenuation of a filter with one pole
  - $A_p = 20\ \text{dB/dec} \cdot 0.94 = 18.8\ \text{dB}$
- For $SNR_a = 60$ dB we need
  - $60\ \text{dB}/18.8\ \text{dB} = 3.2\ \text{poles} \Rightarrow \mathbf{4\ poles}$
- With another oversampling ratio, e.g., 2.5
  - $F_s = 2.5 \cdot 30\ \text{kHz} = 75\ \text{kHz}$
  - $F_s - F_{max} = 75\ \text{kHz} - 15\ \text{kHz} = 60\ \text{kHz}\ \ldots$

Exercise 2

- For the system in exercise 1
  - Indicate the maximum aperture jitter T_{JAmax} for an error due only to aperture jitter $E_{JA} < 0.1\ \%$
- $\frac{\mathrm{d}V}{\mathrm{d}t} = SR\ \text{signal} = \frac{\omega \cdot V_{\mathrm{pp}}}{2} = \frac{6.28 \cdot 15\ \mathrm{kHz} \cdot 5\ \mathrm{V}}{2} = 0.24\ \mathrm{V/\mu s}$
- $E_{\mathrm{ja}} = 0.1\ \% \cdot S = 0.001 \cdot 5\ \mathrm{V} = 5\ \mathrm{mV}$
- $\frac{E_{\mathrm{ja}}}{T_{\mathrm{ja_{max}}}} = 0.24\ \mathrm{V/\mu s} \Rightarrow T_{\mathrm{ja_{max}}} = \frac{5\ \mathrm{mV}}{0.24\ \mathrm{V/\mu s}} = 21\ \mathrm{ns}$

Exercise 2

- For the system in exercise 1
  - Indicate the minimum number of bits to obtain a quantization error E_q at most equal to aliasing error

- $SNR_q = SNR_a = 60\ \text{dB} \Rightarrow 6\ N + 1{,}76 = 60\ \text{dB}$
- $N = \frac{60 - 1.76}{6} = 9.7\ \text{bit} \Rightarrow N = 10\ \text{bit}$

Exercise 3

- For the system in exercise 2 evaluate the total signal-to-noise ratio (SNR_{tot}) and effective number of bits ($ENOB$).
  - Aliasing signal-to-noise ratio: SNR_a = 60 dB
  - Error due only to aperture jitter: $E_{ja} < 0.1\ \%$
  - Quantization error E_q at most equal to aliasing error

Exercise 3

- $SNR_{\mathrm{j}} = 20\log_{10}\frac{S}{E_{\mathrm{j}}} = 20\log_{10}\frac{S}{0{,}001\,S} = 60\ \mathrm{dB}$
- $A_{\mathrm{j}} = \frac{E_{\mathrm{j}}}{S} = 10^{-\frac{60\ \mathrm{dB}}{20}} = 0.001$
- $A_{\mathrm{a}} = \frac{E_{\mathrm{a}}}{S} = 0.001$
- $A_{\mathrm{q}} = 10^{-\frac{60\ \mathrm{dB}}{20}} = \frac{E_{\mathrm{q}}}{S} = 0.001$
- $SNR_{\mathrm{tot}} = -20\log_{10}\left(\sqrt{\sum\left(A_j^2 + A_a^2 + A_q^2\right)}\right) = -20\log_{10}\left(0.001 \cdot \sqrt{3}\right) = 55.2\ \mathrm{dB}$
- $ENOB = \frac{55.2-1.76}{6} = 8.9\ \mathrm{bit} \Rightarrow ENOB = 9\ \mathrm{bit}$