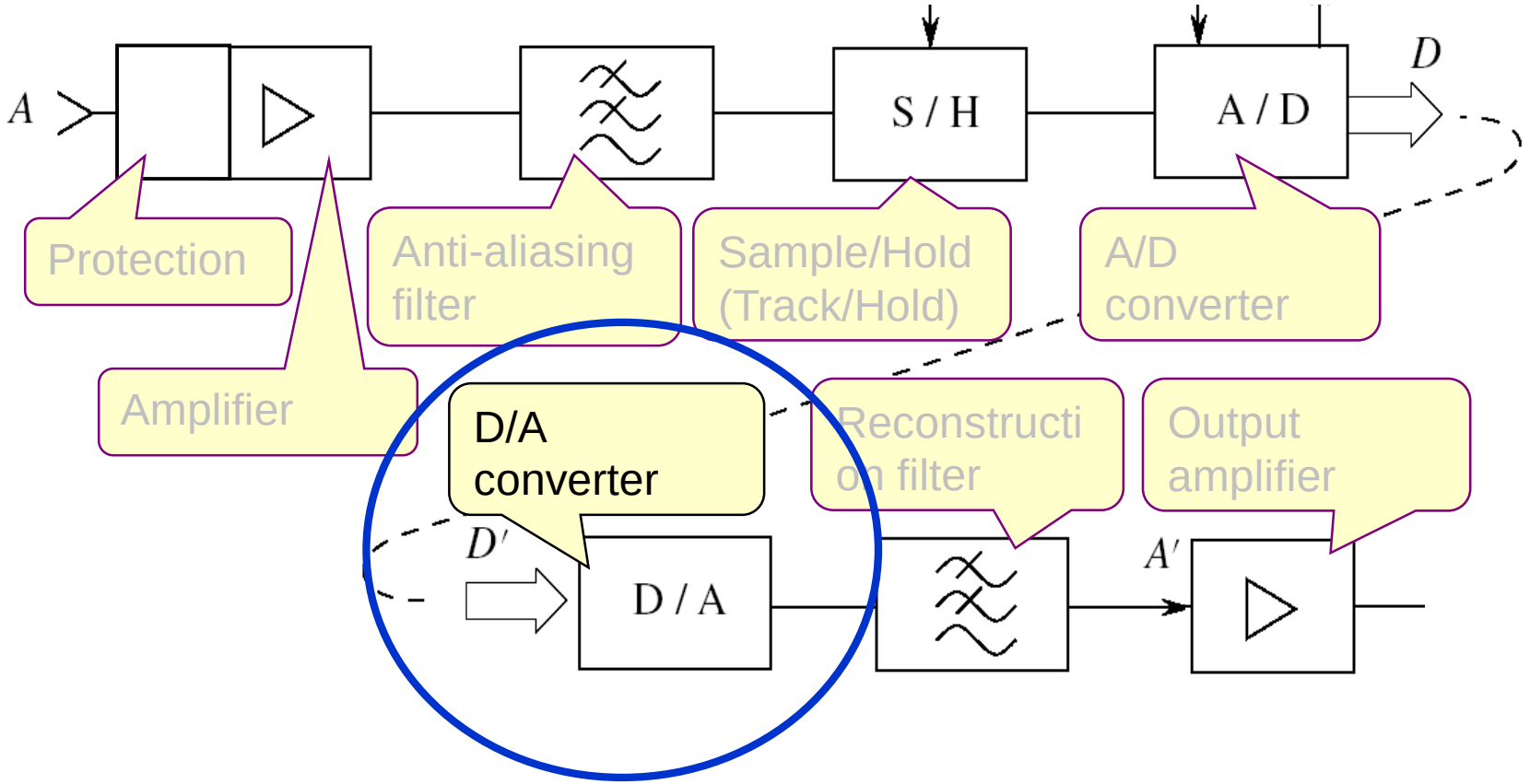
Applied Electronics

D/A Converters

D/A Converters

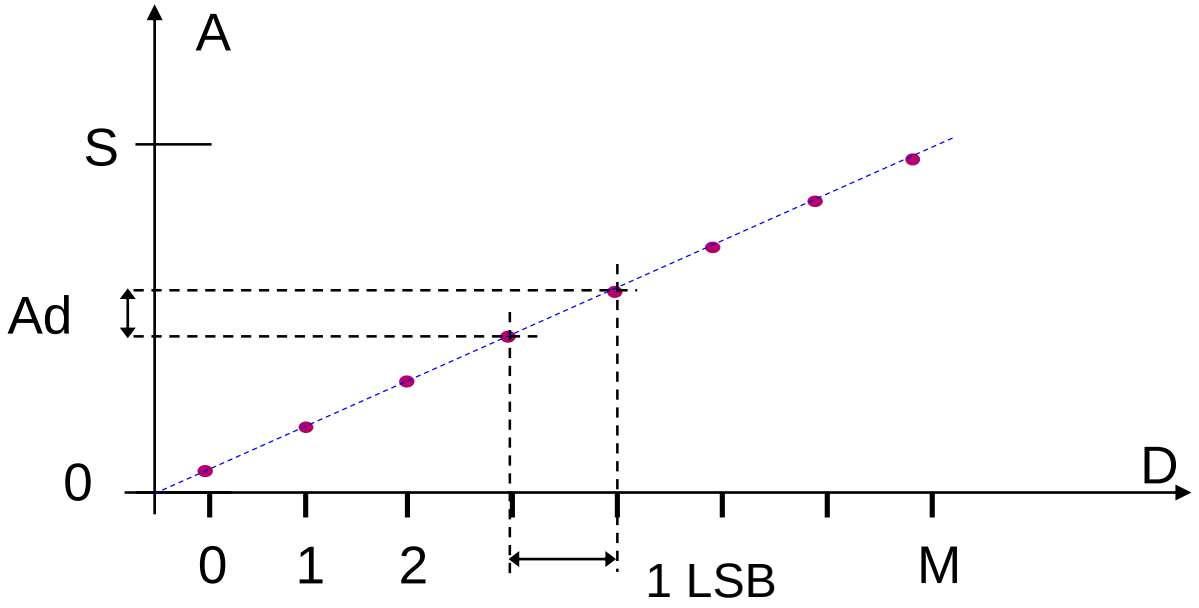
- Parameters of D/A converters
  - Linear: gain and offset error
  - Integral and differential nonlinearity
  - Dynamic parameters
- DAC structures
  - Uniform and weighted architectures
  - Ladder networks
  - Example of circuits
- References
  - F. Maloberti: Understanding Microelectronics…, Ch. 7.4

D/A Converters



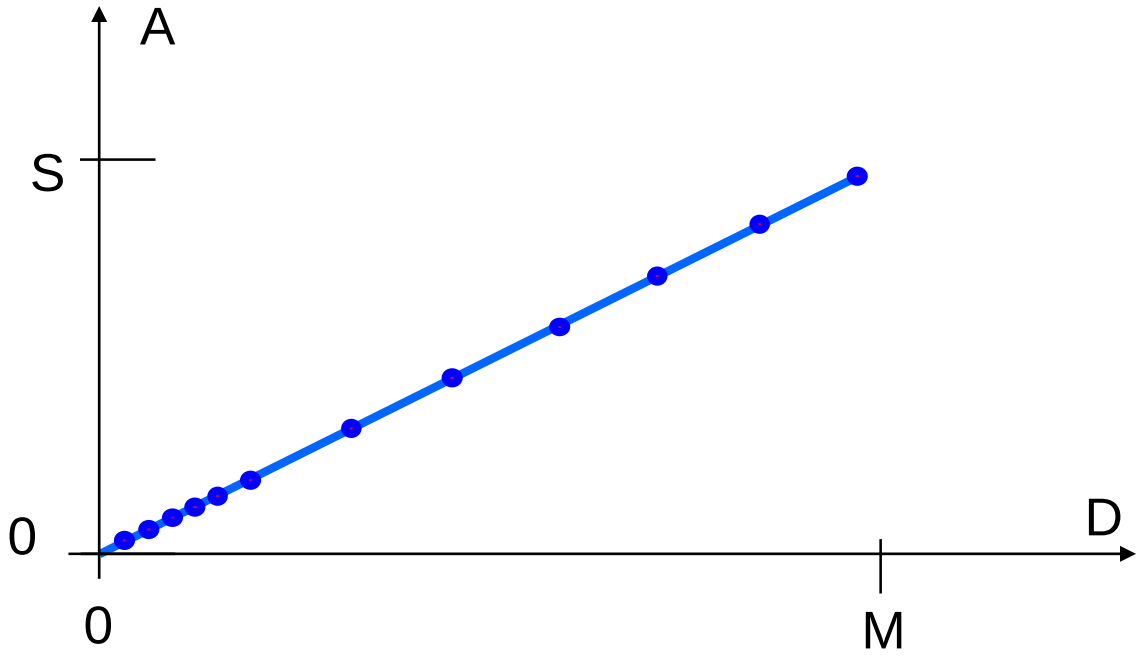
D/A Transfer Function

- Input variable (D) is discrete
  - The $A(D)$ plot is a sequence of dots
  - For a constant A_d, the dots are lined up



Conversion Characteristic

- $M = 2^N$
  - Many dots for high N
  - Dot sequence becomes almost a continuous line



Errors in D/A Converters

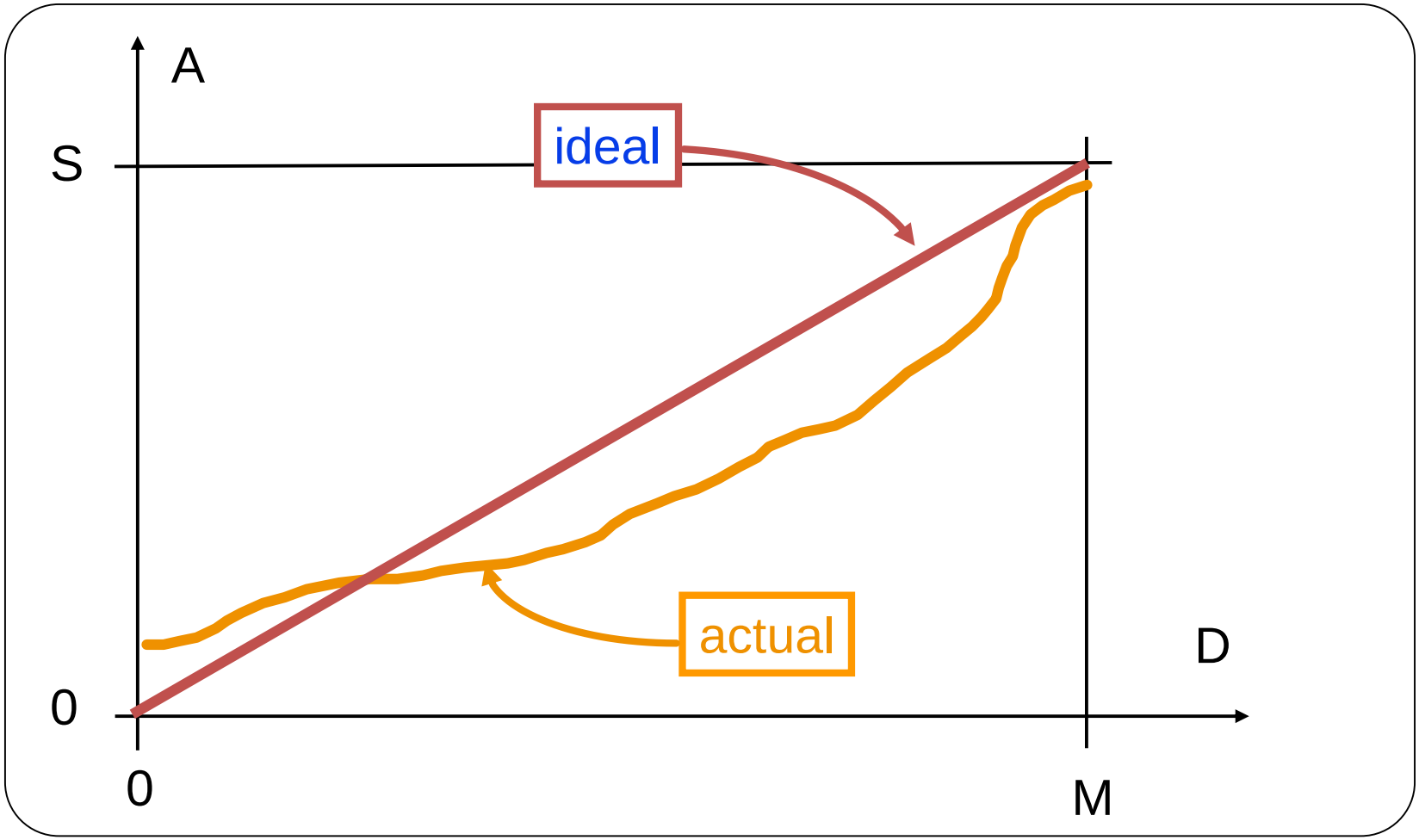
- Static errors
  - Constant input
  - Steady state behavior
  - Can be seen in the $A(D)$ plot
- Dynamic errors
  - Variable input signal
  - Transient behavior
  - Can be seen in the $A(t)$ plot

Static Errors: Two Step Analysis

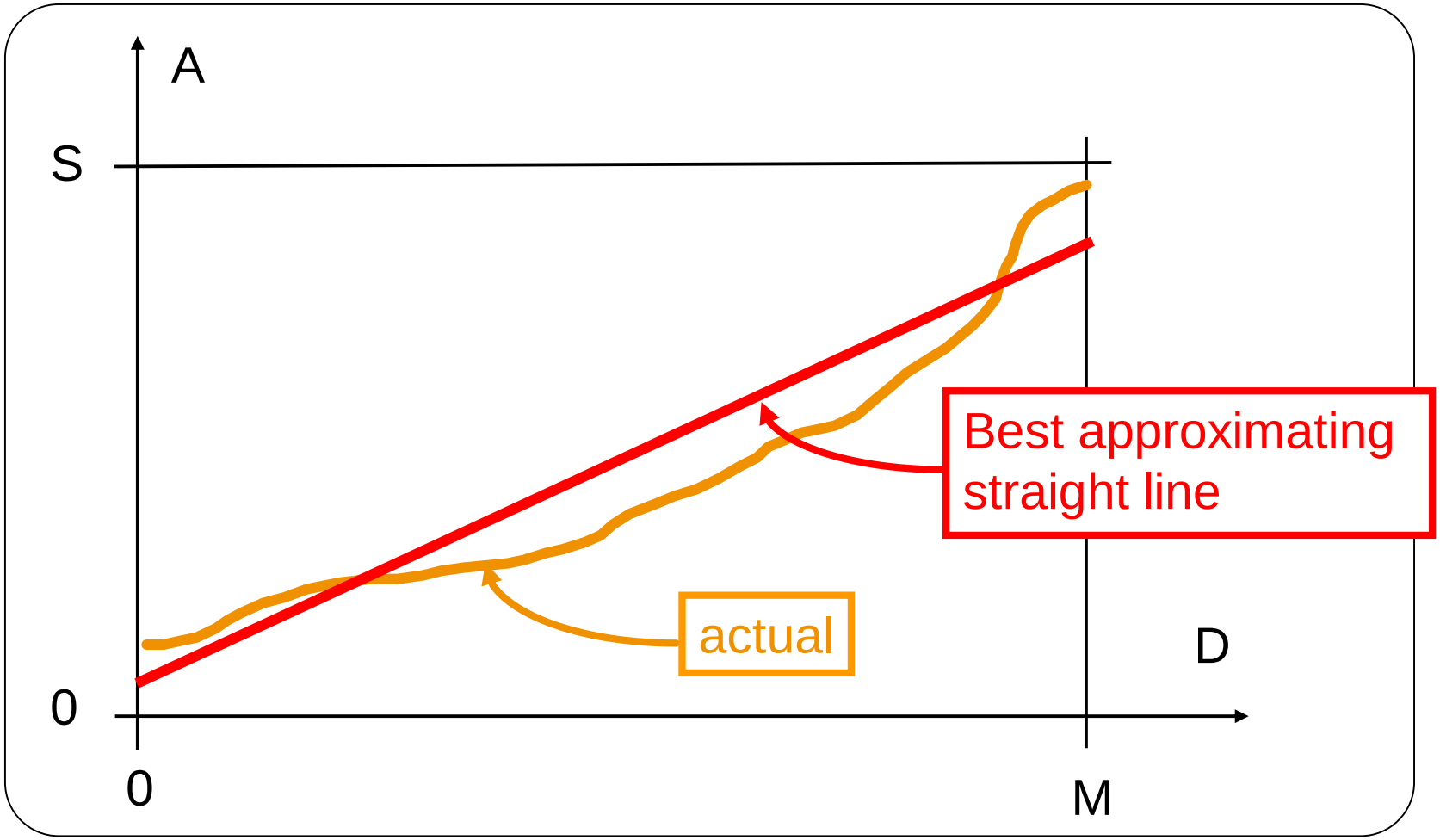
- Which parameters define “how good” is a DAC?
- The actual transfer function is not a straight line
- Plot the best approximating straight line
- Compare actual/ideal transfer functions in two steps

- 1: From real characteristic to best approximating line
  - Nonlinearity errors
- 2: From best approximating line → ideal transfer function
  - Linear errors: offset and gain

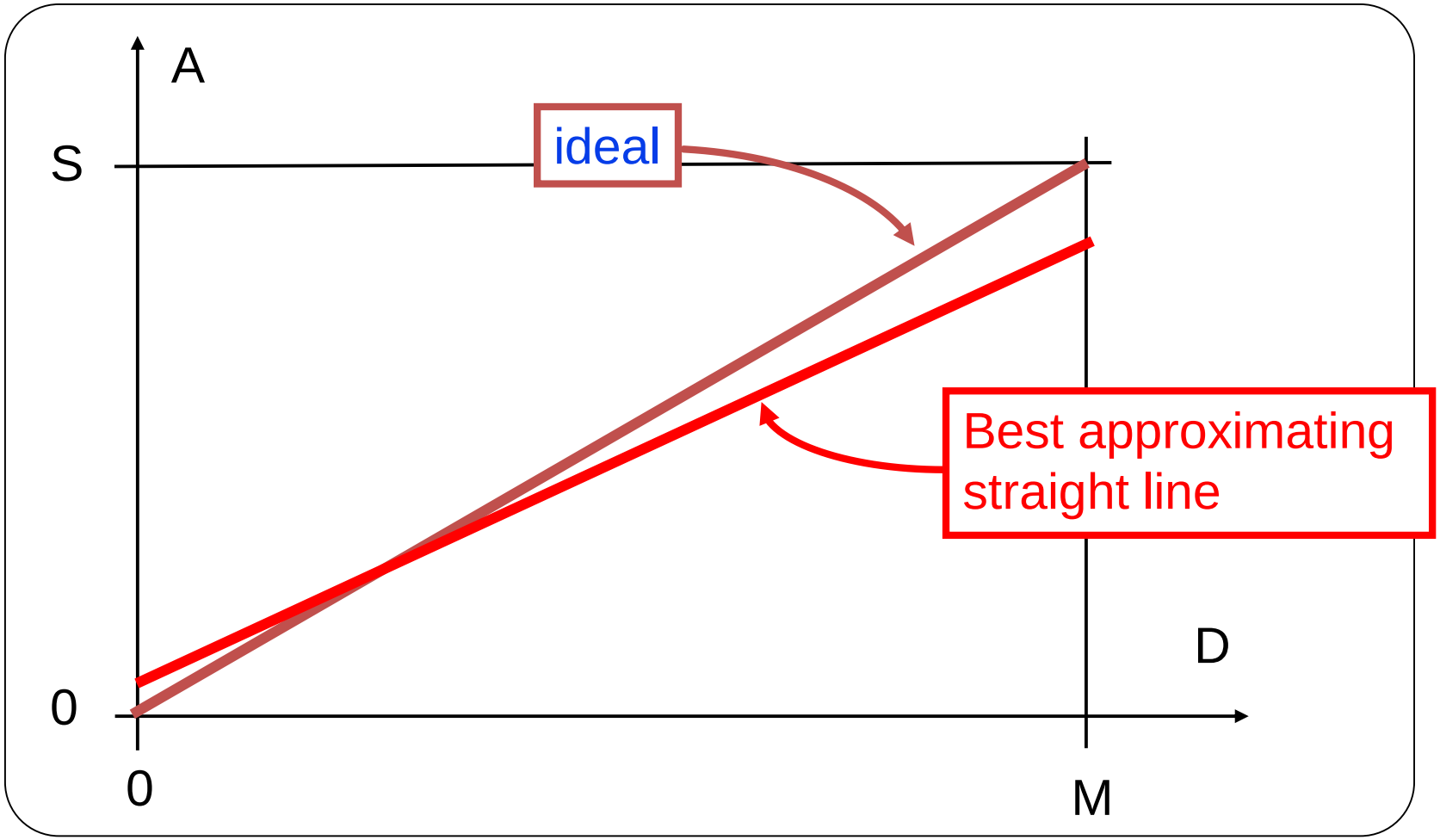
Ideal and Actual D/A Characteristic



Approximation With Straight Line



Ideal vs Best Linear Approximation

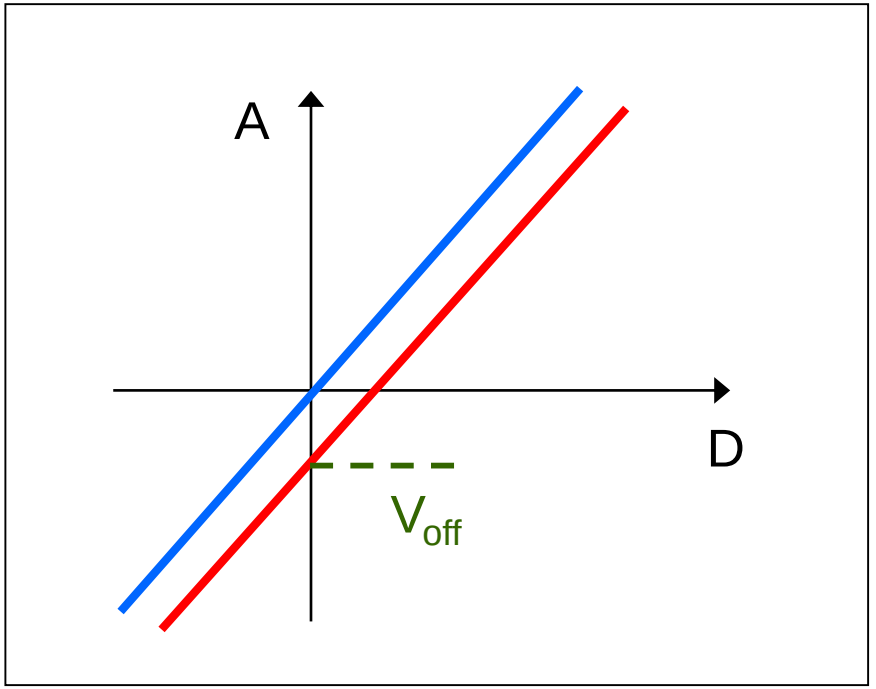


Linear Errors: Offset and Gain

- Best approximating line may miss $(0,0)$ and (M,S)
- Offset $\mathcal{E}_o$
  - Best approximating line intercept of the A axis
  - Can be compensated by adding a constant
- Gain error $\mathcal{E}_g$
  - Difference between slopes of ideal and best approximating line
  - Can be compensated by gain correction
- This methodology applies for any device with a linear transfer function

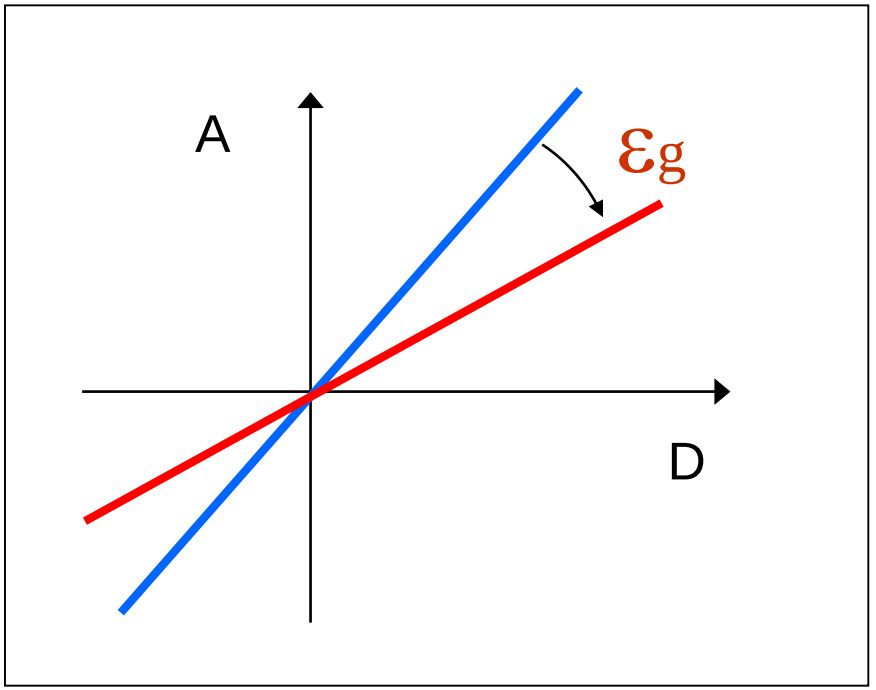
Offset Error

- Ideal transfer function
  - $D = 0 \Rightarrow A = 0$
- Actual best approximating transfer function
  - Not through $(0,0)$
  - $D = 0 \Rightarrow A = V_{\text{off}}$
- Offset error
  - $\mathcal{E}_{\text{o}} = V_{\text{off}}$



Gain Error

- Ideal transfer function
  - $A = KD$
- Actual best approximating transfer function
  - Different slope
  - $A = K'D$
  - $K' = K + \Delta K$
- Gain error
  - $\mathcal{E}_g = \frac{\Delta K}{K}$



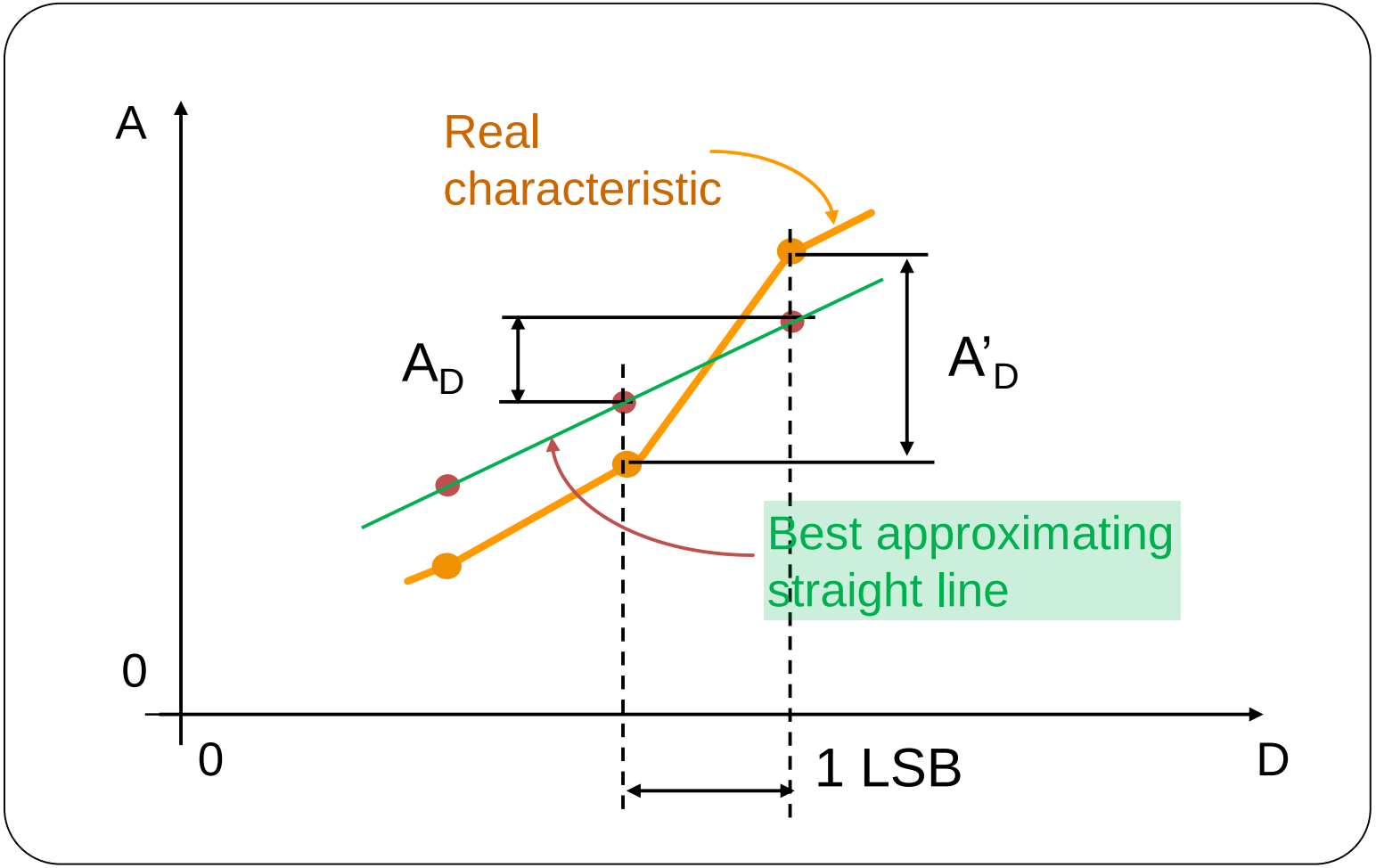
Nonlinearity Errors

- Compare the real characteristic and the best approximating line
- Real characteristic has nonlinearity errors that change from point to point
  - Thus, they *cannot be compensated*
- Nonlinearity defined by two parameters
  - *Differential* nonlinearity (local behavior)
  - *Integral* nonlinearity (overall behavior)
- Maximum difference between the real characteristic and the best approximation line is a nonlinearity band
  - $\mathcal{E}_{\mathrm{inl}}$ is called integral nonlinearity error

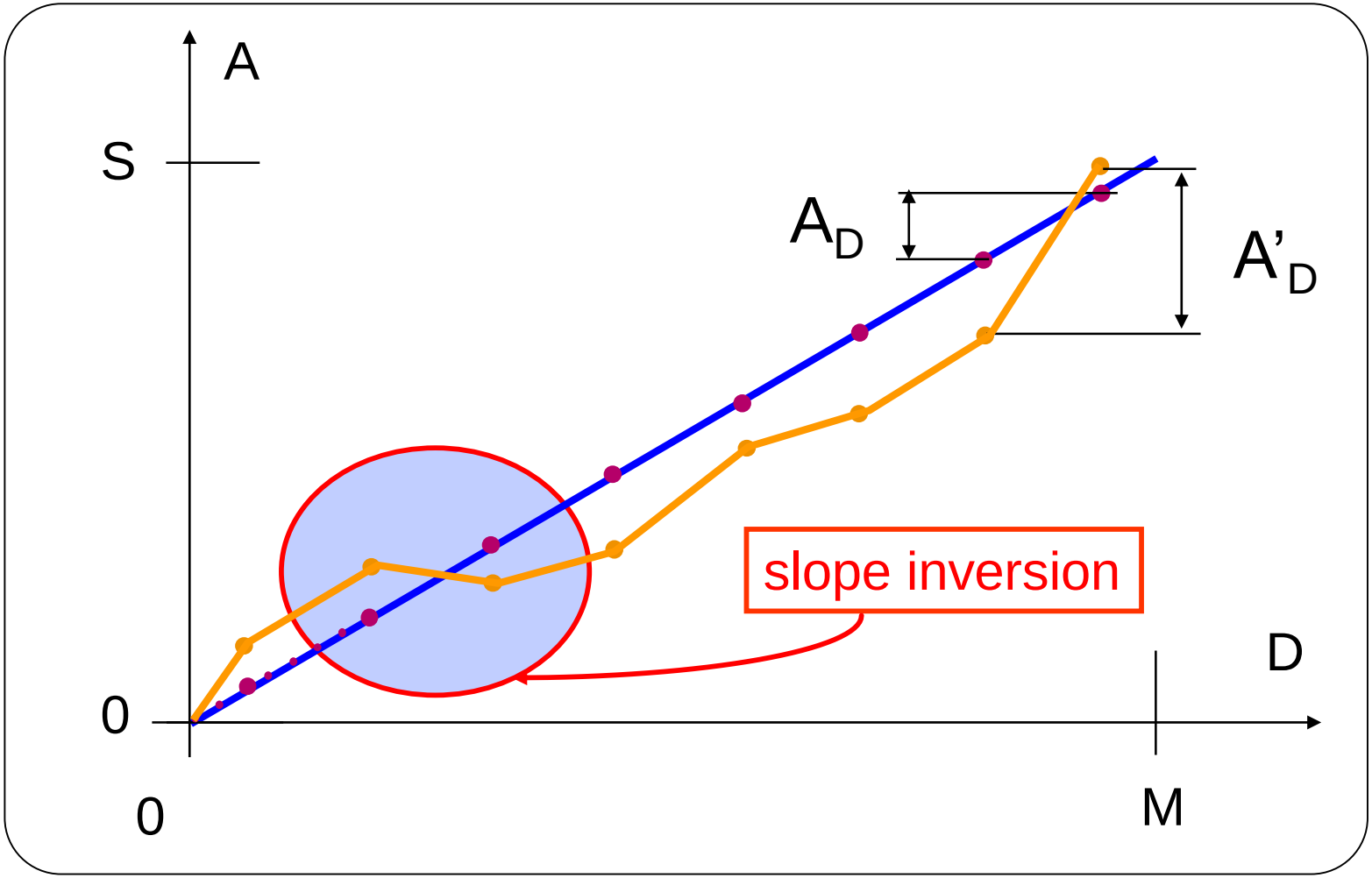
Differential Nonlinearity Error

- Ideal transfer function
  - Dots spaced by A_{D} (A axis) mapped on 1 LSB (D axis)
- Actual transfer function
  - Dots spaced by $A'_{\mathrm{D}} \neq A_{\mathrm{D}}$
- The difference $A_{\mathrm{D}} - A'_{\mathrm{D}} = \mathcal{E}_{\mathrm{dnl}}$
  - Differential nonlinearity
- If $\mathcal{E}_{\mathrm{dnl}} > 1\ LSB = A_{\mathrm{D}}$ (slope inversion)
  - $A_{\mathrm{D}} - A'_{\mathrm{D}} > A_{\mathrm{D}} \rightarrow A'_{\mathrm{D}} < 0$
  - *Non-monotonicity* error

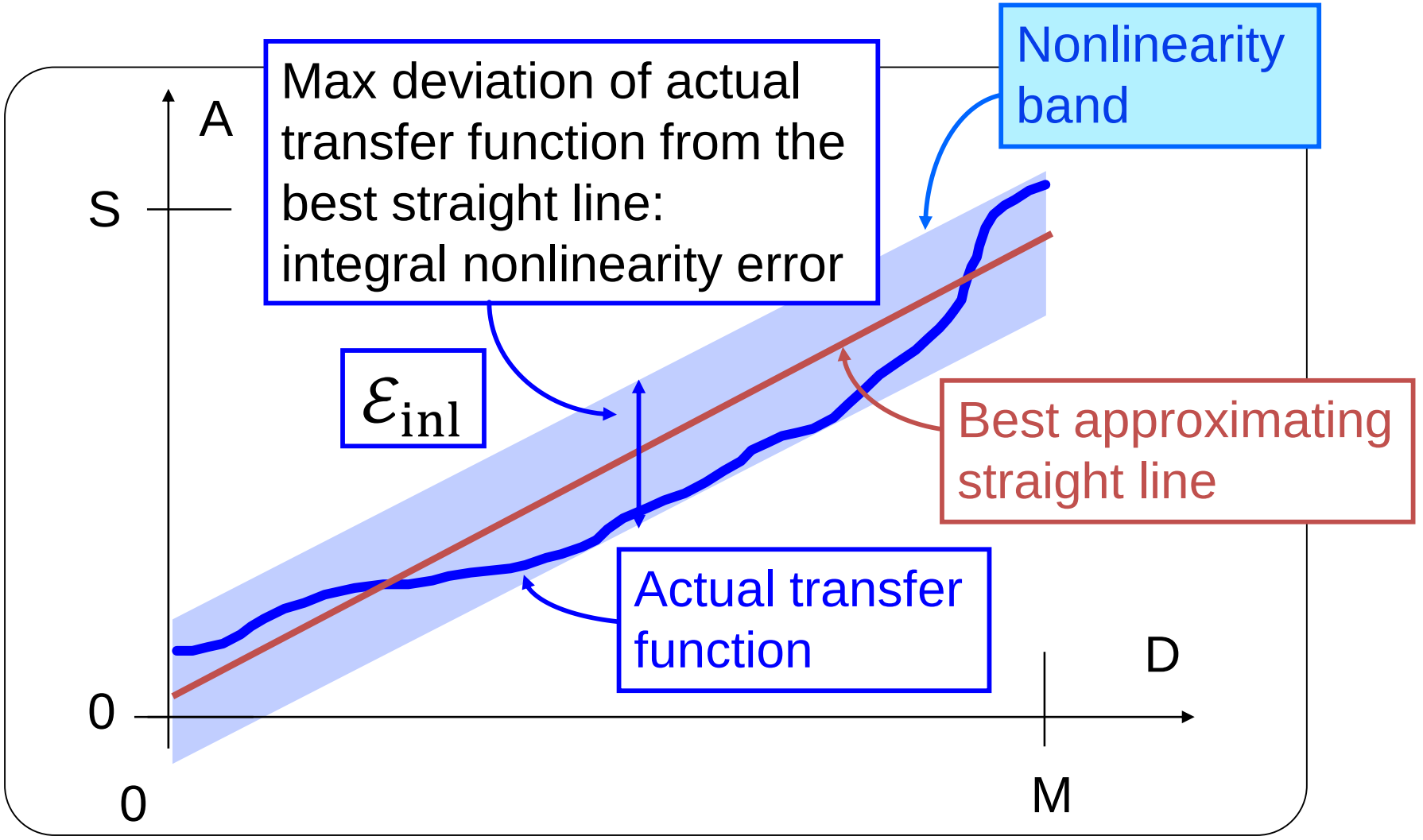
Nonlinearity Errors: Differential



Non-Monotonicity Error



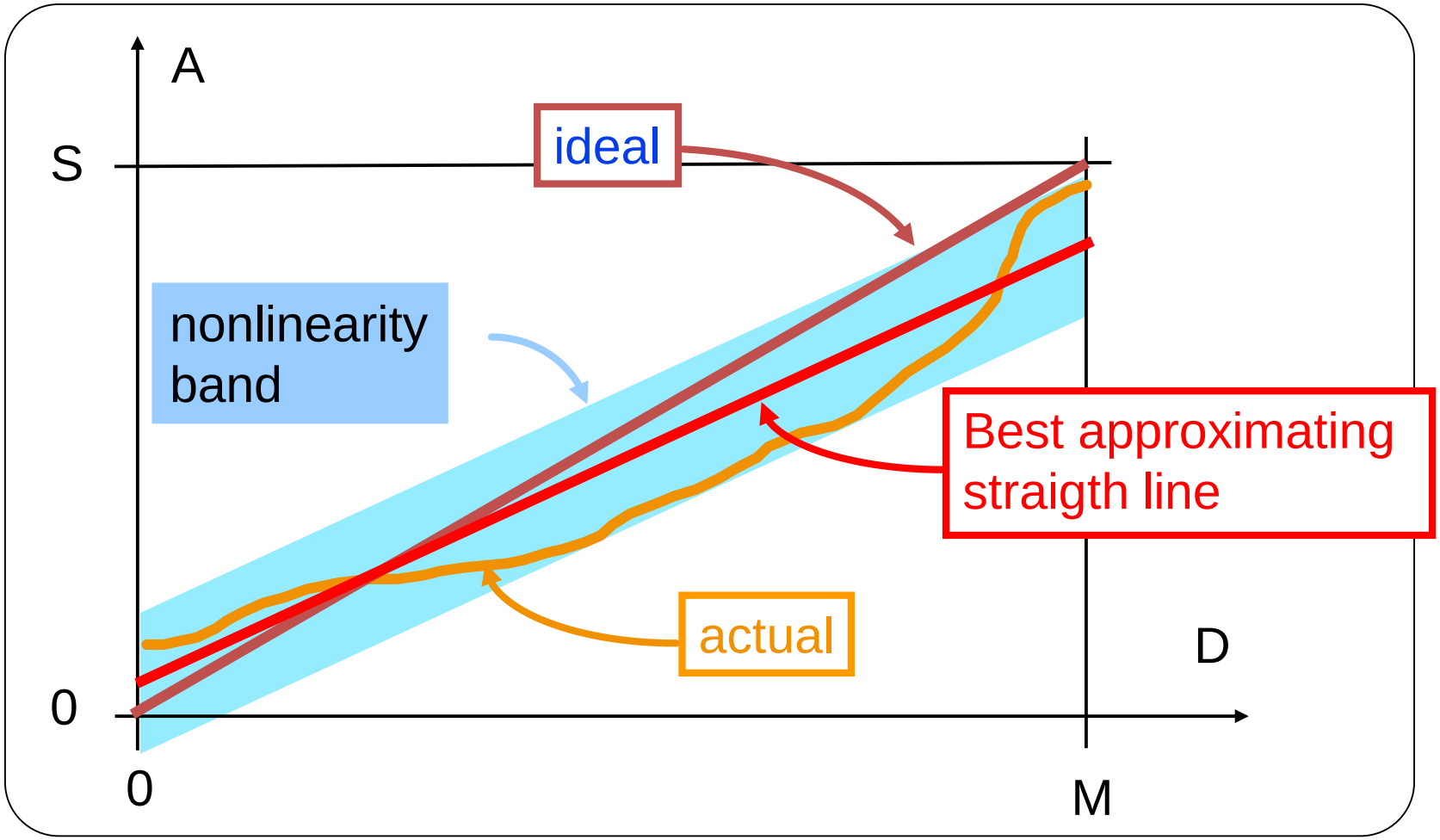
Nonlinearity Errors: Integral



Differential vs. Integral Nonlinearity

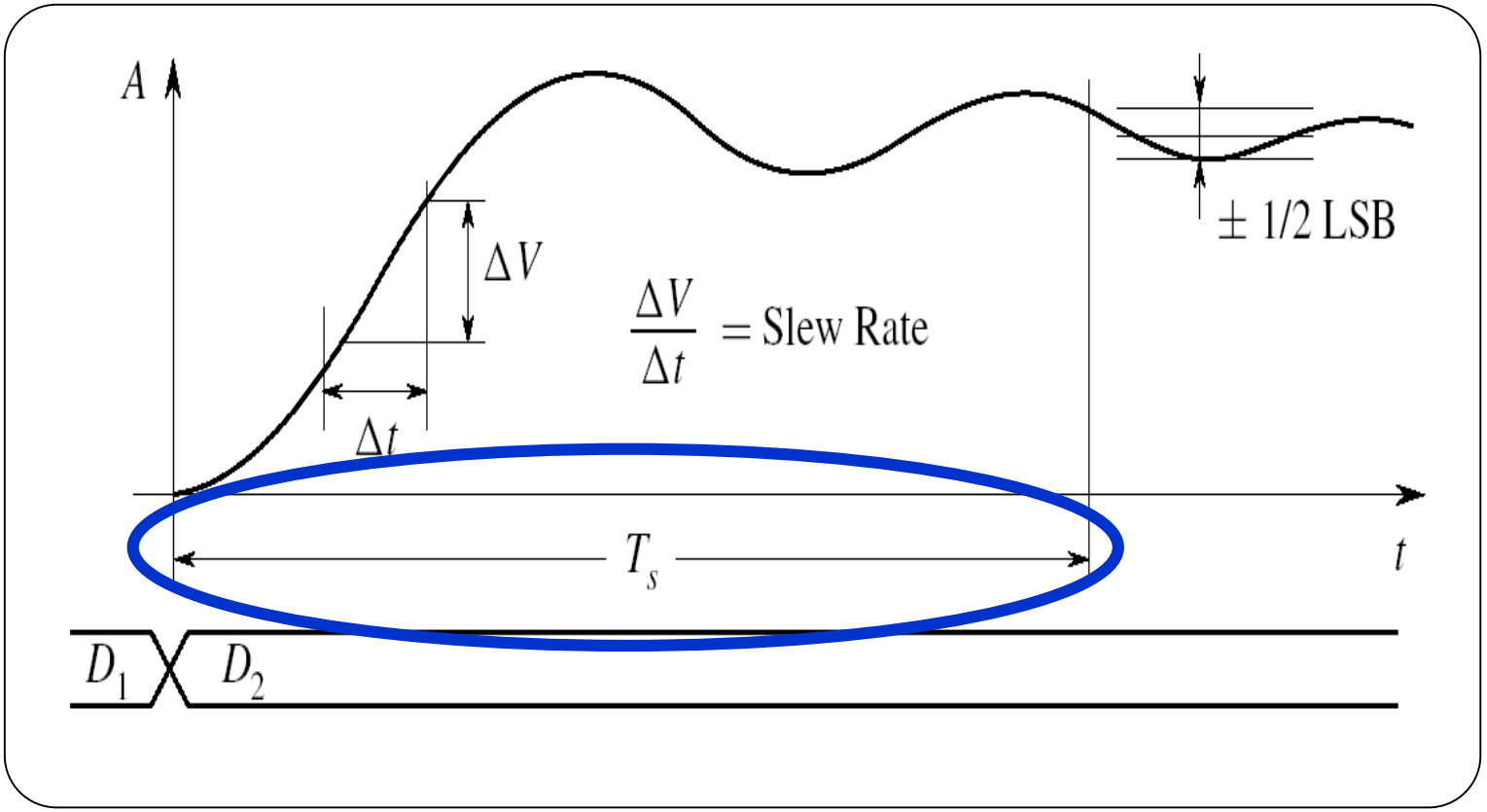
- Draw the characteristic for a 3-bit DAC with
  - $\mathcal{E}_{\mathrm{dnl}} = +1/4\,LSB$ from 000 to 011 ($MSB = 0$)
  - $\mathcal{E}_{\mathrm{dnl}} = -1/4\,LSB$ from 100 to 111 ($MSB = 1$)
- Draw the characteristic for a 3-bit DAC with
  - $\mathcal{E}_{\mathrm{dnl}} = +1/4\,LSB$ when $LSB = 0$
  - $\mathcal{E}_{\mathrm{dnl}} = -1/4\,LSB$ when $LSB = 1$
- Compare the two cases
  - Evaluate integral nonlinearity error $\mathcal{E}_{\mathrm{inl}}$
  - Evaluate differential nonlinearity error $\mathcal{E}_{\mathrm{dnl}}$
  - Evaluate offset and gain errors

Overall View



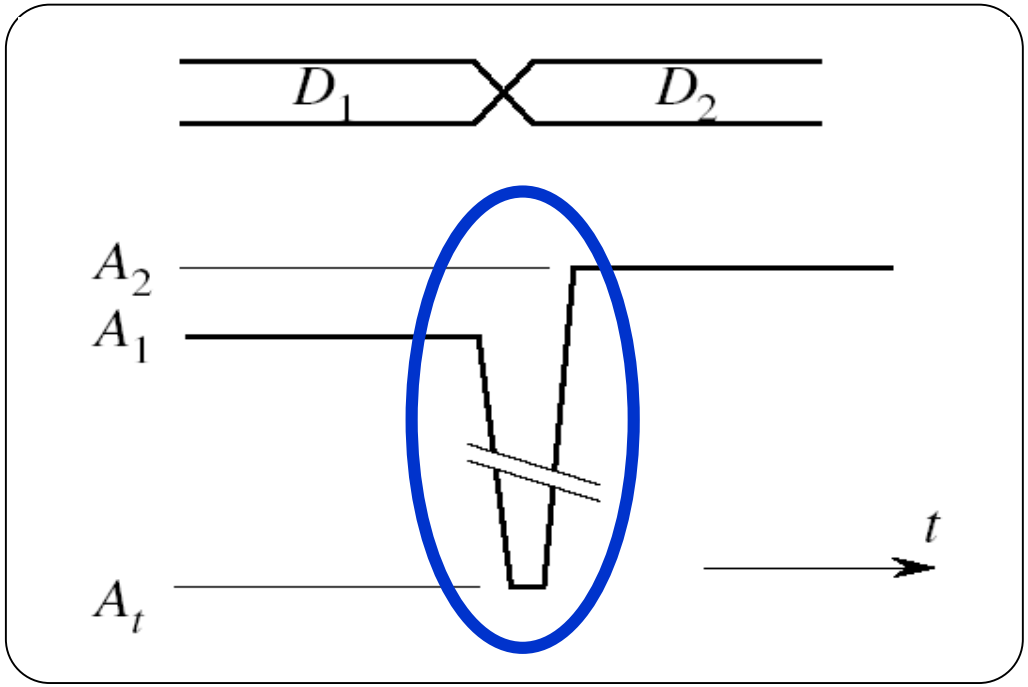
Settling Time

- The D/A output takes a settling time T_S to reach the new value (within a given error)



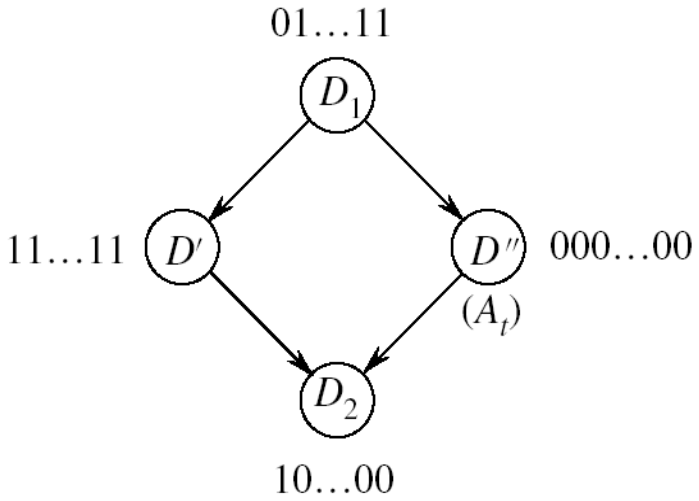
Glitch

- During transients, the output can temporarily reach a widely wrong value (typically $0\,\mathrm{V}$ or full-scale S)
- The spike is called glitch



Where Do Glitches Come From?

- Glitches come from different switching delays of bits
  - These delays cause wrong transient states (e.g., 1111 and 0000 while changing state from 0111 to 1000
  - These states drive the output towards 0 V or full-scale S



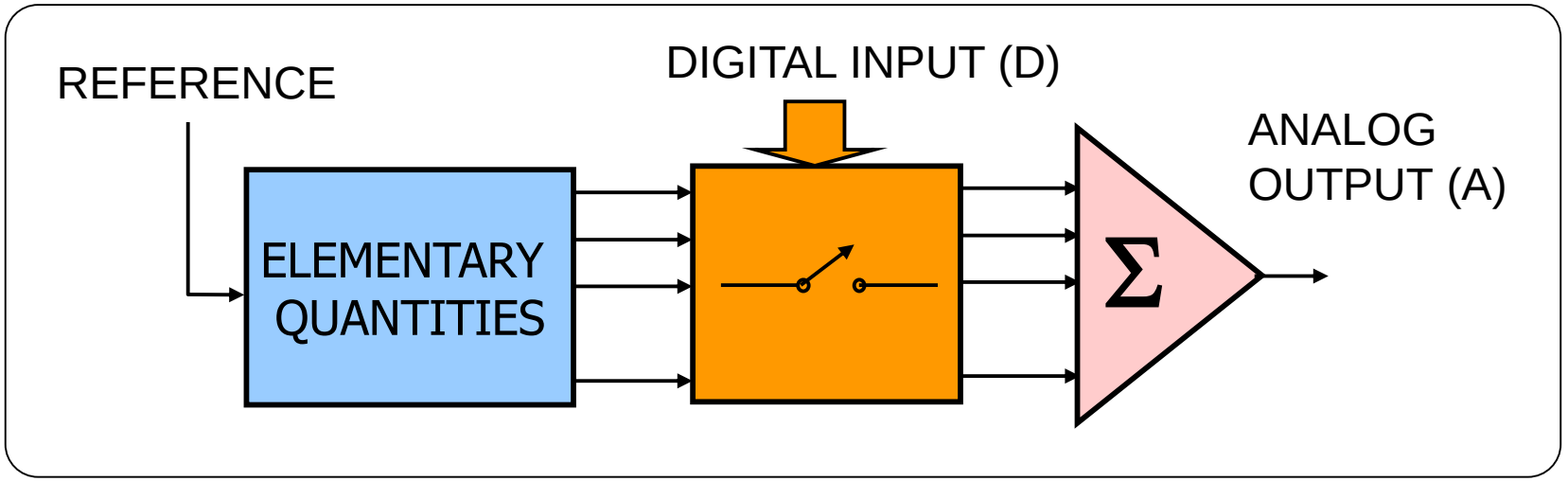
- Glitches occur when several bits flip, e.g., 0111→1000
  - The real change is just 1 LSB
  - But temporary state during the transient can be 0000 or 1111
- Avoid glitches by using Gray encoding
  - Changes only one bit between adjacent states

DAC Error Summary

- Static parameters
  - Bit number N — Full scale S
- Linear errors
  - Gain $\mathcal{E}_{\mathrm{G}}$ — Offset $\mathcal{E}_{\mathrm{O}}$
- Nonlinearity errors
  - Integral nonlinearity $\mathcal{E}_{\mathrm{inl}}$ — Differential nonlinearity $\mathcal{E}_{\mathrm{dnl}}$
- Dynamic parameters
  - Settling time t_S — Glitch
- Measured as
  - % of full-scale S, absolute (mV, …), LSB fraction (1, ½, …)

D/A Conversion Basic Circuits

- Sum of elementary quantities controlled by D



  - Uniform elementary quantities $(1, 1, 1, ...)$
  - Weighted elementary quantities $(1, 2, 4, 8, ...)$

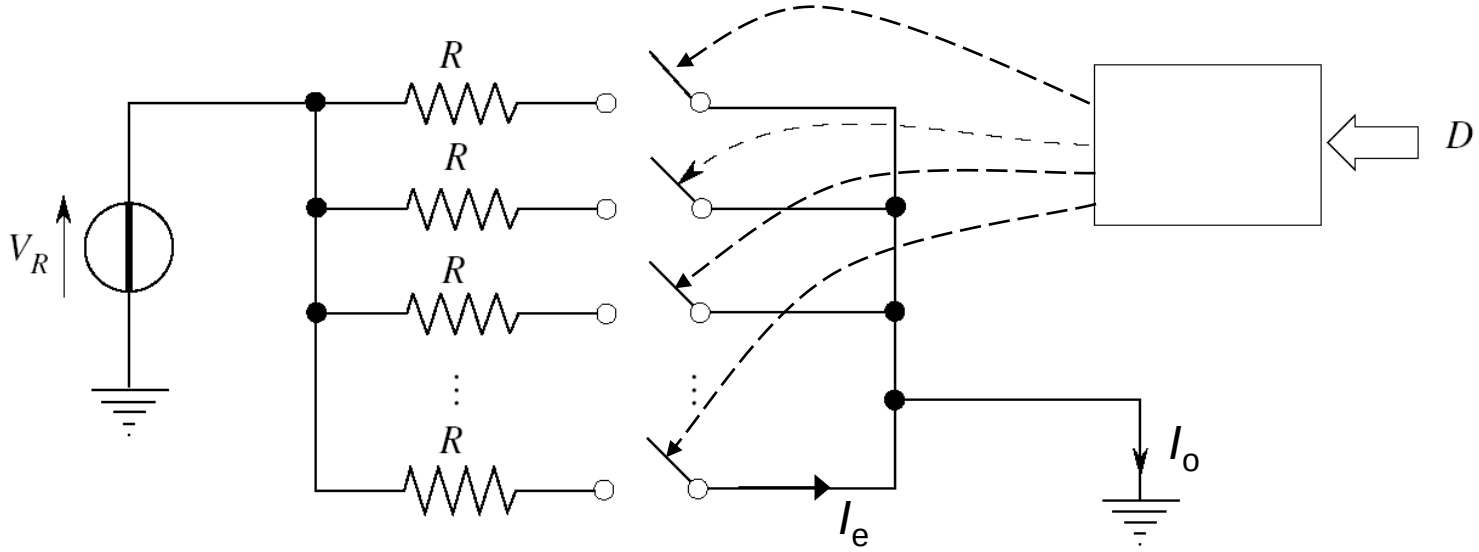
Uniform Quantities

- Sum of elementary units with the same weight (1)
- The number of units is controlled by the digital value
  - $Output = D \cdot LS$
  - Example
    $13_{10} = 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1$
- This is called uniform element conversion

Weighted Quantities

- Called weighted element conversion
- Sum of elementary units with weights powers of 2
- Each unit controlled by the corresponding bit value $(1/0)$
  - $Output = \sum_{i=0}^{N-1} 2^i \cdot D_i$
  - Example: $9_{10} = 1001_2$
  - Weight $2^3 \quad 2^2 \quad 2^1 \quad 2^0$
  - Binary representation $1 \quad 0 \quad 0 \quad 1$
  - $9_{10} = 2^3 \cdot 1 + 2^2 \cdot 0 + 2^1 \cdot 0 + 2^0 \cdot 1$

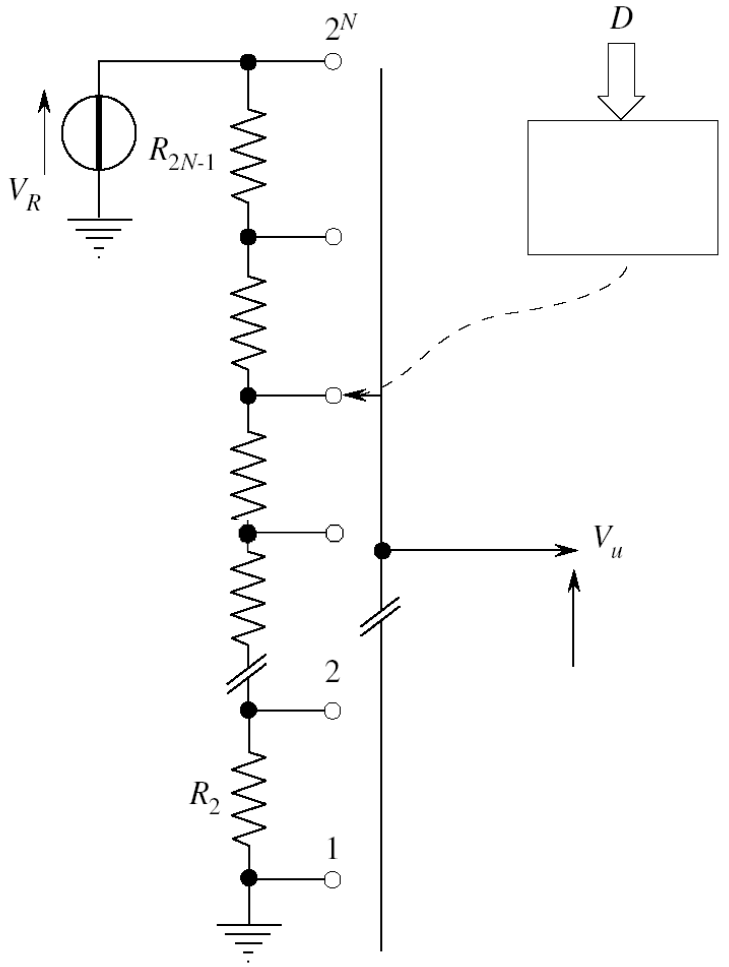
Uniform Currents D/A Converter



- The output current I_O is the sum of a variable number of identical elementary currents I_e, controlled by the N bits of $D \rightarrow M = 2^N$ identical branches

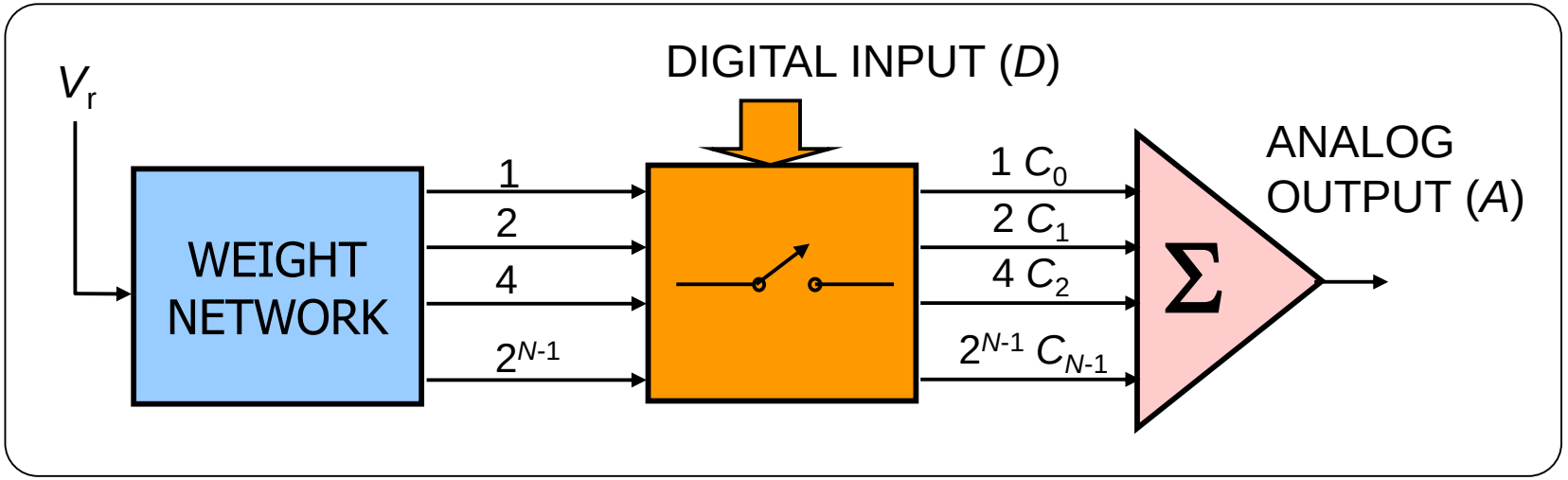
Uniform Voltages D/A Converters

- Output voltage V_O is the sum of elementary voltage drops on the resistor chain made of identical resistors
  → equal voltage drops
- The tap is set by the digital value D
- Also called *potentiometric DAC*



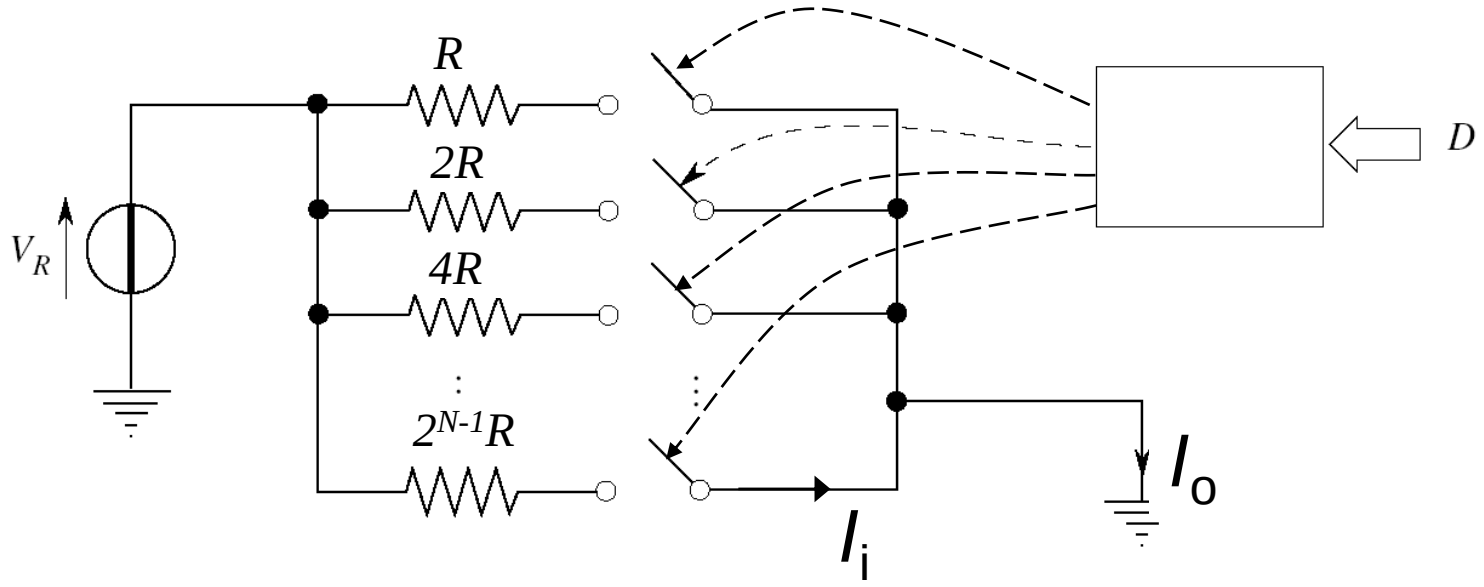
Weighted Elements Converters

- Weighted elements (usually currents)
  - Generated from a reference (usually a voltage V_r)
  - Using a weight network
  - Connected to adder through switches controlled by the bits C_i of D



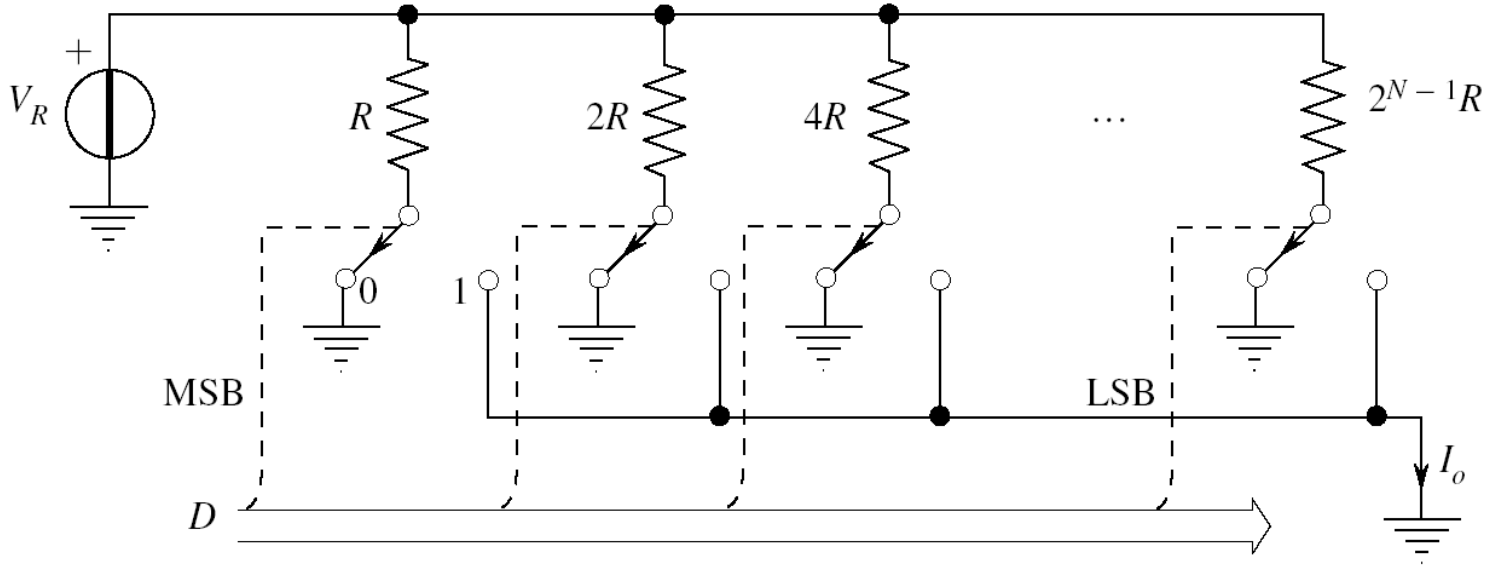
Weighted Currents D/A Converters

- Output current I_O is the sum of weighted elementary currents I_i (weight ratio 2) controlled by D
- N bits → N weighted branches



Weighted Resistor D/A Converter

- Same circuit, with switches steering the currents towards nodes at the same potential (GND)
  - Current switches

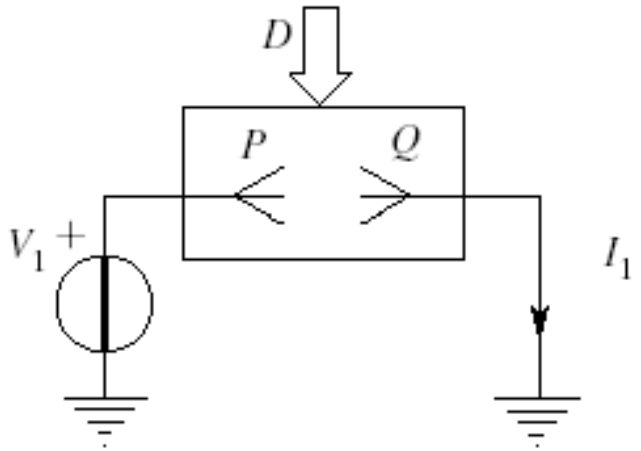


  - *High dynamic range* for resistors (2^{N-1})

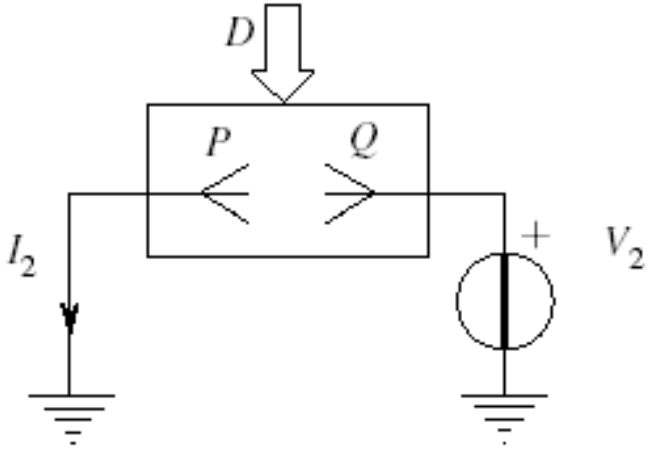
Voltage and Current Switches

- Linear passive networks: reciprocity
  - If input and output are exchanged, same $I(V)$ relation

$$I_1 = D(V_1)$$

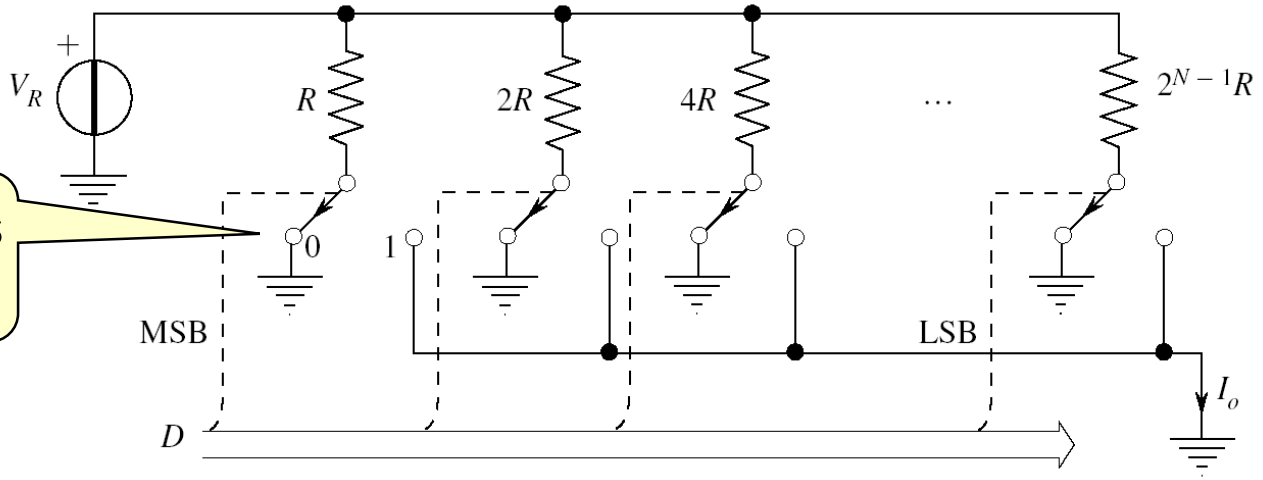


$$I_2 = D(V_2)$$

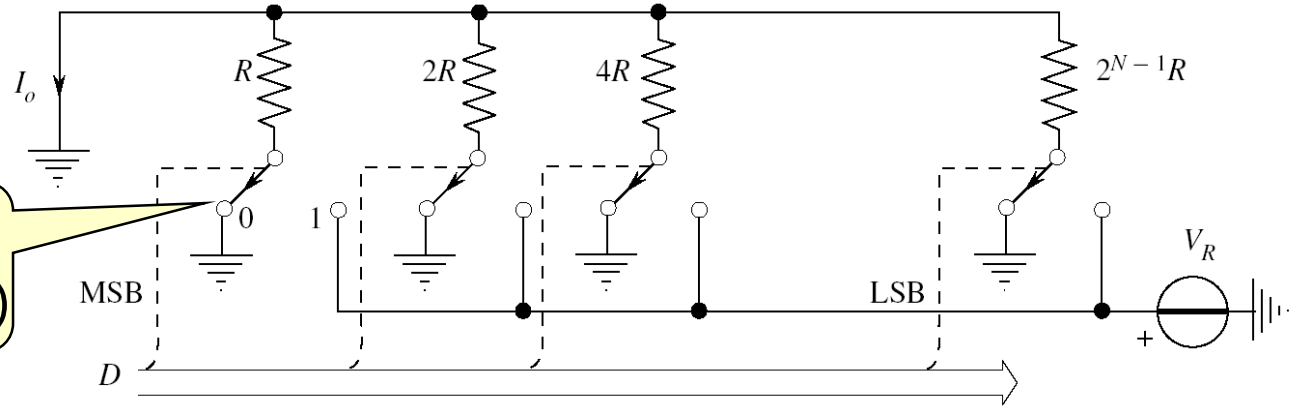


Voltage/Current Switch Comparison

Current switches (both nodes 0 V)

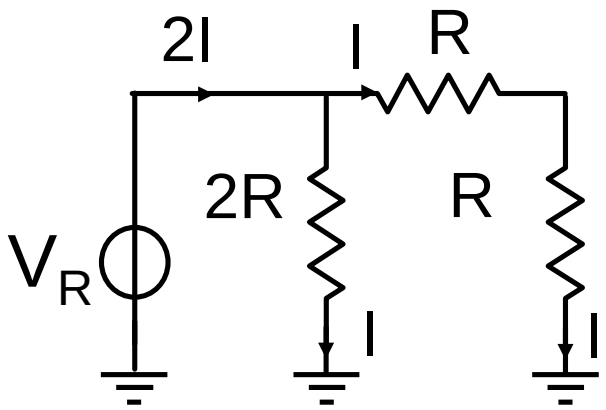


Voltage switches (nodes at V_r or 0 V)



Ladder Network (1)

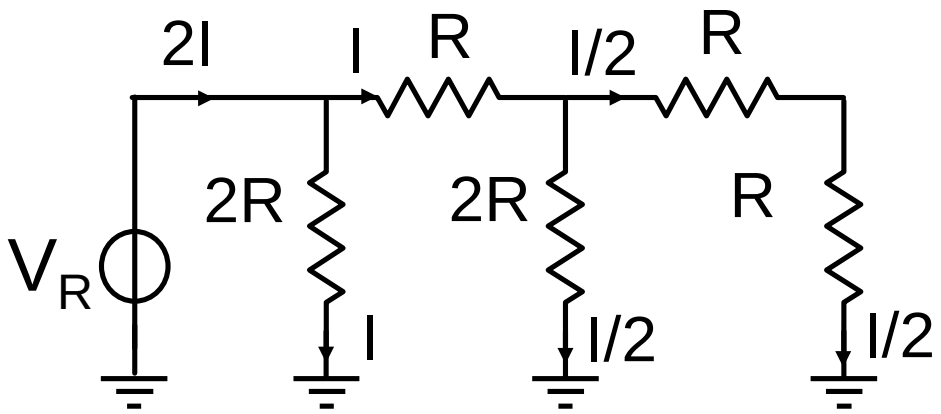
- Splitting a current in two equal parts



$$I = V_R / 2R$$

Ladder Network (2)

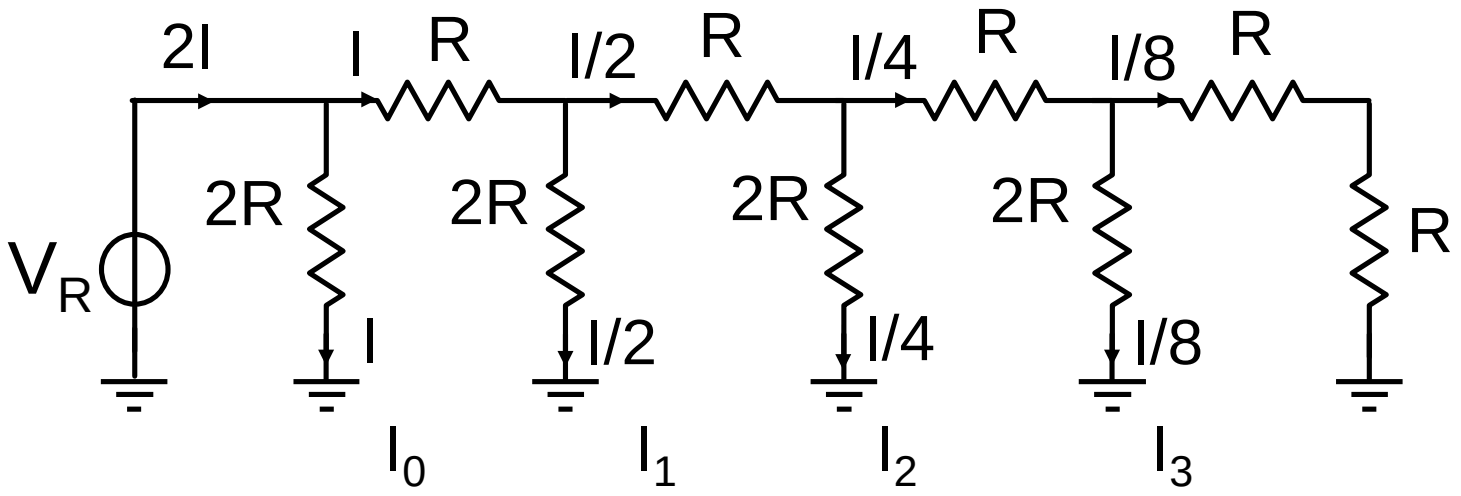
- Repeat the splitting



$$I = V_R / 2R$$

Ladder Network (3)

- Continue splitting (4 currents)

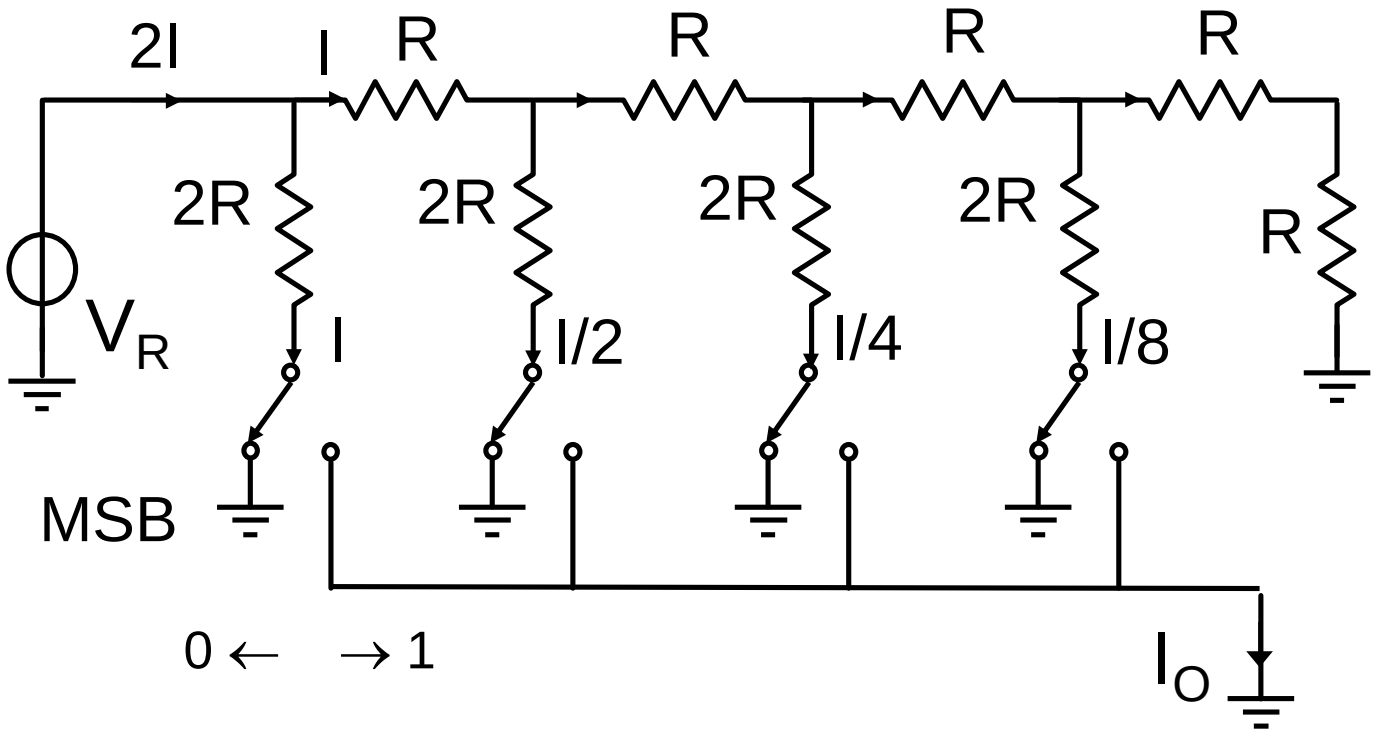


$I = V_R / 2R$ $\qquad$ $I_i = I / 2^i$

Benefits of Ladder Networks

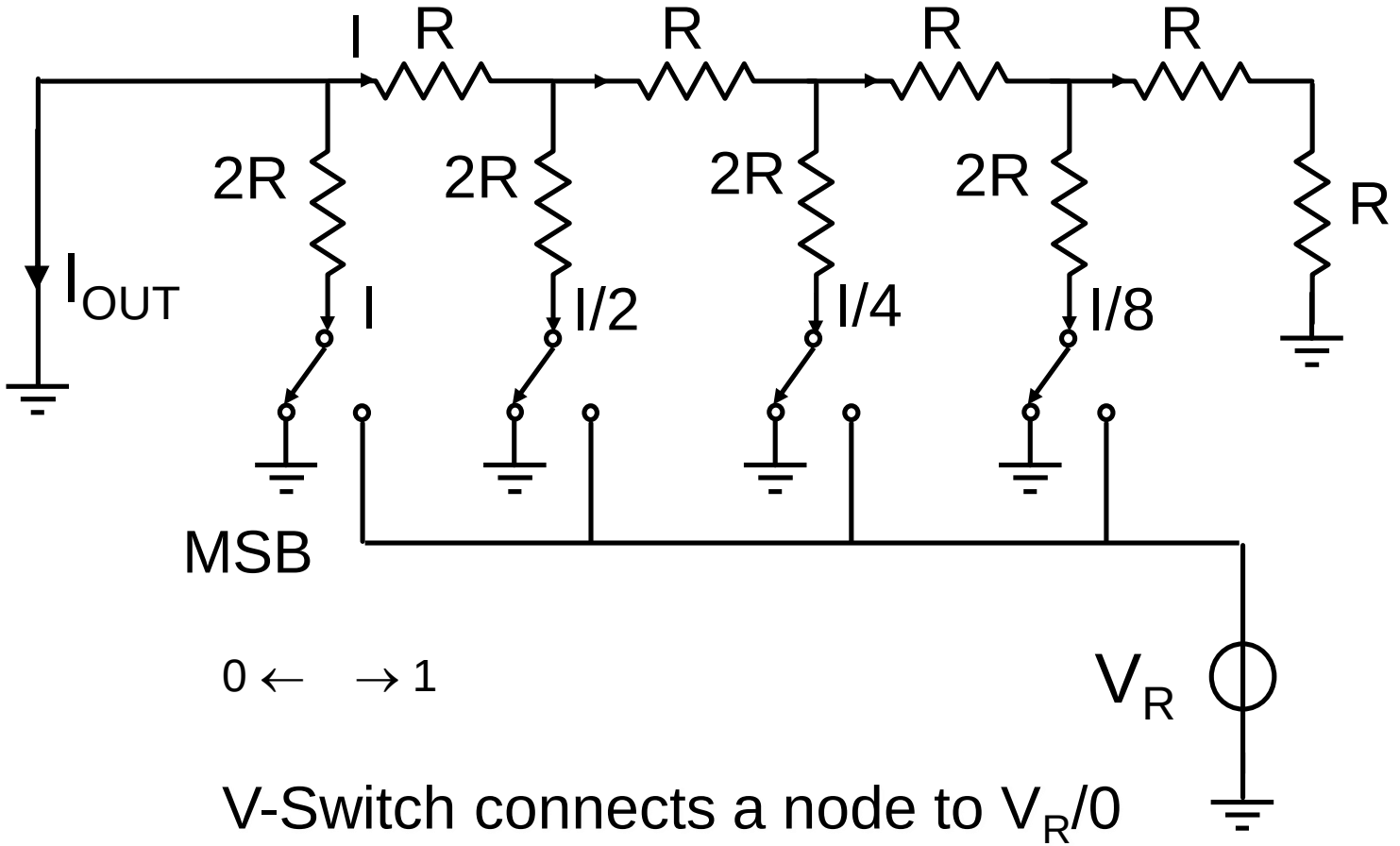
- The ladder network is fully modular
  - Any number of bits
- Uses only resistors of value R and $2R$
  - Same technology, same behavior (temp, aging, …)
  - Precise current ratio
- D/A converter with ladder network
  - Branch currents can be sent to ground/output summing node using current switches
  - Convert output to voltage with Norton/Thevenin conversion
  - Reciprocal network with V-switches feasible

Ladder Network With I-Out and I-SW



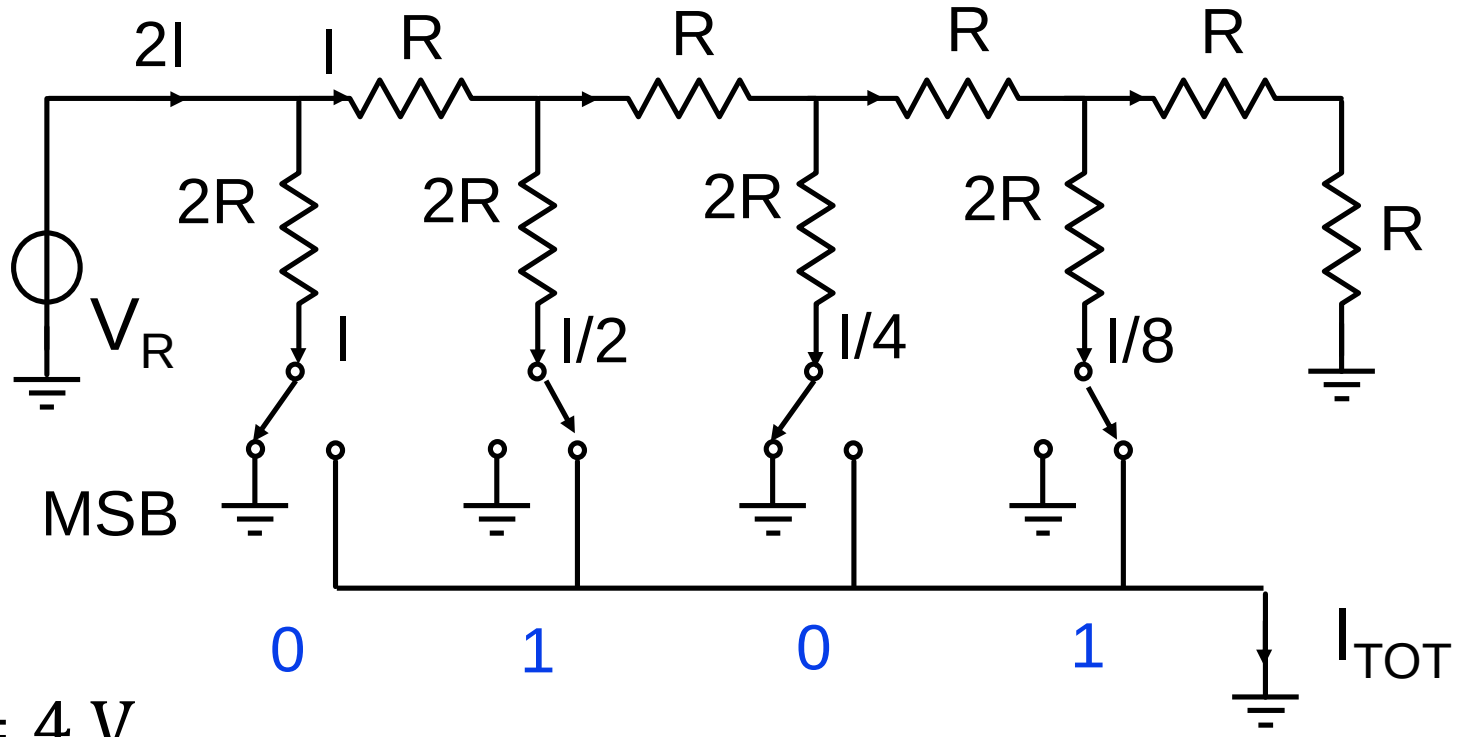
I-switches drive the current between equipotential nodes

Ladder Network with V-Out and V-SW



V-Switch connects a node to V_R/0

Ladder Network – Example



$V_R = 4\ \mathrm{V}$

$R = 10\ \mathrm{k\Omega}$

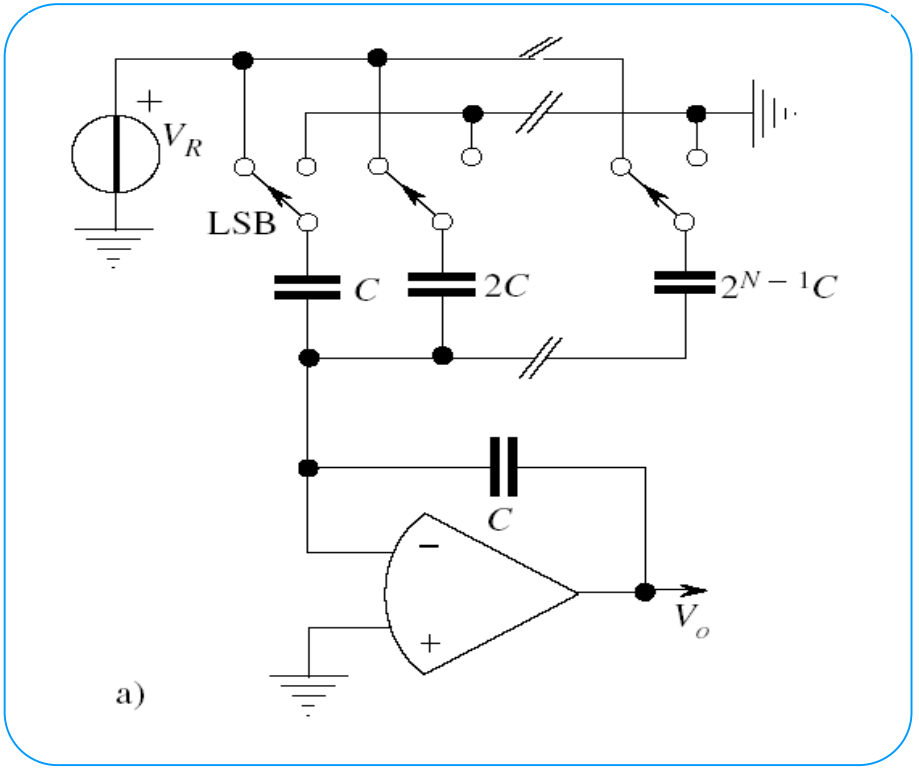
$I = \frac{V_R}{2\,R} = 0.2\ \mathrm{mA}$

$0101 \rightarrow I_{TOT} = \frac{I}{2} + \frac{I}{8} = \cdots$

$0111 \rightarrow I_{TOT} = \cdots$

Capacitive Weighted Networks

- Can add electrical charges (instead of electrical currents)
- Weighted network with electrical capacitances (instead of resistors)
- Conversion accuracy depends on accuracy of capacitance ratios
  - There are also C-2C ladder networks
- Low power consumption



Sources of Linear Errors

- *Gain* error
  - Changes in V_r
  - Systematic error in the weight network
- *Offset* error
  - Leakage current of switches
  - Offset of operational amplifier
- These errors do not depend on the value D
  - A unique correction value works for the whole dynamic range
  - Can be corrected

Branch Errors

- Equivalent resistance of switches (R_{ON})
  - Modifies the total branch resistance
  - Same effects as weight resistor error (tolerance)
  - Modifies the branch current
  - If $\Delta R/R$ is constant across branches → *gain* error
- Leakage current of switches (I_{off})
  - Some output current even for $D = 0$
  - If it is constant: offset error
  - Depends on temperature

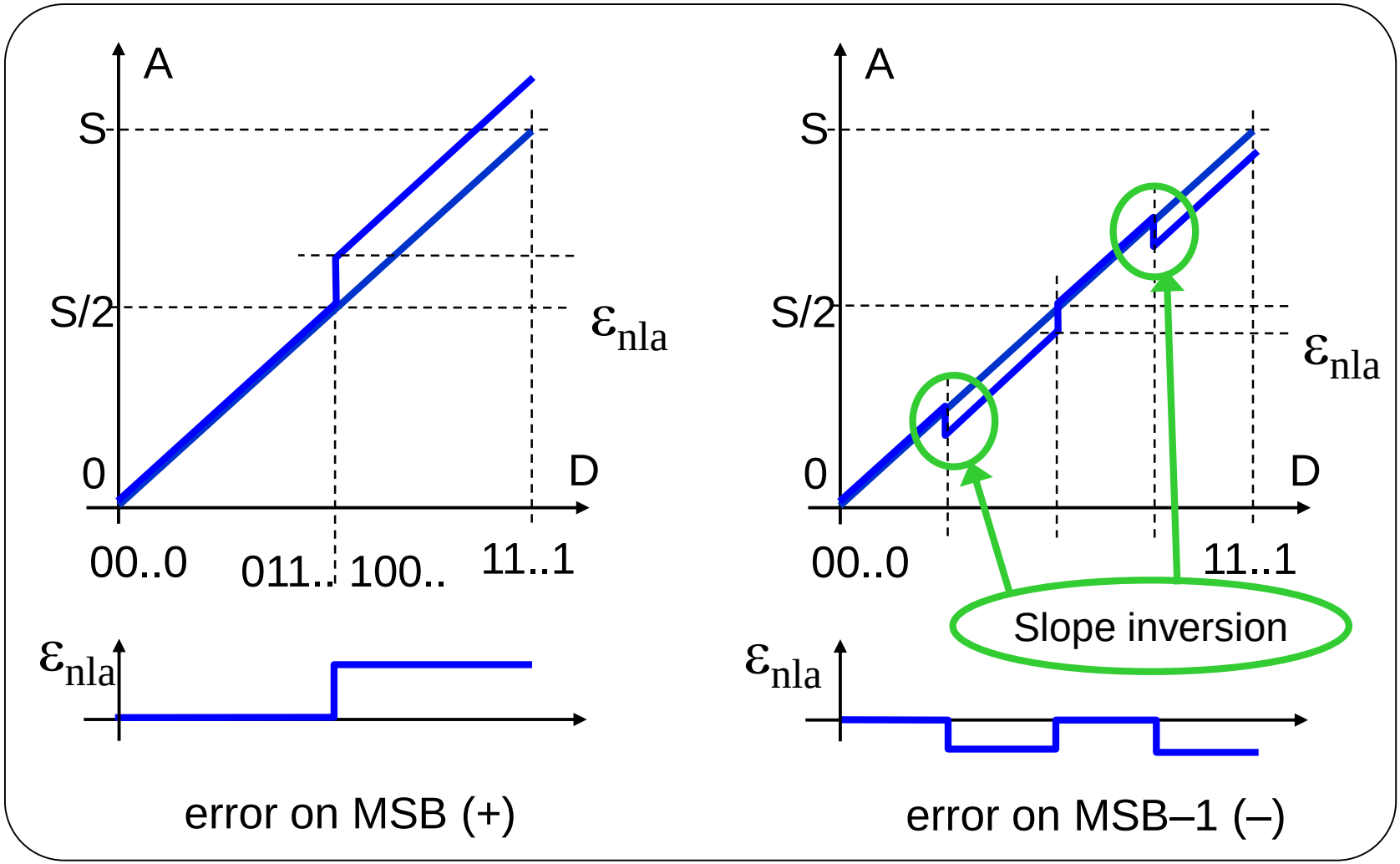
Errors in Weighted D/A Networks

- Each branch contributes to output when the corresponding bit is 1
  - MSB contributes over $S/2$, $MSB-1$ over $S/4$, ...
- Branches have different weights
  - MSB weight is $1/2$, $MSB-1$ weight is $1/4$, …
- $Out_{\text{error}} = branch_{\text{error}} \times branch_{\text{weight}}$
  - *Same* % error in different branches → *different* output errors
  - Higher effects on MSBs
- MSB branches must be more accurate
- Affected parameter: differential nonlinearity

Errors in Weighted D/A – Example

- Error on MSB branch
  - Shifted upper half of characteristic
  - Branch error 10% → output error 5%
- Error on MSB–1 branch
  - Shifted odd quarters (1, 3) of characteristic
  - Branch error 10% → output error 2.5%
- Error on MSB–2 branch
  - Branch error 10% → output error 1.25%
- …

Errors in Weight Network: MSB, $MSB - 1$



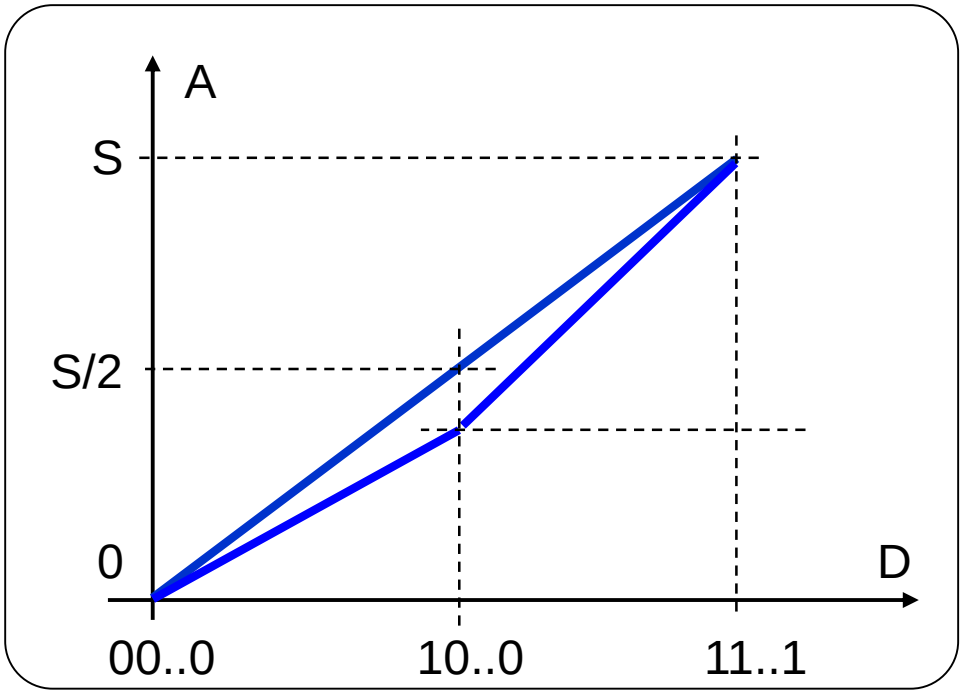
Errors in Uniform D/A Networks

- $Out_{\text{error}} = branch_{\text{error}} \times branch_{\text{weight}}$
  - Each branch has the same weight ($1\,LSB$)
  - The *same* % error in any branch causes the *same* output error
  - Intrinsically *monotonic output*
    - Sum of elements with the same sign
- All branches can have the same precision
- Errors of all branches sum at the output

- Critical parameter: integral nonlinearity

Uniform Elements D/A: Example

- Potentiometric converter
  with systematic errors in resistor chain
  - $-\Delta R$ in the upper half, $+\Delta R$ in the lower half
  - High integral nonlinearity



The voltage divider is unbalanced. Mid node voltage lower than $S/2$

Intermediate nodes have proportional errors.

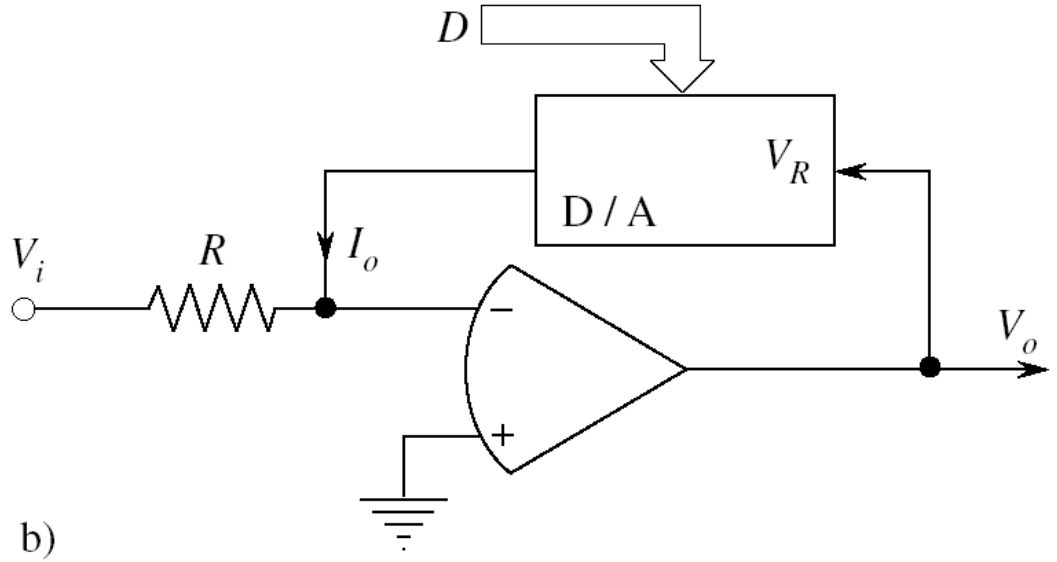
Error Summary

- Gain error
  - Changes of reference voltage V_r
  - Systematic errors in the weight network
- Offset error
  - Offsets of the operational amplifier
  - Leakage current of switches
- Nonlinear errors
  - Random errors in the weight network (N_{LD})
  - Systematic error in the uniform network (N_{LI})

Gain Control With a DAC

- The DAC is used as feedback (or input) transconductance

- The D/A must allow V_R sign inversion: $I_O = KDV_R$



$$\frac{V_i}{R} = KDV_O \Rightarrow V_O = \frac{V_i}{RKD}$$

Lecture D2: Review Questions

- How can be corrected a D/A offset and gain errors?
- Can nonlinearity errors be corrected?
- What is a non-monotonicity error?
- Describe the transient behavior of a D/A converter.
- How can we modify the circuit to avoid glitches?
- What are the disadvantages of weighted networks?
- What are the advantages of the ladder networks?
- What weighted network error may lead to a high differential error?

Exercise 1

- Draw the schematic of a 6-bit D/A converter with weighted resistances and voltage output.
- Defined the R values for $V_{\mathrm{r}} = 5\ \mathrm{V}$ and full scale $-10\ \mathrm{V}$ (assume feedback resistor of the amplifier $R_{\mathrm{F}} = 10\ \mathrm{k\Omega}$).
- Determine the two max absolute output errors (in V) for 5% tolerance resistors in the MSB and in LSB branches.
- Define the required tolerance for the resistors for a max total error of ½ LSB, if each branch has the same absolute error.

Exercise 1

- Draw the schematic of a 6-bit D/A converter with weighted resistances and voltage output.

Exercise 1: Schematic

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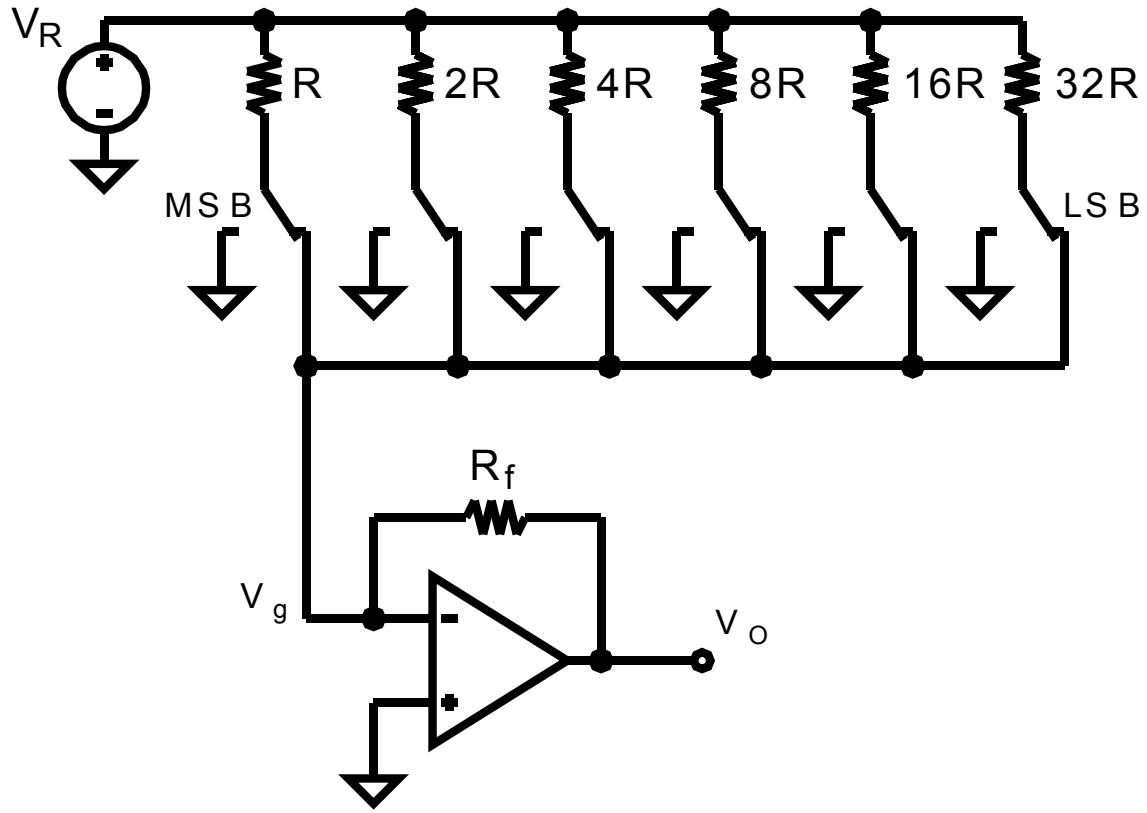
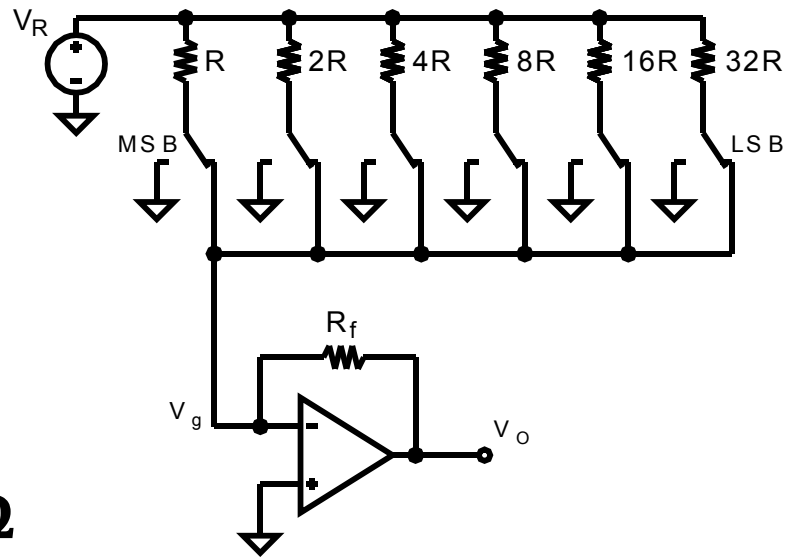


Exercise 1

- Defined the R values for $V_{\mathrm{r}} = 5\ \mathrm{V}$ and full scale $-10\ \mathrm{V}$ (assume feedback resistor of the amplifier $R_{\mathrm{F}} = 10\ \mathrm{k\Omega}$).

Exercise 1

- Defined the R values for $V_{\mathrm{r}} = 5\ \mathrm{V}$ and full scale $-10\ \mathrm{V}$ (assume feedback resistor of the amplifier $R_{\mathrm{F}} = 10\ \mathrm{k\Omega}$).
- Full scale (max V_{O} magnitude) when all bits are 1
  - $R_{\mathrm{eq}} = R \,||\, 2\,R \,||\, \ldots ||\, 32\,R = \frac{32}{63} R$
  - $V_{\mathrm{O}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{R_{\mathrm{eq}}} \Rightarrow R_{\mathrm{eq}} = -R_F \frac{V_{\mathrm{R}}}{V_{\mathrm{O}}}$
  - $\frac{32}{63} R = -10\ \mathrm{k\Omega} \cdot \frac{5\ \mathrm{V}}{-10\ \mathrm{V}} \Rightarrow \boldsymbol{R = 9.84\ \mathrm{k\Omega}}$

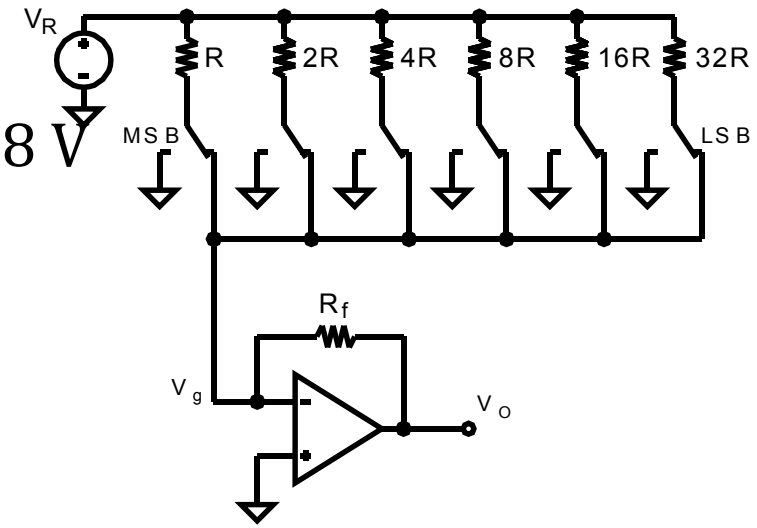


Exercise 1

- Determine the two max absolute output errors (in V) for 5% tolerance resistors in the MSB and in LSB branches.

Exercise 1

- Determine the two max absolute output errors (in V) for 5% tolerance resistors in the MSB and in LSB branches.
- Branches with errors are activated



- $V_{\mathrm{O_{nom}}}^{\mathrm{MSB}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{R} = -5\ \mathrm{V} \cdot \frac{10\ \mathrm{k\Omega}}{9.84\ \mathrm{k\Omega}} = -5.08\ \mathrm{V}$
- $V_{\mathrm{O_{min}}}^{\mathrm{MSB}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{R(1+5\,\%)} = -4.84\ \mathrm{V}$
- $V_{\mathrm{O_{max}}}^{\mathrm{MSB}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{R(1-5\,\%)} = -5.35\ \mathrm{V}$
- $V_{\mathrm{O_{nom}}}^{\mathrm{LSB}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{32R} = -5\ \mathrm{V} \cdot \frac{10\ \mathrm{k\Omega}}{32 \cdot 9.84\ \mathrm{k\Omega}} = -0.159\ \mathrm{V}$
- $V_{\mathrm{O_{min}}}^{\mathrm{LSB}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{32R(1+5\,\%)} = -0.151\ \mathrm{V}$
- $V_{\mathrm{O_{max}}}^{\mathrm{LSB}} = -V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{32R(1-5\,\%)} = -0.167\ \mathrm{V}$

Exercise 1

- Define the required tolerance for the resistors for a max total error of ½ LSB, if each branch has the same absolute error.

Exercise 1

- Define the required tolerance for the resistors for a max total error of ½ LSB, if each branch has the same absolute error.
- Each branch contributes
$$\frac{1/2\ LSB}{6} = \frac{1}{12} LSB = \frac{1}{12} V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{32\ R}$$
- MSB branch contribution
  - $\frac{1}{12} V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{32\ R} = V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{R} - V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{R+\Delta R}$
  - $R + \Delta R = R \frac{12 \cdot 32}{12 \cdot 32 - 1} \Rightarrow \frac{\Delta R}{R} = \frac{1}{12 \cdot 32 - 1} = 0.26\ \%$
- MSB–1 branch contribution
  - $\frac{1}{12} V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{32\ R} = V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{2R} - V_{\mathrm{R}} \frac{R_{\mathrm{F}}}{2R+\Delta R}$
  - $2R + \Delta R = 2R \frac{6 \cdot 32}{6 \cdot 32 - 1} \Rightarrow \frac{\Delta R}{2R} = \frac{1}{6 \cdot 32 - 1} = 0.52\ \%$
- MSB–2 branch contribution…