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电子科技大学2012 -2013学年第_二_学期期_末_考试_A_卷

课程名称: _数字逻辑设计及应用__ 考试形式: 闭卷 考试日期: 20 13 年 07 月 05 日

考试时长: _120___分钟

课程成绩构成: 平时 30 %，期中 30 %，实验 0 %，期末 40 %

本试卷试题由___七__部分构成，共 _7___页。

题号	一	二	三	四	五	六	七	八	九	十	合计
得分											

得 分

I. Fill out your answers in the blanks (3' X 10=30')

1. If a 74x138 binary decoder has 110 on its inputs CBA, the active LOW output Y5 should be (1 or high).

2. If the next state of the unused states are marked as "don't-cares" when designing a finite state machine, this approach is called minimal (cost) approach.

3.The RCO_L of 4-bit counter 74x169 is (0 or low) when counting to 0000 in decreasing order.

4. To design a "001010" serial sequence generator by shift registers, the shift register should need (4) bit at least.

5. One state transition equation is Q*=JQ'+K'Q. If we use T flip-flop with enable to complete the equation，the enable input of T flip-flop should have the function EN=(JQ'+KQ).

6. A 4-bit Binary counter can have (16) normal states at most, 4-bit Johnson counter with no self-correction can have (8) normal states, 4-bit linear feedback shift-register (LFSR) counter with self-correction can have (16) normal states.

7. If we use a ROM, whose capacity is 16 × 4 bits, to construct a 4-bit binary code to gray code converter, when the address inputs are 1001, (1101) will be the output.

8. When the input is 10000000 of an 8 bit DAC, the corresponding output voltage is 2V. The output voltage is (3.98) V when the input is 11111111.

得 分

II. Please select the only one correct answer in the following questions.(2' X 5=10')

1. If a 74x85 magnitude comparator has ALTBIN=1, AGTBIN=0, AEQBIN=0, A3A2A1A0=1101, B3B2B1B0=0111 on its inputs, the outputs are (D).

A) ALTBOUT=0, AEQBOUT=0, AGTBOUT=0 B) ALTBOUT=1, AEQBOUT=0, AGTBOUT=0

C) ALTBOUT=1, AEQBOUT=0, AGTBOUT=1 D) ALTBOUT=0, AEQBOUT=0, AGTBOUT=1

2. As shown in Figure 1, what would the outputs of the 4-bit adder 74x283 be (B) when A3A2A1A0=0100, B3B2B1B0=1110 and S/A=1.

A) C4=1, S3S2S1S0=0010 B) C4=0, S3S2S1S0=0110 C) C4=0, S3S2S1S0=1010

D) C4=0, S3S2S1S0=1110

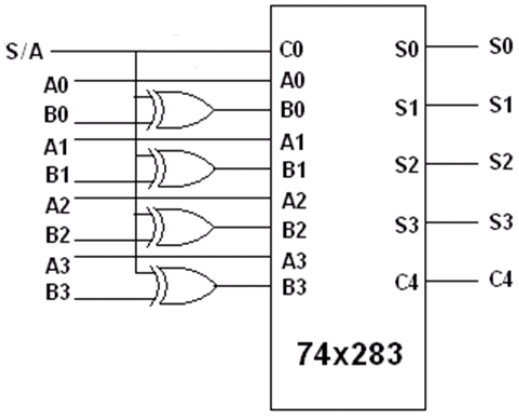


Figure 1

3. Which of the following statements is INCORRECT? (A)

A) A D latch is edge triggered and it will follow the input as long as the control input C is active low.

B) A D flip flop is edge triggered and its output will not change until the edge of the controlling CLK signal.

C) An S-R latch may go into metastable state if both S and R are changing from 11 to 00 simultaneously.

D) The pulse applying to any input of an S -R latch must meet the minimum pulse width requirement.

4. The capacity of a memory that has 13 bits address bus and can store 8 bits at each address is (B).

A) 8192 B) 65536 C) 104 D) 256

5. Which state in Figure 2 is NOT ambiguous (C).

A) A B) B C) C and D D) C

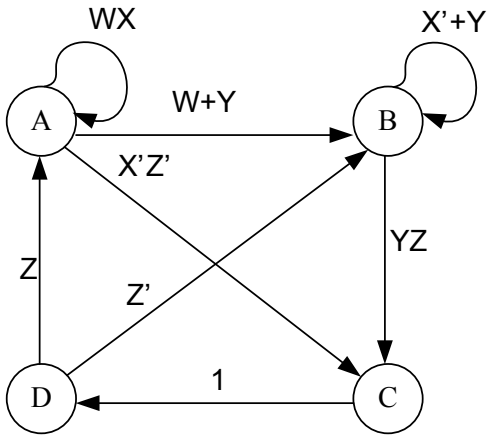


Figure 2

得 分

III. Analyze the sequential-circuit as shown in Figure 3, D Flip-Flop with asynchronous preset and clear inputs. **[15']**

1.Write out the excitation equations, transition equations and output equation. **[5']**

2.Assume the initial state Q_2Q_1=00, complete the timing diagram for Q_2 ,Q_1 and Z. **[10']**

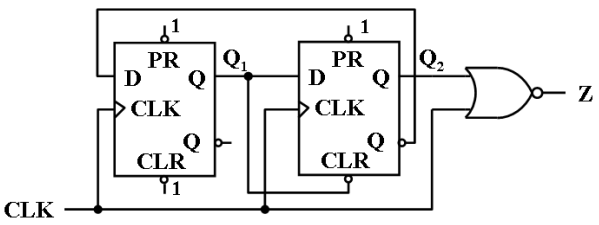
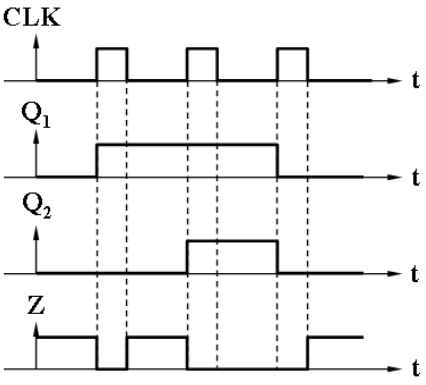


Figure 3



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参考答案：

激励方程: $D_1=Q_2^{/}$，$D_2= Q_1$

转移方程：$Q_1^{*}= D_1=Q_2^{/}$，$Q_2^{*}=D_2= Q_1$

输出方程：$Z= (CLK+Q_2)^{/}$

参考评分标准：

1. 5个方程正确得5分；每错一个扣1分，扣完5分为止；

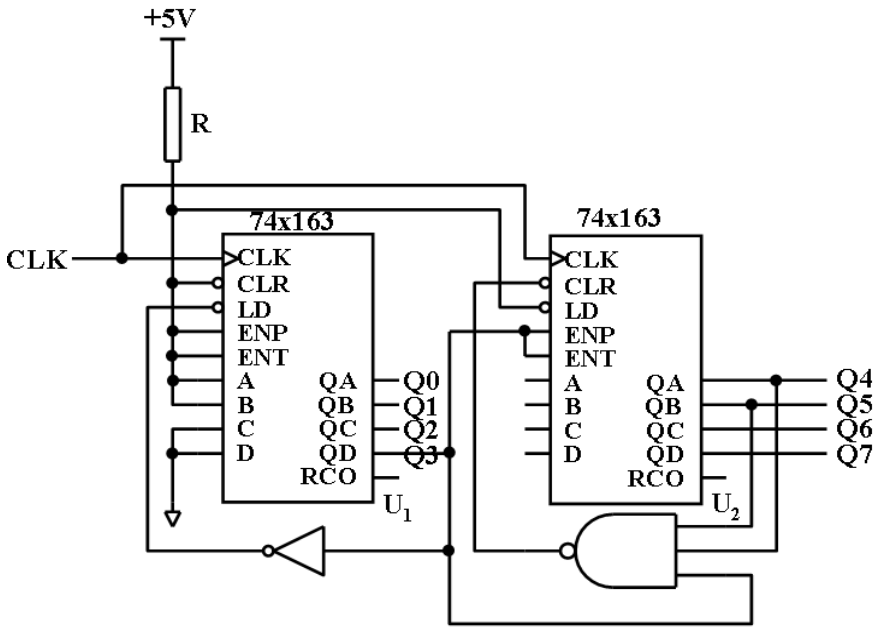
2.

Q_1、Q_2、Z的波形边沿判断正确，得3分，错一个，扣1分，扣完3分为止；每个上升沿和下降沿各0.5分，错1处扣0.5分，扣完7分为止。

得 分

IV. Analyze the sequential-circuit as shown below, which contains two 74x163 4-bit binary counter. **[15']**

1. Write out the logic expression LD_L for U_1 and CLR_L for U_2.[4']
2. Assume the initial state is 3_{10}, write out the state sequence for the circuit. **[8']**
3. Describe the modulus for the circuit. **[3']**



The function table for 74x163

Inputs				Current state	Next state	Outputs
CLR_L	LD_L	ENT	ENP	QD QC QB QA	QD* QC* QB* QA*	RCO
0	X	X	X	X X X X	0 0 0 0	0
1	0	X	X	X X X X	D C B A	0
1	1	0	X	X X X X	QD QC QB QA	0
1	1	X	0	X X X X	QD QC QB QA	0
1	1	1	1	0 0 0 0	0 0 0 1	0
1	1	1	1	0 0 0 1	0 0 1 0	0
1	1	1	1	0 0 1 0	0 0 1 1	0
1	1	1	1	0 0 1 1	0 1 0 0	0
1	1	1	1	……	……	0
1	1	1	1	1 1 1 1	0 0 0 0	1

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参考评分标准:

1. LD_L=Q_3',CLR_L=$(Q_5Q_4Q_3)'$ [4’]
2. 状态序列：十六进制数表示：03,…08,13,…18,23,…28,33,…38,03,…08
   或十进制数表示：3,…8,19,…24,35,…40,51,…56,3,…8[8’]
   错1处扣1分，扣完为止。
3. m=24 [3’]

得 分

V. Design a sequence signal generator with self-correcting to generate a serial output sequence of 101100, using a 74x194 and a 74x151.[15’]

1. List the transition table .[4’]
2. Write out the canonical sum of feedback function LIN.[[4’]
3. Draw the circuit diagram.[7’]

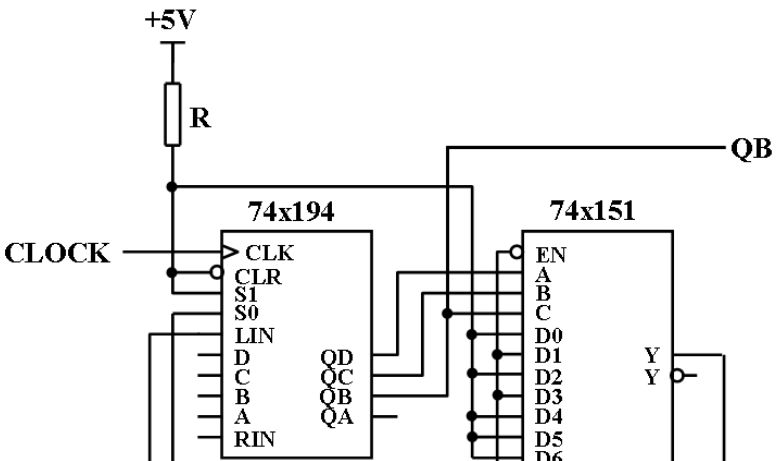
The function table for 74x194

Iutputs	Next state	Function
S1 S0	QA* QB* QC* QD*	
0 0	QA QB QC QD	Hold
0 1	RIN QA QB QC	Shift right
1 0	QB QC QD LIN	Shift left
1 1	A B C D	Load

参考评分标准:

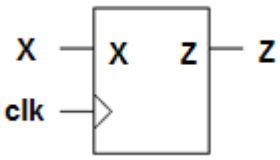
1. 转移表正确4分，错1行扣0.5分。
2. 反馈函数正确LIN=$D_0=\Sigma_m(0,2,4,5)$ [4’]
3. 电路图正确7分，错1处扣0.5分，扣完为止。

Q_2 Q_1 Q_0	Q_2^* Q_1^* Q_0^*	D_0
1 0 1	0 1 1	1
0 1 1	1 1 0	0
1 1 0	1 0 0	0
1 0 0	0 0 1	1
0 0 1	0 1 0	0
0 1 0	1 0 1	1
0 0 0	0 0 1	1
1 1 1	1 1 0	0



得 分

VI. Write out the state/output table for a Mealy machine that can detect the pattern 10101 or 10111 . The output Z=1 when the pattern is detected. Your model should also be able to detect overlapping sequences. (10')



State meaning	S	X	
		0	1
Initial state	A	A, 0	B, 0
Got 1	B	C, 0	B, 0
Got 10	C	A, 0	D, 0
Got 101	D	E, 0	F, 0
Got 1010	E	A, 0	D, 1
Got 1011	F	C, 0	B, 1
		S*, Z	

评分标准:
1.状态定义正确得3分；每错一处扣0.5分，扣完3分为止；
2.状态转移正确，得5分；每错一处扣0.5分，扣完5分为止；
3.输出正确，得2分；每错一处扣0.5分，扣完2分为止。

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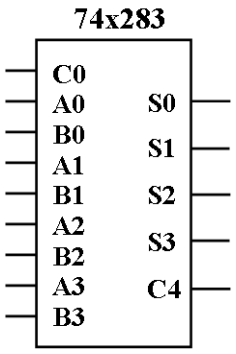
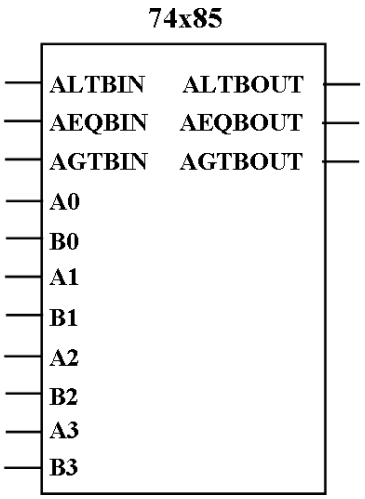
VII. Design a code converter with 2421 code to 8421 code, using a 74x85, a 74x283 and some gates if needed. **[10']**

2421	8421
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 0	0 0 1 0
0 0 1 1	0 0 1 1
0 1 0 0	0 1 0 0
1 0 1 1	0 1 0 1
1 1 0 0	0 1 1 0
1 1 0 1	0 1 1 1
1 1 1 0	1 0 0 0
1 1 1 1	1 0 0 1





参考评分标准:

1.74x85级联输入端连接正确2分，比较值正确3分，74x283的C0端连接正确1分;
2.74x85的A3~A0与74x283的A3~A0连接正确2分;
3.74x85与74x283中间连接的电路正2分。