Chenyuan Chu

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Education

Peking University Beijing, China
B.Eng. degree from the School of Electronic Engineering and Computer Science Sep 2022 - Present
GPA: *3.804/4.0 (91/100, Scholaro: 3.86/4.0)* **Rank**: *2/40(Top 5%)*

Rice University Houston, TX, USA
Vising Student, Department of Electrical and Computer Engineering Aug 2025 - Present
Advised by *Prof.Kaiyuan Yang*

Experience

PRIME Lab Peking University
Undergraduate Researcher, advised by Prof.Xiyuan Tang Sep 2024 - Present

- **AI-Enhanced Analog Circuit Design** Sep 2024 - Feb 2025
  - Started with a reinforcement learning-based automatic analog circuit sizing design tool (PVTSizing, DAC'2024), explored the possibility of using AI to assist in analog circuit design, including topology generation (or selection), schematic design and layout design.
  - Proposed a concept of End-to-End AI-Enhanced analog circuit design tools, which integrates AI agents for different tasks throughout the chip design and tape-out process to automate the entire chip design.
  - Tried out a LLM-based tool to assist in the design of analog circuits, which can help with the generation of circuit parameters.
- **Tape-out of analog circuit with EDA design tools** Feb 2025 - Sep 2025
  - Designed Bandgap and StrongArm Comparator circuits with three different requirements of performance using PVTSizing tools.
  - Partly responsible for the tape-out process, including schematic design and layout design of the Bandgap circuit and StrongArm Comparator circuit.
  - Participated in the floorplan stage of the chips, taped out the chip in the SMIC 55nm process, tested the chip in September 2025, and obtained a patent certification in this design tool.
- **High-performance NS-SAR ADC** Apr 2025 - Present
  - Carried out a comprehensive study of the basic knowledge and internal mechanism of SAR ADC.
  - Responsible for the layout design of several blocks in the entire ADC, including SAR logic, divider and so on.
  - Co-author on this work, which has already been accepted by **IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2026**.

SIMS Lab Rice University
Visiting Student, advised by Prof.Kaiyuan Yang Aug 2025 - Dec 2025

- **Wide-Range and Low-Power Level Shifter at 10MHz Input Frequency**
  - Conducted literature review on level shifters and identified the need for a wide-range, low-power design, analyzed various popular level shifter architectures(such as SLC, DCVS structures) and their trade-offs, and **innovatively proposed a new architecture** that combines the advantages of both.
  - Achieved a wide conversion range that supports an input voltage of 600mV to be shifted to an output voltage of any value between 1V and 5V at 10MHz input, which greatly improves the speed of SLC structure at the cost of 10% power increase.
  - **Completely responsible for the entire tape-out process (TSMC180 process)**, including idea proposal, circuit schematic design, layout design, test circuits and peripheral circuits design, and submitted the GDS file. The chip will be tested in January 2026.
  - Planned to perform another tape-out to compare with other state-of-the-art structures to obtain a more comprehensive result.
- **Low-Power and PVT-Robust Current Reference (In Progress)**

- Studied various types of current reference circuits and their working principles.
- Reproduced several classic structures including Beta-Multiplier structure, ΔV_{BE}-Based structure and Division-Based structure.
- Implemented a 2T voltage reference as a regulator to improve the power supply rejection and reduce the power consumption, producing a 100nA current reference with resistor-trimming, with a temperature coefficient between 33.2ppm/°C and 150ppm/°C over 5 process corners and a temperature range of 0°C to 100°C, PSRR $>$ 180dB at low frequency, and a power consumption of several hundreds of nanoWatts at 1.8V supply voltage.
- Currently working on improving the temperature coefficient and process variation robustness, expecting to solve the problems of complex trimming circuits caused by 2T reference and the sensitivity of output power supply to process variations.

Publications

- Zongnan Wang, Bingrui Li, Haoyang Luo, **Chenyuan Chu**, Jiachang Yang, Yuan Wang, Xiyuan Tang*, "An 85.1dB-SNDR 8MS/s Incremental Pipeline ADC with Dual-Residue-Assisted Exponential Quantization," **IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2026**

Skills

Language:	Mandarin(Native), English
Programming Language:	C/C++, Python, MatLab, Verilog, SystemVerilog, LaTeX
Circuit Design:	Vivado, Modelsim, Cadence Virtuoso, NgSpice, Innovus, Genus

Highlighted Projects

Automated Unstable Combinational Logic Loop Detection *C++, Python*
https://github.com/FileTransferrr/EDA-Project
Undergraduate contestant, advised by Prof. Yibo Lin

- Designed a detection tool for identifying unstable combinational logic loops in ultra-large-scale combinational logic circuits.
- Innovatively proposed a "Reversed Detection" algorithmic approach, realizing high-accuracy detection.
- Applied the method of parallel computing to enable high-speed detection.
- Received an award in a **National Graduate-Level Competition** as an undergraduate contestant.

BCM Solver *C++, Verilog*
https://github.com/FileTransferrr/BCM-Solver

- Develop a tool to solve the Boolean Circuit Matching problem.
- Employ graph algorithms to model and process a logic circuit as a directed graph.
- Implement random computing methods to prune the search space and speed up the solving process.
- Configured the tool to solve the Boolean Circuit Matching problem for circuits with up to 1000 gates in less than 30 seconds.

Vehicle-Routing-Problem-with-ILP-and-SA *Matlab*
https://github.com/a1henu/Vehicle-Routing-Problem-with-ILP-and-SA

- Develop a program to solve the vehicle routing problem.
- Integrate integer linear programming (ILP) algorithm and simulated annealing (SA) algorithm.
- Implement the ILP algorithm using the `intlinprog` function in Matlab.

RISC-V CPU *SystemVerilog, Vivado*
https://github.com/star-power-riscv/Pipeline-Onboard-CPU

- Design a 32-bit RISC-V CPU with a 5-stage pipeline architecture.
- Implement simple branch prediction, hazard detection, and forwarding unit.
- Ensure the CPU can execute 37 RISC-V instructions, including algorithmic, logical, load/store, and control instructions.

- Provide an automated testing framework and verify the CPU by running it on an FPGA board.

Bandgap Voltage Reference Circuit Design *Cadence Virtuoso* (Designed in TSMC180 PDK)

- Design a bandgap reference circuit that provides a stable output voltage of 1.2V with a Temperature Coefficient(TC) of 17.5ppm/°C over a temperature range of -55°C to 125°C.
- Utilize the principles of first and second order temperature compensation to achieve the desired performance, with resistors implemented as non-ideal devices, capacitor implemented as a PMOS Dummy, and employ the parallel compensation to increase the Phase Margin to improve stability.
- Current mirrors are implemented as cascode structures to improve the accuracy of current replication, and the circuit is designed to operate under a supply voltage of 1.8V with a start-up circuit to ensure proper initialization.
- Achieve the specifications (Pre-Layout Simulation) of 17.5ppm/°C TC over -55°C to 125°C with a nominal output voltage of 1.2V, Phase Margin (PM) $> 70°$, PSRR=110.8dB at 1Hz, Output Noise $= 0.8\mu V/\sqrt{Hz}$ at 1KHz noise bandwidth, and standard deviation of output voltage $\sigma = 1.3mV$ under 1000 points Monte-Carlo simulation.

16-bit SAR ADC Design (In Progress) *Cadence Virtuoso, Matlab* (Designed in TSMC180 PDK)

- Design a 16-bit fully-differential SAR ADC achieving a high resolution of over 14 bits ENOB at the sampling rate of 40KS/s.
- Modelize and simulate the entire ADC system in Matlab to determine the specifications of each block.
- Implement bootstrapped switches, Capacitor DAC with bottom-plate sampling, StrongArm Comparator with Floating Inverter Amplifier, and asynchronous SAR logic to optimize performance.
- Employ VCM-based switching technique to protect the common-mode voltage from deviating far from its ideal value, maintaining low power consumption and good performance of the comparator.
- The goal is to achieve an ENOB of over 14 bits at 100KS/s sampling rate with low power consumption under pre-layout simulation. This ADC will be further improved and simulated for post-layout performance if time permits.

Honors & Awards

EECS Academic Scholarship School of EECS, Peking University
Oct 2024
Commendation for Outstanding Academic Performance in the 2023-24 Academic Year.

Outstanding Research Award Peking University
Oct 2024
Commendation for exceptional performance in comprehensive evaluation during the 2023-24 Academic Year.

National Third Prize in EDA Elite Challenge China Graduate Innovation Practice Competitions
Dec 2024
Awarded in the 2024 China Graduate Innovation Contest for outstanding achievement in EDA design.(Undergraduate Awardee in National Graduate-Level Competition)
Team members: Chenyuan Chu, Yitian Sun, Boxin Zheng. Advisor: Yibo Lin.

Tian-Chuang EECS Academic Scholarship School of EECS, Peking University
Oct 2025
Commendation for Outstanding Academic Performance in the 2024-25 Academic Year.

Outstanding Research Award Peking University
Oct 2025
Commendation for exceptional performance in comprehensive evaluation during the 2024-25 Academic Year.

Extra-curriculum Outreach

Member of department's football team at Peking University Sep 2022 - Present

- Silver medal in the 2022 Freshman Cup Football Match.
- Bronze medal in the 2024 Peking University Cup Football Match.