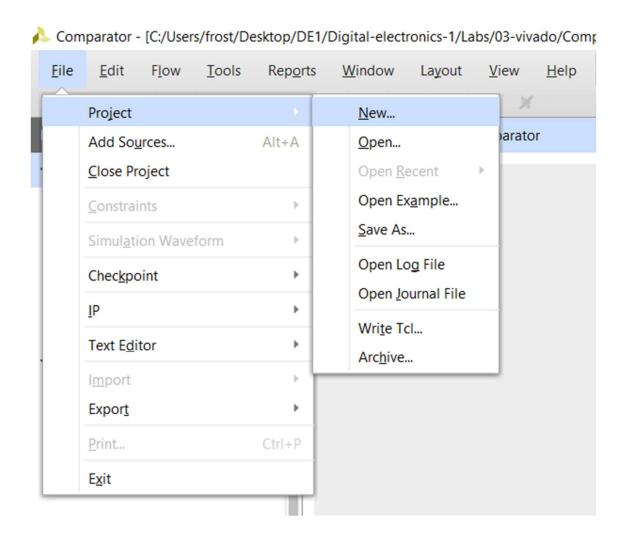
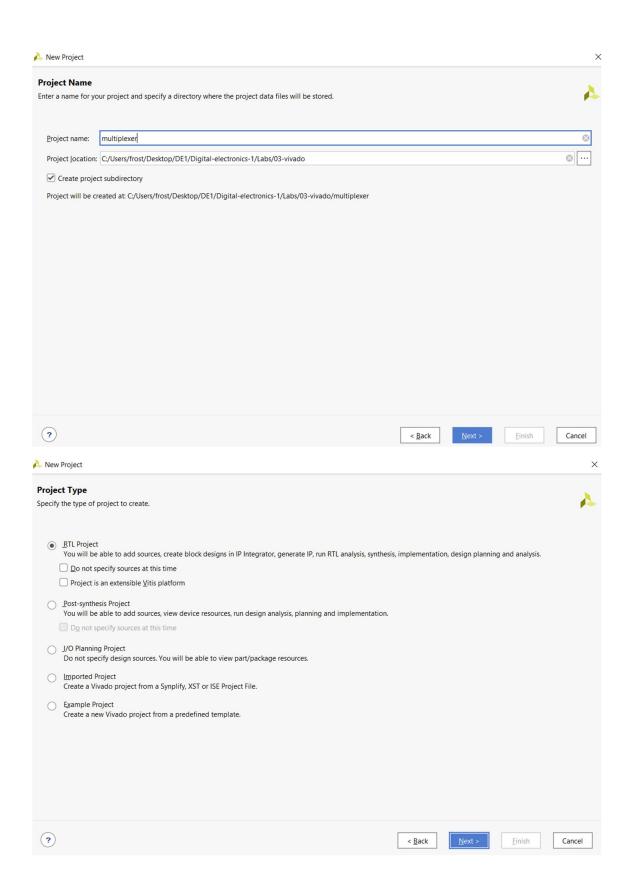
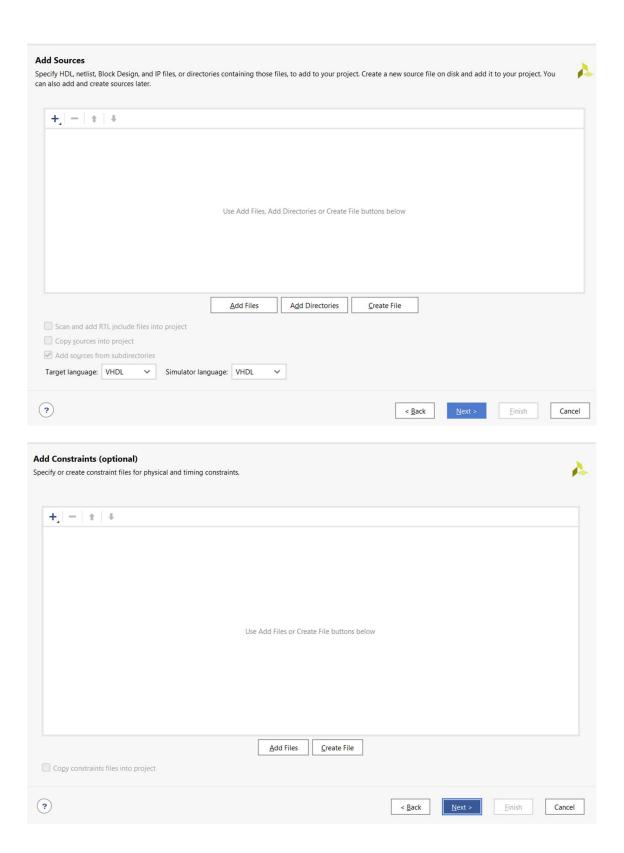
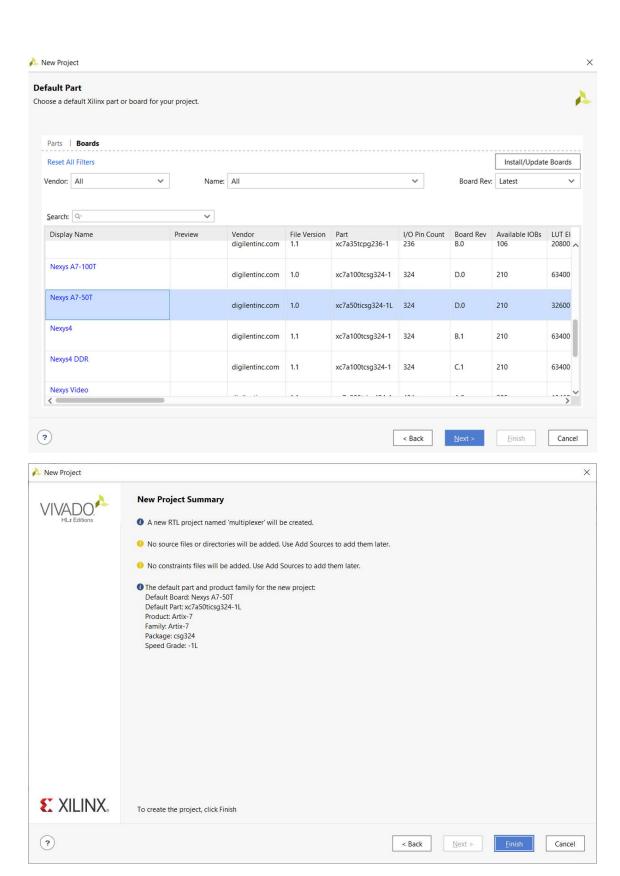
Creating new project



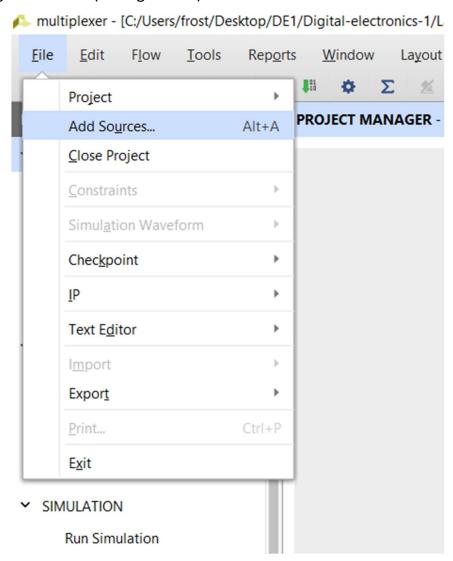


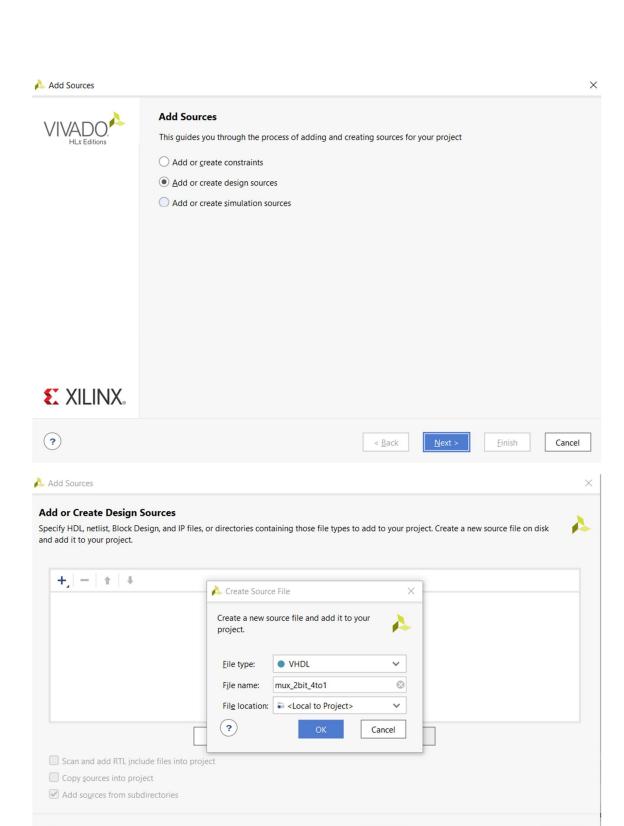






Creating new source (desing source)



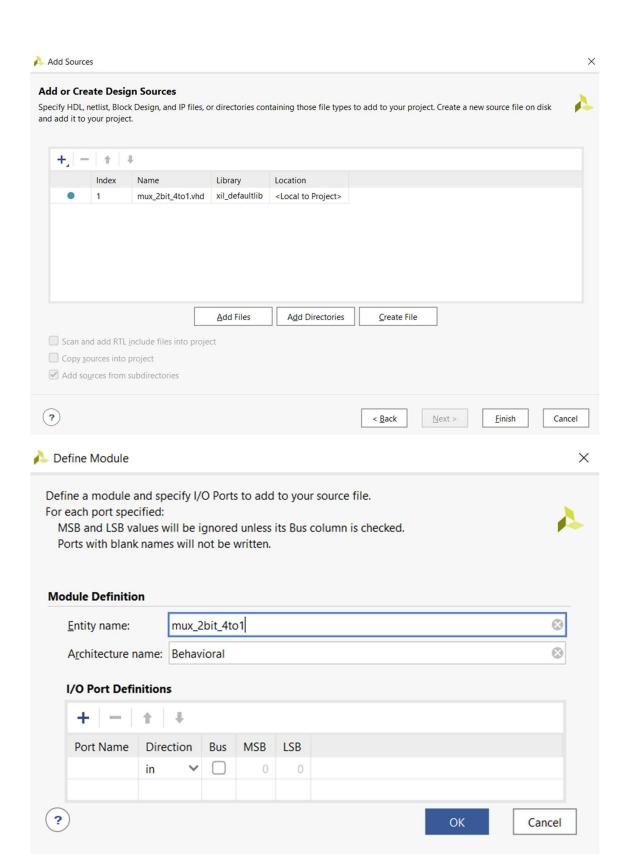


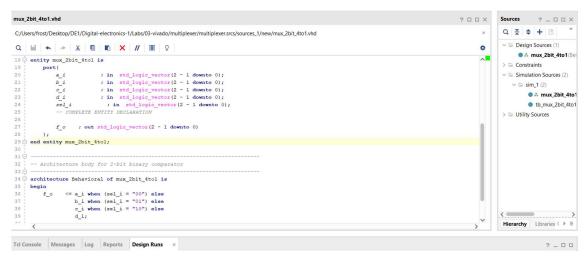
< Back

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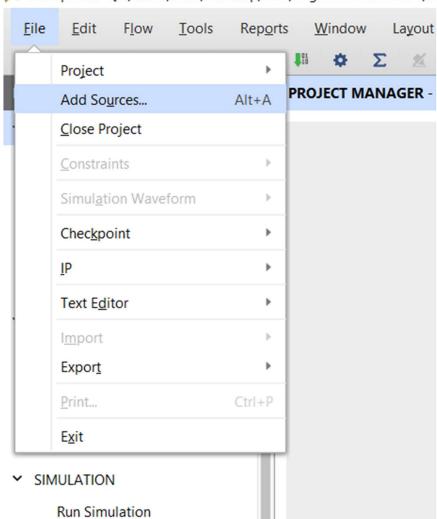
Cancel

?

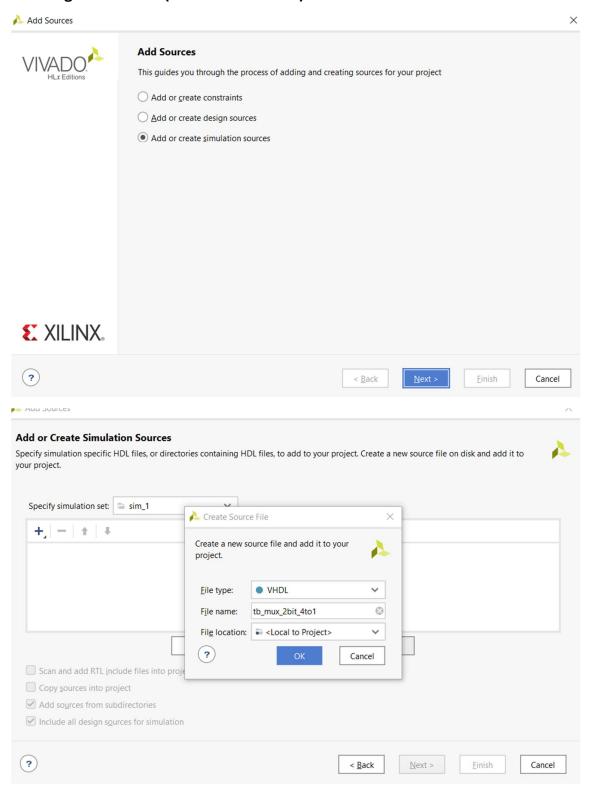


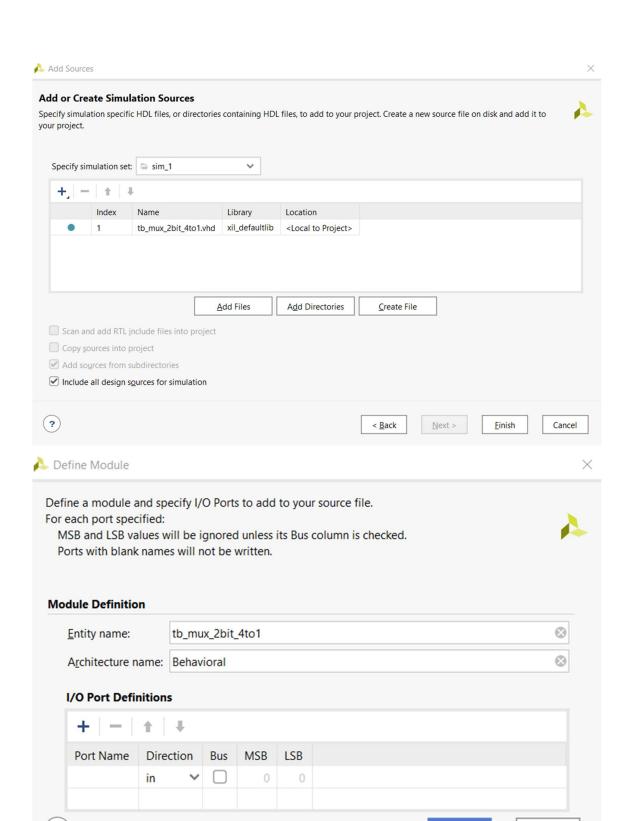


multiplexer - [C:/Users/frost/Desktop/DE1/Digital-electronics-1/L



Creating new source (simulation source)





OK

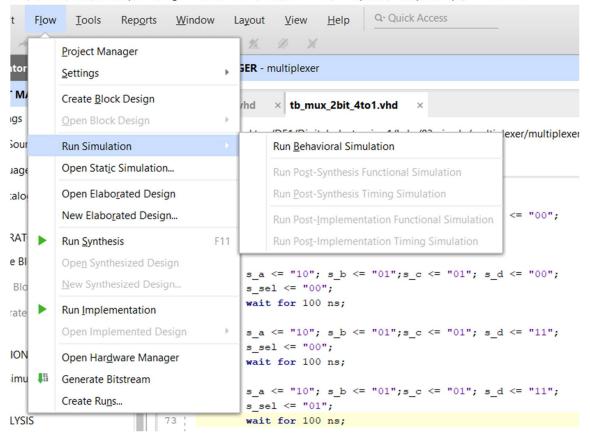
Cancel

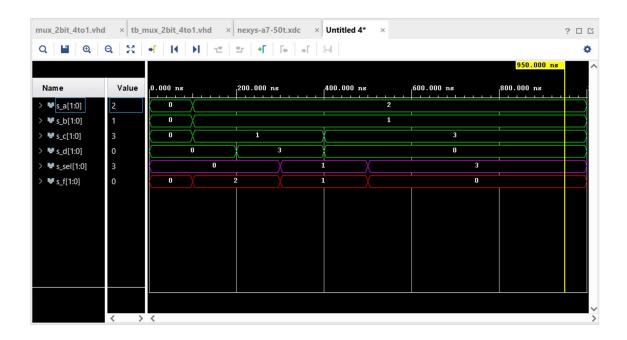
?

```
mux_2bit_4to1.vhd × tb_mux_2bit_4to1.vhd * ×
                                                                                                                                                                                                               ? 🗆 🖸
C:/Users/frost/Desktop/DE1/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.srcs/sim\_1/new/tb\_mux\_2bit\_4to1.vhd
 Q 🕍 🛧 🥕 🐰 🖺 🗈 🗙 // 🖩 🗘
                                                                                                                                                                                                                     Ф
                                                                                                                                                                                                                     ^
 27
28
29
30
              -- Local signals
                                  : std_logic_vector(2 - 1 downto 0);
: std_logic_vector(2 - 1 downto 0);
: std_logic_vector(2 - 1 downto 0);
              signal s_a
              signal s_b
signal s_c
 31
            signal s_d : std_logic_vector(2 - 1 downto 0);
signal s_sel : std_logic_vector(2 - 1 downto 0);
 32 <del>|</del>
34 si
35
36
37 begin
                                  : std_logic_vector(2 - 1 downto 0);
              signal s_f
 38 ∤
              --- Connecting testbench signals with comparator_2bit entity (Unit Under Test)
uut_mux_2bit_4tc1 : entity work.mux_2bit_4tc1
port map(
 40
41
42
43
                         t map(
a_i => s_a,
b_i => s_b,
c_i => s_c,
d_i => s_d,
sel_i => s_se,
                         a_i
b_i
c_i
 44
 45
                          f_o
 47 🖨
```

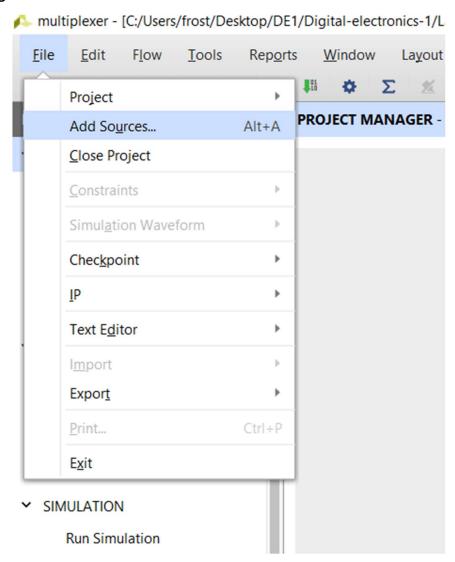
```
mux_2bit_4to1.vhd × tb_mux_2bit_4to1.vhd * ×
                                                                                                                                                                             ? 🗆 🖸
C:/Users/frost/Desktop/DE1/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.srcs/sim_1/new/tb_mux_2bit_4to1.vhd
 Q 🕍 🛧 🥕 🐰 🖺 🛍 🗶 // 🖩 🗘
                                                                                                                                                                                  ^
58
59
60
               -- First test values
s_a <= "00"; s_b <= "00"; s_c <= "00"; s_d <= "00";
s_sel <= "00";
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
               s_a <= "10"; s_b <= "01";s_c <= "01"; s_d <= "00";
s_sel <= "00";
                wait for 100 ns;
               s_a <= "10"; s_b <= "01";s_c <= "01"; s_d <= "11";
                s_sel <= "00";
               wait for 100 ns;
               s_a <= "10"; s_b <= "01";s_c <= "01"; s_d <= "11";
s_sel <= "01";
                wait for 100 ns;
                s_a <= "10"; s_b <= "01";s_c <= "11"; s_d <= "00";
                s_sel <= "01";
wait for 100 ns;
```

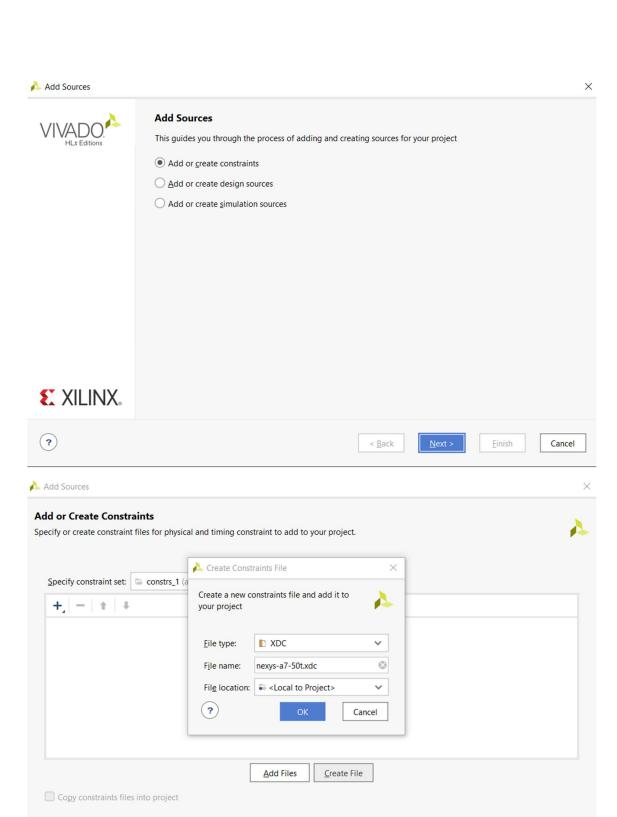
er - [C:/Users/frost/Desktop/DE1/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.xpr] - Vivado 2020.2





Creating new constrain





< <u>B</u>ack

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