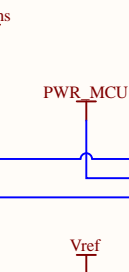
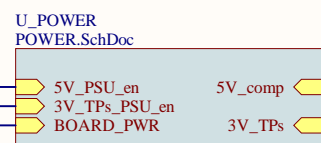


# SYSTEM TOP LEVEL VIEW

MUX_D_6	1	1	2	MUX_D_7
NMOS_SHFT_6TO10_SER	3	3	4	MUX_D_8
NMOS_SHFT_6TO10_NOE	5	5	6	MUX_D_9
NMOS_SHFT_6TO10_RCLK	7	7	8	MUX_D_10
NMOS_SHFT_6TO10_SRCLK	9	7	8	MUXes_6TO10_nEN
NMOS_SHFT_6TO10_SRCLR	11	9	10	MUXes_6TO10_A0
PMOS_SHFT_6TO10_SER	13	11	12	MUXes_6TO10_A2
PMOS_SHFT_6TO10_NOE	15	13	14	MUXes_6TO10_A1
PMOS_SHFT_6TO10_RCLK	17	15	16	5V_en
PMOS_SHFT_6TO10_SRCLK	19	17	18	3V_en
PMOS_SHFT_6TO10_SRCLR	21	19	20	BOARD_PWR
MUX_D_5	23	21	22	5V_comp
MUX_D_4	25	23	24	3V_TPs
MUX_D_3	27	25	26	
MUX_D_2	29	27	28	
MUX_D_1	31	29	30	
MUXes_1to5_A0	33	31	32	
MUXes_1to5_nEN	35	33	34	
MUXes_1to5_A1	37	35	36	
MUXes_1to5_A2	39	37	38	
NMOS_SHFT_1TO5_NOE	41	39	40	
NMOS_SHFT_1TO5_SER	43	41	42	PMOS_SHFT_1TO5_SRCLR
NMOS_SHFT_1TO5_RCLK	45	43	44	PMOS_SHFT_1TO5_SRCLK
NMOS_SHFT_1TO5_SRCLK	47	45	46	PMOS_SHFT_1TO5_RCLK
NMOS_SHFT_1TO5_SRCLR	49	47	48	PMOS_SHFT_1TO5_NOE
	49	49	50	PMOS_SHFT_1TO5_SER

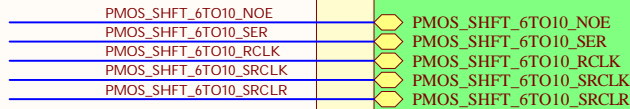
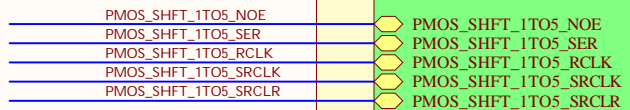
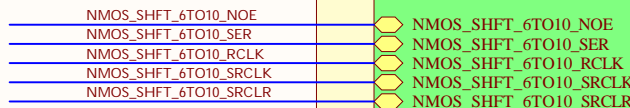
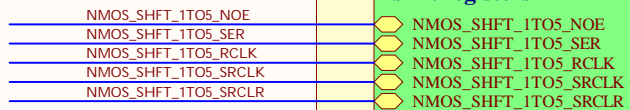
87833-5019



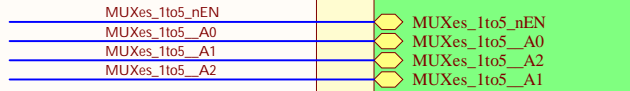
U\_ALL\_channels  
ALL\_channels.SchDoc

## Analog Frontend

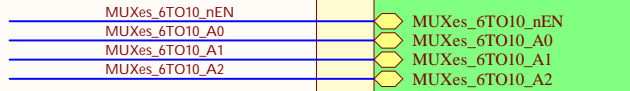
### shift registers



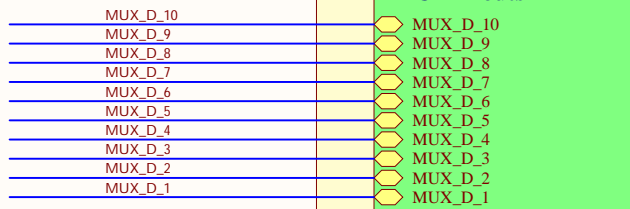
### MUX for channels 1-5



### MUX for channels 6-10



### MUX- Douts



## Power

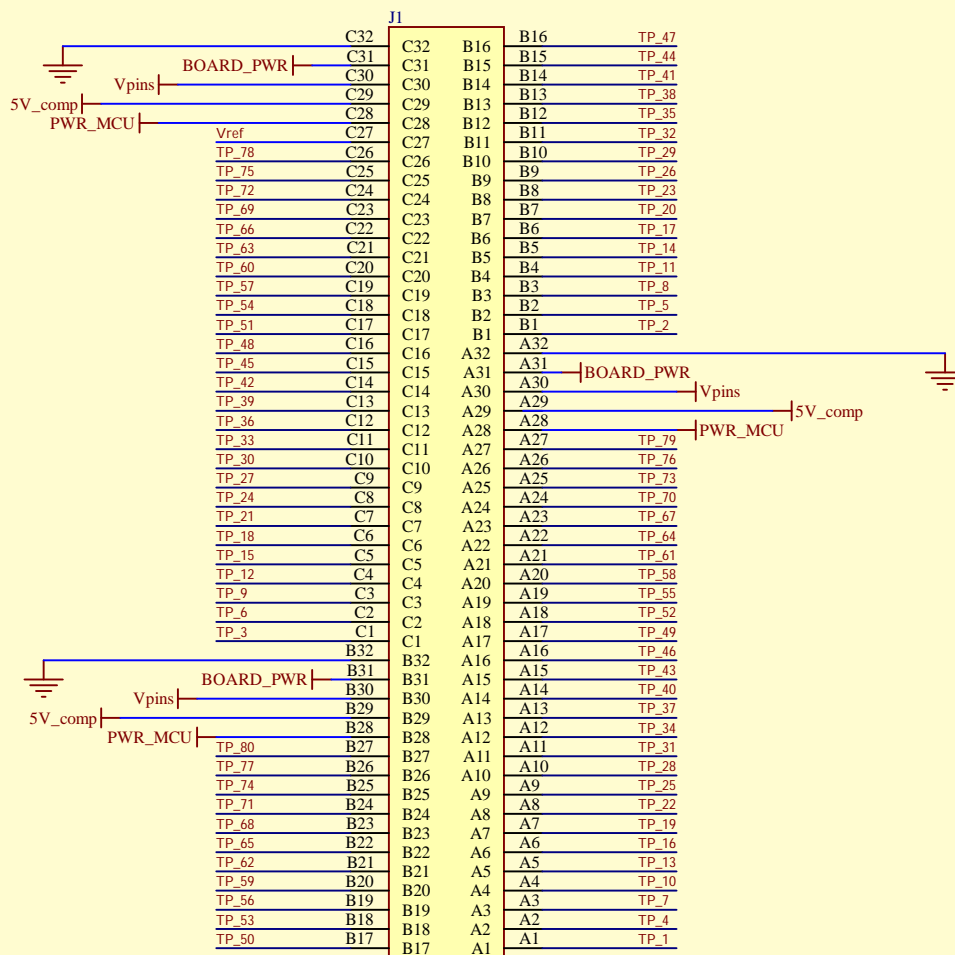
### reference (DAC)



## RESISTANCE MEASUREMENTS

### ANALOG MODULE CONTROLLED BY MUXES AND SHFT REGISTERS + 96PIN connector

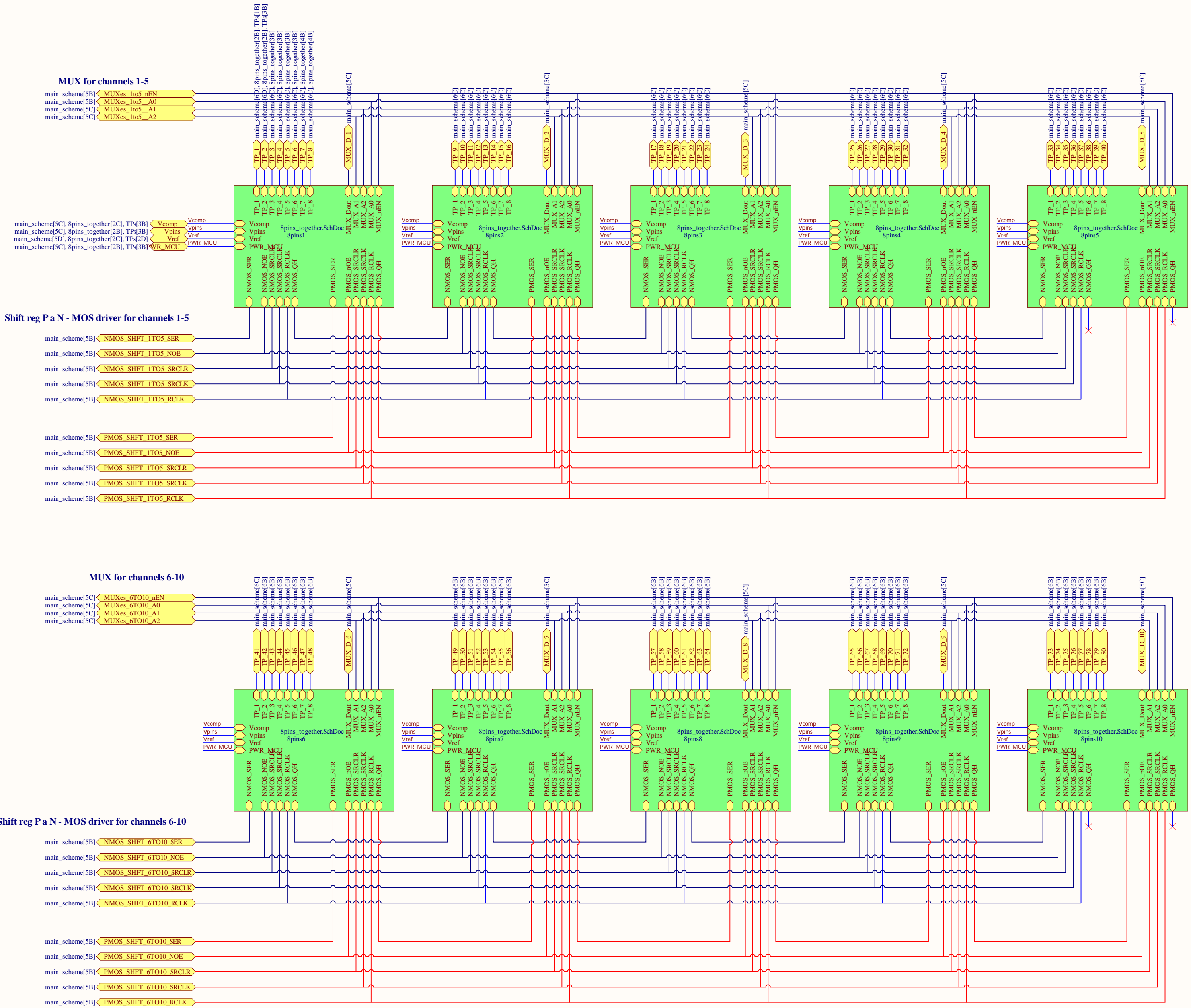
### Connector (80 TPs)



HARTING 96 PIN 3 rows

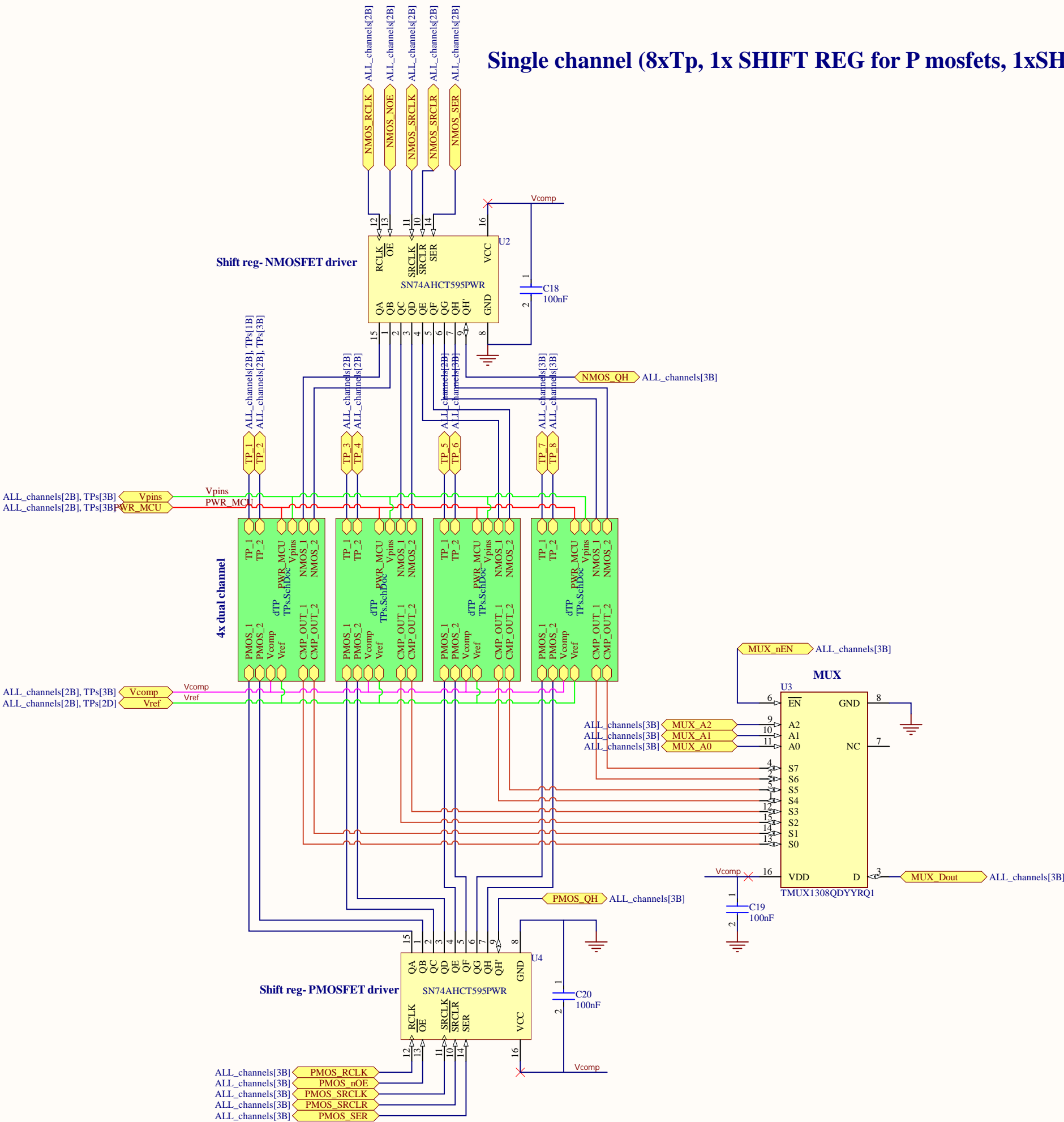
Title		
Size	Number	Revision
A2		
Date:	2.27.2023	Sheet of
File:	C:\Users\main_scheme.SchDoc	Drawn By:

ALL 80 pins - controlled by 2x5 (for P and N MOSFETS) + 2x5MUXES



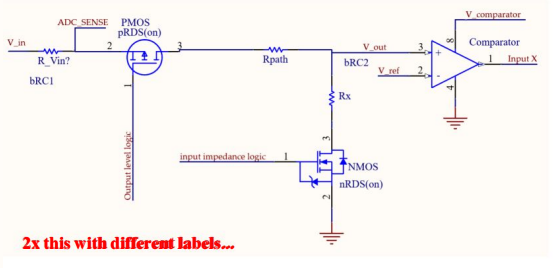
Title		
Size	Number	Revision
A2		
Date:	2.27.2023	Sheet of
File:	C:\Users\... \ALL_channels.SchDoc	Drawn By:

Single channel (8xTp, 1x SHIFT REG for P mosfets, 1xSHIFT REG for Nmosfets, 1X MUX)

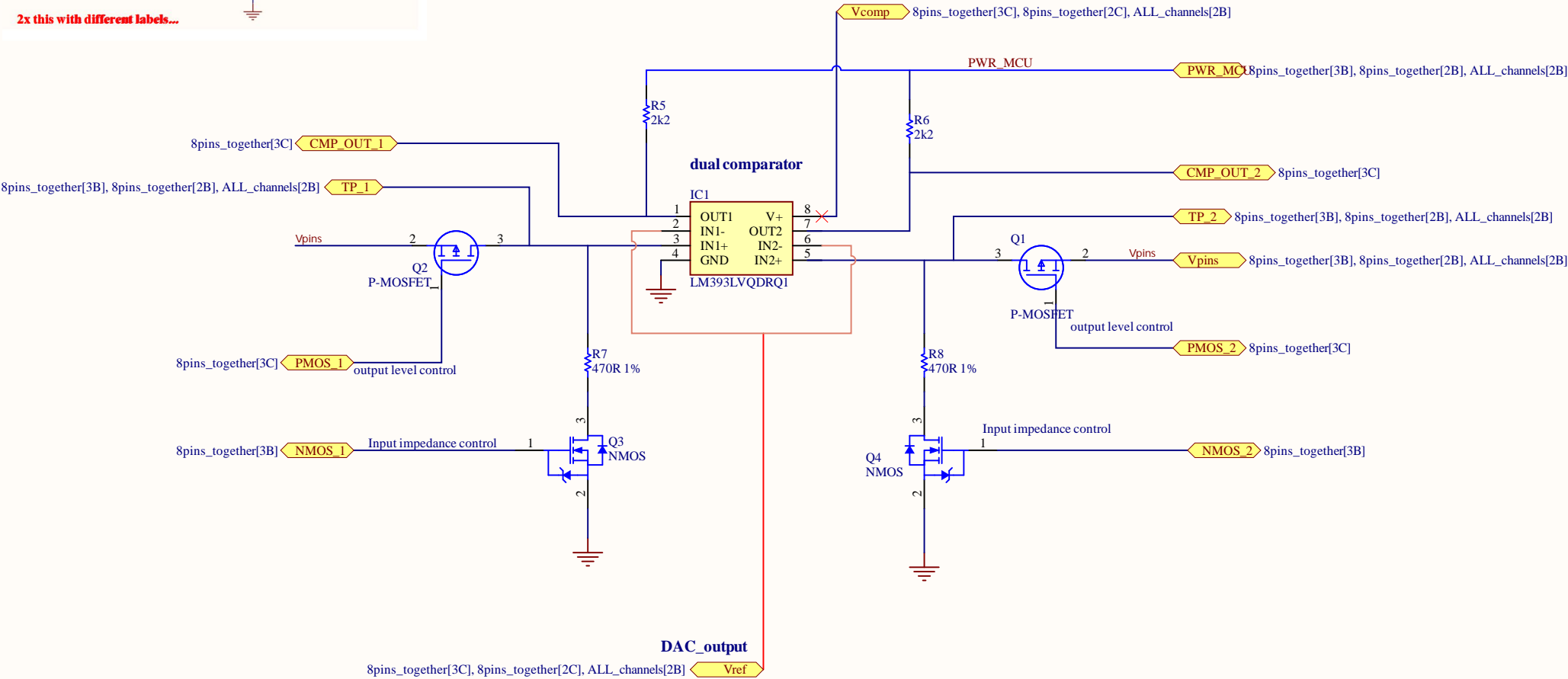


Title		
Size	Number	Revision
A3		
Date:	2.27.2023	Sheet of
File:	C:\Users\...\8pins_together.SchDoc	Drawn By:

Analog frontend for 2 channels (dual comparator with P and N MOSFETS)



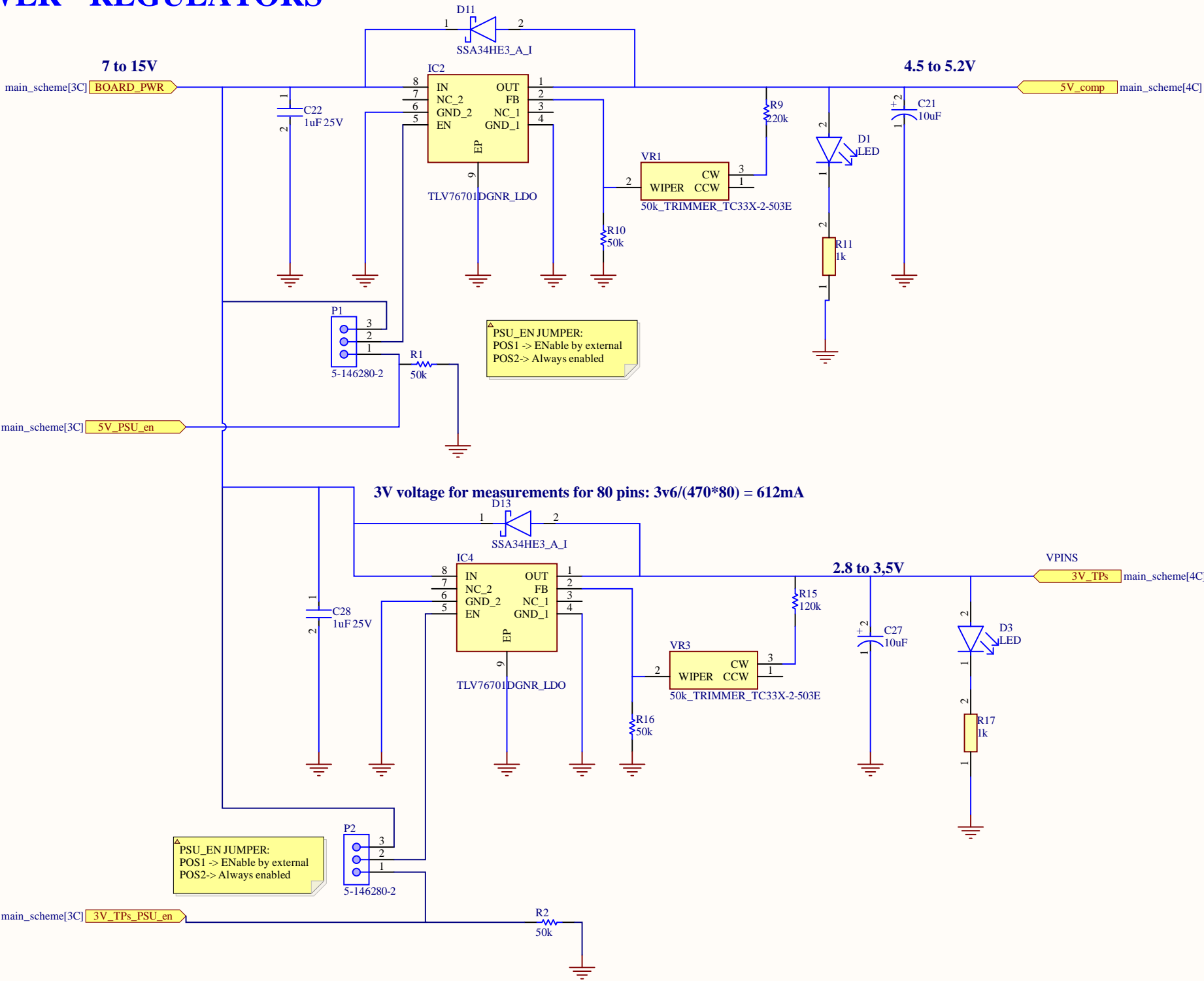
2x this with different labels...



Title		
Size	Number	Revision
A4		
Date:	2.27.2023	Sheet of
File:	C:\Users\...\TPs.SchDoc	Drawn By:

# POWER - REGULATORS

$R1 = (V_{out}/0.8-1)*R2$  ;  $R2 = 50k\Omega$   
5V : shfregs/comps/mux - (Worst case cca 440mA)



Title		
Size	Number	Revision
A3		
Date:	2.27.2023	Sheet of
File:	C:\Users\...\POWER.SchDoc	Drawn By: