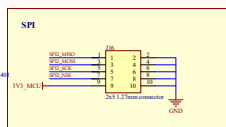
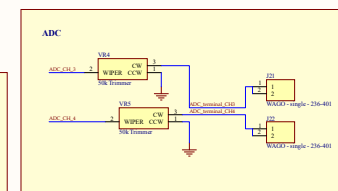
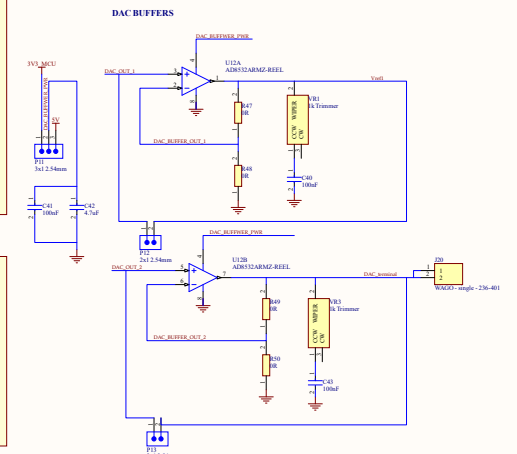
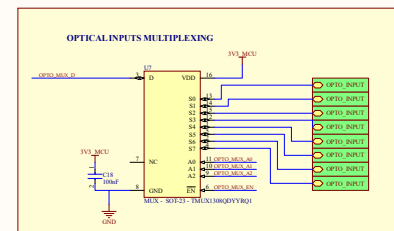
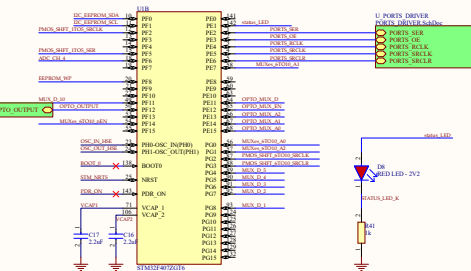
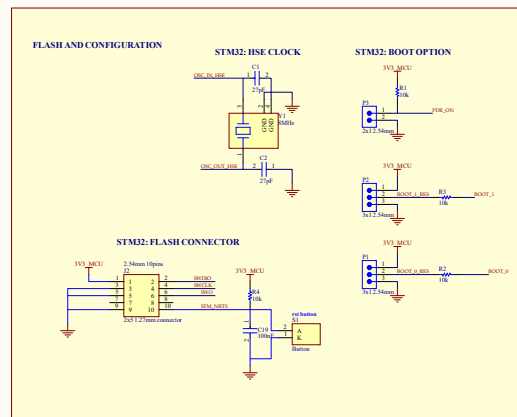
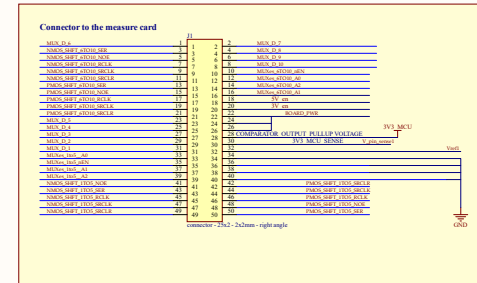
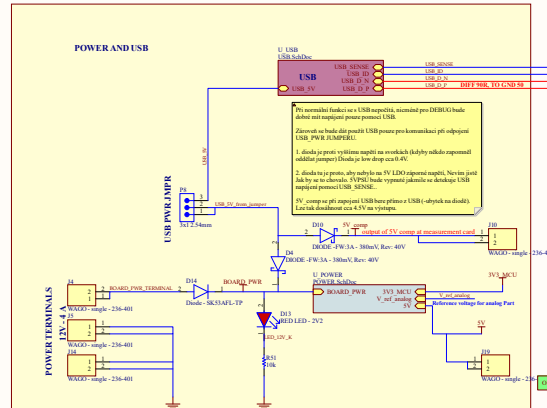
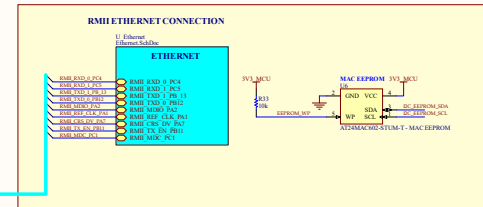
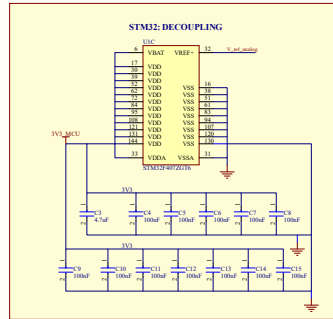
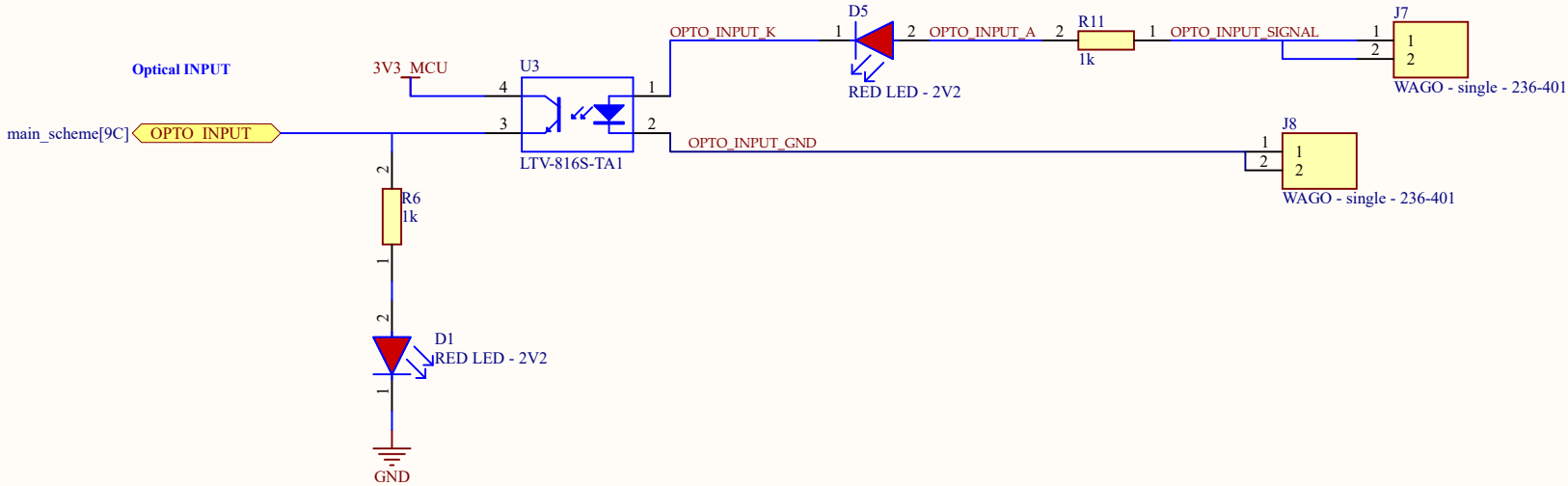


SYSTEM TOP LEVEL VIEW



Title		
Rev	Number	Revision
Rev A1	1	1
Rev A1	1	1
Rev A1	1	1
Rev A1	1	1

OPTICAL INPUT



Title		
Size A4	Number	Revision
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File:	C:\PROJECTS\...\Opto inputs.SchDoc	Drawn By:

The image contains two circuit diagrams for 3V3 MCU and peripheral power regulation. Both diagrams use a 1A LDO (TLV76701DGNR) and a 5k trimmer (VR2/VR6) to regulate the output voltage. The top diagram is for a 2.8 to 3.5V output, while the bottom diagram is for a 4.4 to 5.2V output. Both diagrams include a 1A LDO, a 5k trimmer, and various passive components like capacitors, resistors, and inductors. The top diagram also includes a 3V3 MCU and a 3V3 MCU peripheral power source. The bottom diagram includes a 5V MCU peripheral power source. The diagrams are labeled with component values and names, and include a title for each circuit.

3v3 MCU and peripheral POWER (worst case cca 650mA)

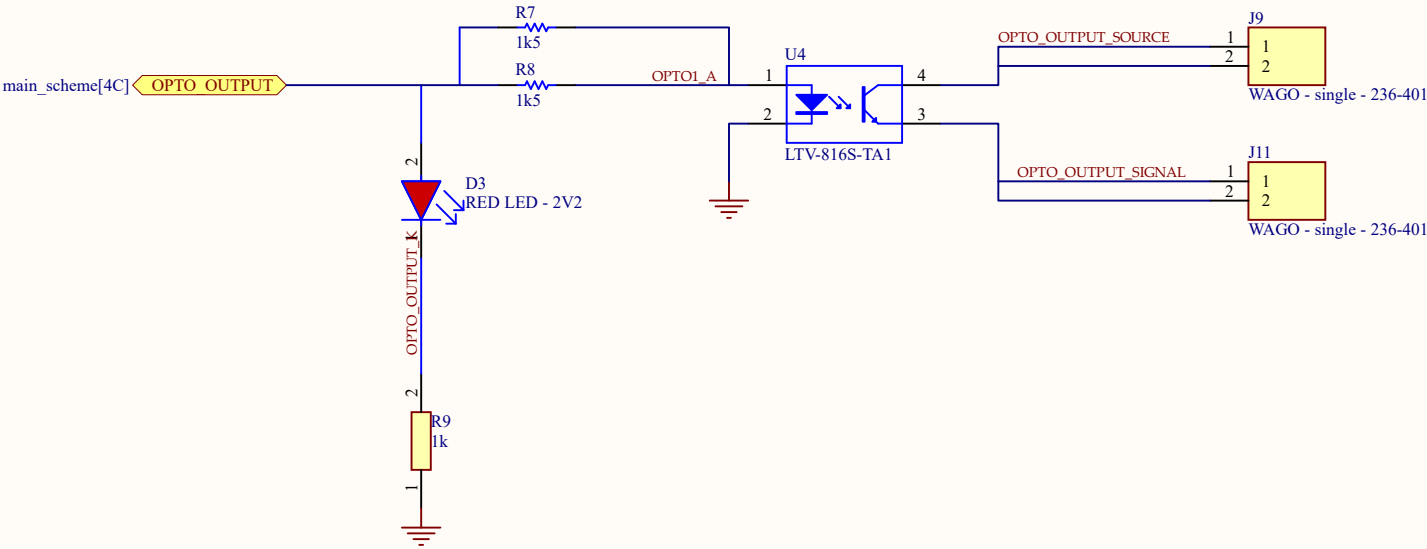
2.8 to 3,5V

3v3 MCU and peripheral POWER (worst case cca 650mA)

4.4 to 5.2V

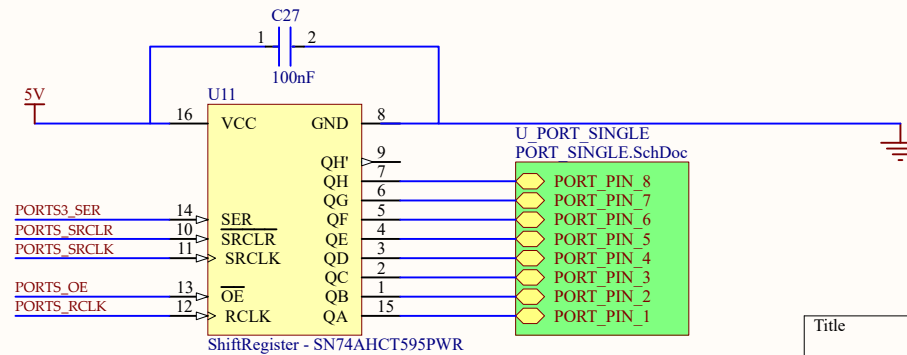
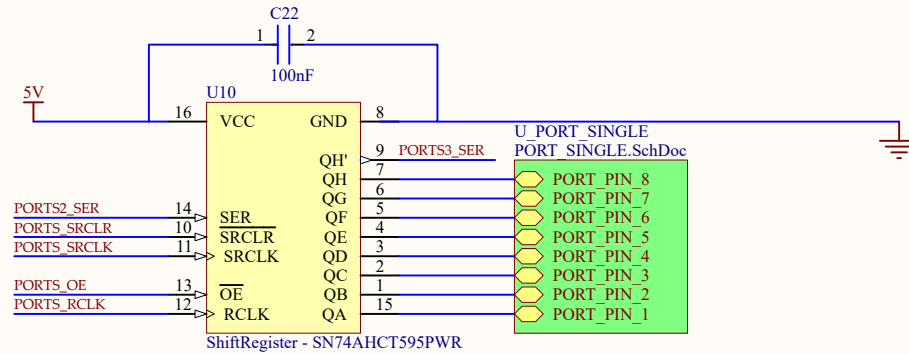
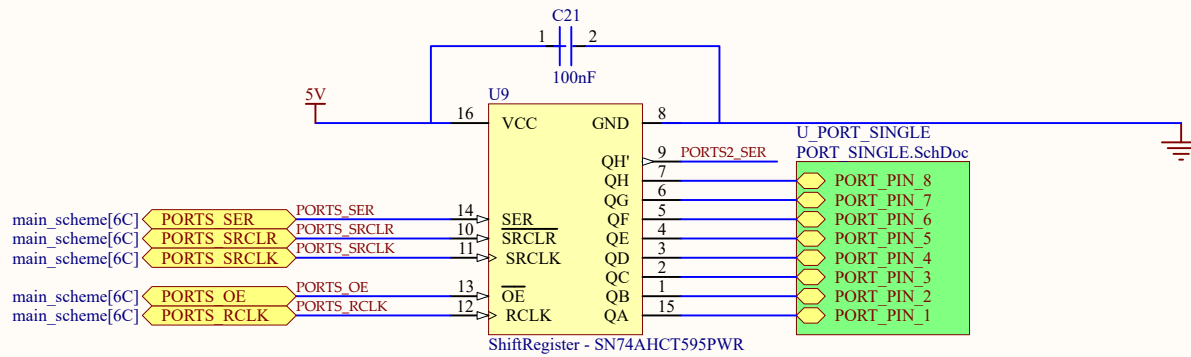
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Optical Output



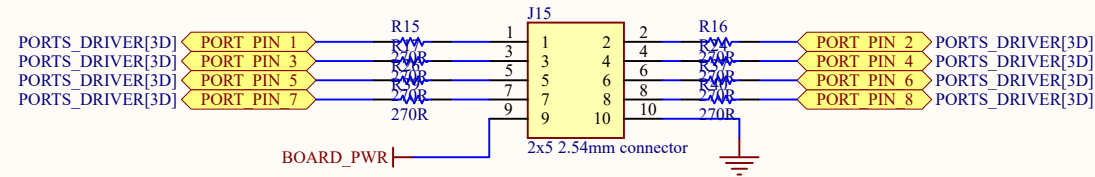
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EXT PORTS



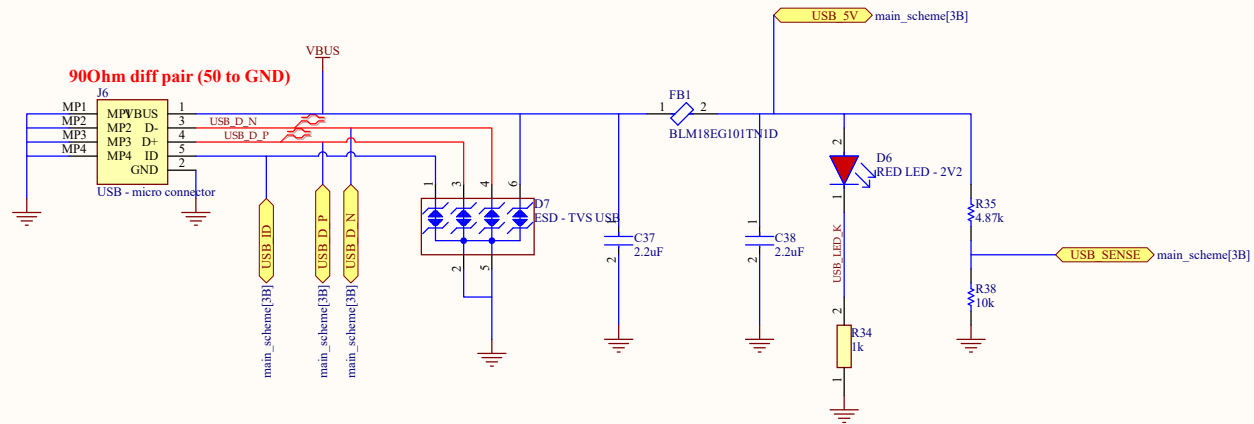
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SINGLE EXT PORT CONNECTOR



Title		
Size A4	Number	Revision
Date:	5.07.2023	Sheet of
File:	C:\PROJECTS\...\PORT_SINGLE.SchDoc Drawn By:	

USB



Title		
Size A3	Number	Revision
Date:	5.07.2023	Sheet of
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