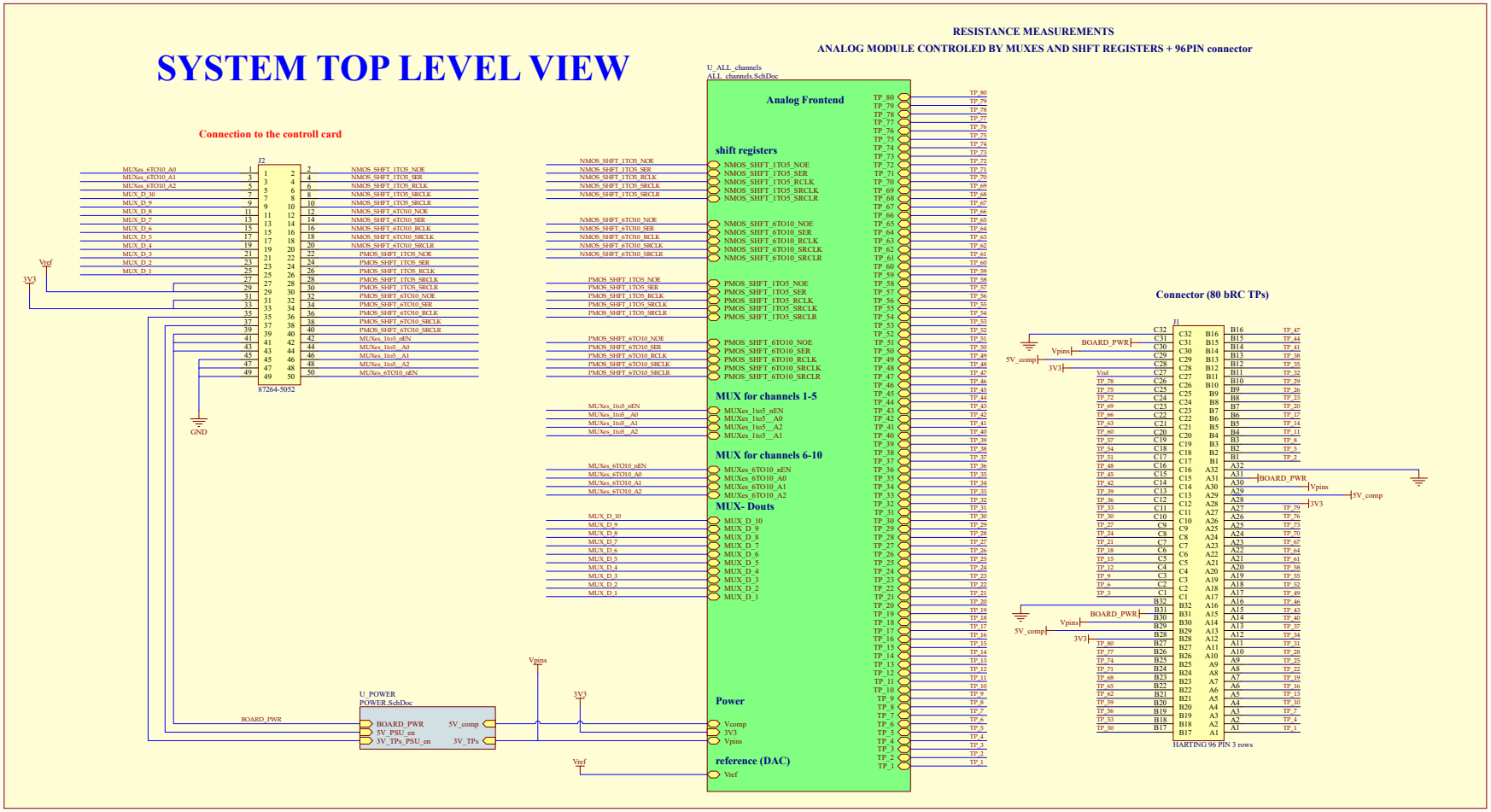
SYSTEM TOP LEVEL VIEW

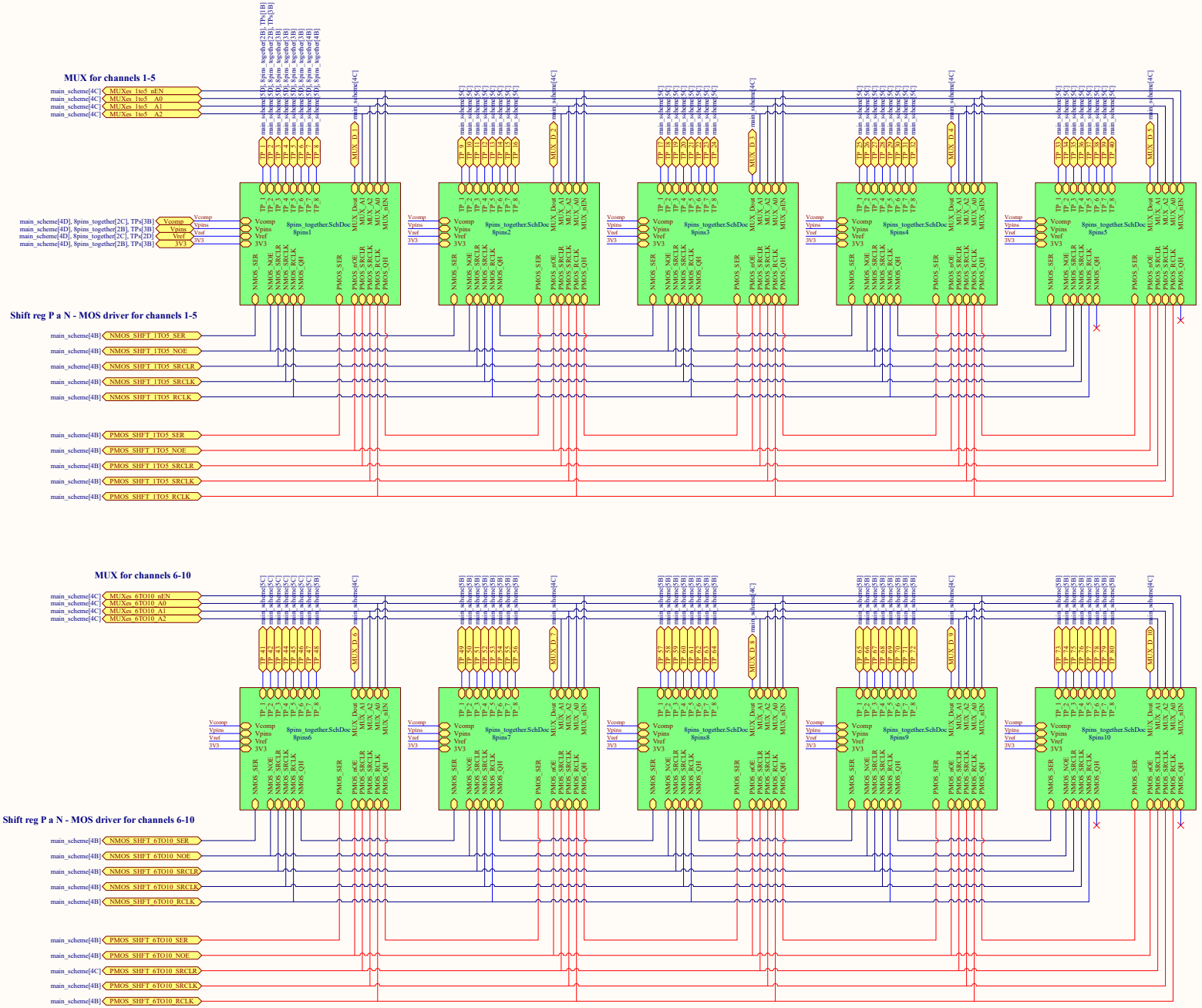
RESISTANCE MEASUREMENTS

ANALOG MODULE CONTROLED BY MUXES AND SHFT REGISTERS + 96PIN connector



Title			
Size: A2	Number		Revision
Date: 12.08.2022		Sheet of	
File: C:\Users\...\main_scheme.SchDoc		Drawn By:	

ALL 80 pins - controlled by 2x5 (for P and N MOSFETS) + 2x5MUXES



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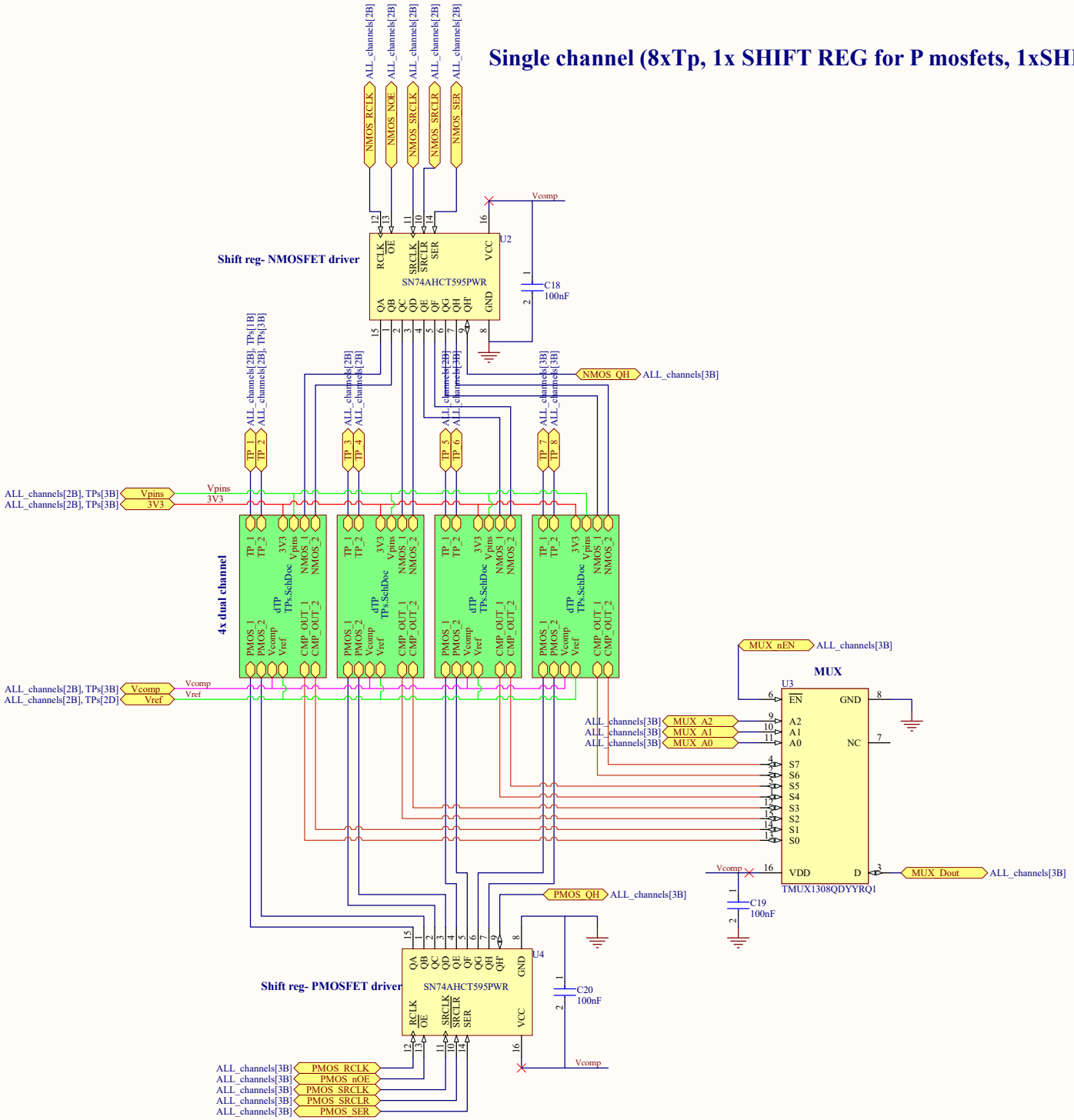
Date: 12.08.2022		Sheet of
File: C:\Users\...\ALL_channels.SchDoc		Drawn By:

Single channel (8xTp, 1x SHIFT REG for P mosfets, 1xSHIFT REG for Nmosfets, 1X MUX)



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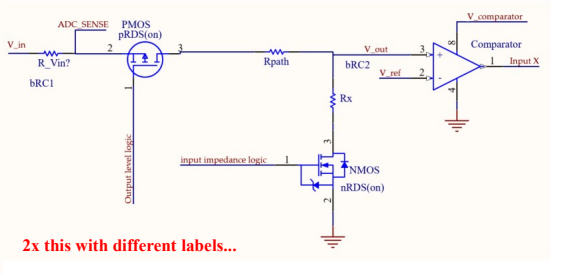
File: C:\Users\...\8pins_together.SchDoc		Drawn By:

Analog frontend for 2 channels (dual comparator with P and N MOSFETS)



2x this with different labels...

Vcomp 8pins_together[3C], 8pins_together[2C], ALL_channels[2B]

3V3 — 3V3 8pins_together[3B], 8pins_together[2B], ALL_channels[2B]

R5 2k2 — R6 2k2

8pins_together[3C] CMP_OUT_1 — CMP_OUT_2 8pins_together[3C]

8pins_together[3B], 8pins_together[2B], ALL_channels[2B] TP_1 — TP_2 8pins_together[3B], 8pins_together[2B], ALL_channels[2B]

dual comparator

IC1

1	OUT1	V+	8
2	IN1-	OUT2	7
3	IN1+	IN2-	6
4	GND	IN2+	5

LM393LVQDRQ1

Vpins — Q2 P-MOSFET — Q1 P-MOSFET — Vpins 8pins_together[3B], 8pins_together[2B], ALL_channels[2B]

output level control

8pins_together[3C] PMOS_1 — PMOS_2 8pins_together[3C]

R7 470R 1% — R8 470R 1%

8pins_together[3B] NMOS_1 Input impedance control — Q3 NMOS — Q4 NMOS — Input impedance control NMOS_2 8pins_together[3B]

DAC_output

8pins_together[3C], 8pins_together[2C], ALL_channels[2B] Vref

Title		
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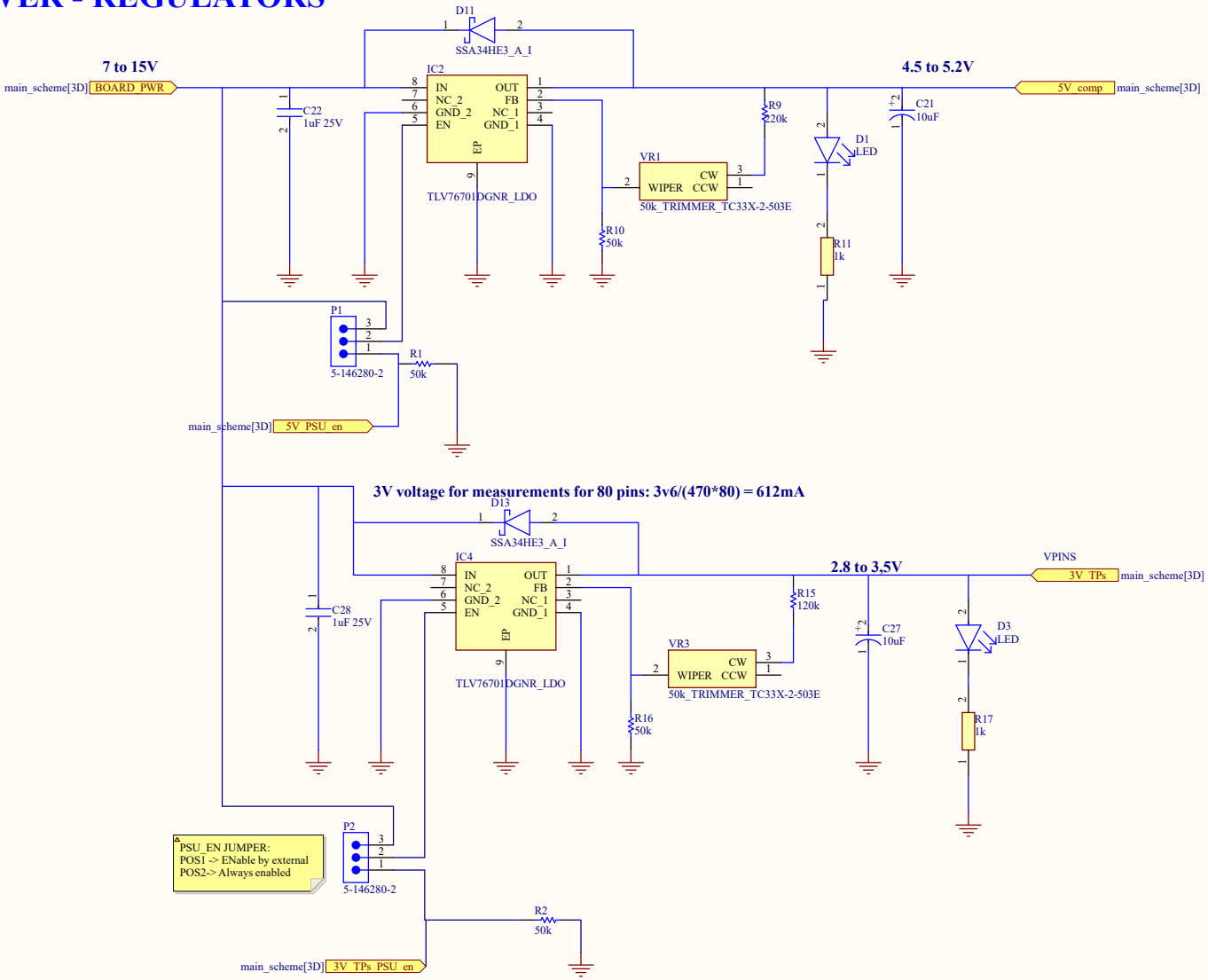
File: C:\Users\..\TPs.SchDoc		Drawn By:

POWER - REGULATORS

R1 = (Vout/0.8-1)*R2 ; R2 = 50kR
5V : shfregs/comps/mux - (Worst case cca 440mA)



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Date: 12.08.2022		Sheet of
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