

Filippo Moro

Research Scientist

Building intelligent systems





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EXPERIENCE

2023 - PRESENT POSTDOC

INI - Zurich, Switzerland

As a Postdoctoral researcher, I contribute to Melika Payvand's group co-developing integrated hardware and algorithms for edge computation. The goal is to design and fabricate a chip that is energy-efficient, computationally powerful, and capable of learning online. Part of my job is supervising 3 Ph.D. students, as well as contributing to the main Lab project both on the algorithms and hardware sides.

• 2019 - 2023 PHD STUDENT CEA Leti - Grenoble. France

My project focuses on biology-inspired sensing and computation, making use of analog, memristive-based electronics. I thus have experience with machine learning, designing analog circuits, electrical characterization of memristors, and analog circuits. My interests led me to take courses on Machine Learning and Deep Learning. I worked in collaboration with Melika Payvand and Giacomo Indiveri from INI (ETH/UZH) and Jerome Casas (Université Tours) while being supervised by Elisa Vianello (CEA Leti).

• 2019 MASTER THESIS ETH/UZH - Zurich, Switzerland

During my 6 months in Zürich, I worked on biologically plausible, memristive-enhanced Reservoir Computing. I built a Recurrent network featuring two plasticity mechanisms, Spike-Driven Synaptic Plasticity, and Intrinsic Plasticity, showing that their implementation on memristive devices leads to improvements in performance.

EDUCATION

• 2019-2023 PHD DEGREE Université Grenoble Alpes - Grenoble, France

Degree in Electronic Engineering

• 2017-2019 MASTER OF SCIENCE Politecnico di Torino - Turin, Italy

Degree in Nanotechnologies for ICT, 110L/110

• 2014-2017 **BACHELOR'S DEGREE** Politecnico di Torino - Turin, Italy

Degree in Physical Engineering

SKILLSET

LANGUAGES:

- Italian (mother tongue)
- English (proficient)
- French (proficient)
- German (basic)

INFORMATICS:

- Python (proficient) DL libraries: Pytorch, Keras, JAX
- Matlab (basic)
- C/C++ (basic)
- Experience with GPU clusters

ENGINEERING:

- Cadence-Virtuoso (intermediate)
- SPICE (intermediate)
- 4 Tapeouts experience