Report 04

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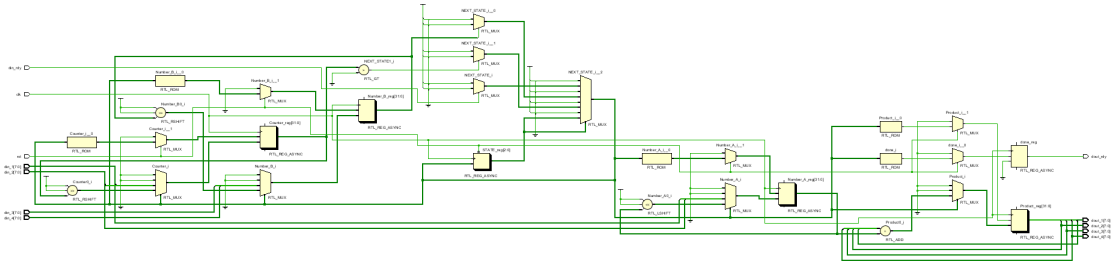
1 Schematics comparison

1.1 Verilog

The number of Nets after the logic synthesis process is almost halved, in fact it goes from `633` in the non-synthesized design, to `361`.

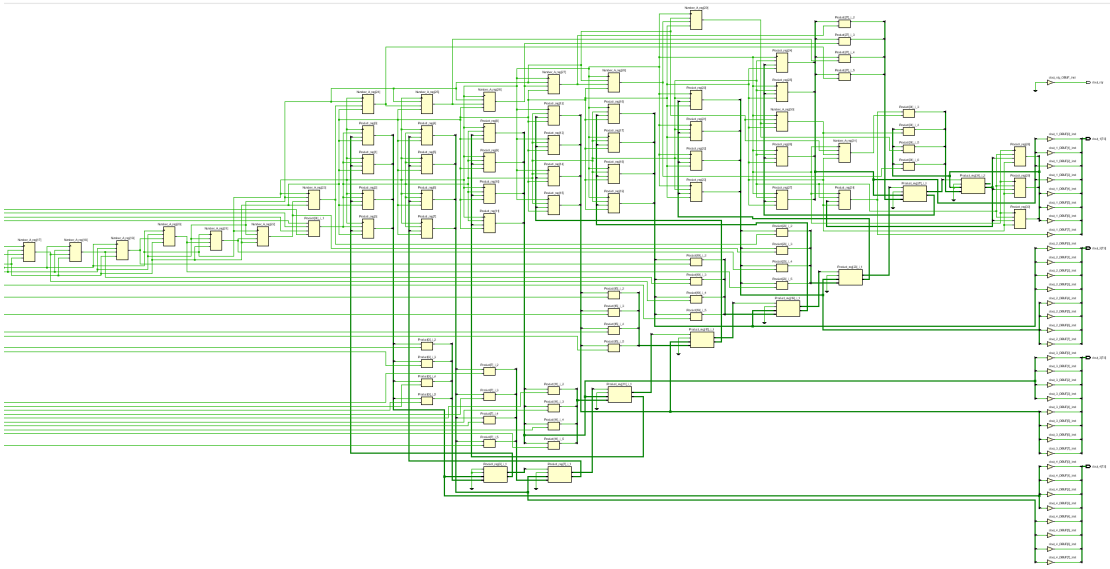
On the other hand, then number of Cells increases from `155` to `269`.

The following image represents the schematics before the synthesis:



While the following image is a partial view of the schematics of the synthesized design.

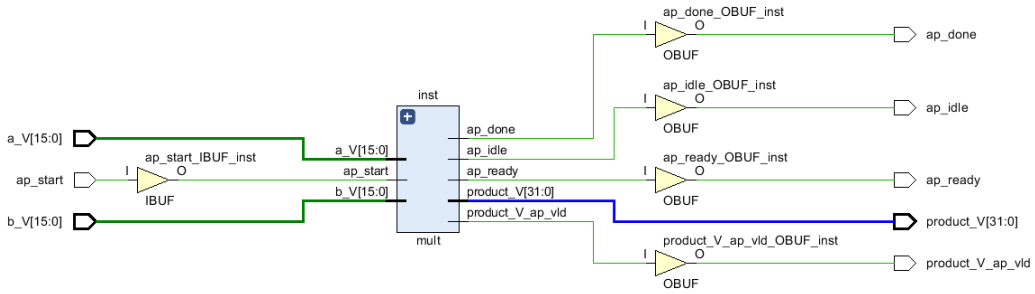
This is the final part of the circuit, in which we can see the carry logic, some of the internal registers LUTs and the output pins. In the unseen part, there are the input pins and the other components that manage the registers.



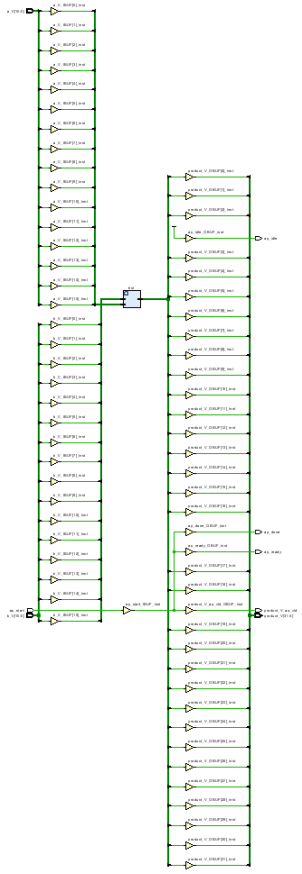
1.2 C++

The number of Nets before computing the synthesis is 74, while after it they are 135. The number of Cells goes from 6 to 70.

This is the schematics before the synthesis:



And this is the schematics after the process:



2 Reports

2.1 Verilog

The **timing** summary reports:

- *Worst Negative Slack*: `4.616 ns`
- *Worst Hold Slack*: `0.070 ns`

These values indicate that the circuit is behaving in a correct way: the output is consistent and the design doesn't have any violation.

Considering the **power**, the reported values are:

- *Total On-Chip Power*: `0.124 W`
- *Junction Temperature*: `26.4°C`

Which are positive values, because the circuit is not overheating nor consuming an excessive amount of power.

Finally, the **usage** values are well below the limit:

- LUT: `0.15%`
- FF: `0.09%`
- I/O: `54.40%`

2.2 C++

Vivado HLS has produced a combinational circuit, which is not clock-dependant because its internal values are only based on the current input signals. For this reason, there isn't a clock signal that can be used to run implementation tests. The only reasonable value that can be observed reading the same reports as for the Verilog synthesized implementation is the **I/O utilization**, which is at `55.20%`.