Report 08

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1 Wrapping the Root module

In order to wrap the Root module, I created a VHDL wrapper (it could be implemented in Verilog as well) which maps the wires of the Root to the AMBA bus ones. Then, in the `top_level.v` file, I had to define Root as the peripheral number 3 (the first is the Multiplier and the second is the I/O Module), by defining the **wires** in the Memory Bus Interface, linking them to the `amba_apb_bus` instance and finally creating an instance of the wrapper in which I linked the peripheral wires to the ones of the wrapper.

1.1 Mapping the signals

From the BUS to Root:

- `pclk` is mapped to **clk**;
- `presetn` is mapped to **rst**;
- `penable` is mapped to **din_rdy**;
- `pwdata` is mapped to **din**.

From Root to the BUS:

- **dout** is mapped to `prdata`;
- **pready** is mapped to `pready`.

1.2 Root FSM

The FSM would originally restart the computation from **ST_0** after reaching the final state **ST_4** and setting `dout_rdy` to 1. This was a problem because the testbench couldn't read the output value, so its `dout` and `dout_rdy` signals wouldn't show the results from Root.

To fix this problem, I created an additional state **ST_5** that does nothing; this way `dout` and `dout_rdy` can have the output values for a time long enough so that the testbench can read them.

The FSM will restart only when the `rst` signal goes to 0. This operation is done each time the driver calls the *root* function from the **routines.c** file.

2 Writing the driver

To write the C driver I had to add a new function to the `routine` library. Its signature is:

```
uint32_t root(uint8_t op1, uint8_t op2, uint8_t op3, uint8_t op4);
```

and it is very similar to the **multiplication** routine, but it has some differences: first of all, it uses `set_pwdata_8`, since there are four 8-bit operands; then it enables the peripheral number 3, which is Root; finally it has to rise to 1 the `presetn` signal, otherwise the FSM won't start because it will stay in a perpetual reset state.