

# Parallel Computer Systems, Fall 2022

## Instructions for Databar Exercise 1:

### Cache Performance

September 2, 2022

## 1 Introduction

In this databar exercise, you will explore cache performance and how program behavior affect cache performance. You will also explore performance optimization and the use of SIMD instructions. You will use the HPC computing facilities at DTU.

You will report on this exercise as part of the first report. You will there write at most one page about your experiences and findings. NB: You will write more in the first report than the outcome of this exercise.

You also need to use the report template pointed to by the `course_documentation.pdf` document.

**Read through this document in entirely before starting working on the exercises!**

## 2 Learning objectives

During this assignment you will be working towards the following learning objectives:

- You can demonstrate with pseudo code how the memory access pattern of a program can greatly influence cache performance.
- Carry out empirical performance evaluations.
- Use SIMD instructions to write data parallel programs.
- You can write down in text and in your own words definitions or explanations of the following concepts: data parallel model; speedup; parallel efficiency.

### 3 Reports and rules

DTU has a zero tolerance policy on cheating and plagiarism. This also extends to the reports and indeed all your work. For example, to copy text passages from someone else without clearly and properly citing your source is considered plagiarism. You are assumed to stay informed of and follow DTU's rules.

### 4 Reference material

Before carrying out the exercise read chapter 1 in Hager&Wellein.

### 5 Observing cache performance

Log on to the HPC machines using the guides at [http://www.cc.dtu.dk/?page\\_id=2501](http://www.cc.dtu.dk/?page_id=2501) and [http://www.cc.dtu.dk/?page\\_id=4354](http://www.cc.dtu.dk/?page_id=4354). The guide refers to the machines as the "LSF 10 Cluster". ThinLinc is probably the easiest way to access the machines from Windows. Please note the change on access options put into effect at DTU. VPN is needed for remotely accessing most DTU systems.

Remember to perform the last step of the guide and execute the `linuxsh` command.

Download `cachetest.c` from DTU Learn into the HPC machine using for example a web browser in the ThinLinc environment.

Study the code. What does it do? What does it print?

Compile and run the code by going to the directory where you downloaded `cachetest.c` and type:

```
gcc -O0 cachetest.c
./a.out
```

Why do you see the numbers you see? Relate the numbers to the memory system. Use the output to figure out the memory system of the HPC machine. For example, how many and how large caches does the machine have and how did you arrive at that? You may need to run the program multiple times if you see odd results.

#### 5.1 Reporting

You report your work, up until now, in the first mandatory report with up to half a page. You need to answer the two questions below.

How many and how large caches does the machine have and how did you arrive at that?

How do you need to write your programs to suit the memory hierarchy?

## 6 Working with SIMD instructions

We will use a lab from Berkeley: <http://www-inst.eecs.berkeley.edu/~cs61c/sp12/labs/08/>

The source codes mentioned are available at: <http://inst.eecs.berkeley.edu/~cs61c/fa11/labs/07/sseTest.c> and <http://inst.eecs.berkeley.edu/~cs61c/fa11/labs/07/sum.c>. You cannot use the direct copy command mentioned in the Berkeley instructions. You do not need to show your findings in exercise 1 to a TA. When coming to exercise 2 read through the exercise but do not perform the steps involving inspecting the assembly code. In exercise 3 you do not show your code to a TA.

**IMPORTANT:** Add the `-std=gnu99` option when compiling.

**IMPORTANT2:** Change `CLOCK_RATE_GHZ` in `sum.c` to `2.3e9`

**IMPORTANT3:** It is not important to spend a lot of time on browsing the available SIMD instruction. There a lot of them! Only spend about 5 minutes to get an impression about what instructions are available. Intel has information at <https://software.intel.com/sites/landingpage/IntrinsicsGuide/#>. Focus on SSE, SSE2, SSE3, SSE4.1 and SSE4.2.

Report on your findings and experiences working with SIMD instructions in exercise 3 and 4 in the first report with up to half a page. You upload, to the upcoming DTU Learn assignment, the source code you wrote as a zip file separately to your report. Your reflection on your findings is more important than that you have correct and working code.

**Your reports are individual. This also extends to the code you write. You must not share the code that you submit as part of assignments.**

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