CAPSTONE PROJECT

IBEX CORE VERIFICATION USING UVM

OPEN SOURCE 32-BIT RISC-V CPU CORE WRITTEN IN SYSTEMVERILOG

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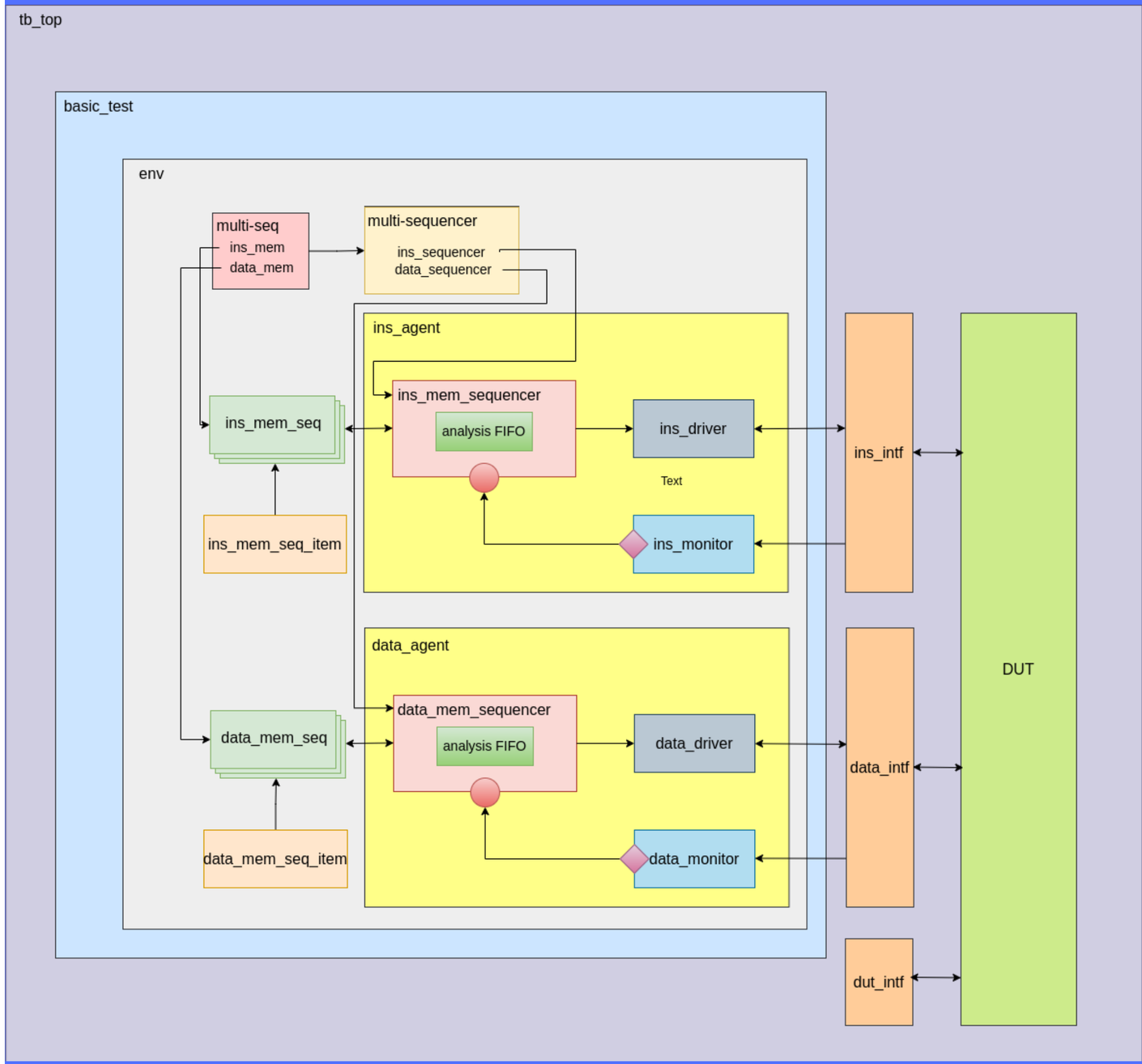
VERIFICATION ARCHITECTURE

- 2 AGENTS:
  INSTRUCTION FETCH
  LOAD STORE
- A VIRTUAL MULTI SEQUENCER IN ENV
- 3 INTERFACES



DESCRIPTION

1. *Core starts execution when fetch signal is send to DUT by DUT Interface.*
2. *INS & DATA Monitors read the respective outputs coming from DUT through INS & DATA Interfaces.*
3. *These outputs are written to Analysis ports which are connected to analysis FIFO of the respective Sequencers.*
4. *INS & DATA Sequences gets the item from the FIFO export port of INS & DATA Sequencers.*
5. *INS & DATA Drivers get the respective Sequences from the INS & DATA Sequencers and drive them onto the Interfaces towards DUT.*
6. *Test terminates as soon as ECALL is detected by INS Interface signal and fetch signal of DUT Interface is disabled.*

SANITY CHECKS

Simple Tests indicating correct working of verification environment

NOP
ECALL

INITIALIZE REGISTERS

LOAD
STORE

TEST CASES

R_TEST

I_TEST

JUMP

MIX_TEST

FACTORIAL

ARRAY

THANK YOU