Verification Plan

Test Id	Test Name	Test Status	Test Description	Stimulus Generation Procedure	Checking Procedure	Comments
1	GPIO_ch_1_all_input	PASS	checks for GPIO channel 1 pins configured as input	Following sequences are executed in order: -> AXI write direction at channel 1 -> GPIO input sequence -> AXI read data at channel 1	Direction of channel 1 pins is set as input thorough AXI interface. Then a gpio sequence with input at channel 1 is executed through GPIO interface. Then the data at channel 1 is verified by reading through AXI interface.	It ensures that if the channel pins are configured as input, then the data obtained from reading these pins must be the input data passed to GPIO
2	GPIO_ch_1_all_output	PASS	checks for GPIO channel 1 pins configured as output	Following sequences are executed in order: -> AXI write direction at channel 1 -> AXI write data at channel 1 -> AXI read data at channel 1	Direction of channel 1 pins is set as output thorough AXI interface. Then a data is written to channel 1 through AXI interface that appears at GPIO channel 1 output. Then the data at channel 1 is verified by reading through AXI interface.	It ensures that if the channel pins are configured as output, then the data obtained from reading these pins must be the data that is written on to these pins thorugh AXI and is output of GPIO
3	GPIO_ch_2_all_input	PASS	checks for GPIO channel 2 pins configured as input	Following sequences are executed in order: -> AXI write direction at channel 2 -> GPIO input sequence -> AXI read data at channel 2	Direction of channel 2 pins is set as input thorough AXI interface. Then a gpio sequence with input at channel 2 is executed through GPIO interface. Then the data at channel 2 is verified by reading through AXI interface.	Same as 1
4	GPIO_ch_2_all_output	PASS	checks for GPIO channel 2 pins configured as output	Following sequences are executed in order: -> AXI write direction at channel 2 -> AXI write data at channel 2 -> AXI read data at channel 2	At first, direction of channel 2 pins is set as output thorough AXI interface. Then a data is written to channel 2 through AXI interface that appears at GPIO channel 2 output. Then the data at channel 2 is verified by reading through AXI interface.	Same as 2
5	GPIO_ch_1_2_input	PASS	checks for GPIO channel 1 & channel 2 pins both configured as input	Following sequences are executed in order: -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> GPIO input sequence -> AXI read data at channel 1 -> AXI read data at channel 2	Direction of both channels pins is set as input thorough AXI interface. Then a gpio sequence with input at both channels is executed through GPIO interface. Then the data at both channels is verified by reading through AXI interface.	Same as 1
6	GPIO_ch_1_2_output	PASS	checks for GPIO channel 1 & channel 2 pins both configured as output	Following sequences are executed in order: -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> AXI write data at channel 1 -> AXI write data at channel 2 -> AXI read data at channel 1 -> AXI read data at channel 2	Direction of both channels pins is set as output thorough AXI interface. Then a data is written to both channels through AXI interface that appears at GPIO output of both channels. Then the data at both channels is verified by reading through AXI interface.	Same as 2
7	GPIO_ch_1_input_2_output	PASS	checks for GPIO channel 1 pins configured as input & channel 2 pins configured as output	Following sequences are executed in order: -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> AXI write data at channel 1 -> AXI write data at channel 2 -> GPIO input sequence -> AXI read data at channel 1 -> AXI read data at channel 2	Direction of both channels pins is set thorough AXI interface. Then a data is written to both channels through AXI interface. Also GPIO sequence is executed through GPIO interface. Then the data at both channels is verified by reading through AXI interface.	Although one channel is set as input and other is set as an output, data is is written to both channels and also input is driven to both channels too. At the end the test is verified by reading from both channels and getting the expected results.

8	GPIO_ch_1_output_2_input	PASS	checks for GPIO channel 1 pins configured as output & channel 2 pins configured as input	Following sequences are executed in order: -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> AXI write data at channel 1 -> AXI write data at channel 2 -> GPIO input sequence -> AXI read data at channel 1 -> AXI read data at channel 2	Direction of both channels pins is set thorough AXI interface. Then a data is written to both channels through AXI interface. Also GPIO sequence is executed through GPIO interface. Then the data at both channels is verified by reading through AXI interface.	Same as 7
9	GPIO_ch_1_2_intr_en_with_input_at_ch_any	PASS	checks for GPIO channel 1 & channel 2 pins configured as input, with interrupt enabled for both channels	Following sequences are executed in order: -> AXI write Global interrupt enable -> AXI write Interrupt enable for both channels -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> GPIO input sequence -> interrupt at channel 1 sequence -> interrupt at channel 2 sequence -> interrupt at both channels sequence	Both global and local interrupt registers are enabled for both channels. Then direction of both channels pins is set as input through AXI interface. GPIO sequence is executed to configure the pins to some initial value. Then interrupts sequences are executed and check whether interrupt appears at output or not. If appears, corresponding interrupt status register bit is set and data at both channels is verified by reading through AXI interface.	It ensures that the interrupt is detected only when the global interrupt register and the local interrupt register bit for corresponding channel is set. Once the interrupt is detected by change at the channel for which interrupt is enabled, it is necessary to set the corresponding channel bit in interrupt status register to get the next interrupt.
10	GPIO_ch_1_intr_en_with_input_at_ch_any	PASS	checks for GPIO channel 1 & channel 2 pins configured as input, with interrupt enabled for channel 1	Following sequences are executed in order: -> AXI write Global interrupt enable -> AXI write Interrupt enable for both channels -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> GPIO input sequence -> interrupt at channel 1 sequence -> interrupt at channel 2 sequence -> interrupt at both channels sequence	Global and local interrupt register bit for channel 1 are enabled. Then direction of both channels pins is set as input through AXI interface. GPIO sequence is executed to configure the pins to some initial value. Then interrupts sequences are executed and check whether interrupt appears at output or not. If appears, corresponding interrupt status register bit is set and data at both channels is verified by reading through AXI interface.	Same as 9
11	GPIO_ch_2_intr_en_with_input_at_ch_any	PASS	checks for GPIO channel 1 & channel 2 pins configured as input, with interrupt enabled for channel 2	Following sequences are executed in order: -> AXI write Global interrupt enable -> AXI write Interrupt enable for both channels -> AXI write direction at channel 1 -> AXI write direction at channel 2 -> GPIO input sequence -> interrupt at channel 1 sequence -> interrupt at channel 2 sequence -> interrupt at both channels sequence	Global and local interrupt register bit for channel 2 are enabled. Then direction of both channels pins is set as input through AXI interface. GPIO sequence is executed to configure the pins to some initial value. Then interrupts sequences are executed and check whether interrupt appears at output or not. If appears, corresponding interrupt status register bit is set and data at both channels is verified by reading through AXI interface.	Same as 9