

Figure 1. Top Module Simulation

The register memory after simulation is as follows:-

Memory Data - /tb_Top_Module/dut/DP/Reg/Register_Files - Default									
0000001f	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
00000017	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0000000f	00000000	00000000	00000000	00000000	00000000	00000000	00000004	00000004	00000004
00000007	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

Figure 2. Register memory

The data memory after simulation is as follows:-

Memory Data - /tb_Top_Module/dut/DP/Data/Data_File - Default									
0000001f	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX
00000017	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	00000000	00000000	00000000	00000000	00000000
0000000f	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
00000007	00000000	00000000	00000000	00000000	00000022	00000004	2356a789	00000000	00000000

Figure 3. Data memory

The instruction memory after simulation is as follows:-

Memory Data - /tb_Top_Module/dut/DP/Inst/Instruction_Files																																	
000001ff	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000001e5	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000001cb	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000001b1	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000197	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
0000017d	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000163	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000149	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
0000012f	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000115	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000000fb	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000000e1	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000000c7	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
000000ad	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000093	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000079	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
0000005f	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
00000045	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	
0000002b	6f	00	00	00	03	25	80	00	23	24	80	00	6f	f0	df	fe	b3	84	84	40	6f	f0	5f	ff	33	04							
00000011	94	40	63	46	94	00	63	0c	94	00	93	04	40	00	13	04	40	01															

Figure 4. Instruction memory

Case:2-

Here is the assembly code for some dump instructions to be tested:-

```
main:
    addi x2, x0, 9
    addi x3, x0, 2
    bne x2, x3, imm
rtype:
    add x4, x2, x3
```

```

sub x5, x2, x3
sll x6, x2, x3
sltu x7, x2, x3
xor x8, x2, x3
srl x9, x2, x3
sra x10, x2, x3
or x11, x2, x3
and x12, x2, x3
bge x2, x3, load
imm:
addi x13, x2, 3
slli x14, x2, 3
xori x15, x2, 3
srli x16, x2, 3
srai x17, x2, 3
ori x18, x2, 3
andi x19, x2, 3
j rtype
load:
lw x20, 0x04(x0)
lb x21, 0x04(x0)
lh x22, 0x04(x0)
j upper_imm
store:
sw x20, 0x14(x0)
sb x20, 0x18(x0)
sh x20, 0x1c(x0)
j end
upper_imm:
lui x25, 0x12345
addi x25, x25, 0x678
lui x26, 0x12346
addi x26, x26, 0xFFFFFA78
auipc x27, 0x23456
bgeu x2, x3, store
end:
j end

```

Listing 2. Assembly code to be executed

The simulation for Top Module for selected signals for above algorithm is as follows:-

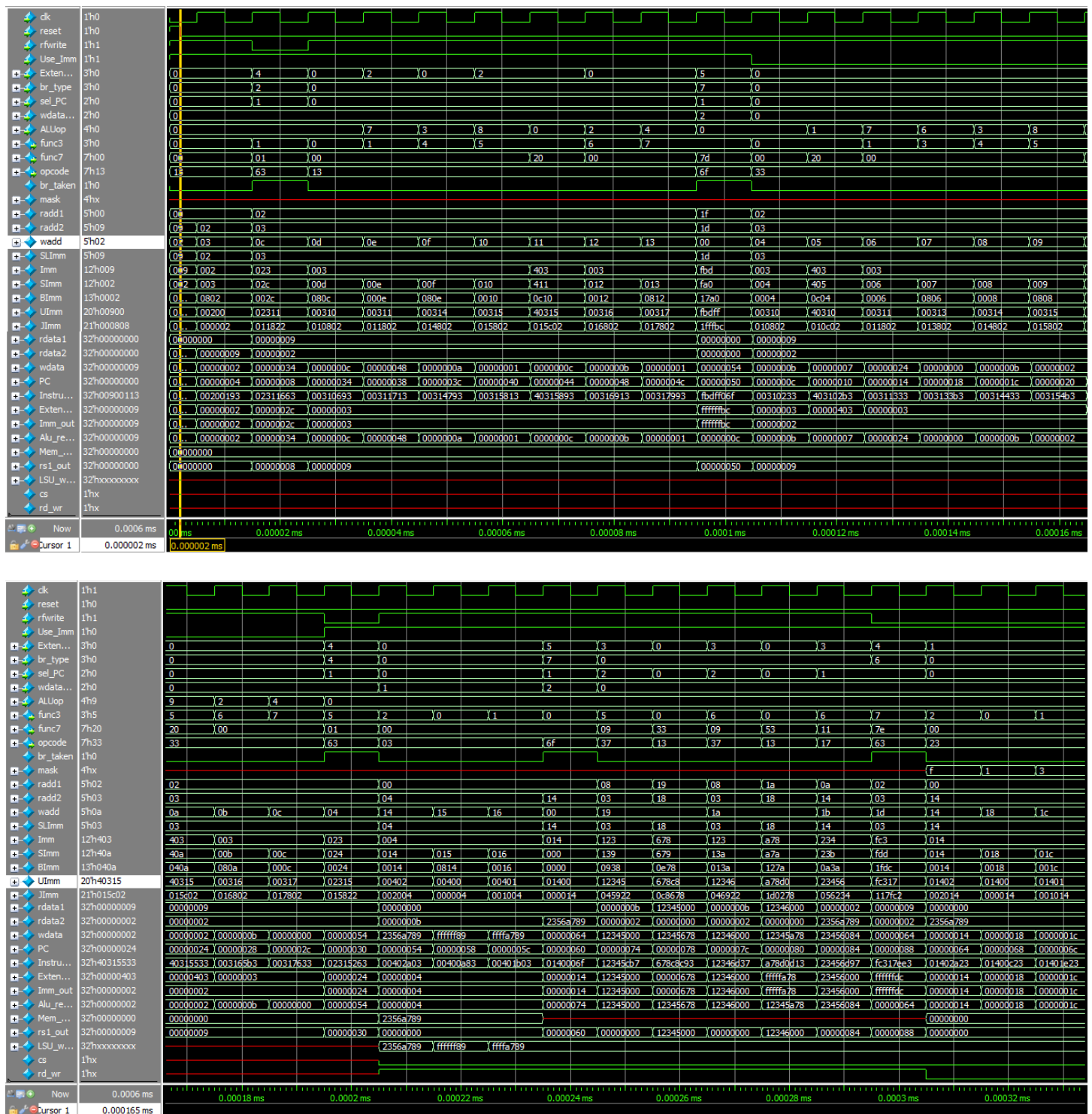


Figure 5. Top Module Simulation

The register memory after simulation is as follows:-

Memory Data - /tb_Top_Module/dut/DP/Reg/Register_Files - Default								
0000001f	00000000	00000000	00000000	00000000	23456084	12345a78	12345678	00000000
00000017	00000000	ffffa789	ffffff89	2356a789	00000001	0000000b	0000000c	00000001
0000000f	0000000a	00000048	0000000c	00000000	0000000b	00000002	00000002	0000000b
00000007	00000000	00000024	00000007	0000000b	00000002	00000009	00000000	00000000

Figure 6. Register memory

The data memory after simulation is as follows:-

Memory Data - /tb_Top_Module/dut/DP/Data/Data_File - Default								
0000001f	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX
00000017	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	00000000	00000000	00000000	00000000
0000000f	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
00000007	0000a789	00000089	2356a789	00000000	00000022	00000008	2356a789	00000000

Figure 7. Data memory

The instruction memory after simulation is as follows:-

Memory Data - /tb_Top_Module/dut/DP/Inst/Instruction_Files - Default																
000001ff	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000001e5	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000001cb	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000001b1	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
00000197	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
0000017d	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
00000163	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
00000149	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
0000012f	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
00000115	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000000fb	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000000e1	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000000c7	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
000000ad	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
00000093	XX	XX	XX	XX	6f	00	00	e3	7e	31	fc	97	6d	45	23	13
00000079	8c	67	b7	5c	34	12	6f	00	c0	01	23	1e	40	01	23	0c
0000005f	03	1b	40	00	83	0a	40	00	03	2a	40	00	6f	f0	df	fb
00000045	31	40	13	58	31	00	93	47	31	00	13	17	31	00	93	06
0000002b	b3	65	31	00	33	55	31	40	b3	54	31	00	33	44	31	00
00000011	31	40	33	02	31	00	63	16	31	02	93	01	20	00	13	01

Figure 8. Instruction memory