Design and Implementation of a Single Phase Full-Bridge Inverter with 120 Degree PWM and Sine PWM

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Abstract

This paper concentrates on modeling and simulation of single phase full bridge inverter as a frequency changer modulated by **Pulse Width Modulation (PWM) and Sinusoidal Pulse Width Modulation (SPWM)**.Inverter is the most important device to utilize the renewable energy sources efficiently. We cannot store energy in the form of Alternating current; it is always stored in the form of Direct Current. An inverter is a circuit that converts DC sources to AC sources. The Sinusoidal Pulse Width Modulation (SPWM) technique is one of the most popular PWM techniques for harmonic reduction of inverters. The **120 degree conduction PWM and SPWM** switching signal is generated with the help of different FPGAs, micro controllers and microprocessors through coding. The concept of Pulse Width Modulation (PWM) for inverters is described with analyses extended to different kinds of PWM strategies. In the end, the simulation and hardware results for a single-phase inverter using the PWM strategies described are presented and analyzed.

Chapter 1

Introduction

The DC-AC converter, also known as the inverter, converts DC power to AC power at desired output voltage and frequency. The DC power input to the inverter is obtained from an existing power supply network or from a rotating alternator through a rectifier or a battery, fuel cell, photovoltaic array or magneto hydrodynamic generator. The controlled full-wave bridge converters can function as inverters in some instances, but an ac source must preexist in those cases. In other applications, the objective is to create an ac voltage when only a dc voltage source is available. The focus of this chapter is on inverters that produce an ac output from a dc input. Inverters are used in applications such as adjustable-speed ac motor drives, transportation, induction heating, stand by power supplies, Uninterruptible Power Supplies (UPS), and running ac appliances from an automobile battery.

There are three types of inverters based on type of output waveform as: **square wave, modified-sine wave and pure sine wave**. A square wave is non-sinusoidal waveform, most typically seen in electronics and signal processing. Square wave have two levels (positive and negative) and alternates regularly between these two levels. The output of a modified sine wave inverter is more like a square wave output except that it has one more level i.e, before switching positive or negative the output goes to zero volts. A pure or true sine wave inverter converts the DC supply into a near perfect sine wave. The sine wave has very little harmonic distortion which results in a very clean supply and makes it suitable for working electronic systems such as computers, motors and microwave ovens and other sensitive equipment without causing problems like noise. Things like mains battery chargers also run better on pure sine wave converters.

Ideally the output waveforms of an inverter should be sinusoidal. However, the waveforms of practical inverters are non sinusoidal and contains certain harmonics. Due to the availability of high speed power semiconductor devices, the harmonic contents present in the output voltage can be minimized significantly by using switching technique. BJTs, MOSFETs or IGBTs can be used as ideal switches.

Chapter 2

Literature Review

Inverters are circuits that convert dc to ac. Inverters are used in applications such as adjustable-speed ac motor drives, uninterruptible power supplies (UPS), and running ac appliances from an automobile battery.
Inverters can be broadly classified into 2 types:-

- Single Phase Inverters
- Three Phase Inverters

Each of these types can be used to switch on/off devices like BJTs, MOSFETs, IGBTs, MCTs, SITs, and GTOs. These inverters usually use PWM control signals for producing an Ac output voltage.

There are two types of single phase inverters:-

- Full Bridge Inverters
- Half Bridge Inverters

2.0.1 Full Bridge Inverter

This inverter circuit converts DC to AC. It is obtained by turning ON and OFF the switches in the right sequence. It has four different operating states which are based on which switches are closed.

2.0.2 Half Bridge Inverter

The half bridge inverter is the basic building block of a full bridge inverter. It contains two switches and each of its capacitors has an output voltage equal to $V_dc/2$. In addition, the switches complement each other i. e. if one is switched ON the other one goes OFF.

2.1 Performance Parameters

2.1.1 Harmonic Factor

It is the measure of individual harmonic contribution.

$$HF_n = \frac{V_{on}}{V_{o1}} \tag{2.1}$$

Where $n > 1$ and V_{o1} is the rms value of the fundamental component an V_{on} is the rms value of the n^{th} harmonic component.

2.1.2 Total Harmonic Distortion

It is the measure of closeness in shape between a waveform and its fundamental component.

$$THD = \frac{1}{V_{o1}} \sqrt{\sum_{n=2,3,4}^{\text{inf}} V_{on}^2} \tag{2.2}$$

2.1.3 Distortion Factor

It is the measure of effectiveness in reducing unwanted harmonics without having to specify the values of a second order load filter. For n^{th} order it is defined as:

$$DF_n = \frac{V_{on}}{V_{o1} n^2} \tag{2.3}$$

for $n > 1$.

2.1.4 Lowest Order Harmonic

LOH is the harmonic component whose frequency is closest to the fundamental one, and its amplitude is greater than or equal to 3% of the fundamental component.

2.2 Switching Operation

The simplest switching scheme for the full-bridge converter produces a square wave output voltage. The switches connect the load to V_{dc} when S1 and S2 are closed or to V_{dc} when S3 and S4 are closed. The periodic switching of the load voltage between V_{dc} and V_{dc} produces a square wave voltage across the load. Although this alternating output is non sinusoidal, it may be an adequate ac waveform for some applications [2].

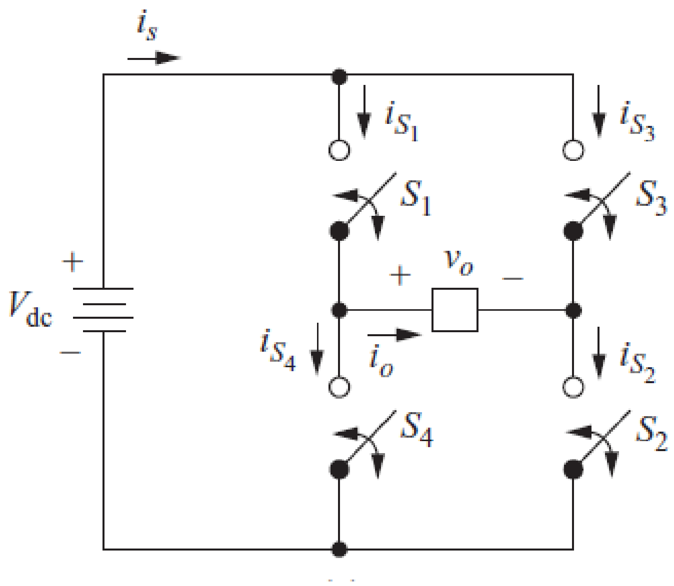

FIGURE 2.1: Full Bridge Inverter Switching Operation

The current waveform in the load depends on the load components. For the Resistive load, the current waveform matches the shape of the output voltage. An inductive load will have a current that has more of a sinusoidal quality than the voltage because of the filtering property of the inductance. An inductive load presents some considerations in designing the switches in the full-bridge circuit because the switch currents must be bidirectional. For a series RL load and a square wave output voltage, assume switches S1 and S2 in the above figure close at t_0. The voltage across the load is V_{dc}, and current begins to increase in the load and in S1 and S2. At $t_{T/2}$, S1 and S2 open, and S3 and S4 close.

When the circuit is first energized and the initial inductor current is zero, a transient occurs before the load current reaches a steady-state condition. At steady state, io is periodic and symmetric about zero. As shown in the figure 2.2

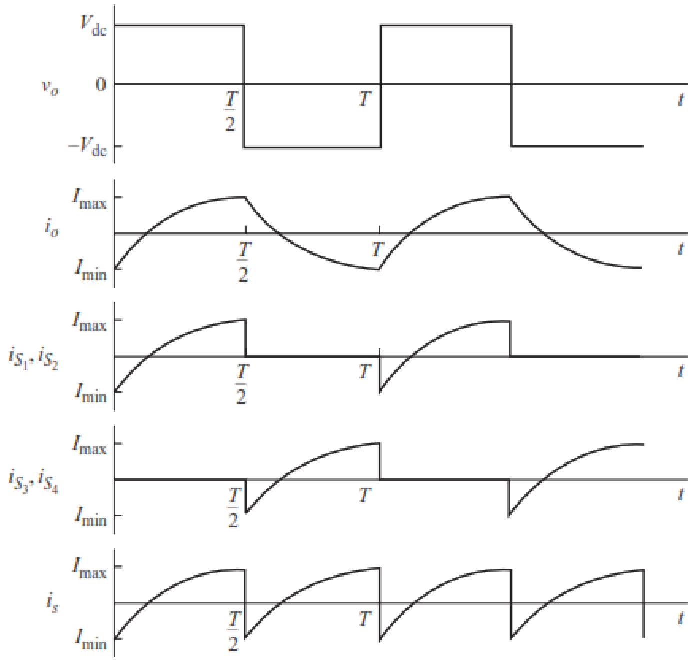

FIGURE 2.2: Square wave output voltage and steady state current waveform for RL Load

2.3 Diode Operation

The switch currents in the figure show that the switches in the full-bridge circuit must be capable of carrying both positive and negative currents for RL loads. However, real electronic devices may conduct current in one direction only. This problem is solved by placing feedback diodes in parallel (anitparallel) with each switch. During the time interval when the current in the switch must be negative, the feedback diode carries the current. The diodes are reverse-biased when current is positive in the switch. Figure 2.3 shows the full-bridge inverter with switches implemented as insulated gate bipolar transistors (IGBTs) with feedback diodes [2].

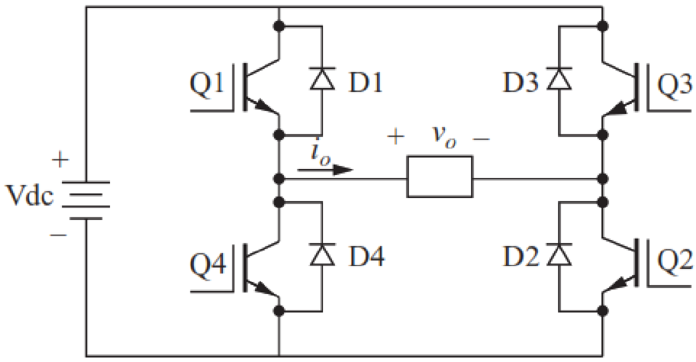

Figure 2.3: Full Bridge Invertor Using IGBTs

When IGBTs Q1 and Q2 are turned off in Fig., the load current must be continuous and will transfer to diodes D3 and D4, making the output voltage V_{dc}, effectively turning on the switch paths 3 and 4 before Q3 and Q4 are turned on. IGBTs Q3 and Q4 must be turned on before the load current decays to zero.

2.4 Single Pulse Width Modulation

As the semiconductor device receives only one pulse during one half cycle, one semiconductor device is switched on. The output voltage of the inverter can be controlled by controlling width of pulse. Figure 2.4 shows the gate signal and output voltage waveform for single phase full bridge inverter. The gate signal is generated by comparing VR amplitude reference signal and VC amplitude control signal. The width of gate pulse can be varies from 0 degree to 180 degrees by controlling the reference signal from 0 to VR. This will control the output voltage of the inverter [1].

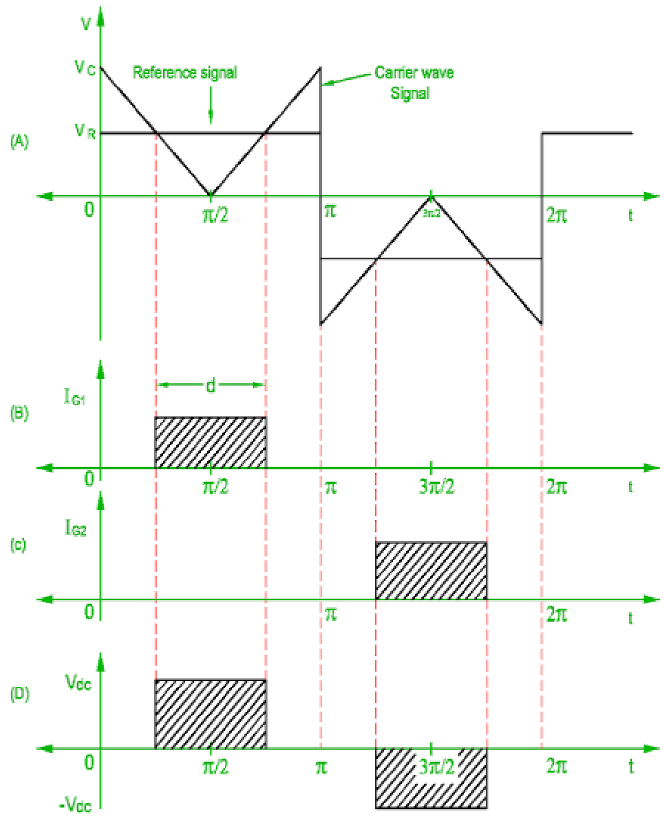

FIGURE 2.4: Single Pulse Width Modulation

The frequency of the output voltage depends upon frequency of reference signal. The amplitude modulation M is ratio of reference signal (V_R) and carrier signal (V_C).

$$M = \frac{V_R}{V_C} \tag{2.4}$$

2.5 Multiple Pulse Width Modulation

There are more than one pulse per half cycle in the MPWM. These gate pulses are used to control output voltage of inverter as well as reduce harmonics. The magnitude and width of the pulses are equal in this method. The reference signal and higher frequencies carrier signals are compared in this method in order to generate more than one gatting pulses. The number of gate pulses depends upon carrier frequencies whereas the output voltage depend frequencies of reference signal [2].

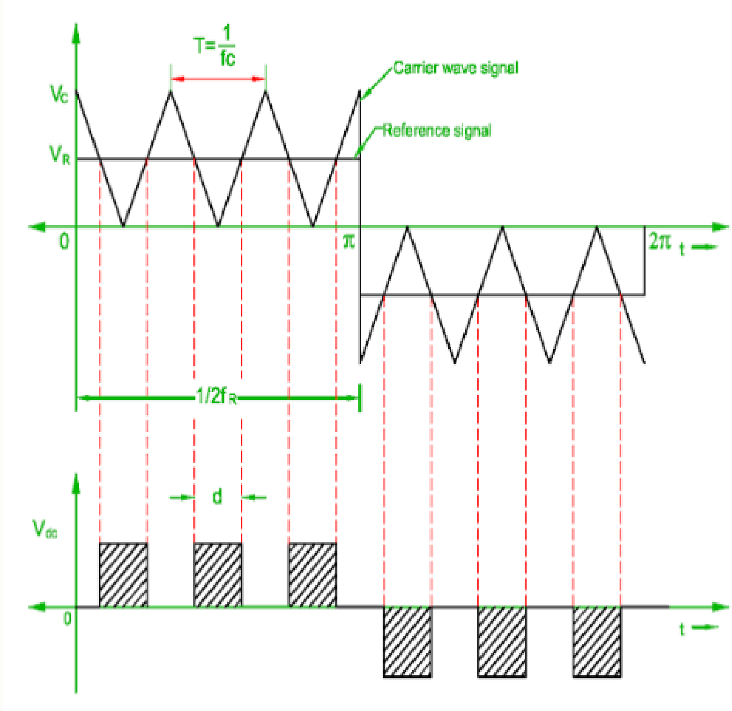

FIGURE 2.5: Multiple Pulse Width Modulation

2.6 Sinusoidal Pulse Width Modulation

The most efficient method of controlling gain is to incorporate PWM controls within the inverters. The SPWM (Sinusoidal Pulse Width Modulation) technique is used to produce sine wave output by the system. In Pulse Width Modulation (PWM) the pulse width is varied to control the output voltage of inverter. The SPWM is a process of varying width of every pulse in pulse train in proportion of the sine wave amplitude evaluated at the centre of the same pulse [1].

A microcontroller is used to obtained Pulse width modulated (PWM) pulses and to achieve the controlled AC output voltage, these PWM pulses are being used as triggering pulses for the inverter circuit. A sine-wave should be the desired output waveform with very low harmonic distortion. The advantages of pure sine wave inverters are such as inductive loads like motors and microwaves run faster, cooler and quieter. It reduces electrical and audible noise in fans, audio amplifiers, TV, fax, fluorescent lights and answering machines. It prevents glitches in monitors and crashes in computers . A single phase inverter control circuit is developed which produces a pure sine wave. The output voltage magnitude and frequency is same as of grid voltage. To operate electrical and electronic appliances smoothly power rating inverter is required.

The example of square wave inverter or quasi sine wave inverter is most of the available commercially uninterruptible power supplies (UPSs). Due to the harmonic contents, the electronic device managed by these inverters gets damaged. The available pure sine wave inverters neither cheaper nor generates pure sinusoidal output while the sine wave generation is extremely important in power electronics. The sinusoidal pulse width modulation (SPWM) switching technique is used for getting a pure sine wave. This involves a certain switching pattern used in the inverter bridges. This inverter reduces the total harmonic distortion (THD) and maximizes efficiency.

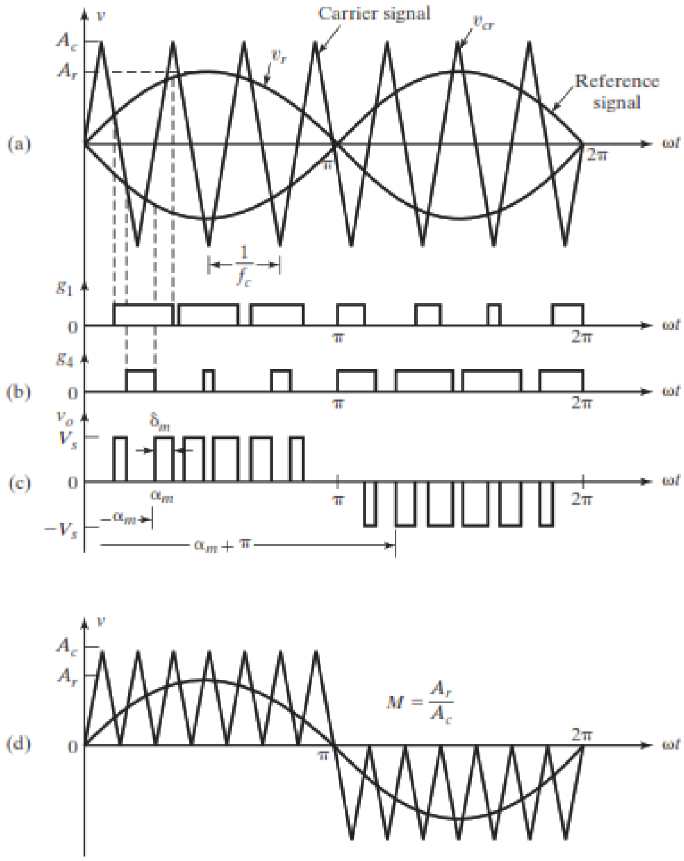

FIGURE 2.6: Sinusoidal Pulse Width Modulation

2.7 Scope

In many industrial applications the control of ac output voltage is important :

- To cope with variations of dc input voltage
- To regulate voltage of inverters
- To satisfy the constant volts and frequency requirements

Chapter 3

Design And Analysis

3.1 Block Diagram

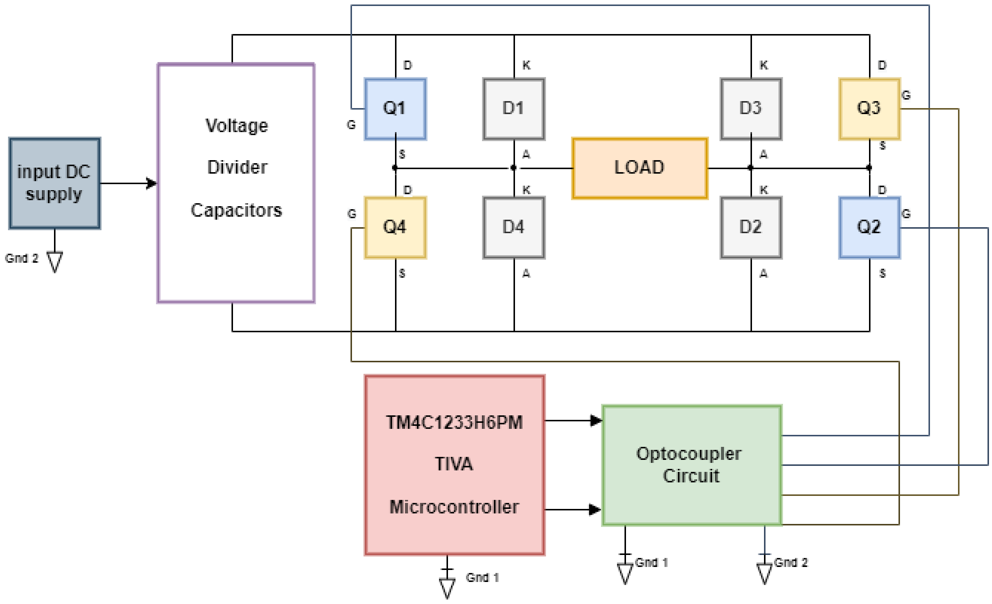

Figure 3.1: Block Diagram of Single Phase Full Bridge Invertor

3.2 Software Design

First of all, we perform the simulation of the circuit in Matlab SIMULINK. We design a single phase bridge inverter circuit by using 4 Mosfets along with diodes. Diodes are connected so that the lag current can have a path for flow in case of inductive load. We provide the input voltage as 40V. We test the circuit by connecting R, RL, and RLC load. First we set the input pulses for 120 degree conduction. One pulse was provided to T1, T2 and then another pulse with delay of 10ms was provided to T3, T4. This pulse was then converted to PWM 120 degree conduction signal. The output voltage and current waveform were recorded in chapter 5.

After that, we set the gate voltages as bipolar SPWM. Two Sine PWMs were provided as gate signal to required Mosfets and then input voltage was feeded. Simulation results were recorded in chapter 5.

3.3 Hardware Design

We designed the hardware circuit as explained in chapter 4. For the gate pulses, we generated PWM and SPWM gate pulses from TIVA Microcontroller (TM4C1233H6PM). After that we patched the circuit on bread boards i.e full bridge circuit on one bread board and optocoupler circuit on other. We used four IRF540 Mosfets in full bridge circuit for switching and diode operations. The load used for testing was R, RL and RLC Load. AFter testing, the results were obtained and recorded in chapter 6.

Chapter 4

Circuit Explanation

4.1 Simulation Circuit

4.1.1 Simulation Using PWM

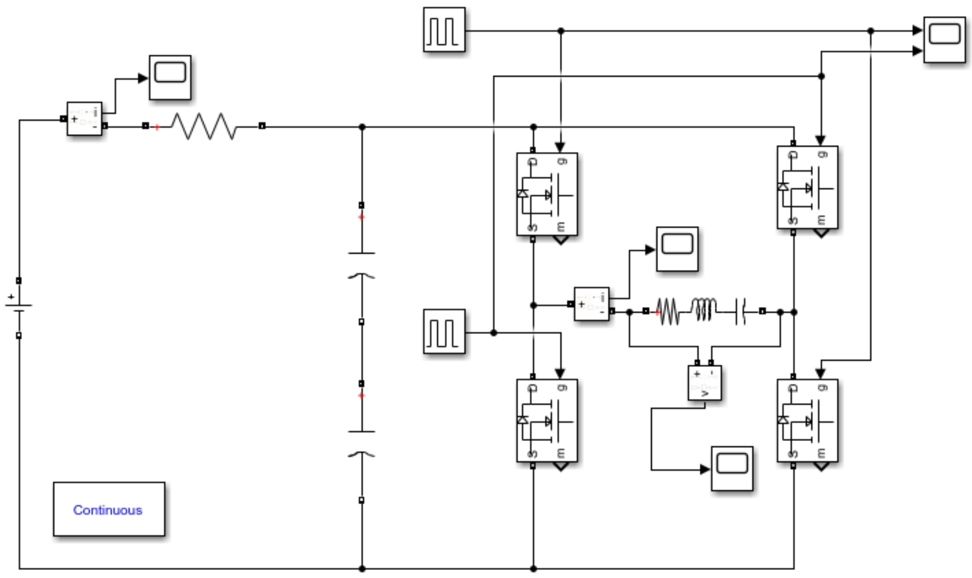

FIGURE 4.1: Single Phase Full Bridge Inverter with PWM

For this circuit, two PWM pulses are taken. To make it 120 degree conduction, first pulse is set to duty cycle of 33.33 % with zero phase. This PWM is applied to as gate signal to T1 and T2 as shown in figure 4.1 . Now the second PWN is also set to 33.33 % of duty cycle but with the phase shift of 180 degrees. This one is applied as gate signal to T3 and T4 as shown in figure 4.1 . The voltage measurement block is connected to observe the PWM waveforms along with their delay. After that T1, T2, T3, T4 along with their respective diodes D1, D2, D3, D4 are connected in the form of full bridge as shown in the figure 4.1 . Now the load is connected between terminals a and b and

voltage and current measurement blocks are applied to measure the output voltage and current of the load.
In this way, Full Bridge Invertor with SPWM input and 120 degree conduction mode is developed. The voltage waveforms recorded on scope and other observations are explained in detail in 5.

4.1.2 Simulation Using SPWM

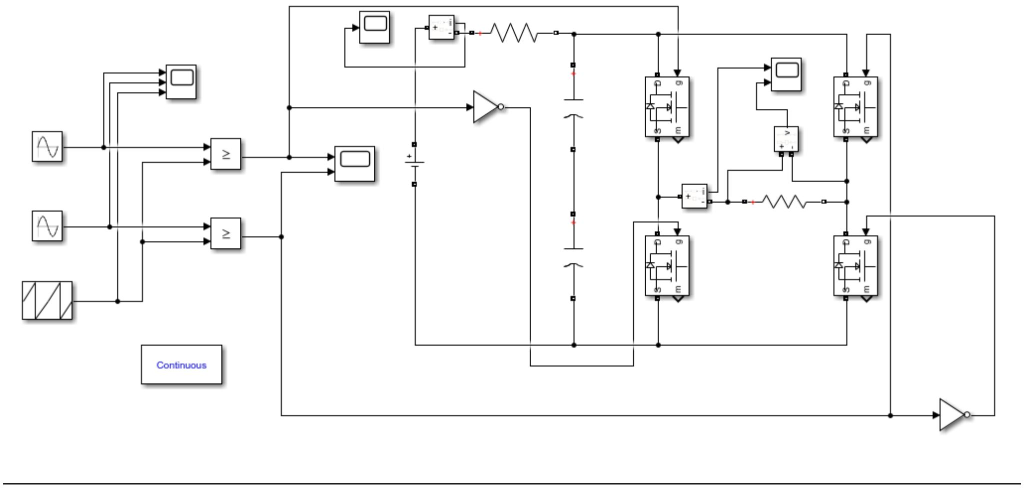

FIGURE 4.2: Single Phase Full Bridge Inverter with Unipolar SPWM

For this circuit, two SPWM pulses are taken. A SPWM Pulse is generated by comparing a simple triangular carrier signal of high frequency with the reference sine waveform of required frequency. The modulation indexes are calculated according to the given frequency i.e. 50 Hz. The resulting output is a SPWM waveform. In this experiment, a Unipolar SPWM is considered.

$$m_f = \frac{f_c}{f_r} \tag{4.1}$$

$$m_f = \frac{500}{50} = 10 \tag{4.2}$$

The voltage measurement block is connected to observe the PWM waveforms along with their delay. After that T1, T2, T3, T4 along with their respective diodes D1, D2, D3, D4 are connected in the form of full bridge as shown in the figure 4.2 . Now the load is connected between terminals a and b and voltage and current measurement blocks are applied to measure the output voltage and current of the load.
In this way, Full Bridge Inverter with SPWM input at gate is developed. The voltage waveforms recorded on scope and other observations are explained in detail in 5.

4.2 Hardware Circuit Diagram

The Hardware designed for this project is shown in figure 4.3 in detail.

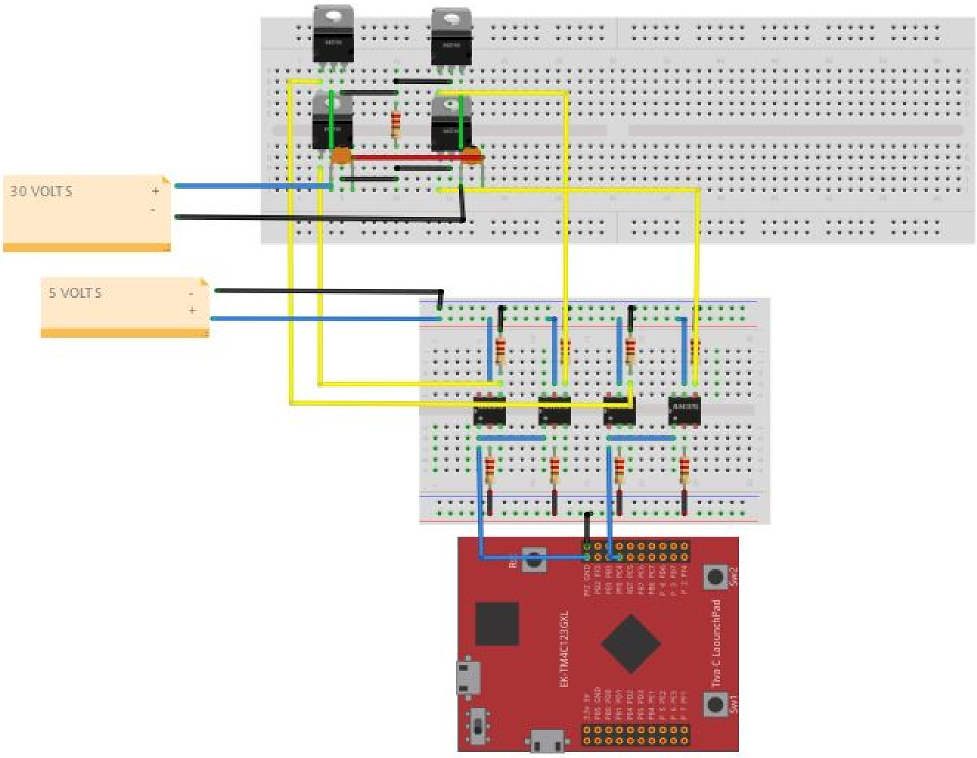

FIGURE 4.3: Circuit Diagram of Single Phase Full Bridge Invertor

4.2.1 Explanation

4.2.2 PWM and SPWM Generation Using TIVA

Micro controller TM4C1233H6PM is used for supplying gate pulses to the circuit. As two pulses are generated, so 2 pins are used. The code for PWM generation is given in Appendix A. From pin PF2, the first PWM is obtained and from PC4 the sencond PWM is obtained with delay of 180 degrees. The output pulses can be seen in chapter 6. Now, the output from pin PF2 is fed to 2 pin 1 of 2 optocouplers and then from pin 4 of these optocouplers, it is connected to gate terminal of T1 and T2 respectively. Then, the output from pin PC4 is fed to 2 pin 1 of other 2 optocouplers and then from pin 4 of these optocouplers, it is connected to gate terminal of T3 and T4 respectively.

4.2.3 Optocoupler Circuit

Optocoupler contain six pins as shown in the figure 4.4. The input from TIVA is provided to pin 1 while the second pin contains 210 ohms resistor connected to ground . Pin 3 is left empty. The next pins provides with the output to the actuator which the provided gate signal to the respective Mosfets, however a pull down resistor is installed at this particular pin. Therefore we collect our signals from the port above the 1k ohms resistor i.e pull down . Pin 5 is supplied by a 5V battery for the functionality of the system and alternatively pin 6 is also left empty.

4 similar circuits as shown in figure 4.4 are patched. Their grounds on both sides are

made common. The input on pin 1 is provided from each of 2 pins of TIVA i.e. 1 pin of TIVA provides input to 2 optocouplers. Pin 5 of four of them is made common and then connected to the 5V input from power supply. The output from pin 4 is fed to the each of 4 gate pulses of MOSFETS. The complete circuit is shown the figure 4.4.

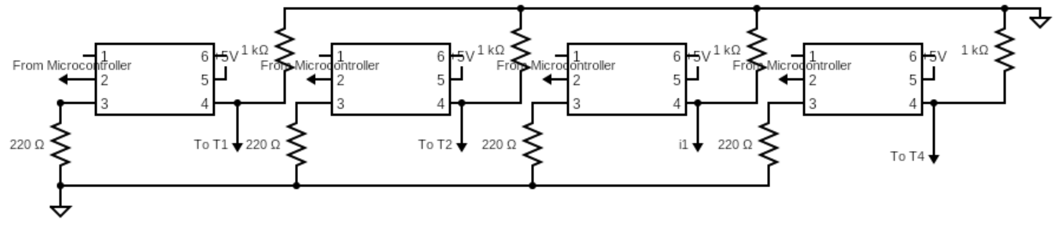

FIGURE 4.4: Circuit Diagram of Opto Coupler Circuit.

4.2.4 Full Bridge Circuit

The full bridge circuit consists of consists of 4 choppers where each chopper consists of a pair of a transistor, mosfet or a thyristor and a diode, pair connected together that is:

- T1 and D1 are connected in parallel,
- T4 and D2 are connected in parallel,
- T3 and D3 are connected in parallel, and
- T2 and D4 are connected in parallel.

A load is connected between the pair of choppers at "AB" and the end terminals of T1 and T4 are connected to voltage source V_{dc}. Between T1, T4 and V_{dc}, 2 capacitors of equal capacitance are used which divides the input dc voltage into 2 equal parts. The circuit is shown in figure 4.5.

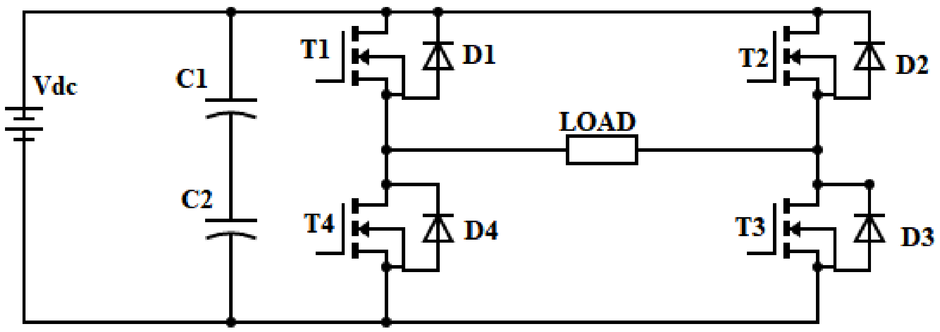

FIGURE 4.5: Circuit Diagram of Single Phase Full Bridge Invertor.

4.2.5 Circuit Testing

The input dc voltage is set as 40V. The load connected is in the range near to 500W. The testing is performed either using R, RL or RLC load. The obtained results, simulated waveforms and the related calculations can be observed in chapter 6.

Chapter 5

Simulation Results

5.1 PWM Simulation

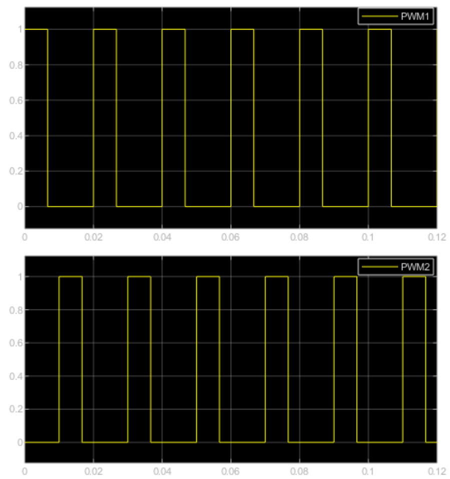

FIGURE 5.1: Gate signal wave forms for 120 degree conduction PWM.

The generation of these gate signals have been discussed in detail in Chapter 4. These gate signals are applied to the MOSFETS to observe the wave forms in figure 5.2. The output voltage is a **Quasi Square Waveform** i.e., it has a zero level between the maximum positive and negative peaks. The full bridge first conducts in forward direction when MOSFET T1 and T2 are conducting, then we have a dead band when none of the switch is on. After that T3 and T4 are conducting in opposite direction. By using 120 degree conduction mode we are able to get a voltage waveform closer to a sinusoidal wave.The current input wave form (figure 5.3) is having alot of harmonics induced in it.

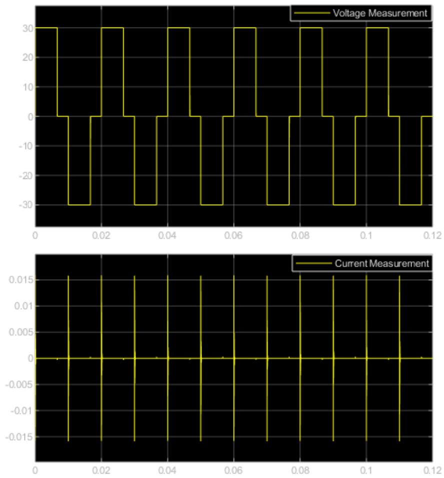

FIGURE 5.2: Output voltage and current wave forms for 120 degree conduction PWM.

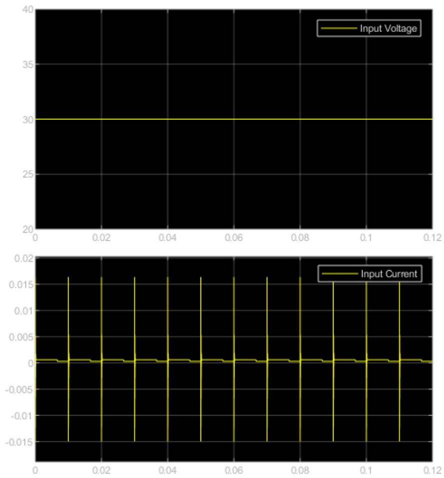

FIGURE 5.3: Input voltage and current wave forms for 120 degree conduction PWM.

If the value of inductor is increased, the output current waveform starts resembling a sinusoidal wave but voltage waveform gets distorted because of stored energy in inductor.

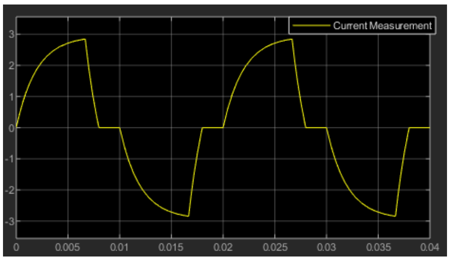

FIGURE 5.4: Current wave form with high inductive load.

5.2 SPWM Simulation

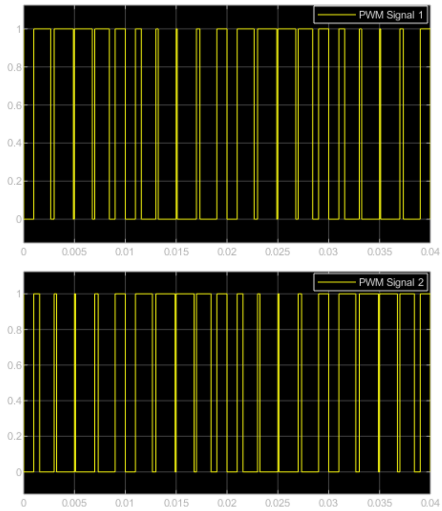

FIGURE 5.5: Gate signal wave forms for unipolar SPWM.

The pulses generated for gate triggering of MOSFETS for the generation of SPWM can be seen in figure 5.5. These SPWM's have frequency modulation index of 10. After applyig these gate signals we get output wave forms as shown in figure 5.6.

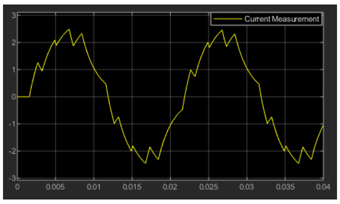

FIGURE 5.8: Current wave form with high inductive load.

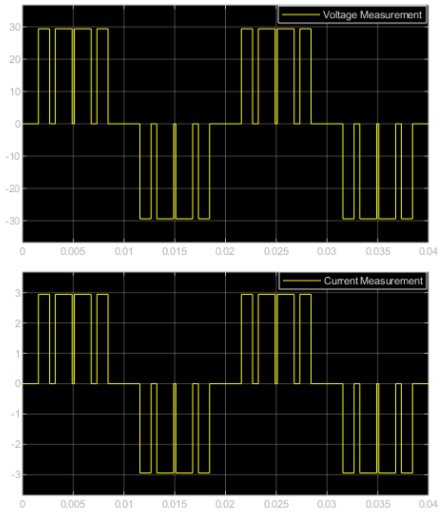

FIGURE 5.6: Output voltage and current wave forms for unipolar SPWM.

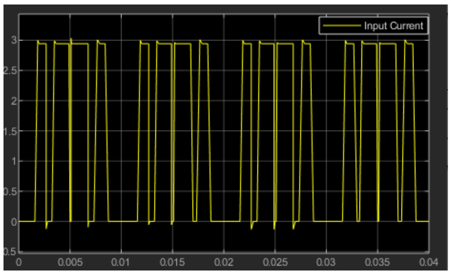

FIGURE 5.7: Input current wave forms for unipolar SPWM.

If the value of inductor is increased, the output current waveform starts resembling a sinusoidal wave as seen in figure 5.8.

Chapter 6

Hardware Results

6.1 PWM generation from TIVA

For testing the circuit, gate signals where generated using TIVA with the help of code given in A. The gate signals with 33.33% duty cycle and with a delay of 10ms can be seen in figure 6.1. These signals are passed through the opto coupler circuits to create isolation between the micro controller and hardware.

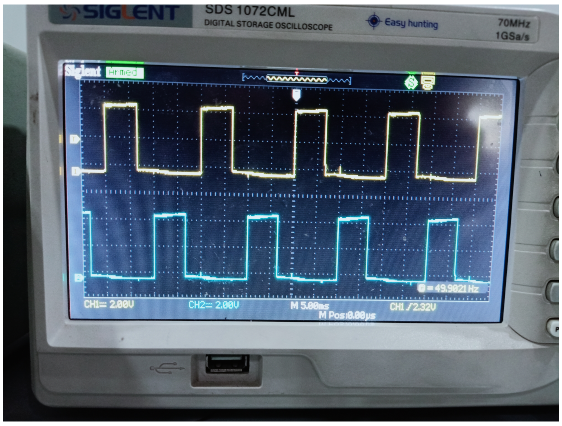

FIGURE 6.1: Gate signals generated by TIVA.

6.2 Output waveform with R Load

When these gate signals are applied to the full bridge inverter, we get a Quasi Square waveform as seen in simulation. The output wave form can be seen in figure 6.2.

FIGURE 6.2: Output wave form for 120 degree conduction mode with R Load

The output voltage V_o is V_{dc}, $-V_{dc}$, or zero, depending on which switches are closed.

Switches Closed	Output Voltage v_o
S_1 and S_2	$+V_{dc}$
S_3 and S_4	$-V_{dc}$
S_1 and S_3	0
S_2 and S_4	0

FIGURE 6.3: Output Voltage Values

Note that S1 and S4 should not be closed at the same time, nor should S2 and S3. Otherwise, a short circuit would exist across the dc source. Real switches do not turn on or off instantaneously. Therefore, switching transition times must be accommodated in the control of the switches. Overlap of switch "on" times will result in a short circuit, sometimes called a shoot-through fault, across the dc voltage source. The time allowed for switching is called blanking time.

The switch currents in Fig. 8-2 show that the switches in the full-bridge circuit must be capable of carrying both positive and negative currents for RL loads. However, real electronic devices may conduct current in one direction only. This problem is solved by placing feedback diodes in parallel (anti-parallel) with each switch. During the time interval when the current in the switch must be negative, the feedback diode carries the current. The diodes are reverse-biased when current is positive in the switch. Power semiconductor modules often include feedback diodes with the switches.

6.3 Output Waveform with RL Load

In case of an RL Load the output voltage waveform is shown in figure 6.4:-

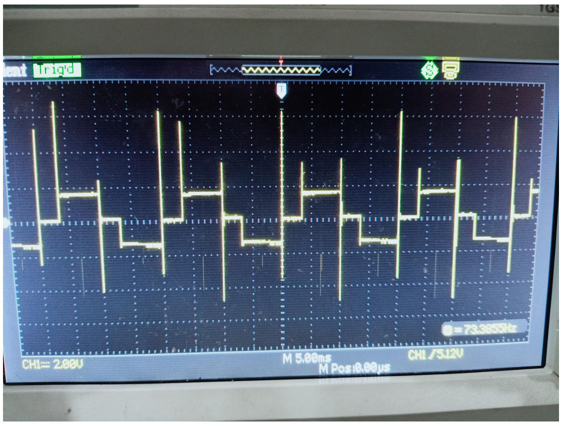

FIGURE 6.4: Output wave form for 120 degree conduction mode with RL Load

Chapter 7

Conclusions

The most simple gate is pulse with some constant duty cycle (usually 50%) and amplitude. We can change the output voltage by changing the dc voltage amplitude but it is usually restricted in most cases. Although we can change the output voltage by varying the duty cycle of gate pulse, but if at lower frequencies it can create large gaps and if we decrease the time period than overlap between the non-shifted and shifted pulse can also occur which may lead to short circuit.

That is the reason we convert the simple into PWM. We take a regular PWM of high frequency and AND it with the applied gate pulse so that the output obtained is the PWM gate pulse. Now, we can change the average value of the output voltage by just changing the duty cycle of the regular PWM as by changing it, area covered under the output voltage waveform changes.

But, it is considered that SPWM is much more better than the PWM gate pulse. The sinusoidal PWM control technique is possibly the simplest to implement and can be synthesized by comparing a sinusoidal reference voltage with a triangular carrier. In the SPWM technique, the switching frequency of an inverter is equal to that of a carrier wave. The switch is turned on/off once every period of the triangular carrier wave. The SPWM technique has an advantage of having a constant switching frequency. A constant switching frequency makes it possible to calculate the losses of switching devices, so the thermal design for them becomes easier. In addition, since the harmonic characteristics will be well-defined, the design of a low-pass filter to eliminate the harmonics becomes easier.

The SPWM technique has been widely popular due to the simplicity of its principle and analog implementation. In the analogue implementation of the SPWM (referred to as naturally sampled PWM), an analog integrator is used to generate a triangular carrier wave, and an analog comparator is used to determine the intersection instants of the triangular carrier wave and modulating signal. Since the SPWM technique can perform voltage modulation every sampling interval with a fixed switching frequency, it exhibits a better dynamic performance.

The output voltage control of invertors requires varying both the number of pulses per half cycle and the pulse widths that are generated by modulation techniques. The output voltage contains odd harmonics over a frequency spectrum. Some applications require either fixed or a variable output voltage, but certain harmonics are undesirable in reducing certain effects such as harmonic torque and heating in motors, inferences and oscillations. In SPWM Technique, we can eliminate certain harmonic along with its multiple by setting the parameters which is very great advantage because due to reduction of non-required harmonics, waveform can be made smoother.

Appendix A

Code For PWM

```
#include "TM4C123GH6PM.h"

#define SYSCTL_RCGCGPIO_R *((volatile unsigned long *)0x400FE608)
#define CPAC_R *((volatile unsigned long *)0xE000ED88)

// Peripheral clock enabling for timer and GPIO
#define SYS_CLOCK_FREQUENCY 16000000

void SystemInit()
{
    CPAC_R |= (0xF << 20);
}

/* Generates 50HZ and variable duty cycle on PF2 pin of TM4C123 Tiva C Launchpad */
/* PWM1 module and PWM generator 3 of PWM1 module is used. Hence PWM channel*/

void init_pwm1()
{
    /* Clock setting for PWM and GPIO PORT */
    SYSCTL->RCGCPWM |= 2;       /* Enable clock to PWM1 module */
    SYSCTL->RCGCGPIO |= 0x20;   /* Enable system clock to PORTF */
    SYSCTL->RCC |= (1<<20);     /* Enable System Clock Divisor function  */
    SYSCTL->RCC |= 0x000E0000;  /* Use pre-divider valur of 64 and after that feed clock to

    /* Setting of PF2 pin for M1PWM6 channel output pin */
    GPIOF->AFSEL |= (1<<2);         /* PF2 sets a alternate function */
    GPIOF->PCTL &= ~0x00000F00; /*set PF2 as output pin */
    GPIOF->PCTL |= 0x00000500;  /* make PF2 PWM output pin */
    GPIOF->DEN |= (1<<2);       /* set PF2 as a digital pin */

    PWM1->_3_CTL &= ~(1<<0);    /* Disable Generator 3 counter */
    PWM1->_3_CTL &= ~(1<<1);    /* select down count mode of counter 3*/
    PWM1->_3_GENA = 0x0000008C; /* Set PWM output when counter reloaded and clear when match
    PWM1->_3_LOAD = 5000;       /* set load value for 50 Mhz 16MHz/64 = 250kHz and (250KHz/5
    PWM1->_3_CMPA = 4999;       /* set duty cyle to to minumum value*/
    PWM1->_3_CTL = 1;           /* Enable Generator 3 counter */
    PWM1->ENABLE |= 0x40;       /* Enable PWM1 channel 6 output */
}

void init_pwm2()
{
```

```
    /* Clock setting for PWM and GPIO PORT */
    SYSCTL->RCGCPWM |= 1;        /* Enable clock to PWM0 module */
    SYSCTL->RCGCGPIO |= 0x04;    /* Enable system clock to PORTC */
    SYSCTL->RCC |= (1<<20);      /* Enable System Clock Divisor function  */
    SYSCTL->RCC |= 0x000E0000;   /* Use pre-divider valur of 64 and after that feed clock to

    /* Setting of PF2 pin for M1PWM6 channel output pin */
    GPIOC->AFSEL |= (1<<4);          /* PC4 sets a alternate function */
    GPIOC->PCTL &= ~0x000F0000; /*set PC4 as output pin */
    GPIOC->PCTL |= 0x00040000;   /* make PC4 PWM output pin */
    GPIOC->DEN |= (1<<4);        /* set PC4 as a digital pin */

    PWM0->_3_CTL &= ~(1<<0);     /* Disable Generator 3 counter */
    PWM0->_3_CTL &= ~(1<<1);     /* select down count mode of counter 3*/
    PWM0->_3_GENA = 0x0000008C; /* Set PWM output when counter reloaded and clear when match
    PWM0->_3_LOAD = 5000;        /* set load value for 50Hz 16MHz/64 = 250kHz and (250KHz/500
    PWM0->_3_CMPA = 4999;        /* set duty cyle to to minumum value*/
    PWM0->_3_CTL = 1;            /* Enable Generator 3 counter */
    PWM0->ENABLE |= 0x40;        /* Enable PWM1 channel 6 output */
}

void SetSpeedB( float speed )
{
    PWM1->_3_CMPA = (100-speed)*50;
}

void SetSpeedA( float speed )
{
    PWM0->_3_CMPA = (100-speed)*50;
}

void delay(int time_ms)
{
    int i, j;
    for(i = 0 ; i < time_ms; i++)
    for(j = 0; j < 3180; j++)
    {}  /* excute NOP for 1ms */
}

// Application main function
int main(void)
{
    init_pwm1();
    delay(10);
    init_pwm2();

    while (1)
    {
        SetSpeedB(33.33);
        SetSpeedA(33.33);
    }
}
```

References

[1] Muhammad H. Rashid. Power Electronics, Devices, Circuits, and Explanation. 4th Edition. Pearson

[2] Daniel W. Hart. Power Electronics. 2011. Tata McGraw-Hill Education