Apoorv Kishore

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EDUCATION

INDIAN INSTITUTE OF TECHNOLOGY BOMBAY | M.Tech and B.Tech
Electrical Engineering | GPA: 8.9/10 *[Jun'16-Jun'21]*
Courses: *Microprocessors, Digital Systems, Digital Signal Processing, Neuromorphic Engineering*
Recipient of ***Undergraduate Research Award***

PUBLICATIONS

A. Kishore, V. Saraswat, U. Ganguly: **Simplified Klinokinesis using Spiking Neural Networks for Resource-Constrained Navigation on the Neuromorphic Processor Loihi.** *The International Joint Conference on Neural Networks*, 2021; in press [Link] *[Jul'21]*

A. Kishore, B. Dasgupta: **A Novel Clock-Path Programming Algorithm to enhance IP-DVFS Design and Verification tasks.** *Samsung Semiconductor India RnD TechCon*, 2023 (White Paper) *[Mar'23]*

WORK EXPERIENCE

SAMSUNG SEMICONDUCTOR INDIA R&D
SoC RTL Design: Power Management and Clock Architecture

ASSOCIATE STAFF ENGINEER *[Mar'23-Present]*

- Complete ownership of design for Power Management IP in Samsung Mobile & Generative AI Accelarator SoCs
- Implemented hardware algorithms to reduce sleep mode power consumption of Samsung Exynos chips by ~40%
- Experienced in Functional ECOs, Verification debugging, Scandump analysis and Silicon Bring-up for Exynos chips
- Worked on booting & initialization sequences for the SoC including ARM V8/V9 CPU Core, and GPUs/NPUs

SENIOR ENGINEER *[Jul'21-Mar'23]*

- Implemented hardware mechanisms like HW Automatic Clock/Power Gating to reduce turn on/off latency by ~75%
- Designed and executed an algorithm in **Python** to engineer the clock-tree design and verification process successfully reducing the combined process timeline by more than 60% as well as improving the architecture robustness

RESEARCH EXPERIENCE

RESOURCE-CONSTRAINED NAVIGATION ON INTEL'S NEUROMORPHIC CHIP LOIHI
Guide: Prof. Udayan Ganguly| Master's Thesis *[Jun'20-Mar'21]*

- Developed a fully spike-based navigational algorithm by approximating numerical functions in neuronal spikes
- Demonstrated comparability to the Python implementation with 1.92% error establishing performance reliability

PERFORMANCE PREDICTION FOR SPEECH RECOGNITION TASKS ON LIQUID STATE MACHINES
Guide: Prof. Udayan Ganguly| Research Project *[Aug'19-Apr'20]*

- Executed analysis of Memory Metric, Network Criticality and Kernel Quality for performance prediction in MATLAB
- Demonstrated maximum outperformance of memory metric by 40.63% for low error regimes on TI-46 speech data

KEY PROJECTS

PIPELINED RISC MICROPROCESSOR
Course: Microprocessors | IIT Bombay

- Designed a pipelined RISC Microprocessor from scratch in VHDL to implement custom Instruction Set Architecture
- Verified the design for functional scenarios, proofed it against hazards and implemented the system on an FPGA

SCENE RECOGNITION USING BAG OF WORDS AND SCALE INVARIANT FEATURE TRANSFORM

- Performed vocabulary detection using K-means clustering and Principle Component Analysis on the SIFT of images.
- Trained a Multi-class Support Vector Machine to classify scenes into one of the 15 classes obtaining 89% accuracy

COMPARISON OF PCA AND FISHER's LINEAR DISCRIMINANT FOR FACE RECOGNITION
Course: Fundamentals of Digital Image Processing | IIT Bombay

- Showed PCA's error rates vary with image light intensity in face recognition, unlike Fisher's Linear Discriminant

TECHNICAL SKILLS

COMPETENCIES Clock and Power Design, SDC, FECOs, Silicon debugging, Deep Learning

TOOLS/LIBRARIES/LANGUAGES Python, C, C++, C#, Assembly, SQL, PyTorch, OpenCV, Git, MATLAB, Spyglass, Xcelium, Magellan, Verilog, VHDL, Quartus, Spice, Perforce, Unix