Apoorv Kishore

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ACADEMIC QUALIFICATION

INDIAN INSTITUTE OF TECHNOLOGY BOMBAY *[Jun'16-Jul'21]*
Electrical Engineering | Dual Degree (M.Tech and B.Tech)
Cumulative GPA: 8.9/10
Recipient of the **Undergraduate Research Award** for significant research contributions

Relevant Courses: Data Structures - 9/10, Applied Linear Algebra - 10/10, Neuromorphic Engineering - 10/10
Advanced Probability and Random Processes - 10/10, Microprocessors - 10/10, Digital Systems - 9/10

PUBLICATIONS

A. Kishore, V. Saraswat, U. Ganguly: **Simplified Klinokinesis using Spiking Neural Networks for Resource-Constrained Navigation on the Neuromorphic Processor Loihi.** *The International Joint Conference on Neural Networks*, 2021 [IEEE Link] [Arxiv Link] *[Jul'21]*

A. Kishore, B. Dasgupta: **A Novel Clock-Path Programming Algorithm to enhance IP-DVFS Design and Verification tasks.** *Samsung Semiconductor India RnD TechCon*, 2023 (White Paper) *[Mar'23]*
[in preparation to be submitted to DAC-2025]

RESEARCH EXPERIENCE

RESOURCE-CONSTRAINED NAVIGATION ON INTEL'S NEUROMORPHIC CHIP LOIHI
Guide: Prof. Udayan Ganguly | Master's Thesis *[Jun'20-Mar'21]*
Published in the International Joint Conference on Neural Networks (IJCNN), 2021

- Developed a fully spike-based novel navigation system inspired by C. Elegans on Intel's neuromorphic chip Loihi, eliminating the need of digital cores and achieving one of the first demonstrations on neuromorphic hardware
- Achieved a completely spike-based implementation by approximating numerical functions through neuronal spikes
- Demonstrated comparability by achieving performance within **1.92%** range of the pure software implementation

CLOCK-PATH PROGRAMMING ALGORITHM TO ENHANCE DESIGN AND VERIFICATION FOR DVFS
Co-Author: Mr. Biswadeep Dasgupta | Research Project *[Sep'22-Present]*
Published in Samsung Semiconductor India RnD TechCon 2023 as a white paper

- Developed a novel path-programming algorithm for clock management networks that improves design & verification timeline efficiency by **more than 60%** by optimizing frequency requirements through intelligent route selection
- Designed & implemented factor-elimination method to calculate optimal division ratios in complex intersecting trees
- Refined the algorithm to **optimize for dynamic power** consumption, PLL locking and other engineering constraints

BIT-INDEPENDENT TEMPORAL BOOLEAN ARITHMETIC ON SPIKING NEURAL NETWORKS
Guide: Prof. Udayan Ganguly| Research Project *[Jul'23-Present]*

- Designed a novel bit-independent temporal arithmetic unit using SNNs that reduces hardware complexity compared to previous solutions, with potential implementation pathway using Single Electron Transistor & VCSEL-neurons
- Architected **infinite-bit temporal multiplication and storage** units using homogeneous Integrate and Fire neurons and a single synaptic rule for learning delays which eliminated the need for multiple firing and forgetting rules

PERFORMANCE PREDICTION METRICS FOR SPEECH RECOGNITION TASKS ON LIQUID STATE MACHINES
Guide: Prof. Udayan Ganguly | Research Project *[Aug'19-Apr'20]*

- Executed analysis of Memory Metric, Network Criticality and Kernel Quality for performance prediction in MATLAB
- Demonstrated maximum outperformance of memory metric by **40.63%** for low error regimes on TI-46 speech data

WORK EXPERIENCE

SAMSUNG SEMICONDUCTOR INDIA R&D
SoC RTL and Software Co-Design: Power Management and Clock Architecture
ASSOCIATE STAFF ENGINEER *[Mar'23-Present]*

- Owned the complete design for Power Management IP in Samsung Exynos Mobile & Generative **AI Accelarator** SoCs
- Implemented automatic hardware power down Finite State Machine (FSM) and embedded algorithms to reduce sleep mode power consumption of **Exynos1580 chipset by ~40%** while maintaining low system wakeup latency
- Performed functional ECOs, Verification debugging, Scandump analysis and Silicon Bring-up for Exynos chips

- Executed the booting & initialization sequences for the SoC using ARM CortexM series V8 and V9 CPU Cores

SENIOR ENGINEER *[Jul'21-Mar'23]*

- Owned the design and implementation of clock-architecture, static timing constraints and clock-domain crossing
- Implemented hardware mechanisms like HW Automatic Clock Gating to reduce dynamic power consumption
- Designed and executed an algorithm in **Python** to engineer the clock-tree design and verification process successfully reducing the combined process timeline by more than 60% as well as improving the architecture robustness

INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
Course: Applied Linear Algebra | Prof. Debasattam Pal
TEACHING ASSISTANT *[Aug'20-Apr'21]*

- **Mentored 50+ students** through personal interactions, **weekly tutorials** and interactive doubt clearing sessions
- Refined and developed content, assignments and quizzes for the course Linear Algebra to be instructed online

KEY PROJECTS

IITB-RISC PIPELINED MICROPROCESSOR
Course: Microprocessors | IIT Bombay

- Designed the architecture of a pipelined RISC Microprocessor to execute a custom Instruction Set Architecture
- Proofed the design against hazards, implemented it on an **FPGA in VHDL** and verified it for functional scenarios

SPIKING NEURAL NETWORK: OPTIMISATION
Guide: Prof. Udayan Ganguly | IIT Bombay

- Optimized accuracy of the system by refining the resistive and capacitive properties of the Neuronal Model
- Achieved a maximum **30% increase** in performance of the Liquid State Machine on Poisson spike classification

INDOOR NAVIGATION USING AUGMENTED REALITY

- Developed and tested AR advertisements and indoor navigation solution for parts of Nexus shopping mall
- Implemented **A* pathfinding** algorithm on the 3D mall mesh in **Unity C#**, using raycasting for ground detection

SCENE RECOGNITION USING BAG OF WORDS AND SCALE INVARIANT FEATURE TRANSFORM

- Performed vocabulary detection using **K-means clustering** and Principle Component Analysis on the SIFT of images.
- Trained a Multi-class Support Vector Machine to classify scenes into one of the 15 classes obtaining **75% accuracy**

COMPARISON OF PCA AND FISHER's LINEAR DISCRIMINANT FOR FACE RECOGNITION
Course: Fundamentals of Digital Image Processing | IIT Bombay

- Demonstrated variation of PCA's error rates with light intensity in the image, unlike Fisher's Linear Discriminant

TECHNICAL SKILLS

COMPETENCIES	Neuromorphic Computing, Speech & Image Processing, Deep Learning Embedded coding, Silicon debugging, Clock and Power RTL Design
LANGUAGES	Verilog, VHDL, C, C++, C#, MATLAB, Python, Assembly, Bash
TOOLS/LIBRARIES	PyTorch, OpenCV, Git, Spyglass, Xcelium, Magellan, Indago, Verdi, Vim Quartus, Spice, Perforce, Unix, Unity, Visual Studio

SOCIAL/ENTREPRENEURIAL VENTURES

NPS CHARITABLE TRUST
Founding member | Non-Profit Organization | [Website]

- Helped contribute to more than **50 social projects** to provide educational resources to underprivileged children

ALPA3D
Co-Founder | Stealth Startup Project

- Collaborated with Nexus Malls, one of the largest mall chains in India, to create and test deployable prototypes for indoor Augmented Reality navigation, interactive entertainment, and 3-Dimensional advertisement solutions

EXTRA CURRICULARS

- Received the **Best Speaker award** at the 27th National Youth Parliament held by the Government of India
- Secured **1st and 2nd position** in Group Dance competition in Inter-IIT Cultural Meet 2017 and 2019 respectively