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A modified high speed and less area BCD adder architecture using Mirror adder

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Abstract— In number system, BCD numbers are well-known for representing numbers in four bit decimal format. Many circuits are designed and developed till today to work with the BCD numbers. In any processor or digital system adder plays major role in effecting the speed of operation of the whole structure. By executing BCD addition by means of BCD adder, the operation gets slow due to the delay in propagating the carry output from one stage to another stage of the adder. Also due to the usage of two RCA adders the area of the adder is also increasing. This delay is going to effect the operation and increasing the area of the entire system in which the BCD adder is used. To overcome this problem of delay and increase in area, a new technique of adder is proposed in this paper i.e., mirror adder. Mirror adder is an adder circuit which is implemented without using XOR gates. In this paper, BCD adder architecture is modified by replacing the 4-bit RCA with 4-bit mirror adder. The proposed design of adder is simulated and synthesized for various input bit sizes and then evaluated in terms of delay (ns) with the existing adders and area occupied (LUTs).

Keywords— BCD Adder; BCD addition; Amendment factor; RCA; Mirror adder;Inverter elimination

Introduction

Decimal number system is preferred among all the various types of number systems. The reason behind this is the most usage of decimal system is in many digital systems and processors. Of course, binary number systems have been chosen as default number system for processors [1] but present there is a huge demand of circuits which have decimal number system support.

In any processor, arithmetic unit is the workhorse of the system. In arithmetic unit, adder is major component [2]. Many number of addition methods are proposed and implemented too. Adder circuit supports various arithmetic operations. The adder working speed affects the working speed of the arithmetic unit which leads to affect the working speed of the complete structure in which it is used [3], [4], [5].For performing BCD addition, BCD adder is required. The main disadvantage of BCD adder is delay in propagating the carry and also the increase in area due to the usage of two four bit RCAs. Different BCD adder designs are proposed using CLA [6], reversible logic [7], [8] and quantum dot cellular method [9], [10]. But nowadays high speed and low power consumption circuits are needed for VLSI circuit design.

To have a high speed BCD adder circuit, the existing architecture of the BCD adder is modified. A new adder circuit called mirror adder replaced the RCA in the BCD adder. This new architecture will have less delay and also the area occupied will be less because mirror adder have less number of gates so the area occupied will be low and also it have less number of gates in its critical path so the delay will be less.

In this paper section 2 explains about the BCD addition rules and then about existing BCD adder architecture. The BCD adder architecture which is proposed using mirror adder is discussed in section 3.Also, section 3 gives detailed explanation about the new adder technique i.e., mirror adder. The synthesis result consists of area and delay information are provided in section 4.

I. CONVENTIONAL BCD ARCHITECTURE

A. BCD addition

The BCD number format represents ten digits (i.e., 0-9) number in the decimal format. In binary number system, 4-bits are required to represent a decimal number. To represent BCD numbers greater than 9 in binary format two four bits are required. Figure 2 shows the flow chart for BCD addition procedure. For performing BCD addition there are certain addition rules [11] which are as follows-

- When BCD numbers are added and the resultant is less than 9, than there is no carry output of the addition operation.
- When BCD numbers are added and the resultant is more than 9, than a amendment factor is added to addition result to get correct sum result.

When BCD numbers are added and the resultant is 9, than the carry input states whether amendment factor required or not and carry output is generated or not.

B. BCD adder architecture

Figure 2 shows the architecture of a 128-bit BCD adder with RCA which consists of 4-bit RCA at top and bottom level of the architecture and also a carry out circuit. The top level RCA consists of four full adders connected in series prototype.

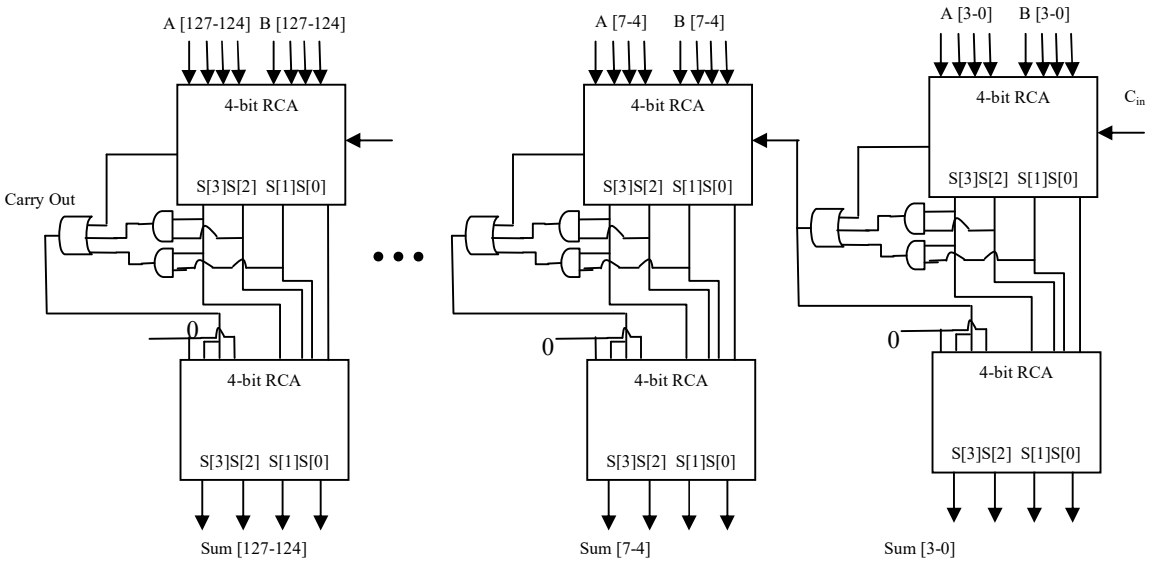

Fig. 1128-bit BCD adder architecture

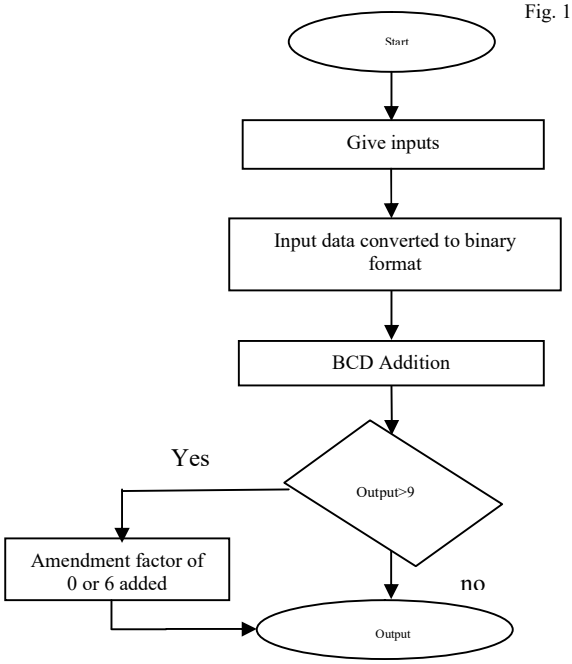

Fig. 2 BCD addition algorithm flow diagram

This top level RCA performs addition of input bits and provide intermediate sum and carry output. The middle level module is nothing but carry output generation circuit designed using one OR gate and two AND gates.

The lower level section is again a 4-bit RCA. This bottom level RCA consist four adders connected in series format in which the first adder is a half adder and remaining three are full adders. The entire operation of the circuit depends on the result of the top level RCA i.e., if it is more than 9, a carry value is produced. Then the output is revised by adding 6 to it. The operation of the carry out circuit is not only to generate carry output for next stages but also its output can be used as bits in amendment factor.

The carry value is generated by the carry output generation circuit which is used directly as carry input to next stage. The bottom level RCA operation is to add amendment factor i.e., 6 to the intermediate sum. The bottom level RCA doesn't require carry input, so it consists of half adder for adding LSB bits. The sum output of first stage RCA are fed as one of the input for bottom level RCA and second input to this is amendment factor. The amendment factor LSB and MSB bits are 0 where as the 1st and 2nd bits in amendment factor are carry output of carryout circuit. When the resultant of the carry output generation circuit is 1 then a amendment factor 6 is added to the sum output of first stage RCA and when the carry output is 0, then 0 is added to the sum resultant of foremost stage RCA.

II. BCD ADDER USING MIRROR ADDER

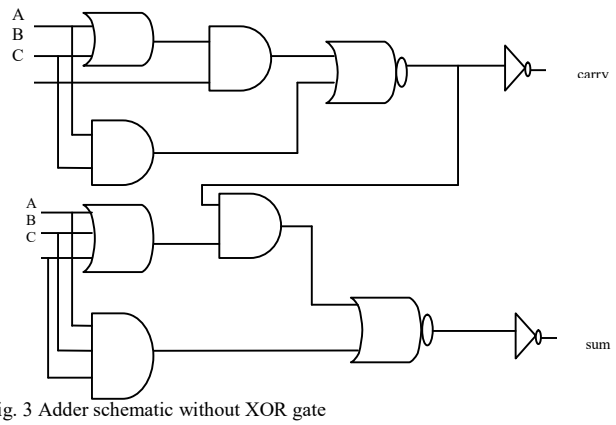

Fig. 3 Adder schematic without XOR gate

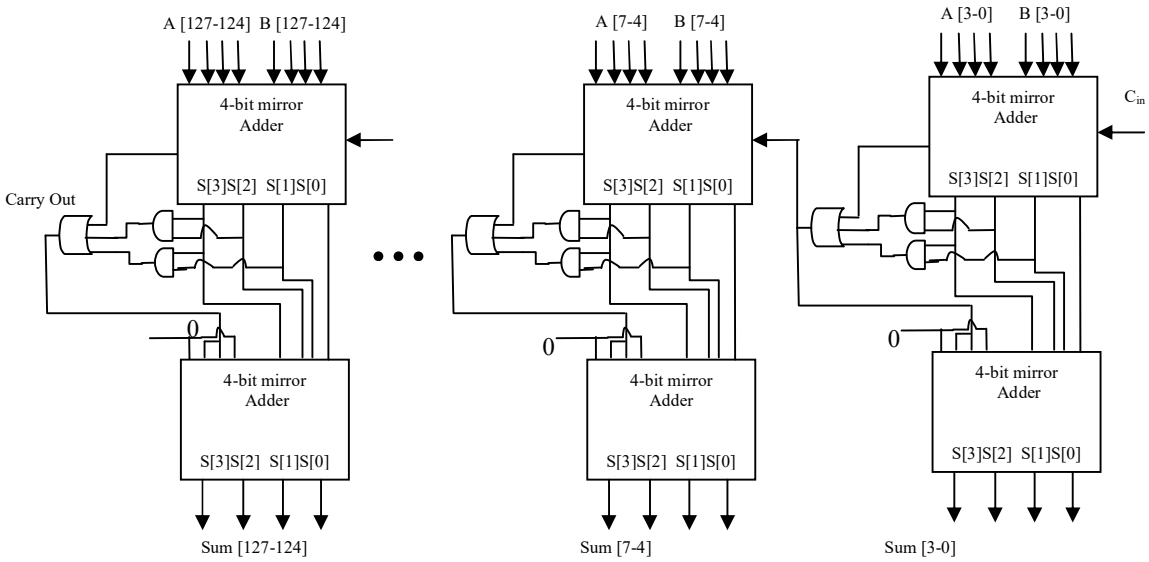

Fig. 4 128-bit Proposed BCD adder with mirror adder

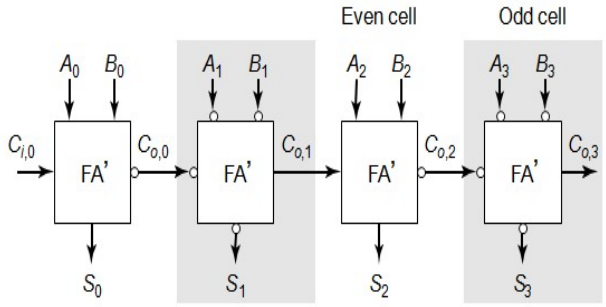

Fig. 5 Even and odd cell for Inverter elimination in carry path

To overcome the problem of delay in propagating the carry, mirror adders [12], [13] are used in place of RCA. Number of adders connected in cascading format forms a RCA. The full adder gate level implementation consists of XOR gates due to which the area occupied is increased. An implementation of adder that does not use XOR gates is shown in fig 3. This uses an alternative implementation that is achieved by realizing that the CARRY term may be reused in the SUM term as a common sub expression.

To optimize the carry delay, the inverter at the output of the carry gate can be omitted. This technique is called inverter elimination in carry path. This result insignificantly decreases carry delay. The adder in which inverter is eliminated in both carry and sum paths is called mirror adder. Figure 5 shows the arrangement of even and odd using cells by using inverter elimination scheme. The inverter removal scheme for odd and even cell formation utilize two properties of the mirror adder. The two properties are as follows-

i) The inputs applied to the full adder are inverted resulting in inverted output values.

ii) Mirror adder first produces the complement of carry output. Later inverts it to produce the carry output.

Figure 4 shows the modified architecture of BCD adder with mirror adders. From the fig 4, it is clear that instead of RCA, mirror adders are used. The top level mirror adder is a 4-bit adder which consists of four adders without using XOR gates (shown in fig 3) connected in series pattern. From fig 3 it is clear that, the gate level implementation of full adder without XOR gates has less number of gates and also the number of gates in critical path is less. The remaining architecture and operation of the proposed adder is same as the existing adder.

III. SIMULATED RESULTS AND COMPARSION

TABLE 1 AREA AND DELAY CONTRAST OF DESIGNED BCD ADDERS

Input size	Type of Adder	Delay (nano sec)	Area (No. of LUTs)
8-bit	BCD adder with RCA	20.16	24
	BCD adder with mirror adder	17.7	22
16-bit	BCD adder with RCA	30.3	48
	BCD adder with mirror adder	28.12	44
32-bit	BCD adder with RCA	55.7	96
	BCD adder with mirror adder	48.95	88
64-bit	BCD adder with RCA	106.4	192
	BCD adder with mirror adder	90.62	176
128-bit	BCD adder with RCA	207.9	384

	BCD adder with mirror adder	173.9	352

Two different BCD adder architecture designs i.e., BCD adder with RCA and BCD adder with mirror adder are developed for different input sizes in VHDL [14]. Xilinx ISIM simulator used to carry out the Functional simulations. With the help of XST synthesizer, all the developed adder designs are synthesized [15]. A synthesis tool called XST synthesizer included in ISE named XST synthesizer dispense different reports including area and delay report. Area report consists of area details in terms of number of LUTs, slices utilized where as delay report consists of delay details in Nano seconds.

The proposed BCD adder with mirror adder is having less delay when evaluated with the BCD Adder with RCA which is shown in table 1. Also the proposed BCD adder occupies less number of LUTs. The proposed BCD adder with mirror adder is said to be quicker in operation and occupies less area.

IV. CONCLUSION

BCD adder architecture is proposed using mirror adder in this paper. The BCD adder architecture using mirror adder is developed for different input sizes (8, 16, 32, 64 and 128) with the help of VHDL and simulated functionally by means of ISIM simulator. The proposed design is synthesized with the help of XST synthesizer tool which is part of Xilinix ISE 14.2 EDA tool. To contrast the proposed adder performance with the conventional adder design, the conventional adder i.e., BCD adder architecture with RCA is also developed with the help of VHDL for identical input bit sizes, simulated for functional verification and synthesis performed by means of the identical tool referred above. After that the developed adder designs are contrasted with one another by means of delay (nano sec) and area (number of LUTs). Table 1 depicts that the proposed BCD adder architecture with mirror adder for every bit size has least delay contrast to BCD adder with RCA.

The number of LUTs occupied by the proposed adder is less when compared with the existing one. As area is low, the power consumed by the design is also less. By considering the result discussion, it can be accomplished that the proposed adder i.e., BCD adder with mirror adder is having a reduced amount of delay and area when evaluated with BCD adder with RCA. The BCD adder with mirror adder can be used for high speed least power applications.

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