0.13 μm modular BCD technology enable to embedding high density E2PROM, RF and Hall sensor suitable for IoT application

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***Abstract*— In this paper, we develop 0.13 μm BCD technology which gives best-in-class LDMOS transistors rated up to 30V with ultra- low leakage logic device. Based on this process, high density EEPROM with the cell size of 0.645 μm^2 and RF devices such as varactor and inductor are integrated. Also, high reliable Hall sensor family can be added. Total Photo mask layers are only 33 for 5 metallization.**

Keywords—BCD, LDMOS, EEPROM, IoT, Hall sensor, RF

I. INTRODUCTION

There have been extremely increasing hopes for Internet-of-Things (IoT) to connect cars, wearable electronics, building automation, and numerous other applications [1-3]. The required chips are low power battery, MCU, RF and sensors. However, their process incompatibility makes difficult to bring low cost solution. In this paper, we propose new modular BCD technology to integrate them into single chip.

II. PROCESS INTEGRATION

The vertical structures of each major device integrated with single process flow are shown in Fig. 1.

After formation of n+ buried layer (NBL) and p type epitaxial layer (p-Epi), deep well for high voltage BCD and EEPROM, ultra-low leakage 1.5V CMOS, 5V CMOS, EEPROM cell, varactor, and Hall sensor are integrated.

A. Ultra-low leakage logic transistors

Currently, in IoT application, logic transistor needs ultra-low leakage level due to lower power consumption, to realize ultra-low leakage logic transistors, source and drain engineering is the most critical factor. We achieved ultra-low leakage level for 1.5 and 5V logic devices.

Table 1 summarizes our ultra-low leakage logic transistors. Their leakage level is less than 0.3pA in minimum channel length.-class level.

TABLE 1 Summary of ultra-low leakage transistors

Parameters	NMOS	PMOS
Vtlin (V)	0.676	0.659
Idsat (uA/um)	337	156
Ioff (pA)	0.16	0.25
BV (V)	> 4	> 5

B. Power LDMOS

With increasing demand for higher frequency power management solutions, to enable smaller size and improved overall efficiency, there is a need to minimize the switching loss of power devices integrated in PowerSoCs. Over the past 10-15 years, most of the optimization of integrated power devices has been focused on minimizing Rsp (Rdson*Area) [4], [5]. As the switching frequency of high-power products increases well beyond 1MHz, the reduction in switching losses has become a critical factor in order to meet the demanding product requirements. This is achieved by minimizing the Ron*Qg Figure of Merit [6].

Fig. 2 reveals Rsp and Ron*Qg values of nLDMOS at different voltage rating. Their Rsp and Qg values are minimized through our optimized device engineering and is appeared world best-in-class level. Note that their breakdown voltage has enough margin to sustain each voltage rating. In addition to nLDMOS, all BCD components such as EDMOS, zener diode, various BJTs are developed.

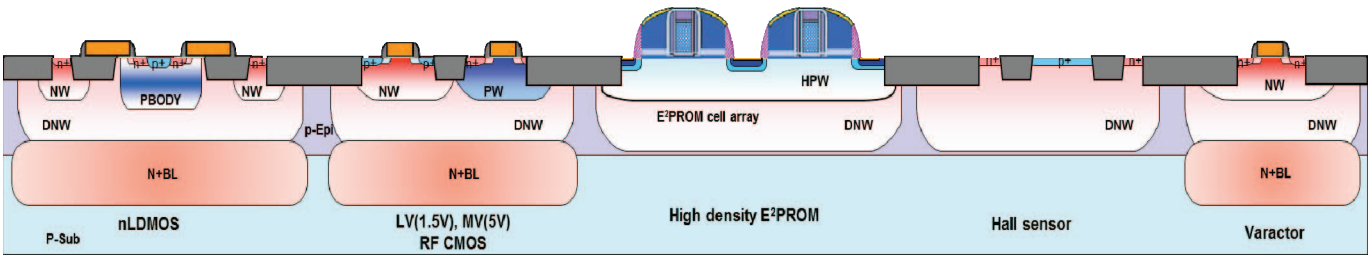

Fig. 1. Vertcal structure of each major device integrated with single process

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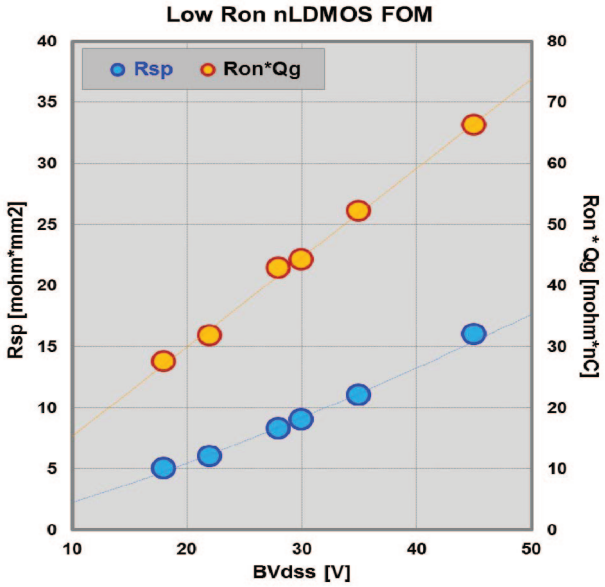

Fig. 2. Rsp and Ron*Qg values of nLDMOS at different voltage rating

C. *High density EEPROM*

Fig. 3 shows a cross-sectional view and transmission electron microscope (TEM) image of the memory cell along the bit line direction. The memory cell has p-well surrounded by deep n-well, shallow trench isolation (STI), double layers of polysilicon, and two layers of metals. As shown, the cell consists of three transistors: One transistor at the central for floating gate and two transistors at the side walls for select gates. The distinguishable characteristic is that select gates are self-aligned to each side of the floating gate, and thus gives small cell size. The cell size is 0.645 μm^2.

In addition, this self-aligned select gates act as control gates. Both programming and erasing of the cell are performed by Fowler-Nordheim (FN) tunneling. Table 1 represents bias conditions for operation. For programming, a 16.5V is applied to word line, while both bit line and well are ground with the floating source line. Note that bit line of unselected cells should be maintained to 9.5V to minimize disturbance between the cells while word line is ground. For erasing, 13.5V is applied to bit line and p-well, respectively, and gate is ground while the source line is floated [7-10].

TABLE 2 Bias condition during programming, erasing and reading for both selected and unselected cells

		Program	Erase	Read
Word Line	Selected	16.5V	0V	3.1V
	Unselected	0V	13.5V	0V
Bit Line	Selected	0V	13.5V	1.0V
	Unselected	9.5V	13.5V	0V
P-Well	Selected	0V	13.5V	0V
Source	Selected	Floating	Floating	0V
	Unselected	Floating	Floating	0V

For fabrication, a 0.13 μm logic process with additional steps to forming EEPROM cell and high voltage is used. The total photo steps for 1.5 & 5V dual voltages are 28. After formation of STI, a tunnel oxide of 82A is grown. Then, bilayer of polysilicon for floating gate and silicon nitride (SiN) are deposited and patterned. The purpose of SiN is to be used for hard mask as well as preventing shortage between controlling and floating gates. After that, thin oxide/nitride/oxide (ONO) multi layers are deposited and patterned. Next, dual gate oxidations are performed to form 125A oxide for 5V and 23A oxide for 1.5V transistors. Again, polysilicon is deposited and patterned to form both control gate in memory cell array and logic gate simultaneously. Separated lightly doped source and drain formation in high voltage as well as logic voltage is performed by ion implantation for both nMOS and pMOS, respectively. After that, normal logic process is used to complete processing.

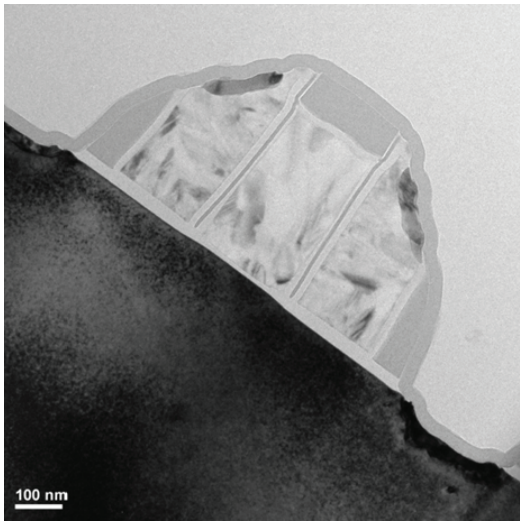

Fig. 3. TEM picture of EEPROM, the smallest cell size, 0.645 μm^2

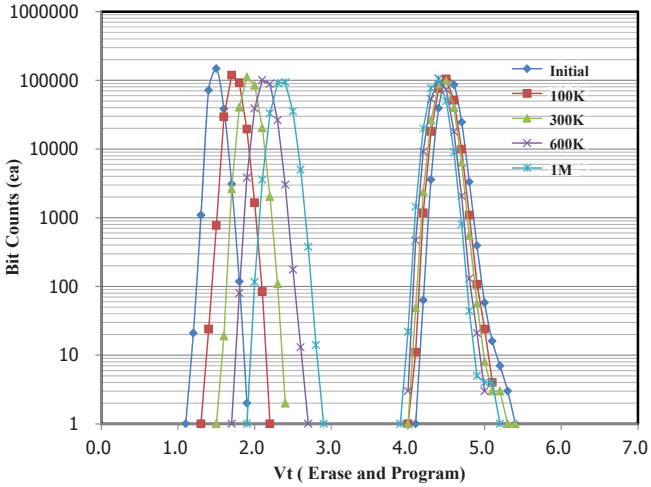

Fig. 4. 1M Endurance with 32KB IP

Fig. 4 reveals erase and program Vt shift after 100K, 300K, 600K, and 1M cycling at 25°C measured from 32KB EEPROM. Also, initial distribution is shown. It appears that erase Vt is increasing with cycling, while program Vt is decreasing. Note that, as shown on Fig. 2, the maximum erase Vt after 100K is 2.3V and this gives enough margin considering that read voltage is 3.1V. For the retention test, the samples are baked at 270°C for 2hr after 100K cycling in 85°C. The minimum program Vt after baking in 32KB EEPROM is 3.6V which is decreased 0.7V. For the embedded application, EEPROM IP size is important item in real chip size.

D. RF CMOS

In general, RFCMOS has been known as a sensitive device in the noise. Therefore it's important to isolate it from substrate and the integrated other devices. We placed it on the fully isolated region which used NBL/DNW layer for substrate isolation and double guard rings for device isolation. Fig. 5 shows RF characteristics of fully isolated 1.5V nMOS and pMOS. They were measured at width/length=2.5/0.13 μm, NF=16. Their cut-off frequency is enough to be used for high frequency RF application.

Fig. 6 shows inductor characteristics prepared with 4 μm Al thick metal. It was measured at symmetric structure with PGS pattern which used for removing eddy current form substrate. Self-resonance frequency is over 5GHz and quality factor is more than 15. It's suitable for wireless applications.

Table 3 summarized on RF performance of RF devices which integrated in this technology

TABLE 3 the summary of RF devices in this technology

Device	Parameter	Unit	Results	Remarks
1.5V CMOS	n/pMOS, Vtlin	V	0.35/0.37	Id=0.1uA*W/L
	n/pMOS, Idsat	uA/um	630/315	
	n/pMOS, Ft	GHz	71.0/35.4	W/L=2.5/0.13um NF=16
1.5V nMOS Varactor	Cmax / Cmin	-	3.0	
MiM Capacitor	Unit cap.	fF/um^2	2.0	Q-factor > 30
HR Poly	Resistance	Kohm/sq	1, 10	
Inductor	Inductance	nH	0.1~10	Symmetric
	Q-factor		> 10	

E. Hall sensor

The Hall sensor evaluated here is a planar type placed on silicon wafer <100>. The sensor was composed of n-type deep well in p-type substrate, four n+ active regions at the each of body corners as the input/output nodes and two metal layers on top of the body as the coil making magnetic field as Fig. 7.

The body, n-type deep well was formed by the suitable ion implantation and followed by well anneal process to deepen the well by the depth of 4~5 μm.

Hall voltage and resistance of the Hall sensor were measured with the each input parameter of forcing voltage, magnetic field and temperature. Hall voltage V_H is proportional to the biased current and orthogonal magnetic field. So, the V_H is defined as [11-12]:

$V_H=S_IIB$ or S_VVB, where S_I and S_V are current sensitivity and voltage sensitivity respectively

Our experimental results showed a good linear relationship to the magnetic field and forcing voltage as Fig. 8 and Fig. 9.

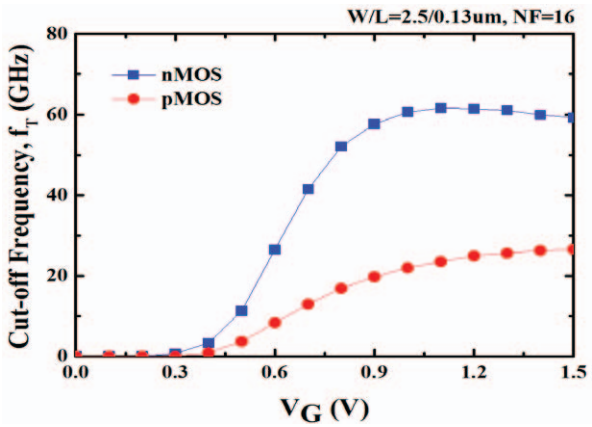

Fig. 5. RF characterisitcs of 1.5V nMOS and pMOS inside NBL/DNW

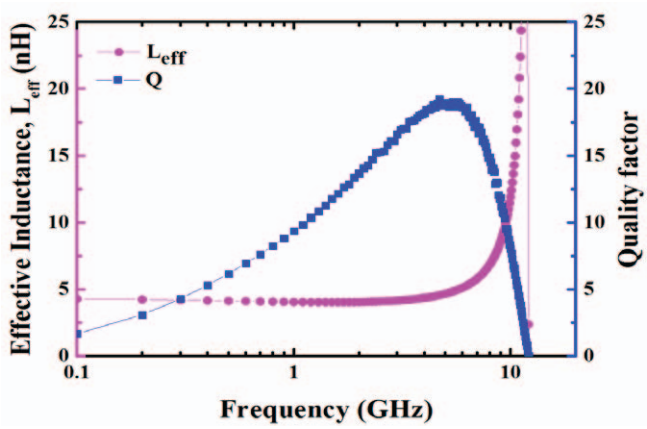

Fig. 6. Inductor characteristic prepared with 4 μm thick metal

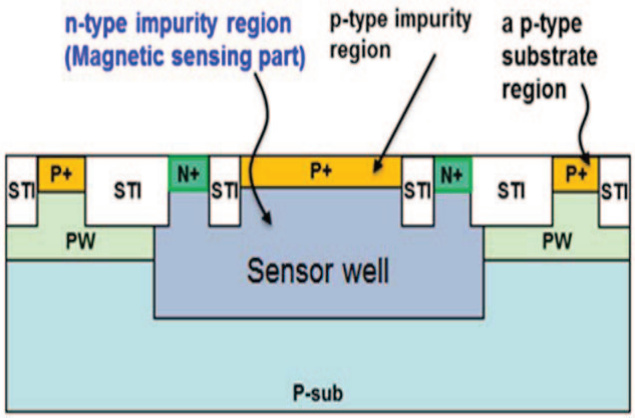

Fig. 7. Cross sectional view of the Hall sensor showing the body of the sensor and the n+ active regions for the nodes. Two metal layers were also plased on the body as the coils generating magnetic field

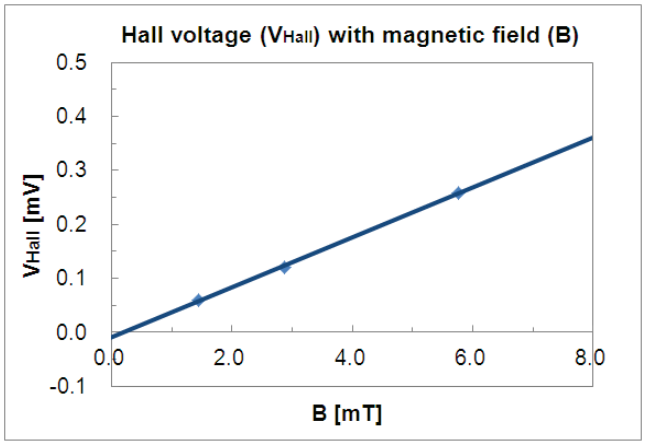

Fig. 8. . Hall voltage shows a good linear relationship to the magnetic field

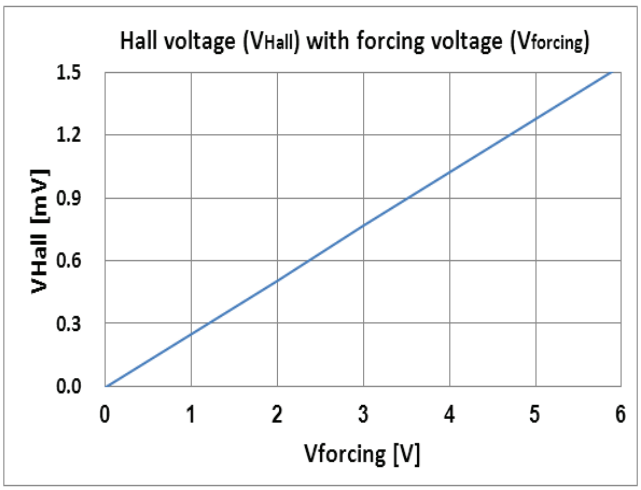

Fig. 9. Measuted Hall voltage is proportional to the forcing voltage

III. Conclusioin

In this paper, we introduced a modular BCD technology with high density EEPROM, RF and Hall sensor for IoT application. For lower power consumption, ultra-low leakage logic transistors and lower Ron and Qg LDMOS have been developed. The leakage level is less than 0.3pA in minimum channel length.-class level and the Ron and Qg of LDMOS are the best-in class level in smart power application.

For MCU of IoT application, high density EEPROM IP with 0.645 μm^2 cell has been verified in this technology and RF devices and Hall sensor also are embedded in 0.13 μm BCD technology.

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