

# Five-Input Majority Gate, a New Device for Quantum-Dot Cellular Automata

Keivan Navi<sup>1,\*</sup>, Samira Sayedsalehi<sup>2</sup>, Razieh Farazkish<sup>2</sup>, and Mostafa Rahimi Azghadi<sup>1</sup>

<sup>1</sup>*Faculty of Electrical and Computer Engineering, Shahid Beheshti University, GC, Tehran 1983963113, Iran*

<sup>2</sup>*Science and Research Branch of IAU, Tehran 14515755, Iran*

Quantum-dot Cellular Automata (QCA) is one of the most attractive technologies for computing at nano-scale. The principle logic element in QCA is majority gate. In this paper, a novel design for 5-input majority gate is presented. A 5-input majority gate study has been proposed; however this study has changed the scheme of basic QCA cells. The new proposed device reduces cell counts and area and uses conventional form of QCA cells. Accuracy of this design is proven by applying some simple physical substantiation and QCADesigner tool is used for verifying majority circuit layout and functionality. Furthermore, a QCA Full-Adder is constructed using the new proposed design. Simulation results demonstrate that the proposed design of majority gates and Full-Adder resulted in significant improvements in designing logical circuits.

**Keywords:** Quantum-Dot Cellular Automata, Majority Gate, Full-Adder, Five-Input Majority Gate, Logic Optimization.

## 1. INTRODUCTION

In recent years CMOS technology demonstrated that it can be readily challenged by other technologies when it arrives at nano-regimes. Due to serious CMOS technology restrictions in nano-scales, researchers have investigated alternative technologies. The ITRS report<sup>1</sup> highlights the summary of future designing technologies. Quantum-dot Cellular Automata is one possible alternative technology. QCA is an emerging technology that offers a revolutionary approach and has demonstrated extra low power, extra high speed and extremely dense digital circuits.<sup>2</sup>

The basic element of QCA circuits is majority gate; hence, efficiently constructing QCA circuits using majority gates has attracted a lot of attention.<sup>3–4</sup> Since a majority-not function forms a universal gate, majority logic can be used for implementing any logical function instead of employing Boolean logic operators. Up to now, most QCA circuits have been investigated and designed only by means of 3-input majority gates. However, if these circuits are constructed using 5-input majority gates, they would be optimized in cell counts, area and complexity.

As the basic element in QCA is majority gate, this paper investigates a novel 5-input majority design. The new proposed scheme for 5-input majority gate uses conventional cells. This new 5-input majority gate has been used to

construct different circuits and functions like Full-Adders and other functions.

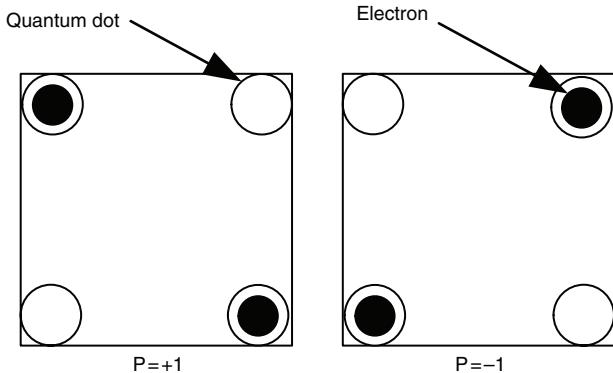
Full-Adders and arithmetic circuits and their optimization methods have attracted a great deal of interests among researchers in VLSI and QCA area.<sup>5–9</sup> A Full-Adder which uses the new majority gate and can be useful in designing other arithmetic circuits like Residue Number System circuits<sup>10–11</sup> is presented. Improving the performance of the Full-Adder cells leads to efficient designing of many arithmetic circuits and the main concern of this paper is to design a high-performance Full-Adder. Simulation results illustrate that the new majority gate resulted in an optimum design for Full-Adder and reduces area and complexity in comparison to the other well-known designs.

In Section 2, a brief review of QCA technology is provided as well as proposal for the implementation of the novel 5-input majority gate. Then accuracy of the proposed design is proven using physical associations. Section 3 introduces an efficient Full-Adder based on the novel proposed 5-input majority gate. Finally, in Section 4 simulation results are presented and conclusions are drawn in Section 5.

## 2. MATERIALS AND METHODS

In this section, some background materials are reviewed in order to understand the structure of QCA. Moreover, the QCA implementation of the new majority gate is

\*Author to whom correspondence should be addressed.



**Fig. 1.** Basic QCA cell and binary encoding.

introduced and some simple physical substantiations which testify to the accuracy of the new design are developed.

## 2.1. Background

A QCA cell, shown in Figure 1, contains four quantum dots positioned at the corners of a square, and two electrons that can move to any quantum dot within the cell through electron tunneling.<sup>12</sup> Due to Columbic interactions, only two stable configurations of the electron pair exist. Assigning a polarization,  $P$ , of  $-1$  and  $+1$  to distinguish between these two configurations leads to a binary logic system.

An array of QCA cells can be arranged to perform as a QCA wire. In a QCA wire, the binary signal propagates from input to output because of the Columbic interactions between cells (Fig. 2).

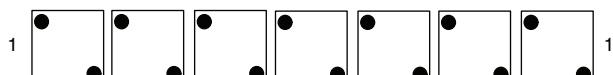
Any QCA circuit can be built using only majority gates and inverters (Fig. 3).<sup>13</sup> Assuming that the inputs are A, B and C, the logic function of a majority gate is shown in Eq. (1).

$$M(A, B, C) = AB + BC + AC \quad (1)$$

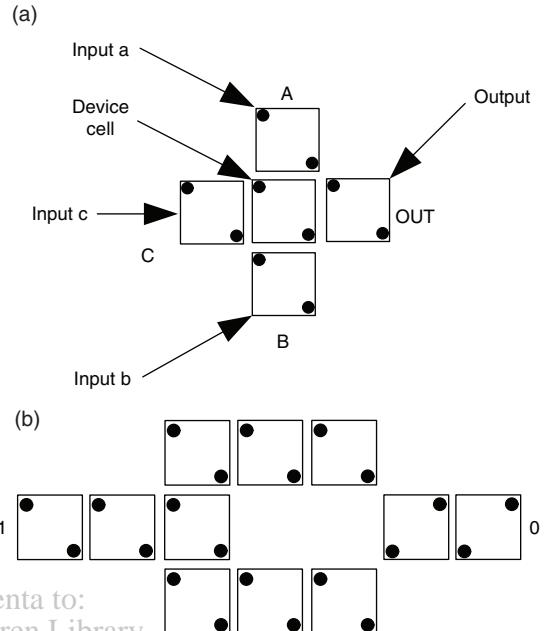
## 2.2. Novel Design for 5-Input Majority Gate

A 5-input majority gate includes five inputs and one output. The logic function of majority voter can be presented as Eq. (2), and the truth table of this majority gate is shown in Table I.

$$\begin{aligned} M(A, B, C, D, E) \\ = & ABC + ABD + ABE + ACD + ACE \\ & + ADE + BCD + BCE + BDE + CDE \end{aligned} \quad (2)$$



**Fig. 2.** A QCA wire.



**Fig. 3.** (a) Majority voter. (b) A QCA inverter.

The new proposed design for 5-input majority gate is shown in Figure 3. In this design, A, B, C, D and E are labeled as inputs and the output cell is labeled as out. Some middle cells, which are device cells are labeled 1, 2, 3, and 4. Equation (3) shows the logical relation of the new proposed majority gate. As depicted in Figure 4, the effect of inputs B, C, D, and E on every single device cells are twice the input A (Eq. (3)) since they are in direct proximity of every two device cells. As an example, assume that input cells A and B have logic 1 values and others have logic 0. In this instance and based on Eq. (3), the logic 1 will have a power equal to  $3 (= 2 + 1)$  out of 9. In other possible case, when input cells C and D have logic 1 value and others have 0 logic, based on Eq. (3), the logic 1 will have a power equal to  $4 (= 2 + 2)$  out of 9 and like the previous example, it is not strong enough to change the vote to logic 1. On the contrary, when more than two inputs are logic 1, their logical power will be equal to 5 or greater, and it leads to a logic 1 in output. The same condition goes for logic 0.

$$\text{Out} = A + 2B + 2C + 2D + 2E \quad (3)$$

**Table I.** Truth table of a five-input majority gate based on sum of inputs.

$\sum(A, B, C, D, E)$	Maj (A, B, C, D, E)
0	0
1	0
2	0
3	1
4	1
5	1

As it is shown in Figure 4(a), in the proposed scheme, a 5-input majority gate using only ten cells and also by considering some physical relation substantiations is implemented. The output of this cell is in the middle and it can go out using another layer and in a vertical manner. It means that the existing feature of QCA circuits which is using in many circuits can be used to the output value of the majority gate comes out.

In all of the computation, the following postulates are assumed:

- All cells are similar and the length of each one is 18 nm and there is a space of  $x$  ( $= 2$  nm) between each two neighbor cells.
- In all figures, squares illustrate a QCA cell and the circles inside illustrate the electrons inside that cell.
- The potential energy between two electron charges is calculated using Eq. (4a). In this equation,  $U$  is potential energy,  $k$  is fixed colon,  $q_1$  and  $q_2$  are electric charges and  $r$  is the distance between two electric charges. By putting the values of  $k$  and  $q$ , we obtain Eq. (4b).  $U_T$  is the summation of potential energies that are calculated from Eq. (5).<sup>14–16</sup>

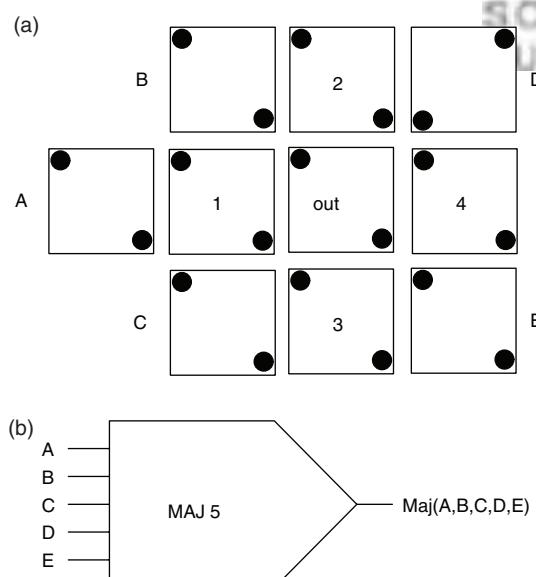
$$U = \frac{kq_1 q_2}{r} \quad (4a)$$

$$kq_1 q_2 = 9 * 10^9 * (1.6)^2 * 10^{-38} = 23.04 * 10^{-29} = A = \text{cte} \quad (4b)$$

$$U_T = \sum_{i=1}^2 U_i \quad (5)$$

### 2.3. Physical Proof

As a 5-input majority gate has 32 different input states, we should check all the states to verify the accuracy of the



**Fig. 4.** Majority gate (a) Proposed 5-input majority gate (b) Symbol of the 5-input majority gate.

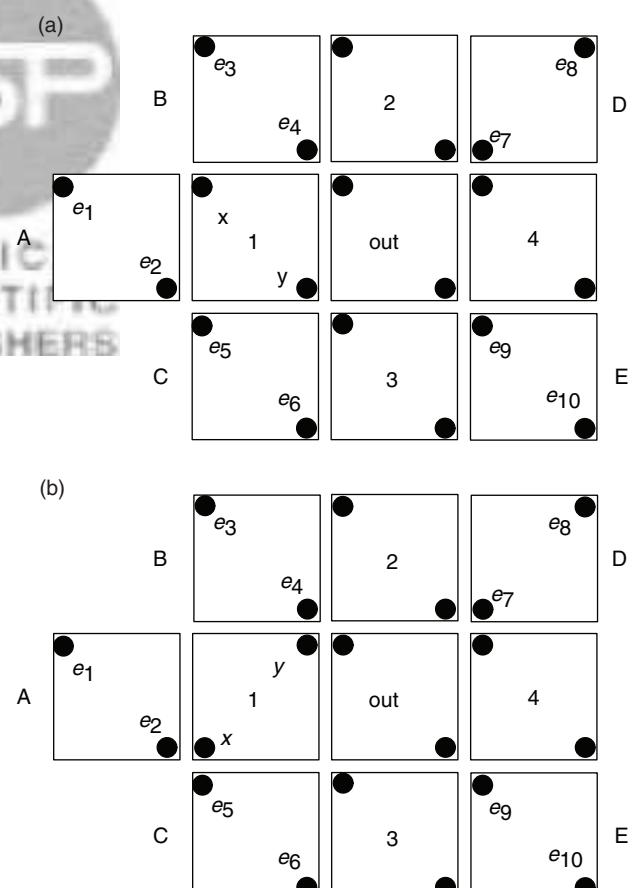
gate. Here, only one state ( $A = B = C = E = 1$  and  $D = 0$ ) is proved while the other states can be proved as well. It should be noted that in order to achieve more stability, electrons of QCA cell are arranged in such a manner that their potential energy reaches the minimum level.

First, we gain the potential energy that exists between each electron ( $e_1, e_2, e_3, e_4, e_5$  and  $e_6$ ) and “ $x$ ” and “ $y$ ” electrons in (a) (Fig. 5(a)) and (b) (Fig. 5(b)) using Eqs. (4a) and (4b). Then we calculate the total potential energy ( $U_T$ ) in both states using Eq. (5). The comparison of total potential energies in both (a) and (b) would indicate which state (a or b) is more stable. With determining the value of cell 1 and with considering input cells B, C, D and E the values of cell 2, 3 and 4 can be simultaneously computed in a similar manner to that for cell 1. Then, having all values of cells 1, 2, 3 and 4, the value of out cell can be computed, which gives us a majority decision of inputs A, B, C, D, and E.

As the proof method is similar for all cells and their values, only the first part of this proof is stated and the rest of relations are omitted due to the lack of space.

Figure 5(a) (electron x):

$$U_1 = \frac{A}{r_1} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20} (J)$$



**Fig. 5.** (a) The one value in cell 1 (b) The zero value in cell 1.

$$U_2 = \frac{A}{r_2} = \frac{23.04 * 10^{-29}}{18.11 * 10^{-9}} \approx 1.27 * 10^{-20}(J)$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J)$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 * 10^{-29}}{18.11 * 10^{-9}} \approx 1.27 * 10^{-20}(J)$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J)$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 * 10^{-29}}{42.04 * 10^{-9}} \approx 0.55 * 10^{-20}(J)$$

$$U_{T_{11}} = \sum_{i=1}^6 U_i = 6.54 * 10^{-20}(J)$$

$$U_{T_1} = \sum_{i=1}^2 U_{1i} = 12.36 * 10^{-20}(J)$$

Figure 5(a) (electron y):

$$U_1 = \frac{A}{r_1} = \frac{23.04 * 10^{-29}}{42.04 * 10^{-9}} \approx 0.55 * 10^{-20}(J)$$

$$U_2 = \frac{A}{r_2} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J)$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 * 10^{-29}}{42.04 * 10^{-9}} \approx 0.55 * 10^{-20}(J)$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J)$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 * 10^{-29}}{18.11 * 10^{-9}} \approx 1.27 * 10^{-20}(J)$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J)$$

$$U_{T_{12}} = \sum_{i=1}^6 U_i = 5.82 * 10^{-20}(J)$$

Since cells D and E are generally a long distance from cell 1, their potential energy can be neglected.

Figure 5(b) (electron x):

$$U_{T_{21}} = \sum_{i=1}^6 U_i = 26.23 * 10^{-20}(J)$$

$$U_{T_2} = \sum_{i=1}^2 U_{2i} = 41.55 * 10^{-20}(J)$$

Figure 5(b) (electron y):

$$U_{T_{22}} = \sum_{i=1}^6 U_i = 15.32 * 10^{-20}(J)$$

With comparison of the achieved results, the electrons in cell 1 will be positioned in state (a) because this state is more stable and has a lower potential energy. As already

mentioned, the computation of potential energies for other cells (2, 3, and 4) is similar to those for cell 1 and only the final results are stated. It is worth mentioning that in all cells  $U_{T_1}$  is the potential energy in +1 polarization and  $U_{T_2}$  is the potential energy in -1 polarization.

cell2:

$$U_{T_1} = 20.52 * 10^{-20}(J)$$

$$U_{T_2} = 21.37 * 10^{-20}(J)$$

cell3:

$$U_{T_1} = 18.23 * 10^{-20}(J)$$

$$U_{T_2} = 31.08 * 10^{-20}(J)$$

cell4:

$$U_{T_1} = 24.73 * 10^{-20}(J)$$

$$U_{T_2} = 32.36 * 10^{-20}(J)$$

Considering the above computation, it is inferable that the proposed structure for implementing a 5-input majority gate is completely correct and resulted in an accurate state for the output cell which shows the majority voter.

After physical proof, we can also check the proposed design using QCADesigner. Simulation of this majority gate is shown in the simulation results section. Next section reviews the previous Full-Adders and also introduces a new design of QCA Full-Adder based on the proposed 5-input majority gate.

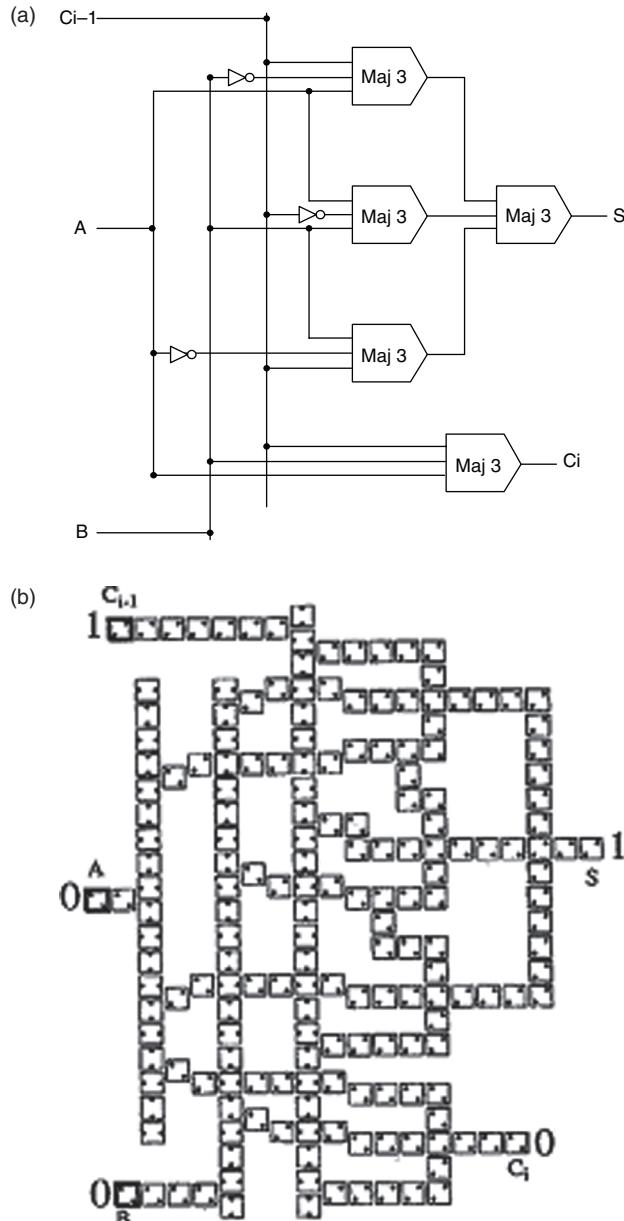
### 3. QCA FULL-ADDERS

The basic building block of QCA circuit is majority gate. Up to now, almost all QCA designs employed three-input majority gates and using five-input majority gates in designing QCA circuits is practically an unexplored research area.

The first QCA Full-Adder consists of five 3-input majority gates and three inverters.<sup>12, 17</sup> The schematic and layout of this Full-Adder is shown in Figure 6. This design can be simplified by applying various methods of reduction such as<sup>18</sup> based on genetic algorithm and also deterministic methods like Ref. [19].

Another Full-Adder design is introduced in Ref. [20]. In this design a new method for reducing the number of majority gates and inverters for a Full-Adder is used. Figure 7 demonstrates this design which includes three majority gates and two inverters. This Full-Adder has four clock phases. After proposing this design, most studies used this scheme for implementing one bit QCA Full-Adder.<sup>2, 21–22</sup>

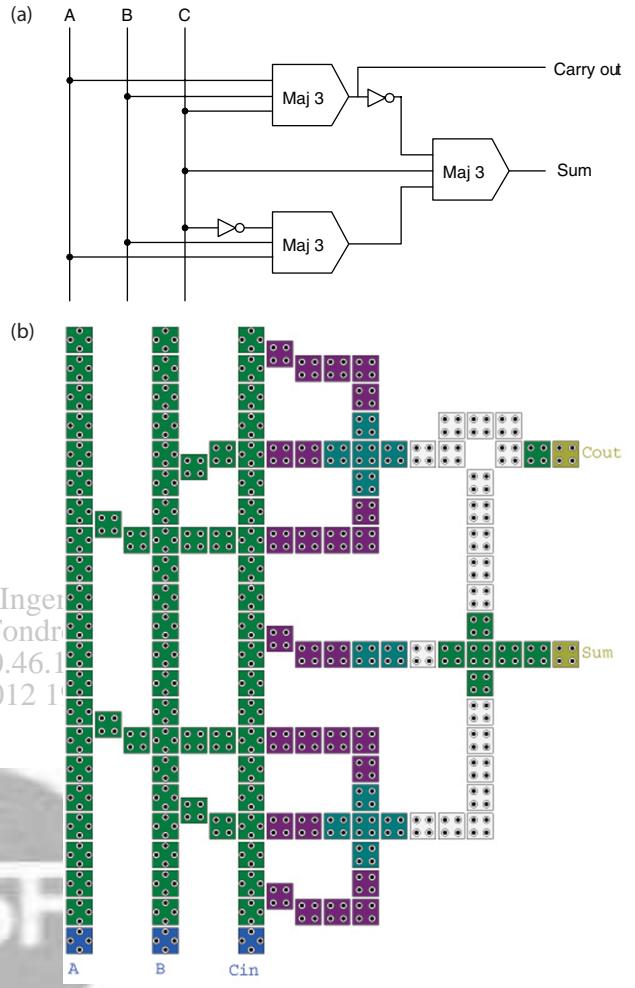
The next QCA Full-Adder has simplified the complexity of previous designs and reduced the number of both majority gates and inverters. The proposed design has only two majority gates and one inverter (Fig. 8). In order to construct this new Full-Adder, another form of majority gate has been presented and also a new scheme of QCA



**Fig. 6.** One bit QCA Full-Adder. (a) Schematic of the first QCA Full-Adder. (b) Layout of this Full-Adder.<sup>12, 17</sup>

cells has been expressed.<sup>8</sup> In Ref. [8] a 3-dimensional scheme for implementing QCA cells was proposed. However, this design is unexplored and it cannot be simulated using the existing QCA simulators. As already stated, this paper presents a new schematic for five-input majority gates which uses only ordinary QCA cells and it can be simply simulated and constructed as other conventional form of QCA circuits can.

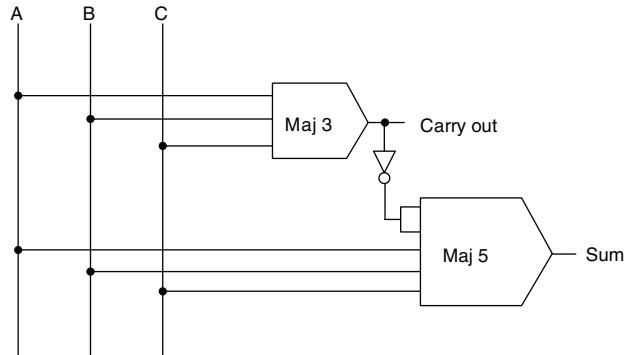
The last QCA Full-Adder is introduced in Ref. [23]. This new design employs the conventional scheme of QCA Full-Adders (three majority gates and two inverters).<sup>2, 20–22</sup> Because the input bit flows downward and carry propagates from right to left, this design is called Carry flow



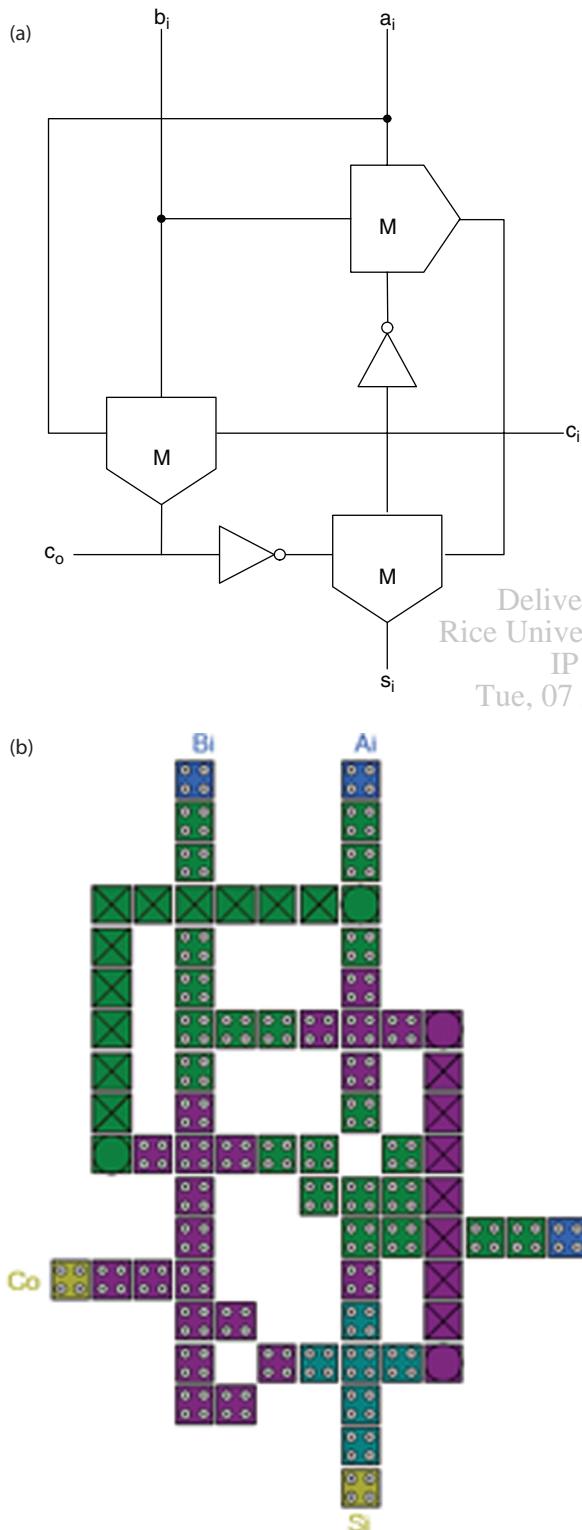
**Fig. 7.** The Full-Adder based on three 3-input majority gates and 2 inverters. (a) Shchematic of the Full-Adder. (b) Layout of the Full-Adder.<sup>20</sup>

Full-Adder. This Full-Adder is optimized to minimize the delay. Figure 9 shows the schematic design and the layout of this Full-Adder.

The proposed Full-Adder is shown in Figure 10. As illustrated in Figure 10(a), the proposed circuit includes two inverters and two majority gates and has a completely

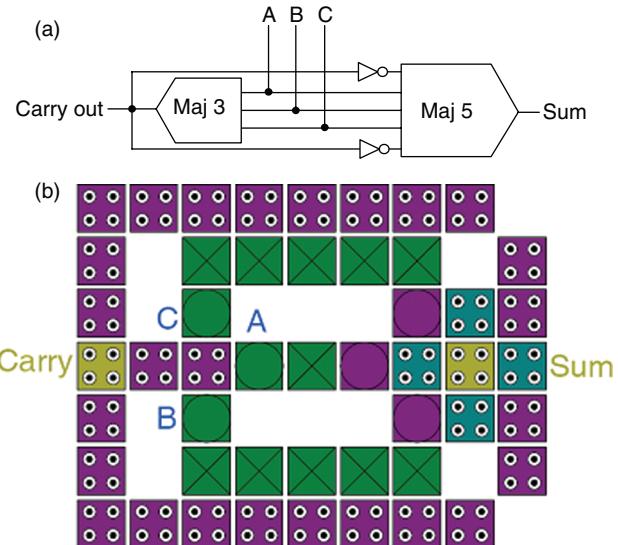


**Fig. 8.** Schematic logic diagram of QCA Full-Adder with only two majority gates and one inverter.<sup>8</sup>



**Fig. 9.** Carry flow Full-Adder (a) Shchematic of this Full-Adder. (b) Layout of this Full-Adder.<sup>23</sup>

symmetric structure. Table II compares the previous QCA Full-Adders with the proposed Full-Adder (Fig. 10) in terms of gate count, area, complexity, and latency. It can be seen in Table II that the proposed design consume smaller



Delivered by Internet  
Rice University, Fondren Library

IP : 93.80.46.15  
Tue, 07 Aug 2022 09:17:58

area, has lesser cell counts while has an equal latency to the fastest previous design.<sup>23</sup>

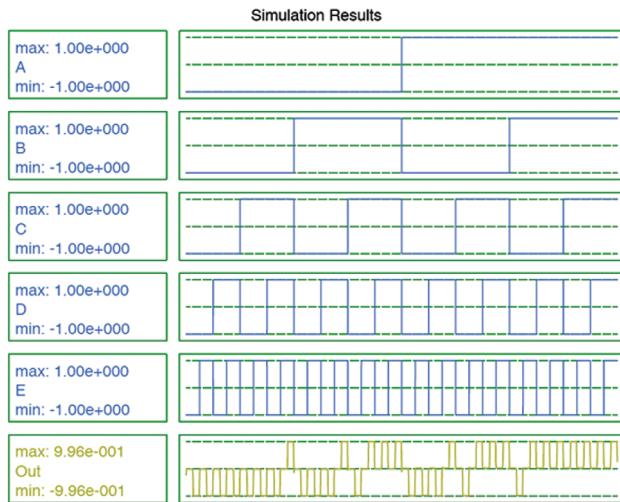
#### 4. SIMULATION RESULTS

The proposed QCA majority gate and Full-Adders are implemented and simulated using QCADesigner version 2.0.3.<sup>24</sup> The following parameters are used for a bistable Approximation simulation engine:

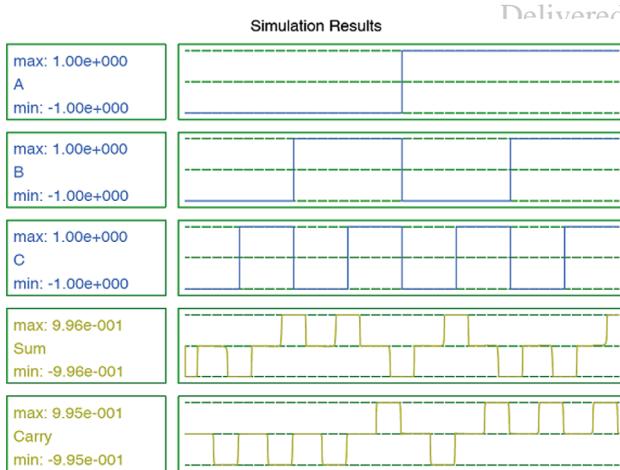
Cell size = 18 nm,  
Number of samples = 50000,  
Convergence tolerance = 0.0000100,  
Radius of effect = 65.000000 nm,  
Relative permittivity = 12.900000,  
Clock high = 9.800000e-022 J,  
Clock low = 3.800000e-023 J,  
Clock shift = 0,  
Clock amplitude factor = 2.000000,  
Layer separation = 11.500000,  
Maximum iterations per sample = 100.

**Table II.** Comparison of QCA Full-Adders in terms of gate count, area, complexity, and latency.

Circuit	Gate count	Area ( $\mu\text{m}^2$ )	Complexity	Latency
The first design in Ref. [17]	5 majority gates and 3 inverters	0.20	192	>1 clock
The second design in Ref. [20]	3 majority gates and 2 inverters	0.17	105	1 clock
The forth design in Ref. [23]	3 majority gates and 2 inverters	0.10	86	0.75 clock
The proposed Full-Adder	2 majority gates and 2 inverters	0.03	61	0.75 clock



**Fig. 11.** Simulation results for the proposed 5-input majority gate.



**Fig. 12.** Simulation results for the proposed Full-Adder.

Most of the mentioned parameters are default values in QCADesigner. The simulation results for novel 5-input majority gate is shown in Figure 11. As it is obvious from this figure, the output signal is in a highly polarized state ( $|p| \approx 1$ ). This simulation results are the same as the results of physical proofs that was mentioned in section II. Moreover, Figure 12 illustrates simulation result of the proposed Full-Adder.

## 5. CONCLUSION

In this paper, a novel 5-input majority gate has been proposed. This device has been implemented in one layer and using only ten QCA cells. As far as verifying the functionality, this proposed majority gate has been proven by some physical relations as well as computer simulations. In order to verify the accuracy and usefulness of the new majority gate design a QCA Full-Adder which is based on the novel 5-input majority gate is presented. This design

requires only two majority gates and two inverters which are implemented by means of diagonal cells.

The new Full-Adder and previous Full-Adder designs have been compared in terms of complexity, area and latency. These designs have been verified in QCADesigner, a QCA simulation and layout verification tool. Simulation results reveal that the new Full-Adder has a simpler structure and also needs less cell counts and area compared to the previous designs while having an equal latency to the best previous one. Since the new Full-Adder has a superior structure it can be inferred that it would result in advances in future arithmetic QCA circuit designs.

**Acknowledgment:** This work is supported by the Research Council Grant of Shahid Beheshti University, GC, under contract number 600/1206.

## References

1. International Technology Roadmap for Semiconductors, (ITRS), Available: <http://www.itrs.net> (2005).
2. H. Cho and Earl E. Swartzlander, Jr., *IEEE Trans. Nanotechnol.* 6, 374 (2007).
3. R. Zhang, K. Walus, W. Wang, and G. Jullien, *IEEE Trans. Nanotechnol.* 3, 443 (2004).
4. J. Huang, M. Momenzadeh, M. B. Tahoori, and F. Lombardi, Design and characterization of an And-Or-Inverter (AOI) gate for QCA implementation, *Proc. Great Lakes Symp, VLSI (GLSVLSI)*, Boston (2004), pp. 426–429.
5. K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, *Integration, the VLSI Journal* 42, 457 (2009).
6. K. Navi, M. Moayeri, R. Faghah Mirzaee, O. Hashemipour, and B. Mazloom Nezhad, *Microelectron. J.* 40, 126 (2009).
7. K. Navi, M. Maeen, and O. Hashemipour, *IEICE Electronic Express* 6, 553 (2009).
8. M. Rahimi Azghadi, O. Kavehei, and K. Navi, *J. Appl. Sci.* 7, 3460 (2007).
9. R. Farazkish, M. R. Azghadi, K. Navi, and M. Haghparast, *World Applied Sciences Journal* 6, 793 (2008).
10. S. Timarchi and K. Navi, *IEEE Transactions on Instrumentation and Measurement* 58, 2959 (2009).
11. A. S. Mollahosseini, K. Navi, C. Dadkhah, O. Kavehei, and S. Timarchi, *IEEE Transactions on Circuit and Systems I* 57, 823 (2010).
12. P. D. Tougaw and C. S Lent, *J. Appl. Phys.* 75, 1818 (1994).
13. K. Kim, W. U. Kaijie, and K. Ramesh, *IEEE Transactions on Fundamentals* E89-A, 1607 (2006).
14. D. Halliday and A. Resnick, *Fundamentals of Physics*, 7th edn., John Wiley and Sons, Inc, New York (2004), Chaps. 3–6.
15. Mc. Dermott and C. Lillian, *Physics Today* 37, 24 (1984).
16. I. Halloun and D. Hestenes, *American Journal of Physics* 53, 1056 (1985).
17. C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, *Nanotechnology* 4, 49 (1993).
18. M. R. Bonyadi, M. Rahimi Azghadi, N. Rad, K. Navi, and E. Afjei, *IEEE, Int. Conf. on Electrical Engineering (ICEE07)* 1 (2007).
19. H. Zhi, Q. Zhang, S. Haruehanroengra, and W. Wang, Logic optimization for majority gate based nanoelectronic circuits, *International Symposium on Circuits and Systems ISCAS*, Island of Kos (2006), pp. 1307–1310.
20. W. Wang, K. Walus, and G. A. Jullien, Quantum-dot cellular automata adders, *3rd IEEE Conference on Nanotechnology*, San Francisco, CA USA (2003), pp. 461–464.

21. H. Cho and E. Swartzlander, Jr., Serial parallel multiplier design in quantum-dot cellular automata, *18th IEEE Symposium on Computer Arithmetic (ARITH'07)*, Montpellier, France (2007), pp. 7–15.
22. A. Vetteth, K. Walus, G. A. Jullien, and V. S. Dimitrov, Quantum dot cellular automata carry-look-ahead adder and barrel shifter, *IEEE Emerging Telecommunications Technologies Conference*, Dallas, TX (2002), pp. 1–5.
23. H. Cho and Earl E. Swartzlander, Jr., *IEEE Transactions on Computers* 58, 721 (2009).
24. K. Walus, T. Dysart, G. Jullien, and R. Budiman, *IEEE Trans. Nanotechnol.* 3, 26 (2004).

Received: 11 November 2009. Accepted: 18 December 2009.

Delivered by Ingenta to:  
Rice University, Fondren Library  
IP : 93.80.46.15  
Tue, 07 Aug 2012 19:17:38

