Proper QCA Five-input Majority Gate to Design Optimal Complex Circuit

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***Abstract*— This article analyzes and compares previously published five input majority gates. These designs do not give good results in physical properties. Therefore, a low-power five-input majority gate is proposed in a single layer, which uses a minimum number of cells and a smaller area, and achieves a highly polarized output compared to previous designs. Structural and power dissipation analysis is conducted to assess implementation. The results of the analysis show that this structure works well compared to existing designs. The QCADesiner tool is used to verify the simulation results of the proposed design, and the QCAPro tool is used to evaluate the power dissipation of all considered designs.**

Keywords—majority gate; QCA; fundamental circuit; power dissipation

I. INTRODUCTION

CMOS has served as a superior technology for implementing schemes in recent years [1]. Over the years, the size of the transistors was reduced on demand, and eventually reached at the nanoscale. However, this leads to many problems such as rising chip temperature and increasing power consumption [2-5]. Many researchers are proposing new promising technologies that do not face similar problems, with smaller in size, have better power consumption and faster speeds. One of the proposed technologies is a quantum-dot cellular automata (QCA).

The new transistor-less paradigm QCA is presented for the implementation of a nanoscale device with a high density and terahertz speed switching.

The main logic device in QCA, a majority gate has attracted the attention of many researchers. Depending on the number of entrances, generally majority gate can be divided into three and five input majority gate [5]. As the complexity of the circuit increases, most of the five input majority gate have unique advantages in some circuits, such as a full adder.

In this work, a contribution is to propose low complexity 5-input majority gate with low power dissipation. The article is further divided into four parts. Section II describes the QCA's background. Related works to the paper is provided in Section III. Section IV explains the proposed work with detail analysis. Comparison part is also included in section V. Conclusion is displayed in the last section, section VI.

II. QCA BACKGROUND

A. QCA cell

The QCA cell has a square shape consisting of four quantum dots, where a pair of electrons are occupied diagonally due to the columbic push. Here electrons can move through a tunnel between adjacent dots [3-10]. However, due to the high potential in the QCA cell, it cannot tunnel between neighboring cells. Therefore, depending on the polarity of the QCA cell, there are two states, as shown in Fig 1.: - 1 (logic "0") and + 1 (logic 1).

B. QCA Logic Gates

A fundamental element that has attracted the attention of many researchers on the QCA platform is the majority gate. Using this gate, designers can make logical AND or OR gates by entering values of -1 or +1, respectively. The Majority Gate (MG3) is shown in Fig 2. The logical equation of the Maj-3 gate is given by the equation. 1 [9-16].

$$MG3 = AB+BC+AC \quad (1)$$

C. QCA Clock

Clocking is important for QCA paradigm for the following reasons: synchronization, power compensation, and data direction management. It also provides the power to encourage the scheme. To achieve clock signal synchronization, management of potential barriers between dots within the cell is required. When the potential barriers rise to their maximum value, the electrons localize them. At this time, the polarization of the cell occurs [13-22]. The clock signal has four time zones, and four phases in each zone as shown in Fig 3.

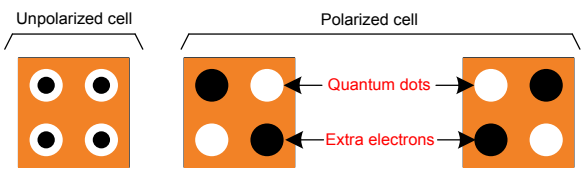

Fig. 1. Basic QCA cell

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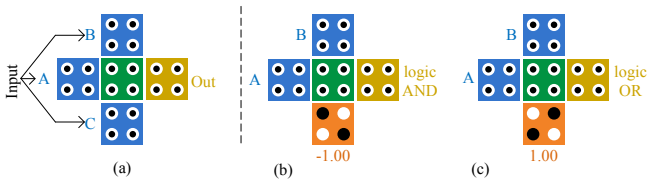

Fig. 2. QCA 3-input MG: (a)original form, (b)AND gate, (c)OR gate

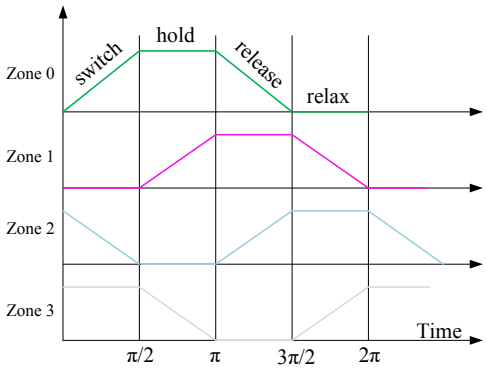

Fig. 3. QCA clock

D. QCA 5-input MG

The five-input majority gate is a logical gate that can vote for the majority of the five input cells. That is, if 3 or more input cells are 1, only the polarity of the output cell is 1. The logical expression for this gate can be written as follows:

$$MG5=ABC+ABD+ABE+ACD+ACE+ADE+BCD+ +BCE+BDE+CDE \quad (2)$$

III. Related Works

To reduce the cost of QCA schemes, researchers are trying to theorize an optimal and minimized structure for the five input majority gates. So far, most of the various five-input structures have been proposed. Compared to multi-layer QCA design, single-layer QCA design is simple to implement. Most multilayer MG5 have natural advantages over singlelayer counterparts.

The first MG5 structure was proposed in a multilayer layer [9]. Its output cell is surrounded by other cells. This prevents this door from being used in the design of single-layer QCA schemes. Later, many structures were proposed in various schemes, such as full adder and RAM designs [10-14]. However, most of these gates do not work very well in physical features or applications. In this study, it is difficult to apply in some schemes because the input cells are closed to each other. Some recommended five-inlet structures with minimal cell and area may be noise resistant.

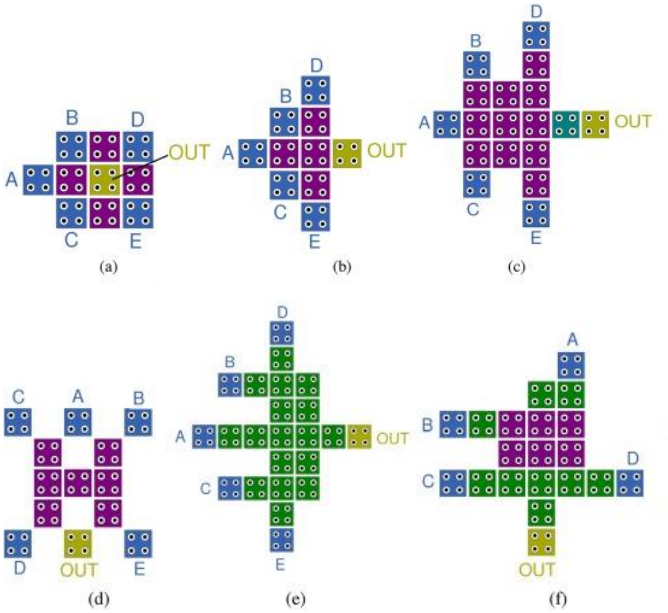

Fig. 4. QCA 5-input MG: (a) design in [9], (b) design in [10], (c) design in [11], (d) design in [12], (e) design in [13], (f) design in [14]

IV. Proposed Aproaches

In the bistable approximation model in QCADesigner[22], each QCA cell(18 *nm* × 18 *nm*) has a spacing of 2 *nm*. The radius effect of between two cells is about 65 *nm*. In a coplanar system with a radius of 41 nm, the drive cell can act up to two cells in one direction. The location of cells can be defined as regions, and the location of input and output cells can be defined as input regions and output regions, respectively.

In this article, based on the above principle, a new five-input majority gate is designed. The proposed low complexity and ultra-low power consumption five-input majority gate is shown in Fig. 5.

A. Structural analysis

The implementation and simulation is carried out on QCADesigner tool which is accurate simulation tool for QCA. Simulation parameters is presented in Table II. There are 12 quantum cells in implementation with a usage area of 11858 nm^2. The output is generated after 0.25 clock cycle delay. The simulation result confirms that the proposed structure is working well, as shown in Fig 6.

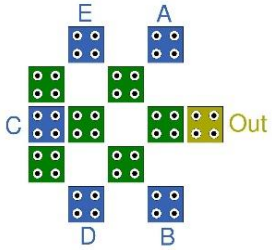

Fig. 5. QCA design of the proposed MG5

Fig. 6. The simulation result of the proposed structure

B. *Power dissipation analysis*

For a detailed analysis of the proposed design, the energy dissipation through QCAPro tool [23] was calculated. In QCA circuits, QCAPro analyzes the total energy dissipation in two main energy categories called 'leakage energy' and 'switching energy' dissipation. The energy losses corresponding to the switching cycles and energy losses corresponding to clock transaction of the QCA cells leads to the 'switching energy' and 'leakage energy' dissipation, respectively. The power analysis is conducted by considering three different energy levels (0.5 E_k, 1.0 E_k and 1.5 E_k) at a temperature of 2 *K*.

In Table 3, the power dissipation results of the proposed design are given in according to the average leakage energy, switching energy, and circuit power dissipation, respectively, for the three different tunnelling energy levels at 2*K* temperature.

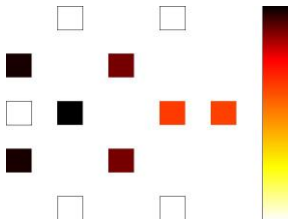

Fig. 7. Power dissipation map of the proposed MG5

TABLE I.

Circuits	QCA circuit complexity		
	The cell count	*Total area (nm^2)*	*Latency (clock cycle)*
Design in [9]	10	6318	0.25
Design in [10]	10	9438	0.25
Design in [11]	18	18998	0.25
Design in [12]	13	11858	0.25
Design in [13]	23	27738	0.25
Design in [14]	20	22218	0.75
Proposed	12	11858	0.25

TABLE II.

Parametrs	The simulation Engine	
	Bistable approximation	*Coherence vector*
Cell size	18 nm	18 nm
Dot diameter	5 nm	5 nm
Cell separation	2 nm	2 nm
Layer separation	11.5 nm	11.5 nm
Clock high	9.8e -022 J	9.8e -022 J
Clock low	3.8e -023 J	3.8e -023 J
Clock shift	0	0
Clock amplitude factor	2.0	2.0
Relative permittivity	12.9	12.9
Radius of effect	65 nm	80 nm
Number of samples	50 000	-
Convergence tolerance	0.001	-
Max. iterations per sample	100	-
Temperature	-	1 K
Total simulation time	-	7e -011 s

V. COMPARISON

To verify the performance of the proposed structure, physical properties of the design is compared with previous designs in terms of cell counts, area and latency. The proposed gate uses a minimum number of cells and a smaller area as shown in Table I. The power dissipation of the proposed gate is also lower than the previous designs. Fig. 7 shows the power dissipation map for proposed gate at 0.5 E_K tunneling energy at 2 K. Table III lists power dissipation results of the proposed gate and previous designs. The received results confirm that utilizing the suggested approach to QCA circuits provides significant optimization for the system.

TABLE III.

The circuits	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Avg. energy dissipation of circuit (meV)		
	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k
[9]	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
[10]	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
[11]	3.44	10.67	19.52	32.66	29.89	27.01	36.1	40.56	46.53
[12]	3.72	9.34	15.39	7.34	6.12	5.1	11.06	15.45	20.49
[13]	4.44	14.25	26.61	45.51	41.59	37.29	49.96	55.84	63.9
[14]	4.41	13.55	24.73	31.24	28.31	25.21	35.66	41.85	49.94
Proposed	2.98	8.11	13.58	7.07	5.54	4.4	10.06	13.66	17.98

VI. Conclusion

This article proposes five input MG with ultra-low complexity. Its accuracy is further verified using simulation in QCADesigner. Compared to previous designs, this structure uses a minimum number of cells and a smaller area to achieve the expected high polarization result. The results show that the physical properties of the proposed 5-input MG are the best in the previous structures. The cost of a particular physical schemes based on this gate can be significantly reduced, especially in power consumption.

References

[1] J. C. Jeon, “Designing nanotechnology QCA–multiplexer using majority function-based NAND for quantum computing,” J Supercomput, (2020). https://doi.org/10.1007/s11227-020-03341-8.

[2] G. H. Bernstein, Quantum-dot cellular automata: computing by field polarization, in: Proceedings of Design Automation Conference, 2003, pp. 268-273.

[3] N. Safoev, and J. C. Jeon, “Reliable Design of Reversible Universal Gate Based on QCA,” Advanced Science Letters, vol. 23(10), pp. 9818-9823, 2017.

[4] N. Safoev and J. C. Jeon, "Implementation of high-speed shifting operation in quantum-dot cellular automata technology." Int J Mech Eng Technol. Vol. 10 (2), pp. 576-586, (2019).

[5] F. Deng, G. Xie, S. Wang, X. Cheng and Y. Zang, " An ultra-low power five-input majority gate in quantum-dot cellular automata." Journal of Circuits, Systems and Computers. doi:10.1142/S0218126620501765, (2019).

[6] N. Safoev and J. C. Jeon, "Coplanar Qca Adders for Arithmetic Circuits." International Journal of Engineering & Technology. Vol. 7 (4.4), pp. 15-16, (2018).

[7] N. Safoev and J. C. Jeon, "Peres Gate Realization in QCA for Reversible Binary Incrementer." Advanced Science Letters. Vol. 23 (10), pp. 9812-9817, (2017).

[8] N. Safoev, and J. C. Jeon, A novel controllable inverter and adder/subtractor in quantum-dot cellular automata using cell interaction based XOR gate, Microelectronic Engineering, vol. 222, (2020), 111197

[9] K. Navi, S. Sayedsalehi, R. Farazkish, and M. R. Azghadi, Five-input majority gate, a new device for quantum-dot cellular automata, Journal of Computational and Theoretical Nanoscience. 7 (2010) 1546-1553..

[10] K. Navi, R. Farazkish, S. Sayedsalehi, and M. Rahimi Azghadi, A new quantum-dot cellular automata full-adder, Microelectronics Journal. 41 (2010) 820-826.

[11] R. Akeela, and M. D. Wagh, "A five-input majority gate in quantum-dot cellular automata." pp. 978-981.

[12] S. R. Kassa, and R. K. Nagaria, A novel design of quantum dot cellular automata 5-input majority gate with some physical proofs, Journal of Computational Electronics. 15 (2015) 324-334.

[13] S. Angizi, S. Sarmadi, S. Sayedsalehi, and K. Navi, Design and evaluation of new majority gate-based ram cell in quantum-dot cellular automata, Microelectronics Journal. 46 (2015) 43-51.

[14] S. Hashemi, and K. Navi, A novel robust qca full-adder, Procedia Materials Science. 11 (2015) 376-380.

[15] N. Safoev and J. C. Jeon, "Low Complexity Design of Conservative QCA with Two-Pair Error Checker." Advanced Science Letters. Vol. 23 (10), pp. 10077-10081, (2017).

[16] N. Safoev and J. C. Jeon, "Compact RCA based on multilayer quantum-dot cellular automata." Information Systems Design and Intelligent Applications. pp. 515-524, (2018).

[17] Jeon J. C. (2019) Low complexity QCA universal shift register design using multiplexer and D fip-fop based on electronic correlations. J Supercomput. https ://doi.org/10.1007/s1122 7-019-02962 -y

[18] N. Safoev, J. C. Jeon (2020) Design of high-performance QCA incrementer/decrementer circuit based on adder/subtractor methodology. Microprocess Microsyst 72:102927

[19] N. Safoev, and J. C. Jeon, "Design and Evaluation of Cell Interaction Based Vedic Multiplier Using Quantum-Dot Cellular Automata." Electronics. Vol. 9(6), pp. 1036, (2020).

[20] J. C. Jeon (2016) Low hardware complexity QCA decoding architecture using inverter chain. Int J Control Autom 9:347–358.

[21] N. Safoev, and J. C. Jeon, “Cell Interaction Based QCA Multiplexer for Complex Circuit Design,” Advanced Science Letters, vol. 23(10), pp. 10097-10101, 2017.

[22] Walus K, Dysart TJ, Jullien GA, Budiman RA (2004) QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans Nanotechnol 3:26–31

[23] Srivastava, S., Asthana, A., Bhanja, S., Sarkar, S.: QCAPro-an error-power estimation tool for QCA circuit design. In: Circuits and Systems (ISCAS), 2011 IEEE International Symposium on 2011May 15, pp. 2377–2380. IEEE