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Efficient Design of Full Adder and Subtractor using 5-input Majority gate in QCA

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***Abstract*— Quantum dot cellular automata is the recent trend in the field of technology for the designing of any digital circuit involving inverters and majority gates that has the potential to substitute the age old technology of CMOS at the order of Nano level. Herein a full adder and full subtractor circuit is proposed using 5-input majority gate. The new full adder and subtractor reduced the requirement of occupied area, number of cells and energy dissipation. QCAPro tool is used for the calculation of energy dissipation. QCA designer 2.0.3 is used to design and simulate the circuits. A 4-bit ripple carry adder is also designed by one bit full adder.**

Keywords—QCA, CMOS, Majority gate, Clocking, Adder, Subtractor.

I. INTRODUCTION

VLSI is one of the crucial technology known for high rate processing speed and abrupt scaling in feature size. But now a days due to short channel effects, ultra thin gate oxide, doping fluctuations and expensive lithography at nano scale level [1], it possesses some complications. In order to overcome the limitations of VLSI technology, QCA technology has come out with more quality attributes like high speed, less energy dissipation and small size [2,3].

In the past several circuits based on QCA are designed but are peril to fluctuations, robustness and lack of efficiency in terms of cell number and area. Some of which are 5-input majority gate (MG) structures [4-9], one bit full adders [4,10-15], one bit full subtractors [13,16-19], binary array divider [20], reversible ALU [21], flip-flops, registers etc. In this paper efficient full adder and full subtractor demanding lesser cell area, lesser energy dissipation along with less number of majority gates using single layer coplanar wire crossing have been proposed. Furthermore a 4-bit full adder also has been designed.

The remaining part of this work is described as: The basic concept of QCA technology is interpreted in section II. Section III describes about 5-input MGs and energy dissipation analysis. An efficient QCA adder and subtractor is given in section IV. Simulation results of designed circuits and comparative study with existing works is described in section V and finally the paper is concluded in section VI .

II. QCA REVIEW

To implement any boolean logic function using QCA we use arrays of paired quantum dots. The location of electrons is used in QCA to indicate the binary values 0 and 1 unlike voltage and current levels in conventional digital technologies.

A. QCA Cell

QCA cell uses a couple of quantum dots to execute any Boolean logic function. Unlike conventional transistor based technology which uses the transport of electrons, it puts into operation the reconciliation of coupled electrons in a small squared nano area. The presence of four potential wells at the four corner of this nano squared area provides locking of two electrons [3]. The relocation of these two electrons in four quantum wells through tunnel junctions are subjected to clock signal control. Now the two electrons will experience coulombic interaction and move further away from each other in one of the two positions of diagonals, represented by logic "1" and other by logic "0" as seen by Fig. 1(a).

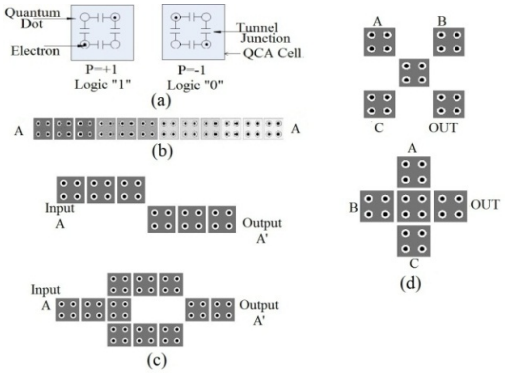

Fig. 1. QCA (a) Two different illustration of digital logic in QCA cell (b) QCA wire (c) Illustration of QCA Inverter (d) Representation of 3-input MG

B. QCA Wire

Wire here indicates basically the representation of an array of QCA cell as seen by Fig. 1(b). So the position of one QCA cell containing the electrons will determine the alignment of adjacent QCA cell's electrons due to coulombic interaction [3].

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C. Basic QCA Elements and Gates

The fundamental building block is QCA cell whose primary recipient is 3-input majority QCA gate. The making of 3-input MG can be done easily by 5 QCA cells arranged in two different ways [3,22] as shown in Fig. 1(d), whose expression can be written by (1).

$$M_3(A,B,C) = AB + BC + CA \quad (1)$$

By taking one of the three inputs as 1 or 0, the expressions for OR & AND gate can be written by (2) and (3) respectively.

$$A + B = M(A,B,1) \quad (2)$$

$$A \cdot B = M(A,B,0) \quad (3)$$

Using some organization of QCA cells, NOT gate can be represented as depicts in Fig. 1(c).

D. Clocking in QCA

Switch, Hold, Release & Relax are the four clock phases of QCA cell. Each phase have 90^0 phase shift from the previous phase [23]. Here high and low denote the states of clock signal, in which the transition from high to low indicates decrement of tunneling energy and increment of potential barrier and vice-versa for low to high. The attainment of fixed polarized state of electrons is done at low state and the ability to remain at a relaxed unpolarized state is take place at high state in Fig. 2.

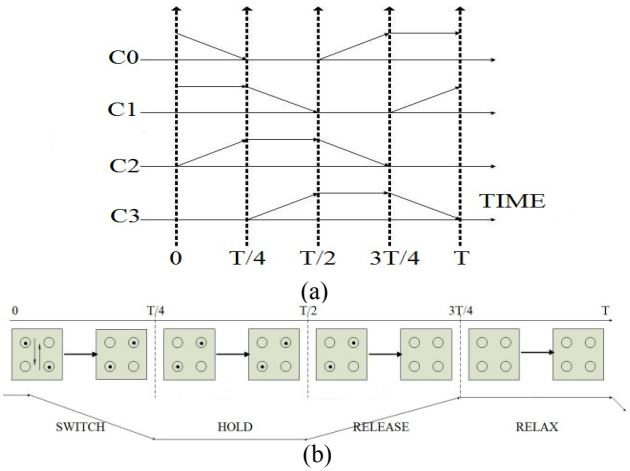

Fig. 2. (a) Clocking in QCA with 4 phase, (b) Operation in QCA through one clock phase

E. Crossover

To design any QCA circuit sometimes we require crossing the wire for connecting the components. The crossover in QCA is classified into two types :

Multilayer crossover: It is used for the interconnection of components as shown in Fig. 3(a).

Coplanar crossover: Here, wire crossing is performed by two different types of cell [15]. One wire has cells with 90^0 orientations and other wire has cells with 45^0 orientation, as depicted in Fig. 3(b).

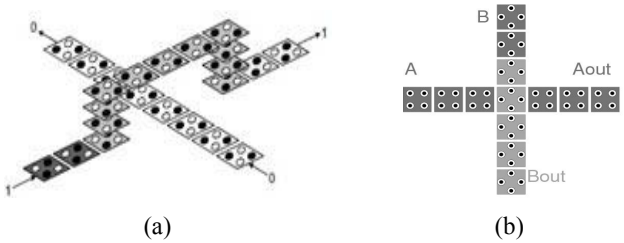

Fig. 3. (a) Multilayer crossover, (b) Coplanar crossover

III. Five Input Majority Gate

Initially the researchers have used 3-input majority gates to design the QCA circuits. After that with the requirement of more efficient circuits many five input MGs have been designed [4-9] whose expression can be written by (4).

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (4)$$

We have compared some of the 5-input majority gates as given in Table I. Here, we can see that the majority gate designed in [9] has depicted in Fig. 4, which is more efficient than other in relations of area and number of cells with input-output accessibility of single layer. In [9] it can also be seen that this majority gate has lesser energy dissipation than other.

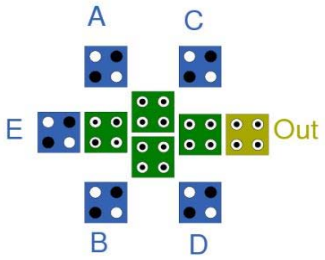

Fig. 4. QCA layout of 5-input MG

A. Energy Dissipation Analysis

The overall instantaneous power for a QCA cell [24,25] can be written by (5).

$$P_{total} = \frac{d}{dt}E = \frac{\hbar}{2}\left(\frac{d}{dt}\vec{\Gamma}\right).\vec{\lambda} + \frac{\hbar}{2}\vec{\Gamma}.\left(\frac{d}{dt}\vec{\Gamma}\right) = P_1 + P_2 \quad (5)$$

Where $\hbar$ =reduced plank constant, $\vec{\lambda}$ =coherence vector, $\vec{\Gamma}$ =3D energy vector. P_1 indicates the intercell power transfer & difference of power of input and output signal while P_2 is the dissipated power (P_{diss}). The overall energy dissipation will be the sum of energy dissipation of individual cell.

This concept has been used in [26] to develop a power estimator tool named QCAPro. It is used to determine the overall energy dissipation comprises of two dissipation i.e. leakage & switching. The information flow in QCA is controlled by clock change. The energy loss that occurs in the course of the clock change is termed as leakage energy

dissipation and the energy loss occurs in each particular cell at a given clock cycle is termed as switching energy dissipation.

To evaluate the energy dissipation we have taken $0.5E_k$, $1.0E_k$ and $1.5E_k$ as 3 different tunneling energy levels at Two Kelvin temperature. The energy dissipation analysis of devised adder and subtractor is performed using QCAPro.

TABLE: I
Layout analysis of 5-input MGs

5-input maj. gate structure	Number of cells	Area occupied (nm^2)	Accessibility of input and output cell in single layer
[04]	13	9604	Yes
[05]	13	9604	No
[06]	11	9604	Yes
[07]	10	4524	Not possible to access output in single layer
[08]	10	7644	Undesired effect as input cells are very close
[09]	10	7644	Yes

IV. FULL ADDER AND SUBTRACTOR

In the literature, many circuits for QCA full adder and full subtractor have been presented. Single layer designs are preferred over multilayer designs due to fabrication advantages. The important factor to design a QCA circuit is that it should have less complexity, lesser area and faster processing speed.

A. 1-bit Full Adder

In a single bit full adder circuit there are 3 input A, B and C_{in}, where A and B are two inputs being added and C_{in} is the carry input. Sum represented by S and output carry represented by C_o are the two output. The equation can be represented by (6).

$$C_o = AB + BC_{in} + C_{in}A$$
$$S = ABC_{in} + A'B'C_{in} + A'BC_{in}' + AB'C_{in}' \quad (6)$$

To implement full adder in QCA it required to represent the expression in terms of MGs, which can be given by (7).

$$C_o = M_3(A, B, C_{in})$$
$$S = M_5(A, B, C_{in}, C_o', C_o') \quad (7)$$

Where M_3 denotes the 3-input MG and M_5 denotes the 5-input MG. The schematic of full adder design using MGs is depicts in Fig. 5(a). The use of 5-input MG make the circuit more simple than using only 3-input MG and inverter. QCA layout of 1-bit full adder circuit is shown by Fig. 5(b).

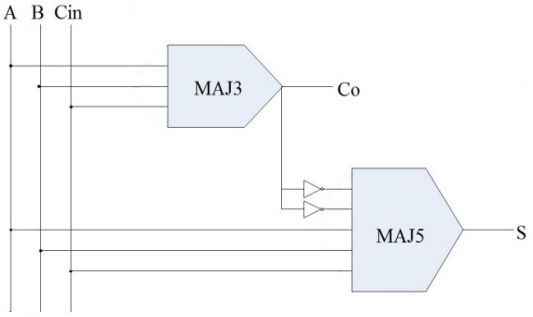

Fig. 5(a). Schematic of Full Adder design

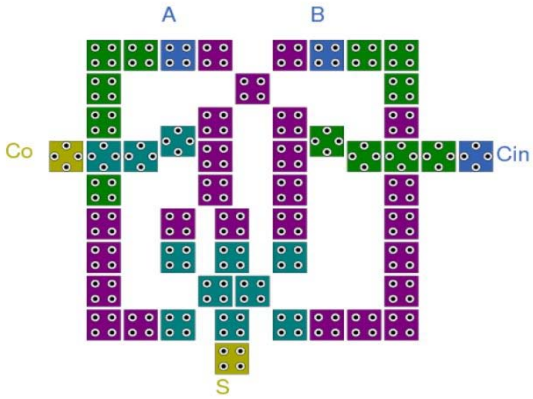

Fig. 5(b). QCA layout of Full Adder

B. 1-bit Full Subtractor

A full subtractor is used to performs the subtraction of two input A and B with borrow input C. The two output of subtractor circuit are difference 'D' and borrow 'B'. So the expression of 1 bit full subtractor can be written by (8).

$$B_o = A'B + BC + CA'$$
$$D = ABC + A'B'C + A'BC' + AB'C' \quad (8)$$

To implement full subtractor in QCA it required to represent the expression in terms of MGs, which can be given by (7).

$$B_o = M_3(A', B, C)$$
$$D = M_5'(A', B, C, B_o', B_o') \quad (9)$$

The schematic description of full subtractor circuit is shown by Fig. 6(a). The use of 5-input majority gate make the circuit more simple than using only 3-input MG and inverter. QCA implementation of 1-bit full subtractor circuit is shown by Fig. 6(b).

C. 4-bit Ripple Carry Adder

Using above designed 1-bit full adder we have designed 4-bit ripple carry adder as given by Fig. 7. It can be designed by linking the C_{out} of one full adder as a input to C_{in} of next full adder.

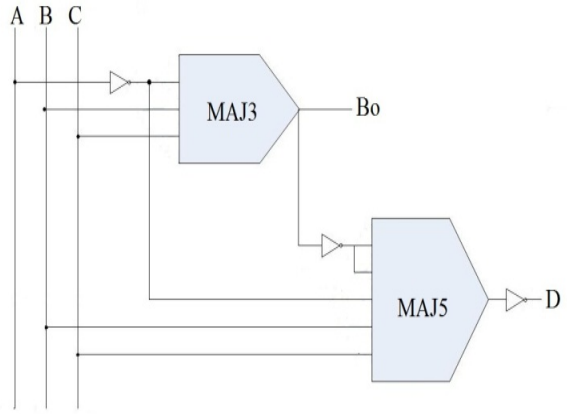

Fig. 6(a). Schematic of Full Subtractor design

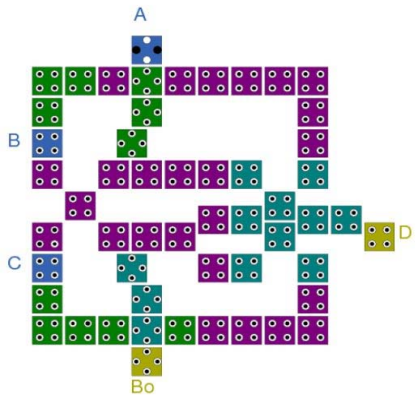

Fig. 6(b). QCA layout of Full Subtractor

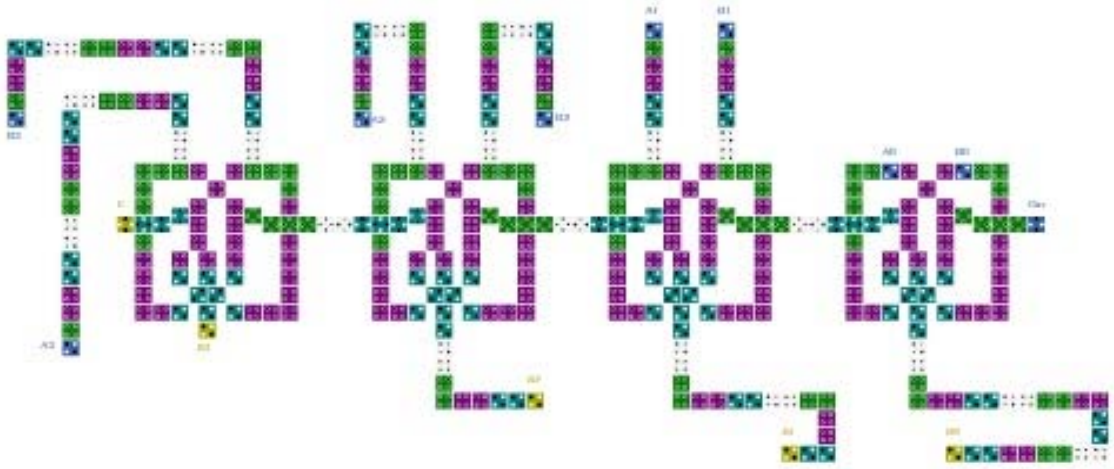

Fig. 7. QCA layout of 4-bit Ripple Carry Adder

V. SIMULATION RESULTS AND DISCUSSION

The simulation result of designed circuits and their comparison table with some performance parameter are cover in this section. The simulator "QCA Designer 2.0.3" is used for simulation of all designed circuits with coherence vector as simulation engine setup [27]. The parameter of coherence vector setup is specified in Table II.

The Table III shows the comparative study of proposed one bit full adder circuit with previous works. It can be seen from the Table III that the new designed full adder circuit implements well in area occupation, required number of cells, delay and complexity in single layer design as compared to the previous work. The energy dissipation analysis of full adder circuits can be seen by comparative study of Table IV. Here we can see that new devised circuit dissipates less energy as compared to other. Fig. 8 illustrates the energy dissipation thermal layout in each individual cell of new devised QCA full adder for the energy level of $0.5E_k$ at the temperature of 2Kelvin. In Fig. 8 QCA cells having dark color dissipate more energy in comparison to QCA cells having light color. Fig. 9 depicts the simulation result of new devised 1-bit full adder circuit to validate the circuit.

TABLE: II
Coherence vector parameter for QCA designer 2.0.3 simulator

Parameter	Value
Dot diameter	5 *nm*
Cell size	18*18 nm^2
Relaxation time	1.000000e-015s
Time step	1.000000e-016s
Relative permittivity	12.9
Radius of effect	80 *nm*
Clock low	3.8e-23J
Clock high	9.8e-22J
Layer separation	11.5000 *nm*
Clock amplitude factor	2.000000
Total simulation time	0.000000e+000
Clock shift	7.000000e-011s

Fig.10 depicts the simulation result of 4-bit ripple carry adder circuit. It requires 362 number of QCA cells, 0.63 μm^2 of area and 3.75 clock cycles delay. Here A(3:0) & B(3:0) represents the decimal value of 4-bit input A and B whereas C_{in} is the carry input. S(4:0) represents the decimal value of the sum of A & B with carry input. S(4:0) has 5-bit value including S_3, S_2, S_1, S_0 with carry output C. For the simulation, at first clock cycle we have taken input B(3:0) as 1100 and A(3:0) as 1011 which decimal equivalent is 12 and

11 respectively.The input carry C_{in} is taken as 1 for the first clock cycle. So the sum S(4:0) will be 11000 having decimal equivalent of 24, where the most significant bit represents the carry out C. So sum S(4:0) has appeared after 3.75 of clocks delay as indicated in Fig. 10. Similarly for 2nd and 3rd clock according to the given input the sum has appeared after 3.75 clocks of delay with repect to input.

Table V shows the comparison of proposed one bit full subtractor circuit with previous works over some performance parameter. Table V shows that the proposed full subtractor circuit is more efficient than the previous circuits under the parameter of number of cell, area occupied, complexity and input-output delay. Fig. 11 depicts the simulation result of 1-bit full subtractor circuit to validate the new devised circuit.

TABLE: III
Comparative study of layout of full adder designs

Full adder designs	Number of cells	Area in μm^2	Delay in Clock cycles	Crossover type
[10]	105	0.14	0.75	Multilayer
[04]	52	0.04	0.75	Multilayer
[11]	105	0.17	1	Coplanar
[12]	102	0.097	2	Coplanar
[13]	63	0.05	0.75	Coplanar
[14]	59	0.043	1	Coplanar
Proposed	53	0.047	0.75	Coplanar

TABLE: IV
Power dissipation analysis of full adder designs

Full adder designs		[11]	[12]	[14]	[13]	Proposed
Avg. leakage energy dissipation (meV)	0.5 E_k	92.85	58.37	12.54	37.21	31.20
	1.0 E_k	246.89	160.30	41.25	98.50	83.79
	1.5 E_k	409.09	272.09	78.22	165.04	140.62
Avg. switching energy dissipation (meV)	0.5 E_k	149.34	102.00	139.17	61.97	65.84
	1.0 E_k	114.32	83.83	127.29	50.90	60.83
	1.5 E_k	90.29	68.83	113.85	42.31	49.51
Total enegy dissipation (meV)	0.5 E_k	242.19	160.37	151.71	99.18	97.04
	1.0 E_k	361.21	244.13	168.54	149.4	144.62
	1.5 E_k	499.38	340.92	192.07	207.35	190.13

TABLE: V
Layout analysis of full subtractor designs

Full subtractor designs	No. of cells	Area in μm^2	Delay(Clock cyles)	Layer type
[16]	235	0.20	2	Multilayer
[17]	52	0.04	0.75	Multilayer
[18]	136	0.168	1.75	Multilayer
[19]	104	0.1043	1.75	Coplanar
[13]	63	0.05	0.75	Coplanar
Proposed	53	0.047	0.75	Coplanar

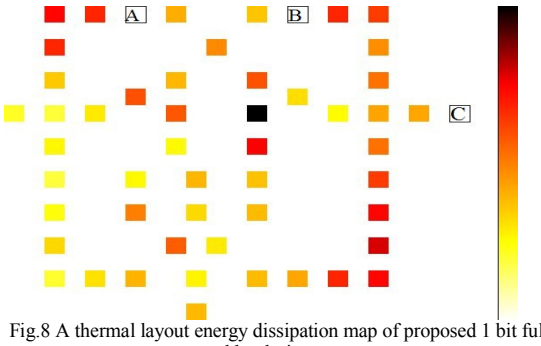

Fig.8 A thermal layout energy dissipation map of proposed 1 bit full adder design

Fig. 9. Simulation result of proposed full adder circuit

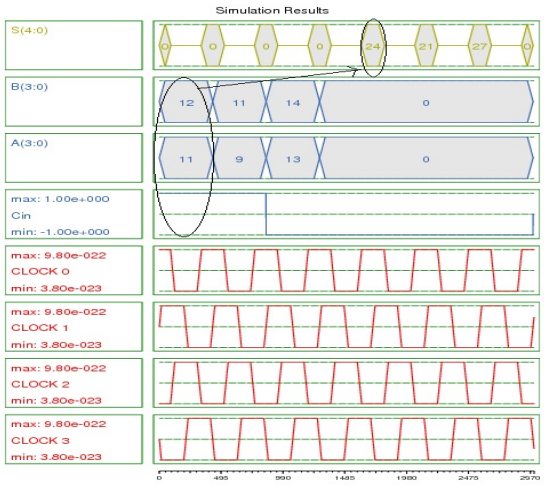

Fig. 10. Simulation result of designed 4-bit ripple carry adder

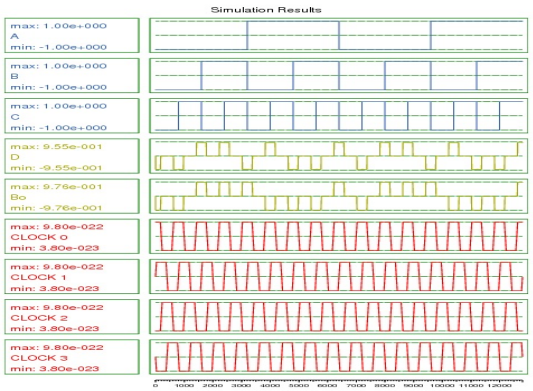

Fig. 11. Simulation result of proposed full subtractor circuit.

VI. Conclusion

In this work, efficient full adder and subtractor circuit have been designed using 5-input majority gate in "QCA Designer 2.0.3" with the requirement of lesser cell area along with less cell counts and clock cycles delay. Energy dissipation analysis of one bit full adder circuit is also performed using QCAPro. A 4-bit ripple carry adder circuit is also designed using proposed one bit full adder circuit. Proposed efficient structures can be used to design more complex and high performance QCA circuits at nano scale level in future.

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