Integration of Split-gate Flash Memory in 130nm BCD technology For Automotive Applications

Xiaobo Ma[1], Zin Tun Thant[1], Huihua Jiang[1], Namchil Mun[1], Kok Foong Chong[1], Ee Ee Yeoh[1], Bai Yen Nguyen[1], Ke Dong[1], Hung Chang Liao[1], Jianbo Zhou[1], Zhongxiu Yang[1], Shiang Yang Ong[1], Jeoung Mo Koo[1], Soh Yun Siah[1]

Liz Cuevas[2], Mandana Tadayoni[2], Joseph Norman[2], Yuri Tkachev[2], Steven Lemke[2], Sheng-Hsiung Hsueh[2], Henry Nguyen[2]

[1]GLOBALFOUNDRIES Singapore Pte, Ltd., Singapore, shiangyang.ong@globalfoundries.com

[2]Silicon Storage Technology, Inc., A Subsidiary of Microchip Technology Inc., San Jose, U.S.A.

Abstract

In this work we successfully integrated the split-gate SuperFlash® ESF1 cell into our 130nm BCD (Bipolar-CMOS-DMOS) platform for automotive applications. The platform enhances the modularity of flash macro in addition to logic devices, high performance power devices up to 85V as well as complimentary analog devices such as a BJT, MIM and Poly Resistor. Besides maintaining BCD device performance, the embedded flash operating temperature range from -40ºC to 170ºC, programmability, chip erase & read access time well meet the specifications. Endurance cycling of up to 20k cycles and data retention of over 20 years well satisfy AECQ-100 Automotive Grade 0 requirements.

(Keywords: Manufacturing, BCD, ESF1)

Introduction

GLOBALFOUNDRIES 130nm BCD process technologies offer modular platform architecture for industrial and automotive power ICs, provide world-class Rsp with 5V to 85V options [1].

As the automotive powertrain and in-vehicle networking marketing demands, in this work we enhance the 130nm BCD platform with high reliability, low cost and automotive Grade 0 qualified ESF1SuperFlash. The Split gate ESF1 flash was chosen due to highly efficient & erase, low-voltage read, and unique advantages in providing over-erase immunity [2]. It offers good manufacturability and high reliability [3] which ideally serves the automotive industry.

The current BCD+ESF1 process is based on 0.13um technology with voltage capability from 1.5v up to 85V. The RSP–BVDSS performance for the HV devices is best-in-class with respect to similar technologies [4,5]. To realize the integration of ESF1 modular flash, the overall thermal budget is well considered to keep original CMOS and high voltage device performance.

The presented BCD process integrates logic, analog, memory and power switching functions into one chip as shown in Fig. 1. All devices including 1.5v N/PMOS, 5v N/P MOS, 40-85V HV LDMOS and embedded Flash macro are located on n-doped epitaxial layers to ensure insensitivity of logic blocks to parasitic disturbances coming from the power areas. The power chips are directly isolated from each other by Deep Trench Isolation (DTI), which ensures the lateral isolation of the epi-wells. This isolation technique consumes less area and makes far better physical isolation than the traditional approach achieved by junction isolation.

Fig. 2 shows process flow used to create embedded Flash and its peripheral circuit modules, integrated into a BCD baseline. The final Flash cell structures are clearly shown by a TEM cross-section along the cell channel. The key point of the integration is to avoid impacting the baseline logic devices. Necessary device tuning is needed as thermal or wet processes change. The first integration is the flash p-well, the second is the NVM floating gate module. The floating gate oxide and following tunnel oxide quality are important because of the split-gate flash memory cell utilizing source-side channel hot electron injection for program, and poly-to-poly Fowler-Nordheim (F-N) tunneling for erase [3,6]. The Logic device gate and NVM WL are formed in the same process. The last added step is for source line (SL) ion implantation. After this step, the whole NVM module is integrated into the BCD baseline. The back end of line shares the same process with 130nm copper connection baseline, up to eight metal layers if needed.

Results and Discussion

First, before evaluation the eflash performance, we characterized the logic CMOS and high voltage devices. Fig.3 shows the most critical 85V device ID-VD curves; silicon data are well matched to the simulation curves. For devices at high voltage like 85V, the demonstrated best-in-class performances are Rsp ~ 96 mΩ-mm2 for NLDMOS BV equals 107 V, and Rsp ~ 269 mΩ-mm2 for PLDMOS BV equals 105 V, respectively.

The BCD+ESF1 qualification wafer delivers good

978-1-5386-6508-4/19/$31.00 ©2019 IEEE

yield consistently in high double digits, which indicates good process control. Key design specs are summarized in Table 1.

Fig. 4 shows the BCD ESF1 Flash Macro Random Read Access Time Shmoo Plots with wide temperature range. The new process well meets the 50ns spec time for -40°C° to 170°C.

We also evaluated the BCD ESF1 endurance cycling performance. Both the erase and program voltage before and post 20k cycling show enough margin to standard voltage needed. Samples with 20k cycling at -40°C, 25°C, 160°C also passed data retention test criteria. Fig. 5 shows the typical erase voltage distribution before and after 20k cycling.

Conclusion

We successfully integrated the ESF1 memory to BCD process, which is cost optimized and suitable to a growing power IC market. The functionality of the combination of flash-memory and power devices was also verified, with improved reliability and flexibility. The highly modular integration platform is targeted at both consumer and automotive applications.

References

[1] Mun Namchil, et al, "Advanced 300mm 130nm BCD technology from 5V to 85V with Deep-Trench Isolation", Int. Symp. on Power Semiconductor Devices and ICs, 2016, pp. 403-406.

[2] Robert Strenz, "Embedded Flash Technologies and their Applications: Status & Outlook", Int. Electron Devices Meeting, 2011, pp. 942-944.

[3] S. Kianian, et al, "A novel 3 volts-only, small sector erase, high density flash E2PROM", Proc. Symp. VLSI Technol., pp. 71-72, 1994.

[4] Hoon Chang, et al, "Advanced 0.13um smart power technology from 7V to 70V", Int. Symp. on Power Semiconductor Devices and ICs, 2012, pp. 217-220.

[5] Hongning Yang, et al, "Approach to the silicon limit: Advanced NLDMOS in 0.13 μm SOI technology for automotive and industrial applications up to 110V", Int. Symp. on Power Semiconductor Devices and ICs, 2013, pp. 357-360.

[6] Xian Liu, et al, "Endurance Characteristics of SuperFlash® Memory", Int. Conf. on Solid-State and Integrated Circuit Technology Proceedings, 2006, pp. 763-765

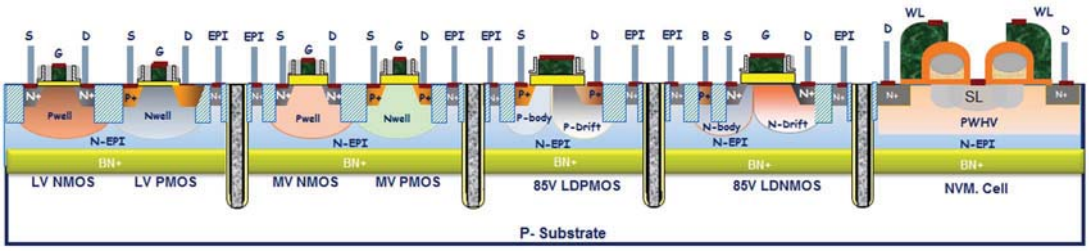

Fig. 1: Schematic of logic & flash and power areas embedded in N-Buried epitaxy with deep trench isolation.

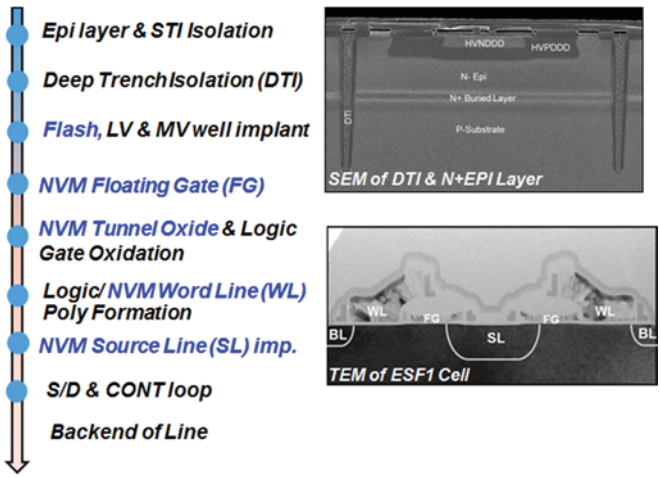

Fig. 2: Schematics of the ESF1 eFlash Process flow integrated with BCD baseline (Black: Logic, Blue: embedded Flash).

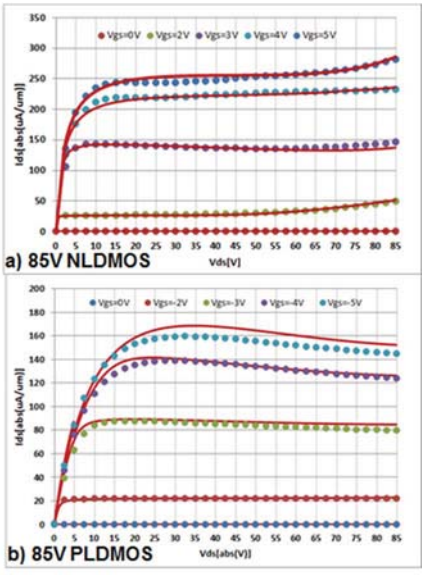

Fig. 3: Id-Vd curve of a) NLDMOS, b) PLDMOS with ESF1. (Line: Simulation, Symbol: Si Data).

Table 1 BCD ESF1 Automotive Macro Flash Key Specs & Silicon data

Flash Macro	Flash Spec	Silicon Data
Memory Size	512 Kbit	
Power Supply	VDDQ: 5V +/-10%, VDD: 1.5V +/-10%	
Operation Temperature Tj	-40 ºC to 170 ºC	
Byte Program Time	< 60 us	Pass
Sector Erase Time	< 12.5 ms	Pass
Chip Erase Time	< 30 ms	Pass
Read Access Time	< 50 ns	Pass
Endurance	20K	>20K
Data Retention	20 years at 85°C	>20 years

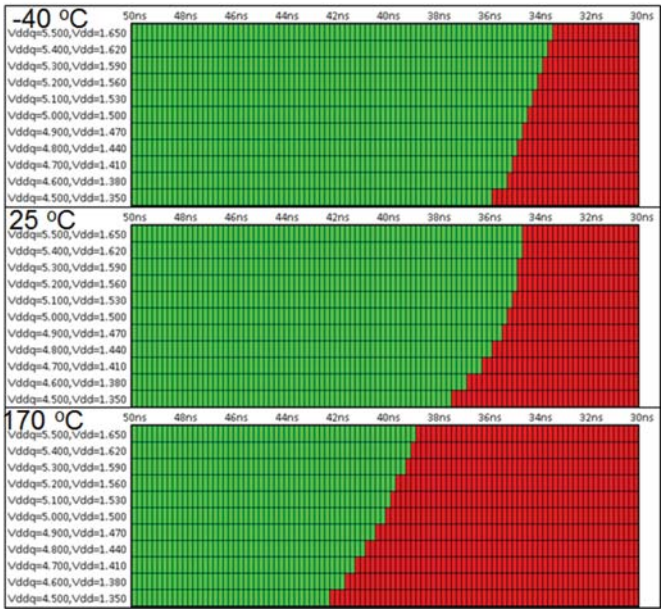

Fig. 4: BCD ESF1 Flash Macro Random Read Access Time Shmoo Plots with wide temperature range. New process meets the 50ns spec time for -40 ºC to 170 ºC

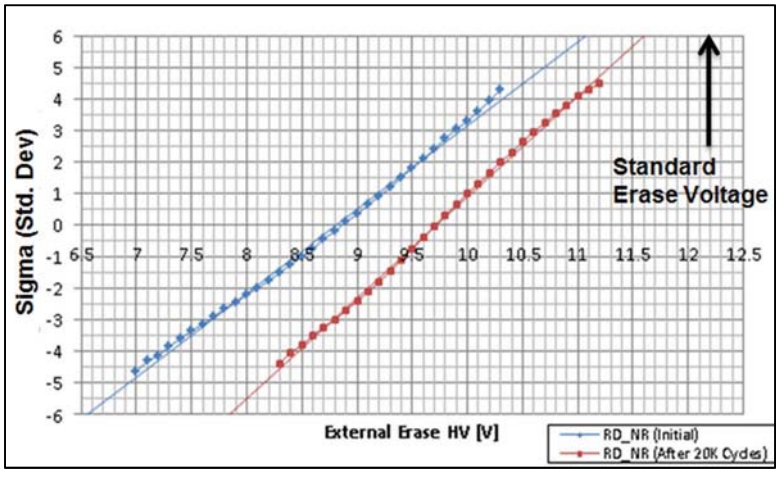

Fig. 5: BCD ESF1 Flash full array endurance cycling Erase Voltage distribution. (Blue: Initial, Red: post 20K Cycling)