An Input Buffer with Monolithic JFET in Standard BCD Technology for Sensor Applications

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***Abstract* — A new input buffer with monolithic integrated JFET in standard BCD technologies is presented in this work. The JFET has been implemented without any modification to the standard BCD process. An input buffer with PMOSFET was also fabricated for comparison. Measurements showed that the low-frequency input referred noise of the JFET input buffer is much smaller than that of the PMOSFET buffer. The proposed circuit can be applied to low-noise front-end amplifiers of sensors.**

Keywords—Input Buffer, JFET, Standard BCD Process

I. INTRODUCTION

It is imperative to make the front-end amplifiers of many sensors such as microphones, radiation detectors, and capacitive accelerometers have low noise figures at low frequencies. Since the first-stage circuit of an amplifier dominates the overall noise figure, the 1/f noise occurred in the input buffer of an amplifier must be reduced as much as possible. For designing a high-impedance input buffer, the main-stream MOSFET is a natural choice of device. Unfortunately, MOSFET suffers severe flicker noise. Compared with MOSFET, JFET exhibits much lower 1/f noise and still owns high input impedance. Therefore, it has been quite common for audio amplifier modules to adopt discrete JFET's as the input transistors. When the form factor and the cost of an amplifier are of concern, integrating the JFET input buffer and the subsequent MOSFET circuits on the same chip becomes important. Monolithic integration also reduces the parasitic capacitance at the node between the JFET and the following stage, thus further improving the signal-to-noise ratio. And it is even more cost-effective to do the integration in standard, commercial technologies without any extra process addition or modification. There have been several attempts to implement JFET's in CMOS and bipolar-CMOS-DMOS (BCD) technologies [1-6]. However, these developments required extra implantation steps and/or SOI wafers, and the processes thus developed were all proprietary. For cost- and size-sensitive applications such as the pre-amplifiers of MEMS microphones, implementing JFET's in standard, commercial processes is most beneficial and needed.

In this work, an input buffer with integrated JFET developed in the commercial TSMC 0.25 μm BCD technology is demonstrated. The design of the JFET structure is described and the resultant characteristics are presented. Two versions of input buffer have been designed, fabricated, and compared. One is with the proposed JFET and the other is with a MOSFET in the same process. The JFET input buffer functions well and shows superior noise performance over the MOSFET counterpart.

II. DEVICE STRUCTURE AND CHARACTERICTICS

A cross-sectional illustration of the proposed JFET is shown in Fig. 1. All the doping regions are available in the commercial TSMC 0.25 μm BCD technology without any modification or additional process. The advantage of using a BCD process is that there are lightly doped high-voltage well regions inherent in the technology. Therefore, in order to be able to pinch off the channel, the JFET channel region is composed of the lightly doped high-voltage n-well (HVNW). The channel conductance is controlled by two gate voltages via the top gate and the bottom gate which are formed with the more heavily doped low-voltage p-well (LVPW) and deep p-well (DPW), respectively. The bottom gate is connected to the surface contact by the high-voltage p-well (HVPW). The higher resistance of the HVPW imposes no DC loss problem since the gate-channel junction is reverse biased during operation. It may introduce larger charging time constants but this is fine for low-frequency applications. For high-frequency applications, this drawback may be avoided by holding the bottom gate voltage constant while modulating only the top gate voltage. At the source and drain contacts, low-voltage n-wells (LVNW) are used to reduce parasitic series resistance. It is worth mentioning that n-type high-voltage guard ring (HVNW) and n-type buried layer (NBL) are placed at all the sides and at the bottom of the device, respectively, for good isolation. Figure 2 shows the layout of a typical JFET test device.

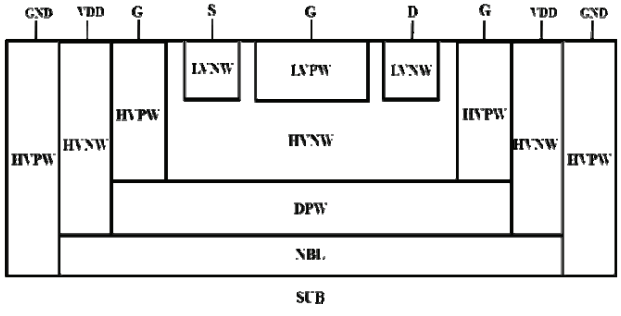


Fig.1 Cross-sectional view of the proposed JFET in BCD technology

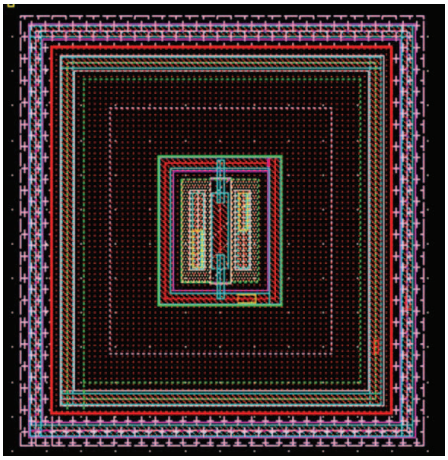


Fig. 2 Layout of a JFET test device

Figure 3 and Fig. 4 show the measured I-V characteristics of a fabricated JFET test device whose channel length and channel width were designed to be 3 µm and 15 µm, respectively.

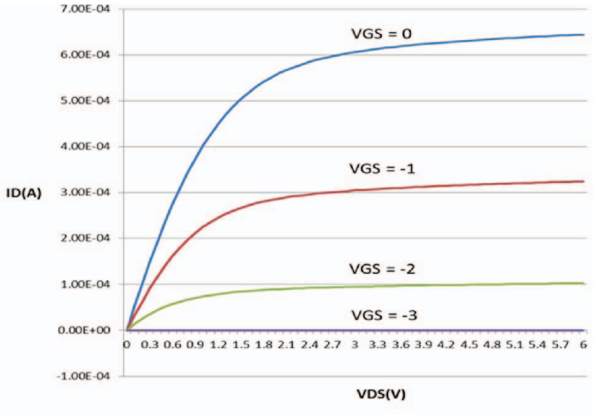


Fig. 3 Measured output characteristic (I_D vs. V_{DS}) of the JFET test device under various V_{GS} (V)

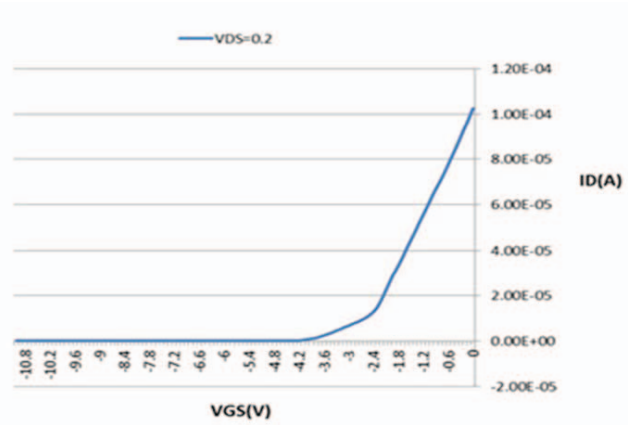


Fig. 4 Measured transconductance characteristic (I_D vs. V_{GS}) of the JFET test device under V_{DS}=0.2 V

The analytic model of the I-V characteristics of an n-channel JFET can be expressed as:

(a) In the triode region

$$Vp \le V_{GS} \le 0,\ V_{DS} \le V_{GS} - Vp,$$

$$I_{DS} = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{Vp}\right)\left(-\frac{V_{DS}}{Vp}\right) - \left(\frac{V_{DS}}{Vp}\right)^2\right], \quad (1)$$

where Vp is the pinch-off voltage and I_{DSS} is the saturation current at zero V_{GS};

(b) In the saturation region

$$Vp \le V_{GS} \le 0,\ V_{DS} \ge V_{GS} - Vp,$$

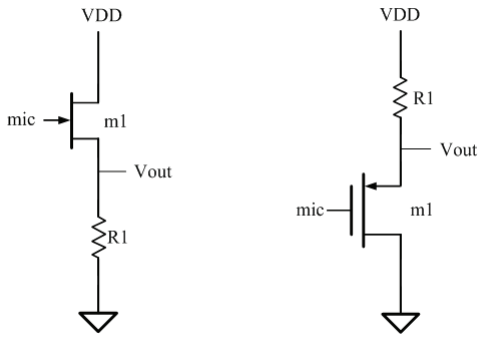
$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{Vp}\right)^2 (1 + \lambda V_{DS}), \quad (2)$$

where λ is the channel-length modulation parameter.

By fitting the measured results to the above analytic model of JFET, it can be found that this n-channel JFET has a Vp of -4.3 V and an I_{DSS} of 0.62 mA. Despite the fairly long channel-length, non-negligible channel-length modulation effect can still be observed in Fig. 3. The value of λ is found to be 0.86 $(mV)^{-1}$ for this device.

III. Input Buffer Implementation

The proposed JFET has been applied to implement a high-impedance input buffer circuit for the purpose of MEMS microphone signal pickup. In order to show the advantage of using JFET, a similar input buffer using a standard PMOSFET in the same process was also designed and fabricated for comparison. The reason of using PMOSFET instead of NMOSFET is to get a more critical comparison, since it is well known that a PMOSFET has less flicker noise than an NMOSFET of the same size does. Both versions of input buffer circuit are of the source follower configuration. Figure 5 shows the schematics of the implemented JFET and PMOSFET versions of input buffer. To mimic the condition of real application to MEMS microphones, the device parameters of the circuits were designed to make the gains of both versions be at the same level under a VDD value of 2.5 V. Table I lists the values used. In order not to introduce additional flicker noise, MOSFET bias circuits were avoided. Instead, resistive bias with diode pairs was adopted. In addition, the input buffers were implemented in differential pair configuration in the hope to reduce possible common-mode noise from the environment during measurement.



(a) JFET Source follower (b) MOSFET Source follower

Fig. 5 Schematics of the (a) JFET and (b) PMOSFET versions of input buffer

TABLE I. DEVICE PARAMETERS OF THE CIRCUITS SHOWN IN FIG. 5

	JFET	MOSFET
m1 (W/L)	15 μm/3 μm	8 μm/1 μm, m=10
R1	60 kΩ	100 kΩ

The designed voltage gains of the two input buffer circuits under VDD=2.5 V are both around 0.87. It was expected that the design is more precise and accurate for the MOSFET version since the device model of the MOSFET was provided by the foundry, was more sophisticated, and allowed us to do SPICE simulation for the circuit. Figure 6 and Fig. 7 show the measured output voltage signals of the two versions of input buffer when a 1 kHz, 100 mV_{p-p} sinusoidal input signal was applied. The measured voltage gain of the JFET input buffer is 0.681, lower than that of the MOSFET version, which is 0.806. This lower gain could be due to the higher channel-length modulation effect in the JFET and the fact that the output bias point of the JFET input buffer has deviated from the targeted 1.25 V to 1.165 V, while the output bias point of the MOSFET input buffer stayed at 1.283 V. It also implies that the analytic model we used for the JFET could be further improved.

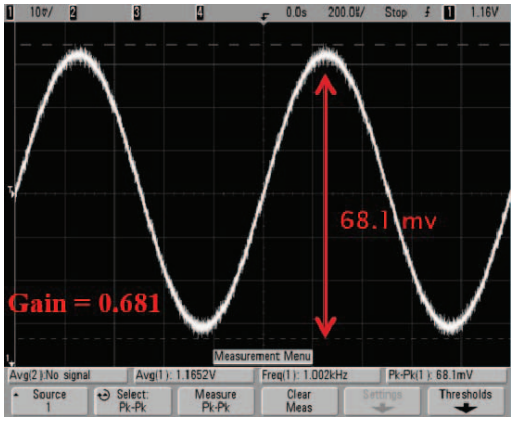


Fig. 6 Output waveform of the JFET input buffer. The input signal is a 1 kHz, 100 mVp-p sinusoidal wave

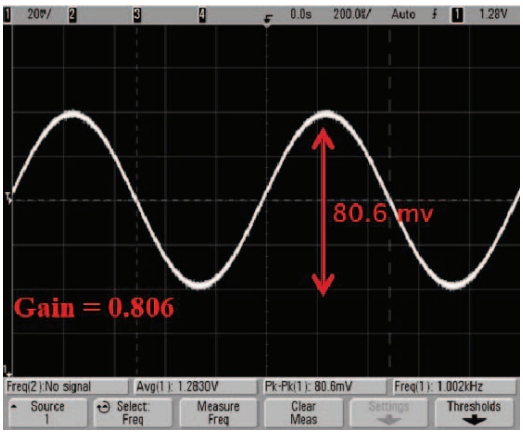


Fig. 7 Output waveform of the MOSFET input buffer. The input signal is a 1 kHz, 100 mVp-p sinusoidal wave

Fig. 8 shows the measured noise spectra at the output nodes of both buffers. The spikes shown in the figure are due to the 60 Hz and harmonics noise coupled from the measurement environment, indicating the existence of mismatch in the differential pairs. However, it can be clearly seen that the 1/f noise of the JFET input buffer is lower than that of the PMOSFET input buffer. The lower the frequency is, the larger the difference in noise appears. When connected with a 5 pF capacitive load, such as a MEMS microphone, at the input node, both versions of input buffer showed low-frequency corners around 20 Hz. For such cases, the noise spectral density above the corner frequencies is of interest. And it is more appropriate to look at input referred noise rather than the output noise only, because the voltage gains of the two input buffers are not the same. From the measured spectra as shown in Fig. 8, the integrated input referred noise from 20 Hz to 400 Hz for the JFET buffer is calculated to be 14.4 μV_{rms} which is much less than the 22.8 μV_{rms} for the PMOSFET version. The effectiveness of using the JFET is clearly shown.

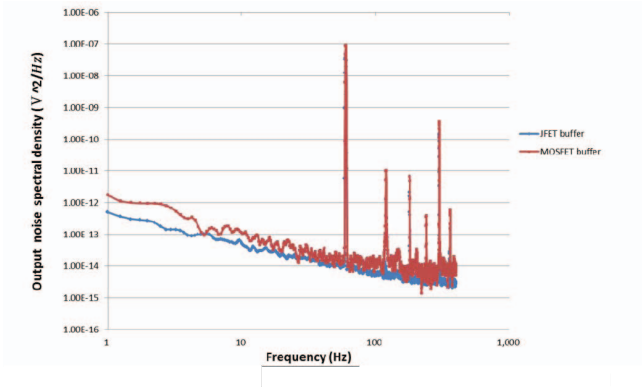


Fig. 8 Measured output noise spectra of the JFET and PMOSFET input buffers

IV. CONCLUSION

In order to reduce low-frequency noise, a JFET device has been successfully developed in TSMC standard 0.25 μm BCD technology. The input buffer circuit with the proposed JFET showed superior noise performance over PMOSFET input buffer. It is suitable to be used in low-noise front-end amplifiers for cost- and size-sensitive sensor applications.

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