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Quantum Dot Cellular Automata (QCA) design for the realization of basic logic gates

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***Abstract*— An promising technology that provides a very efficient computational platform than CMOS is a nanotechnology approach i.e. Quantum cellular automata (QCA). It represents the digital information by polarization of electrons. It is attractive for its size, faster speed, feature, highly scalable, higher switching frequency and low power consumption compared to CMOS technology. In near future QCA can take over CMOS because of its significant benefits. This paper mainly projects the implementation and simulation results of various logic gates using quantum dot cellular automata (QCA) designer. Further complex designs can be carried out using these design methodologies. Comparative analysis of QCA design and CMOS is carried to measure performance analysis in terms of covered area (size).**

Keywords—QCA designer; logic gate; quantum dot; CMOS; majority gate.

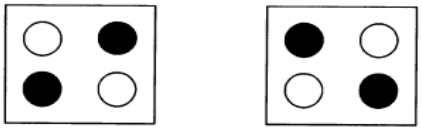
I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) is an emerging paradigm in the developing Nano electronic technology, which has been technologically advanced to support simulation of multidimensional quantum circuits and devices. Compared to classical computer, in QCA the digital information are represented as configurations of pair of electrons coupled together to form quantum dot arrays. Boolean logic functions are implemented using these quantum dot arrays in QCA designer. With the advancements in QCA and due to the enhancements in the field of the quantum mechanical effects, digital circuits designed using QCA have significant size reduction and hence the area, and achieves high speed of operation at very low power levels [1]. Hence the neighboring cells interacts with each other the state changes happened in QCA due to electrostatic or magnetic fields. Consequently, in QCA, electron localization are used to represent the binary values in quantum dots, instead of using ranges of voltages and currents to indicate binary values as used in traditional computers. Large number of QCA integrated circuits are designed and implemented in densities up 1014 cells/cm2and there is a rapid increase in circuit switching frequency which is almost close to a terahertz.

In spite of having some prominent features such as stability, high speed, reduced area and less energy consumption, QCA circuits lack design automation tools and modular architecture which facilitates the design and simulation of large electronic circuits and circuit fabrication as hindered the full development of Nano electronic technology.

II. QCA PRELIMINARIES

A cell is a basic building block in QCA. The logical bit representation in QCA cell is done through an appropriate configuration of charge. Each cell consists of four charge carriers arranged in corners of a cube known as quantum dots. In terms of size these quantum dot represents a semiconductor nanostructure that explores quantum mechanical properties. These four quantum dots represents a QCA cell, in which one of the electron pair out of the four quantum dots occupies diagonally opposite positions as shown in Figure 1. Because of less Columbic repulsion these electron pair in QCA occupies opposite corner i.e.in diagonal locations instead of adjacent locations. The four Quantum dots in a cell are connected by tunnel junctions [2].



1(a) 1(b)

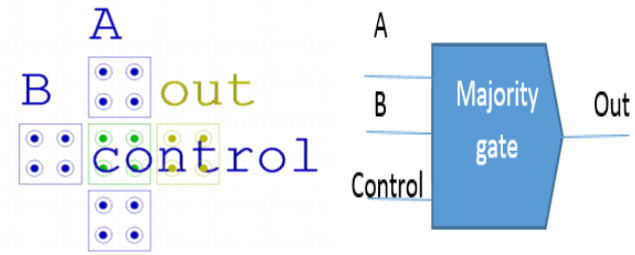
Figure 1: Quantum cellular automata cells with four quantum dots. 1 (a) P= +1 (Binary 1), 1 (b) P= -1 (Binary 0).

Depending upon the location of electron pair charge in the QCA cell, polarizations are represented by two ground state polarizations namely -1 for binary 0 and +1 for binary 1. These -1 and +1 state polarization is formulated as-

$$P = \frac{(P1 + P3) - (P2 + P4)}{P1 + P2 + P3 + P4}$$

Majority gate is designed by arranging five QCA cells in cross patterns, shown in Figure 2. Depending on majority of inputs the majority gate produces the output. This majority gate forms the basic building block to implement various logic gates in QCA circuits. For example if the input provided to majority gate is "001", then output is "0" which indicates the maximum digit repetition in the input. Similarly for input "111", output of majority gate is "1" and so on. In general, the majority gate takes inputs in odd number to produce an output. A

two dimensional QCA cell, permits only three inputs (such as two cells for input and one cell for control) and produces one output provided that there are only four directions. Extensions to three dimensional will permit further additional inputs. Moreover, for many arithmetic applications, three inputs in QCA seem to be appropriate.



2(a) 2(b)

Figure 2: A majority gate designed with five QCA cells. 2(a) Majority gate in QCA. 2(b) Block diagram of Majority gate.

III. LOGIC GATE DESIGN IN QCA

➢ The inverter or NOT gate can be implemented using QCA by placing two QCA cells at 45 degrees with respect to each other such that they interact inversely. Using QCAD tool NOT gate design is as shown in Figure 3.

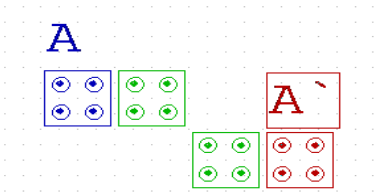


Figure 3. NOT gate design in QCA

➢ AND gate can be designed by setting one of the inputs to zero (set polarization to -1) in majority gate shown in Figure 4.This can be shown as M(A,B, 0) = AB.

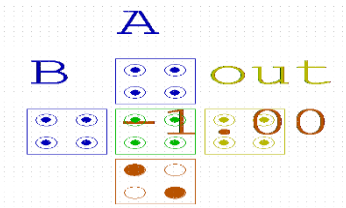


Figure 4. AND gate design in QCA

➢ OR gate can be designed by setting one of the inputs of majority gate to one (set polarization to +1) as shown in Figure 5. This is given by M(A,B, 1) = A + B.

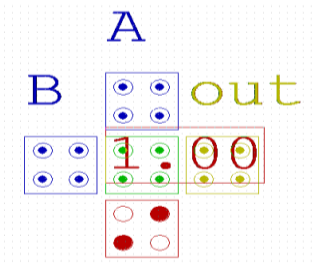


Figure 5. OR gate design in QCA

➢ By inserting inverter to the output of AND gate, NAND gate can be designed as shown in Figure 6.

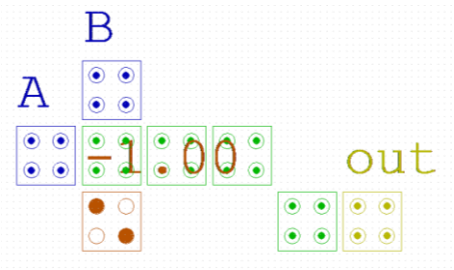


Figure 6. NAND gate design in QCA

➢ NOR gate can be designed by inserting inverter to the output of OR gate, NOR gate can be created as shown in Figure 7.

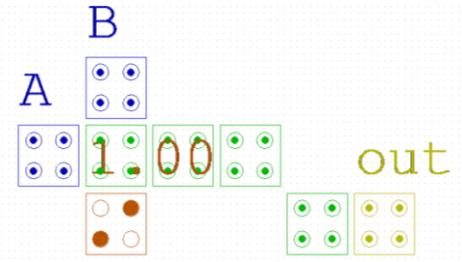


Figure 7. NOR gate design in QCA

➢ XOR gate can be created by using logic implementation shown in Figure 8 [5]. QCA design implementation of XOR gate is as shown in Figure 9.

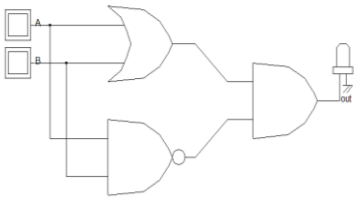


Figure 8. Logic gate implementation of XOR gate

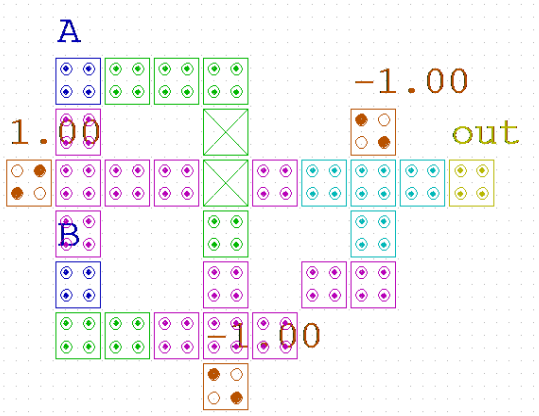


Figure 9. XOR gate design in QCA

➢ Placing inverter to the output end of XOR, XNOR gate can be created Figure 10.

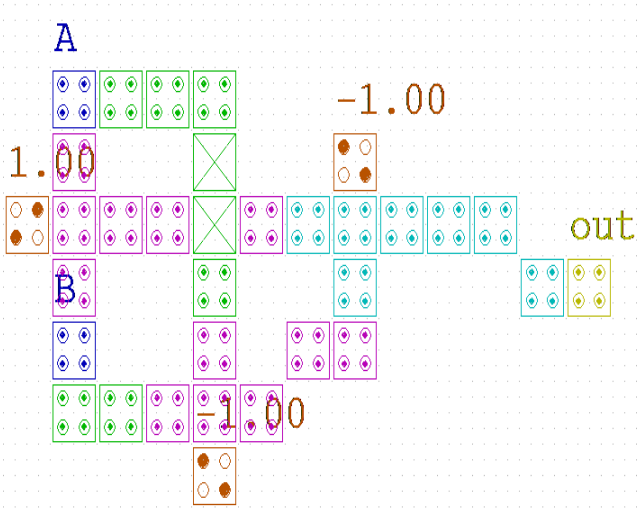


Figure 10. XNOR gate design in QCA

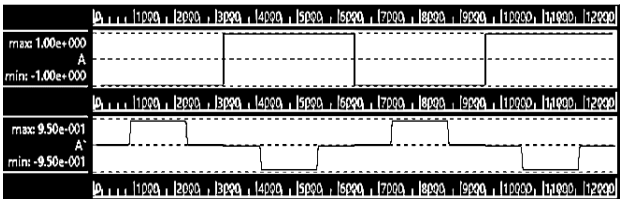
IV. SIMULATION AND RESULT ANALYSIS

The simulation results obtained by QCAD for all the basic logic gates are presented in Figure 11. By applying default parameters of bistable approximation the logic gates can be simulated with below listed parameters-

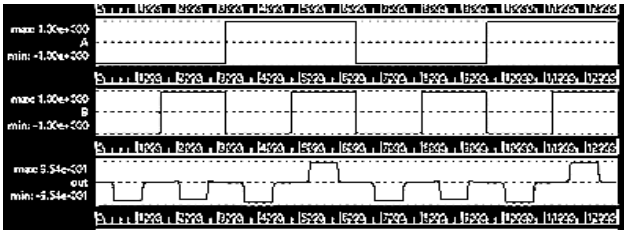
- Cell size = 18 nm
- Clock amplitude factor = 2.0000
- Clock high = 9.8000e−022 J
- Clock low = 3.8000e−023J
- Clock shift = 0
- Convergence tolerance = 0.0000100
- Layer separation = 11.50
- Maximum iterations per sample = 100
- Number of samples = 50000
- Radius of effect = 65.0000 nm
- Relative permittivity = 12.9000.

Results are verified with truth table and comparison results holds satisfactory with QCA tool and truth table.

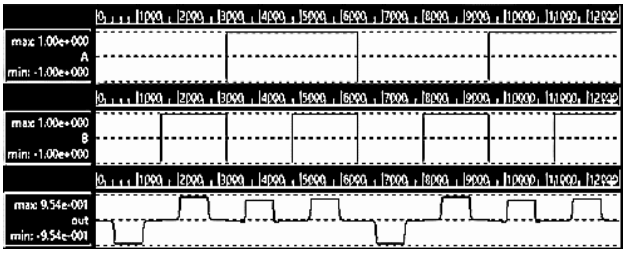
A. NOT gate



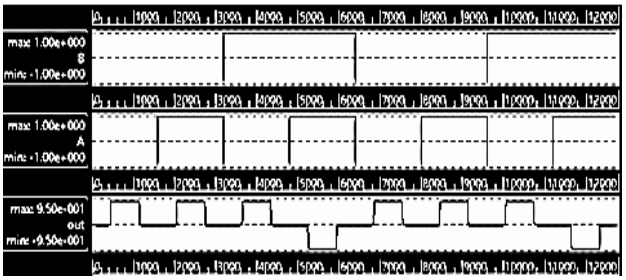
B. AND gate



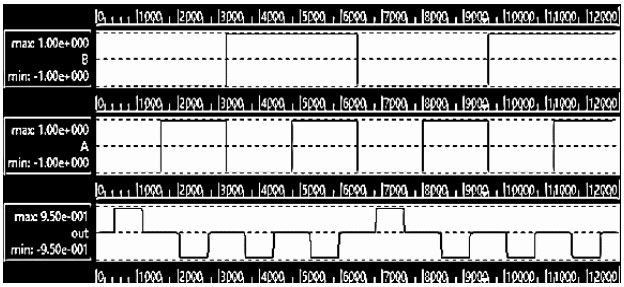
C. OR gate



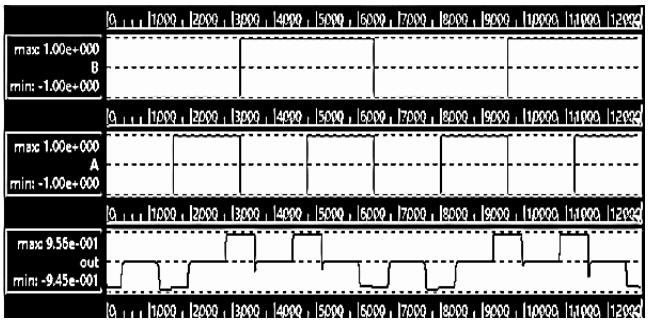
D. NAND gate



E. NOR gate



F. XOR gate



G. XNOR gate

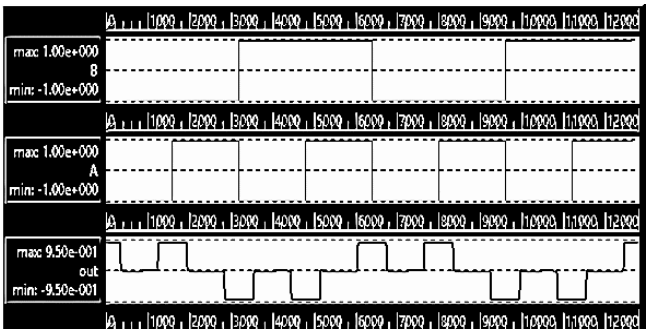
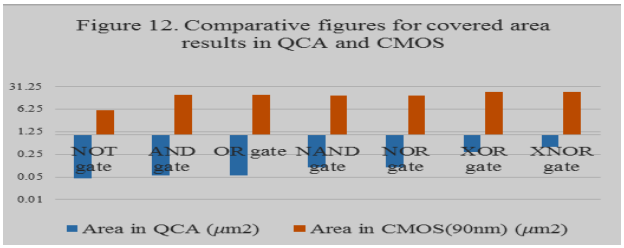


Figure 11. Simulation results of logic gates realized using QCA

Table 1 tabulates the performance analysis parameters of the realized logic gates in QCA and CMOS. Table 1 infers that logic gates designed using QCA technology provides highly efficient integrated design in comparison with CMOS technology. Total number of QCA cells deployed in the design of logic gates and total area used for realization of each gate in both QCA and CMOS technologies are shown in Table 1. QCA results tabulated shows the improvements over CMOS results. Here, the CMOS software tools like schematic editor (Dsch3) and layout editor (Microwind) are used to design and obtain covered area of all realized logic gates. In summary, the number of cells used to implement logic gates is found to be much lesser in QCA compared to CMOS FETs.

TABLE I. PERFORMANCE ANALYSIS OF REALIZED LOGIC GATES

Parameters	**NOT gate**	**AND gate**	**OR gate**	**NAND gate**	**NOR gate**	**XOR gate**	**XNOR gate**
Number of cells in QCA	4	5	5	8	8	29	33
Area in QCA (μm2)	0.045	0.05716	0.05716	0.10021	0.10021	0.30005	0.426
Area in CMOS(90nm) (μm2)	5.8	17.7	17.9	16.3	16.5	21.6	21.7



V. CONCLUSION

Quantum-dot cellular automata (QCA) is a new technology at Nano scale circuit design level that are suitable for the design of highly scalable logic circuits. As logic gates are rudimental for most of digital circuits, having high speed, less complex and reduced area designs are significantly important. The implemented designs and simulation results obtained are the solution for the proposal of QCA based digital circuits using lesser number of QCA cells and minimal size specification. This paper has demonstrated the improved design and implementation of various logic gates using QCA designer which have outperformed all prior designs and shows significant improvements. The major aim of this paper is to design simple QCA based logic gates using majority gate with capable versatility and compatibility. In addition, obtained results are checked with corresponding truth table.

REFERENCES

[1] I. Amlani, A. Orlov, R. Kummamuru, G. Bernstein, C. Lent, and G. Snider, "Experimental demonstration of a leadless quantum-dot cellular automata cell," Applied Physics Letters, vol. 77, no. 5, pp. 738– 740, 2000.

[2] A. Orlov, I. Amlani, G. Bernstein, C. Lent, and G. Snider, "Realization of a functional cell for quantum-dot cellular automata," Science, vol. 277, no. 5328, pp. 928–930, 1997.

[3] C. Lent, P. Tougaw, W. Porod, and G. Bernstein, "Quantum cellular automata," Nanotechnology, vol. 4, no. 1, p. 49, 1993.

[4] P. Tougaw and C. Lent, "Logical devices implemented using quantum cellular automata," Journal of Applied physics, vol. 75, no. 3, pp. 1818–1825, 1994. http://dx.doi.org/10.1063/1.356375.

[5] Beigh M.R., Mustafa .M, and Ahmad .F, "Performance Evaluation of Efficient XOR Structures in Quantum-Dot Cellular Automata (QCA)," Circuits and Systems, vol. 4, p.147-156. http://dx.doi.org/10.4236/cs.2013.42020.

[6] Karthigai Lakshmi .S, and Athisha .G, "Efficient Design of Logical Structures and Functions Using Nanotechnology Based Quantum Dot Cellular Automata Design," International Journal of Computer Applications, 2010.

[7] Walus K., Wang W, and Jullien G.A., "Majority Logic Reduction for Quantum Cellular Automata," Proceedings of IEEE Conference on Nanotechnology, 2004

[8] Walus K., Schulaf G. and Jullien G.A., "Circuit Design Based on Majority Gates for Application with Quantum Dot cellular Automata," Proceedings of the IEEE Conference on Nanotechnology, vol.4, p.1350-1356, 2004.

[9] Vicky S. Kalogeiton, Dim P. Papadopoulos, Orestis Liolis, Vassilios A. Mardiris et al. "Programmable Crossbar Quantum-Dot Cellular Automata Circuits," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017.

[10] Kumari N. Prameela, Prashant V. Joshi, and K.S. Gurumurthy., "Realization of Basic Gates Using Universal Logic Blocks in Quantum Dot Cellular Automata," 2013 6th International Conference on Emerging Trends in Engineering and Technology, 2013.