Bounded Model Checking for Software

COMP6210 - Automated Software Verification

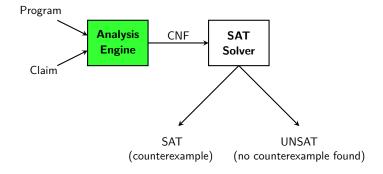
ECS, University of Southampton

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Previously...

 \underline{CBMC} : the \underline{C} \underline{B} ounded \underline{M} odel \underline{C} hecker

<u>Main idea</u>: Given a C program and a claim, use a SAT solver to check of there is an execution that <u>violates the claim</u>.

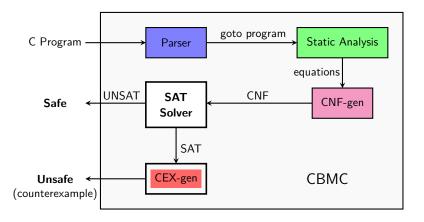


CBMC: How Does It Work?

Transforms a C program into a set of equations.

- Simplify control flow
- Unwind all the loops
- Sonvert into Single Static Assignment (SSA)
- Convert into equations
- Bit-blast
- 6 Solve with a SAT solver
- Convert SAT assignment into a counterexample

CBMC: How Does It Work?



Control Flow Simplification

- All side effects are removed e.g. j=i++; is transformed into j=i; i=i+1;
- Control flow is made explicit
 continue and break are replaced by goto
- All loops are simplified into one form
 e.g. for, do, while are replaced by just while.

- All loops are unwound can use different unwinding bounds for different loops can check whether unwinding is <u>sufficient</u> using a special unwinding assertion
- If a program satisfies all of its claims and all unwinding assertions, then it is correct.
- Recursive functions and backward goto are similar (use inlining).

while loops are unwound *iteratively*; break/continue replaced by goto.

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| gotoletic | property | propert

Loop Unwinding 将循环展开为if

while loops are unwound *iteratively*; break/continue replaced by goto.

```
void f(...) {
    ... // some code
    if(cond){
        Body;
        while(cond){
            Body;
        }
     }
    Remainder;
}
```

while loops are unwound *iteratively*; break/continue replaced by goto.

```
void f(...) {
      ... // some code
      if(cond){
        Body;
        if(cond){
          Body;
6
          while(cond){
            Body;
10
11
      Remainder;
12
13
```

while loops are unwound *iteratively*; break/continue replaced by goto.

```
void f(...) {
      ... // some code
      if(cond){
        Body;
        if(cond){
6
          Body;
          if(cond){
             Body;
             while(cond){
10
               Body;
11
12
13
14
15
      Remainder;
16
```

Assertion inserted after last iteration: violated if the program runs longer than bound permits.

```
void f(...) {
      ... // some code
      if(cond){
        Body;
        if(cond){
          Body;
          if(cond){
            Body;
            assert(!cond); //Unwinding assertion
10
11
12
1.3
      Remainder;
14
```

未发期望终止循环

Assertion inserted after last iteration: violated if the program runs longer than bound permits. Positive correctness result!

```
void f(...) {
      ... // some code
      if(cond){
        Body;
        if(cond){
          Body;
          if(cond){
            Body;
            assert(!cond); //Unwinding assertion
10
11
12
13
      Remainder;
14
```

Example: Sufficient Loop Unwinding

```
unwind = 3
```

```
void f(...) {
j = 1;
while(j<=2){
j = j + 1;
}
Remainder;
}</pre>
```

```
void f(...){
     j = 1;
   if(j<=2){
      j = j + 1; 2
      if(j<=2){
       j = j + 1; 3
       if(j \le 2) {
         j = j + 1;
         assert(!(j<=2));
10
11
12
13
     Remainder;
14 }
```

Example: Insufficient Loop Unwinding

unwind = 3

```
1 void f(...) {
2    j = 1;
3    while(j<=10){
4    j = j + 1;
5    }
6    Remainder;
7 }</pre>
```

```
void f(...){
     j = 1;
     if(j<=10){
      j = j + 1;
      if(j<=10){
        j = j + 1;
       if(j<=10){
         j = j + 1;
         assert(!(j<=10));
10
11
12
13
      Remainder;
14 }
```

植贵的

It is trivial to translate a program into a set of equations if each variable is only assigned once!

```
1 x = a;
2 y = x+1;
3 z = y-1;
```

This program is directly transformed into

$$x = a \wedge y = x + 1 \wedge z = y - 1$$
.

Static Single Assignment (SSA) form.

- Every variable is assigned exactly once.
- Every variable is defined *before it is used*.

When a variable is assigned multiple times, we use a new variable for each assignment.

```
1 x=x+y;

2 x=x*2;

3 a[i]=100;

1 x1 = x0 + y0;

2 x2 = x1*2;

3 a1[i0] = 100;
```

Static Single Assignment (SSA) form.

- Every variable is assigned *exactly once*.
- Every variable is defined *before it is used*.

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1 x=x+y;

2 x=x*2;

3 a[i]=100;

1 x1 = x0 + y0;

2 x2 = x1*2;

3 a1[i0] = 100;
```

What about conditionals?

Converting conditionals to SSA.

```
1 if(v)
2    x = y;
3 else
4    x = z;
5 w = x;
```

```
1 if(v0)
2    x0 = y0;
3 else
4    x1 = z0;
5 w1 = x?? // which x?
```

Converting conditionals to SSA.

```
1 if(v)
2    x = y;
3 else
4    x = z;
5 w = x;
```

```
1 if(v0)
2    x0 = y0;
3 else
4    x1 = z0;
5    x2 = v0 ? x0 : x1;
6    w1 = x2;
```

For each joint point and new variables with *selectors*.

Starting from the following C code:

```
int y;
int x;
x=x+y;
if(x!=1)
x=2;
else
x++;
sassert(x<=3);</pre>
```

Simplify control flow

```
int y;
int x;
x=x+y;
if(x!=1)
  x=2;
else
  x=x+1;
assert(x <= 3);
```

Convert to SSA (Static Single Assignment form)

```
1  x1 = x0+y0;
2  if(x1 != 1)
3   x2 = 2;
4  else
5   x3 = x1 + 1;
6  x4 = (x1 != 1) ? x2 : x3;
7  assert(x4<=3);</pre>
```

Convert to SSA (Static Single Assignment form)

```
x1 = x0+y0;
 2 if(x1 != 1)
 x2 = 2;
 4 else
 x3 = x1 + 1;
 6 \times 4 = (x1 != 1) ? x2 : x3:
 7 assert(x4<=3):</pre>
Generate constraints (if SAT, then assertion is false):
       x_1 = x_0 + y_0 \land x_2 = 2 \land x_3 = x_1 + 1
     \land ((x_1 \neq 1 \land x_4 = x_2) \lor (x_1 = 1 \land x_4 = x_3)) [selector]
     \wedge (\neg)x_4 \leq 3) [negated assertion]
```

Starting from the following C code:

```
int i;
int p;
p=5;
for (i=0; i<=n; i++) {
   p = p * m;
}
assert(p>=5);
```

Transform the for loop into a while loop

```
int i;
int p;
p=5; i=0;
while (i<=n) {
   p = p * m;
   i = i + 1;
}
assert(p>=5);
```

Unroll the loop twice and add an assume statement to exit the loop

```
int i;
2 int p;
  p=5; i=0;
  if(i<=n) {
p = p * m;
i = i + 1;
  while (i<=n) {
      p = p * m;
      i = i + 1;
10
  assert(p>=5);
11
```

Unroll the loop twice and add an assume statement to exit the loop

```
int i;
  int p;
  p=5; i=0;
  if(i \le n)
     p = p *
   i = i +
   if (i<
       i = i
       assume(!(i<=n));
10
11
   assert(p>=5);
12
```

Assign all variables exactly once, compute guards for conditionals and add conditionals for merging values.

```
p1=5;
  i1=0;
  g1=i1<=n1;布尔条件 变量
    p2=p1*m1; // q1
  i2=i1+1; // q1
  g2=(i2<=n1);
      p3 = p2*m1 //g1 88 g2
                                 依设证列
      i3 = i2 + 1; //g1 \& g2
      assume( !(i3<=n1));
9
  p4=g1 ? (g2 ? p3 : p2) : p1;
10
  i4=g1 ? (g2 ? i3 : i2) : i1; //
11
  assert(p4 >= 5);
12
```

Convert to logical expression (if UNSAT, then assertion holds).

$$p_1 = 5$$

$$\land i_1 = 0$$

$$\land g_1 = (i_1 \le n_1)$$

$$\land p_2 = p_1 * m_1$$

$$\land i_2 = i_1 + 1$$

$$\land g_2 = (i_2 \le n_1)$$

$$\land p_3 = p_2 * m_1$$

$$\land i_3 = i_2 + 1$$

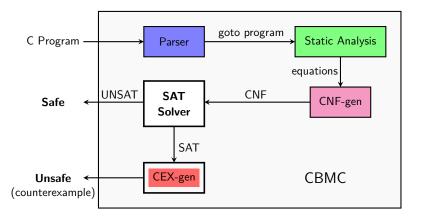
$$\land \neg (i_3 \le n_1) \quad [\text{assume statement}]$$

$$\land p_4 = g_1 ? (g_2 ? p_3 : p_2) : p_1$$

$$\land i_4 = g_1 ? (g_2 ? i_3 : i_2) : i_1$$

$$\land \neg (p_4 \ge 5) \quad [\text{assert statement}]$$

CBMC: How Does It Work?



Bit Blasting

So far, formulas such as $x_2 = x_1 + 1 \land y_2 = x_2$ are *not* stated in propositional logic!

The operations are performed on *bit vectors*.

In order to convert these formulas into a format acceptable to a SAT solver, one needs to apply *flattening/bit blasting*.

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Intuitively, we can build Boolean circuits for the bit-vector operations; these can be described by Boolean formulas (unfortunately with a lot more variables).

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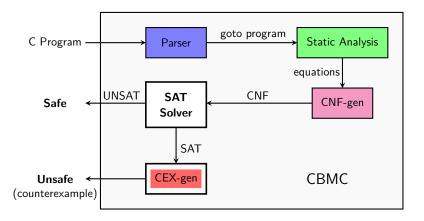
The operations are performed on bit vectors.

In order to convert these formulas into a format acceptable to a SAT solver, one needs to apply *flattening/bit blasting*.

Intuitively, we can build Boolean circuits for the bit-vector operations; these can be described by Boolean formulas (unfortunately with a lot more variables).

A Boolean formula can be (cheaply) brought into CNF using Tseytin transformation (at the cost of yet more new Boolean variables).

CBMC: How Does It Work?



Further Reading:

- CBMC Tutorial: http://www.cprover.org/cprover-manual/cbmc/tutorial/
- Edmund Clarke, et al. "Behavioral consistency of C and Verilog programs using bounded model checking." " Proceedings 2003. Design Automation Conference. IEEE, 2003.

CMU-CS-03-126.pdf

Optional :

■ Lucas Cordeiro, et al. "SMT-based bounded model checking for embedded ANSI-C software." IEEE Transactions on Software Engineering 38.4 (2011): 957-974. https://core.ac.uk/download/pdf/59348834.pdf

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