Hasso Plattner Institute
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Proposal Master's Thesis

Hardware-Conscious SIMD-Accelerated Sort-Merge Joins in Multi Core In-Memory Database Systems

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1 Motivation

Historically, many systems were designed for computer systems and architectures where I/O dominates performance. However, modern systems with multi-core architectures, larger DRAM capacities, advanced instruction sets, and other hardware accelerants like vector operations (SIMD), which allow us to perform the same operation on multiple data items simultaneously, have significantly altered this landscape. Hence, we must reconsider how we implement modern systems.

In-memory database systems, which store data directly in the main memory rather than on disk, provide significantly faster data access and processing due to reduced latency. Therefore, they are no longer I/O bound and, need high intra-operator parallelism. To fully utilize the multi-core architecture and other hardware features such as cache locality and SIMD instructions for higher data parallelism should be considered to achieve maximum performance.

In this thesis we want to look at one common database operator: the join [5]. The join operator is a fundamental component of a database system. In recent years, the difference in performance between the sort-merge and radix-hash join has been the subject of ongoing debate. Kim et al. [10] projected that Sort-Merge Join would outperform hash-based alternatives with 512-bit SIMD. Albutiu et al. [1] reinforced this claim with recent results reporting that their implementation of sort-merge join is superior to that of hash joins (without leveraging SIMD). Balkesen et al. [2] experimentally show contradicting results by implementing optimized versions for sort-merge and radix-hash join, showing that their implementation of radix-hash join is still superior.

Despite ongoing research, public implementations of join algorithms optimized for modern hardware are hard to find. Most existing implementations are proprietary or experimental[1], limiting their accessibility and usefulness to the research community and database developers. An open-source, state-of-the-art implementation of a sort-merge join optimized for different architectures would help address this need. Such an implementation serves as a valuable baseline for researchers looking to evaluate or improve upon existing methods, and it also contributes to advancing database system design by providing a solid foundation for future innovation.

2 Goal of Thesis

This thesis aims to efficiently implement the sort-merge join algorithm, explicitly optimized for specific architectures and hardware components. As equi-joins are the most common type of join operation, we will restrict ourselves to an equi-join implementation and then optionally extend upon this. While multiple papers exist about modern implementation approaches for sort-merge joins in in-memory database sys-

[1]Implementation by Balkesen et al.: `https://archive-systems.ethz.ch/node/334`

tems and SIMD sorting, only some have public implementations[2]. The goals of this thesis include an open-source implementation of a sort-merge join algorithm integrated into the Hyrise in-memory database. The sorting should be accelerated through SIMD parallelism and support AVX2 and AVX-512. The implementation should support int, float, and string data. We also want to experiment with other architectures like Arm and Power and run benchmarks to evaluate our approach.

2.1 Hyrise Integration

While some public implementations exist for modern and optimized sort-merge join, they have usually isolated implementations with a strong focus on the sorting step using randomly chosen input data, often already in the required data format. Also, they often skip the lookup of matching rows and the construction of the joined table. Hence, in this thesis, we want to integrate our implementation of the sort-merge join into Hyrise [8], a research in-memory database. Hyrise contains both a radix-based hash-join and sort-merge join. The sort-merge join uses radix cluster sorting, which uses "pdqsort" (Boost C++ library) but no explicit SIMD instructions. It fundamentally differs from the modern approaches in the literature. These differences allow us to test our implementation against the existing sort-merge and hash-based join.

2.2 SIMD Sorting

Most SIMD sorting algorithms presented in the literature are not directly applicable to join operations as they usually use sorting keys of only 32 bits. We must additionally track the row ID (rid) corresponding to the sorting key for a join, resulting in 64-bit elements. Most architectures only support 8-, 16-, 32-, and 64-bit elements for SIMD. Therefore, larger elements like 128-bit are usually not supported.

The current implementations of sort-merge join in literature use SSE and AVX2 intrinsics, but to our knowledge, there has yet to be an implementation using AVX-512. Therefore, in the scope of this thesis, we want to integrate support for modern AVX-512 sorting algorithms [18, 19].

2.3 Architectures

It would also be of value to see how new and existing approaches transfer to other CPU architectures like Arm with its Scalable Vector Extension (SVE) or Power with its Vector Scalar Extension (VSX).

Hence, in addition to x86 systems, we optinally want to experiment with AWS Graviton 4 and Power10. This requires adapting the implementation to use the respective architecture's vector extension (e.g., ARM SVE or Power VSX).

[2]Implementation of [2] published at `https://archive-systems.ethz.ch/node/334`

2.4 Benchmarking

Complete integration into an in-memory database allows us to run decision support benchmarks like TCP-H, TCP-DS, and the Join Order Benchmark (JOB) [11] to compare operators to other implementations in a more realistic scenario.

Benchmarks like TCP-H have schemas and datatypes carefully designed by experts in database design. Hence, they can fail to capture the chaotic nature of real-world applications [17]. For instance, TCP-H only uses integer values for keys.

However, many Business Intelligence applications use strings for various data types, e.g. to deal with dirty data that is not parsable. Hence, we frequently encounter string-type join keys. For that, we chose JOB due to its real-world data and ease of use, as it has already been integrated into Hyrise. The Public BI benchmark[3] also provides a realistic setting but is more difficult to use, and we only consider it optional.

Benchmarking should also include measuring the sorting throughput in tuples per second and all algorithmic steps: initial data construction in the format of (key, rid) from the input relations, sorting, finding join partners, and the final construction of the joined table.

3 Approach

The sort-merge join involves sorting both input relations. It is the most crucial and time-consuming part of the sort-merge join operation. Therefore, high optimization efforts should be spend on this step, as it largely determines the runtime.

Due to modern multi-core architectures, sorting should intensively utilize thread-level parallelism by multithreading. With the recent architectural trends of wider register widths for SIMD, sorting should also heavily use SIMD instructions to exploit data parallelism.

In a multi-core context, we prefer mergesort over quicksort, as the parallelization of the divide-and-conquer approach is straightforward, and it has other advantages over quicksort such as more predictable and cache-friendly memory access patterns and better load balancing through equal-sized partitioning.

3.1 Data Preparation

Before we can sort our input relations, the colum values need to be translated into a SIMD sortable format. Usually, a 64-bit pair (key, rid) (key & rid both 32-bit) is assumed. We, therefore, support a maximum relation size of 2^{32}. With most value types greater than 32 bits, e.g. strings, we need to compress the values of the join columns to 32 bits. Methods like key-prefix [14] and XOR- and shift-based hash functions [6] have been used to generate keys of 32 bits.

[3] `https://github.com/cwida/public_bi_benchmark`

As strings are variable in size, it makes sense to consider their internal representation and encoding. Certain string representations allow for cheap access to a prefix or short string. For instance, Umbra's string representation [13] consists of a 128-bit struct and is adopted by more recent databases like CedarDB and DuckDB. The first 32 bits represent the length. The remaining bits hold the complete string if the length is at most 12. Otherwise, the struct consists of the 32-bit length, a 32-bit prefix, and a pointer to a storage location. Due to saving pointer dereferences, this can speed up comparison, lexicographical sorting, and other prefix operations.

3.2 Partitioning

To make use of the multi-core architecture, the unsorted column data of both join relations are partitioned into chunks and distributed among the available threads. One option for partitioning is to divide the unsorted inputs into thread counts of many contiguous sections of equal size. Using this strategy, occurrences of the same value can happen in multiple partitions, always requiring a global merge over all partitions (even if global sorting is not required). Another option is range partitioning, e.g., through radix partitioning. We can often improve radix-partitioning through software-managed buffers and non-temporal streaming stores (for x86 provided by AVX instruction set) [16]. For architectures with non-uniform memory access (NUMA), it can make sense to distribute equally over NUMA regions and let threads read from their closest NUMA region. However, for this thesis, we will keep NUMA optimizations optional.

3.3 Sorting and Merging

3.3.1 SIMD Sort- and Merge-Networks

To efficiently utilize SIMD, we need an algorithm that aligns with the SIMD execution model. Sorting and merging networks meet these criteria. For a network of input size n, n items enter the network from left to right through a series of comparators that emit the larger value to the top and the smaller value to the bottom. We can implement such a network with only min/max operators. The input is in arbitrary order for a sorting network, leaving the network sorted. For a merging network, the input comprises two sorted halves that merge into one sorted list of size n. There are two standard merging network types: bitonic merge networks and odd-even merge networks [7].

We can replace each input item with a SIMD vector and use vectorized min/max operations to take advantage of SIMD. The input items are sorted across SIMD registers, therefore requiring additional transposition. Due to the merge networks' poor scaling [12], we can use small merging networks within a merging algorithm for larger lists [9].

3.3.2 Merging Higher Levels

We can merge different subparts of the data in different threads as long as we have enough sorted sublists. In the later round of the merge tree, with only a few sorted sublists remaining, parallelizing becomes more challenging. However, parallelization is still possible through algorithms like Merge Path [15]. This conceptual path allows us to parallelize a two-way merge by splitting it into non-overlapping segments that form disjoint sets of elements. We can then merge these segments in parallel. In the later stages, out-of-cache merging becomes necessary, potentially creating a bottleneck through memory bandwidth limitations. Therefore, multi-way merging [2, 7] solves this problem by saving roundtrips to memory. It implements a merge-tree. Each node is a two-way merge unit, with nodes connected via FIFO queues. Only the leave nodes directly access memory. By pausing and starting the execution of nodes, we always ensure that all combined FIFO queues still fit into the cache. By doing so, we step-by-step propagate buffers of merged data through the merge tree until all data is merged. Optionally, we could explore merging through other primitives, such as tournament trees and priority queues.

3.4 Joining

After sorting both input relations, a final loop over both sorted input relations suffices to find all join candidates. The sorted data is of the form (key, rid). Hence, we can use the row ID (rid) to find the respective tuples. As compression can result in false positives in the merging step, we might require additional validation and filtering. Further parallelization of this final merge step is also possible.

4 Related Work

Several papers describe how SIMD-accelerated sorting can be done efficiently on modern multi-core architectures. Chhugani et al. [7] describe the concepts needed for efficient SIMD sorting for both single- and multi-core execution. MergePath [15] presents an algorithm for merging a few very large sublists in parallel. Kim et al. [10] implemented a sort-merge join using SSE intrinsics, projecting performance for wider SIMD widths that would outperform hash joins. Albutiu et al. [1] present MPSM, a sort-merge join implementation without SIMD, concluding that their sort-merge join implementation is faster than the hash join implementation of Blanas et al. [4]. Balkesen et al. [2] experimentally studied the performance of sort-merge and radix-hash join. They claim to provide the fastest in-memory join algorithms using sorting and hashing. Still, they conclude that the radix-hash join exceeds the sort-merge join for 256-bit SIMD. They also claim that their parallel radix-hash join is the most efficient hash-join implementation yet [3]. The hash join operator implemented in Hyrise is also based on [3] and [2].

None of the papers mentioned above take advantage of 512-bit SIMD. There is research on SIMD sorting using AVX-512 [18, 19]. To the best of our knowledge, no literature exists on implementing sort-merge join with the same optimizations and concepts like multiway merging for AVX-512.

5 Project Plan

Table 1: Planned Time Table

Time	**Writing/Research**	**Prototype**
Oct - Nov	– Setup for different architectures – SIMD sorting building blocks – Single-threaded SIMD sorting – Adapt to all architectures	– Setup for x86, IBM Power, AWS Graviton. – Implement sorting- and bitonic-merge networks on different architectures. – Implement single-threaded SIMD sorting (for 64-bit keys and starting with 256-bit support)
Nov - Jan	– AVX-512 specific sorting – Multiway-Merging – Hyrise integration – Simd sorting of string types	– Scale up sorting- and bitonic-merge networks to wider bit width. – Explore further possible improvements through AVX-512 specific instructions. – Implement Multiway Merging (Explore alternatives: tournament-trees, priority-queue). – Working sort-merge-join implementation for integer/float types on different architectures. – Implement prefix- and hash-based key compressions (real string data from Public BI benchmark).

Jan-Feb	– Benchmarking & Evaluation	– Parameter tuning for different architectures. – Compare to hash-join and old sort-merge join (Hyrise). – Run TCP-H, TCP-DS and Public BI benchmark.
Feb-Mar	– Thesis Writing & Evaluation	– Draft of master thesis
Mar-Apr	– Thesis Writing & Evaluation	– Finished master thesis

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