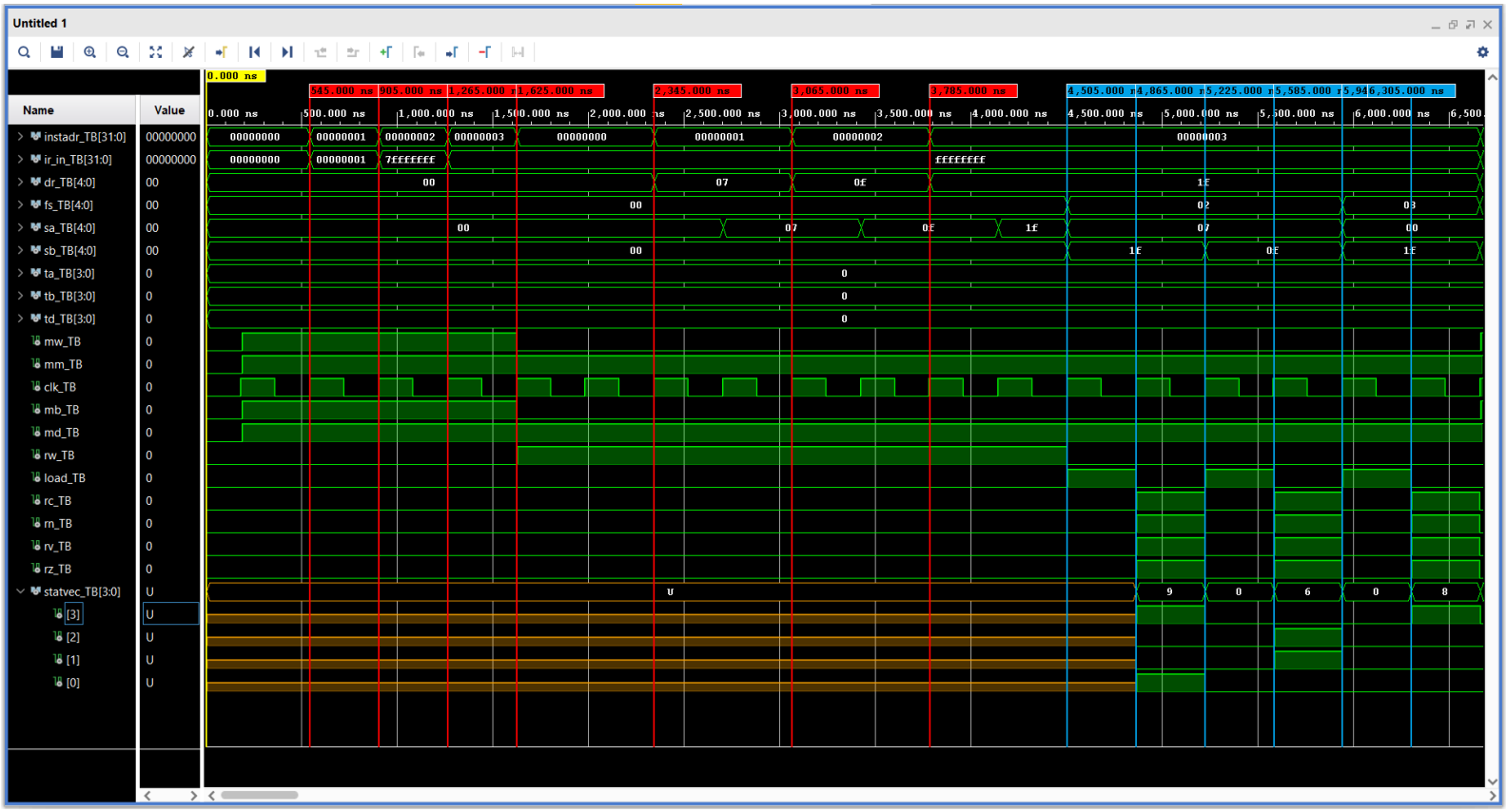
CPU_Processor_Test02_21363904



The timing diagram for the second Processor Test is shown above. All numbers are in Hexadecimal notation. Each Clock Cycle lasts 360ns.

The red lines denote when the Instruction Address changes, loading 4 different values into the first 4 memory address: 0x00000000, 0x00000001, 0x7FFFFFFF and 0xFFFFFFFF. These values are then loaded into registers 0, 7, 15 and 31 so that some microoperations can be performed on them. The effects of these operations on the status vector is reflected by looking at the blue lines which denote when the flags are set or reset in the status vector. Adding 0x00000001 and 0xFFFFFFFF generates a Carry and a Zero Flag, adding 0x00000001 and 0x7FFFFFFF generates a Negative and an Overflow flag, and ANDing 0x00000000 with 0xFFFFFFFF generates a Zero Flag. The flags are reset after each operation.