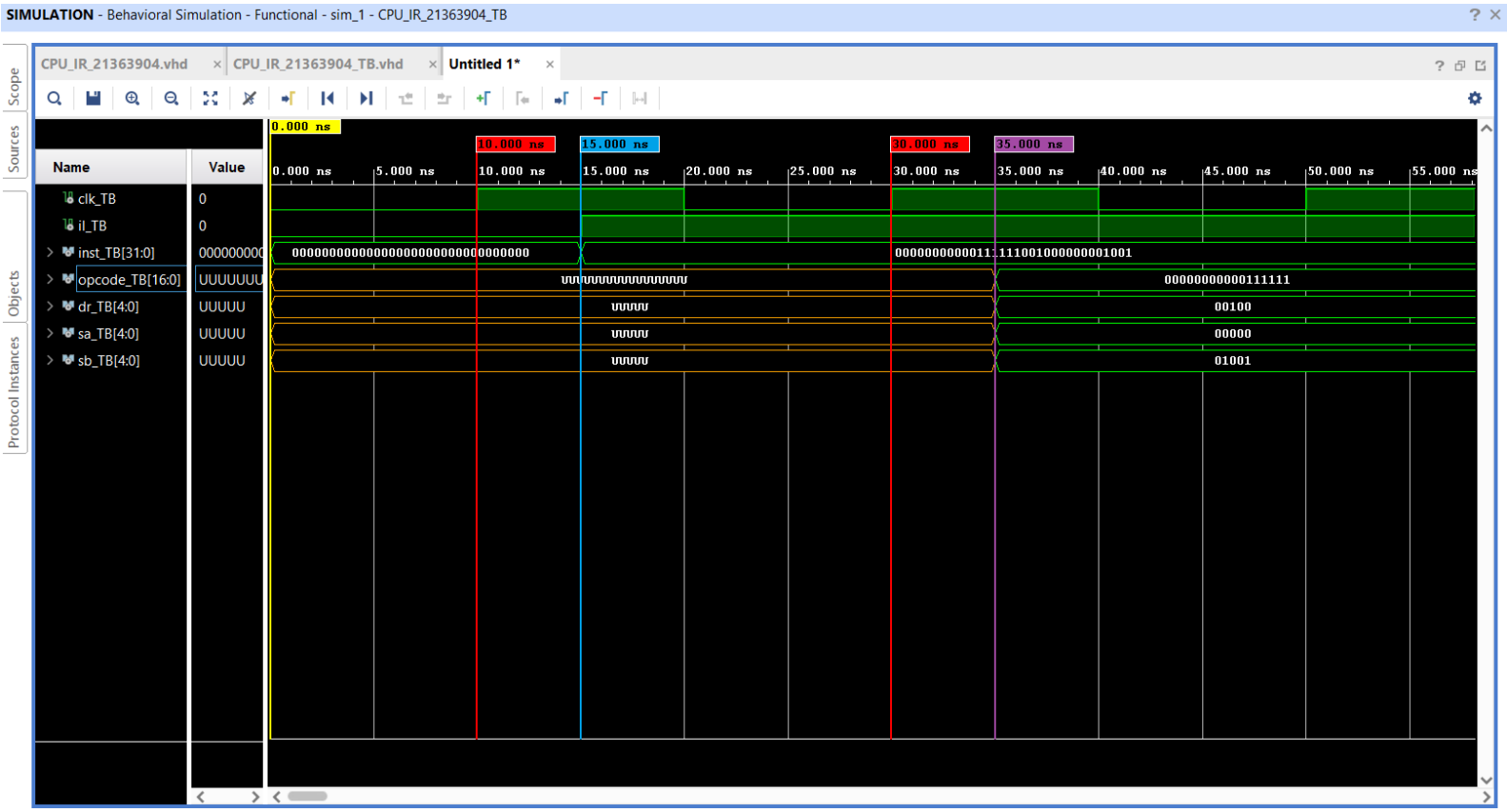
CPU_IR_21363904



The timing diagram for the Instruction Register is shown above. All numbers are in Binary notation. Each clock cycle takes 20ns.

The red lines denote the rising edges of the clock, the blue line shows when the input is changed, and the purple line indicates when the correct value appears at the output. On the first cycle, the data appears at the input after a 5ns delay, and on the second cycle the corresponding outputs appear after the same delay. The input instruction is constructed so that the four outputs give the desired values for the Opcode (63), Destination Register (4), Source Register A (0) and Source Register B (9), which are digits 4 and 3, digit 0, digit 1 and digit 2 of my Student ID respectively.