CPU_RAM_21363904

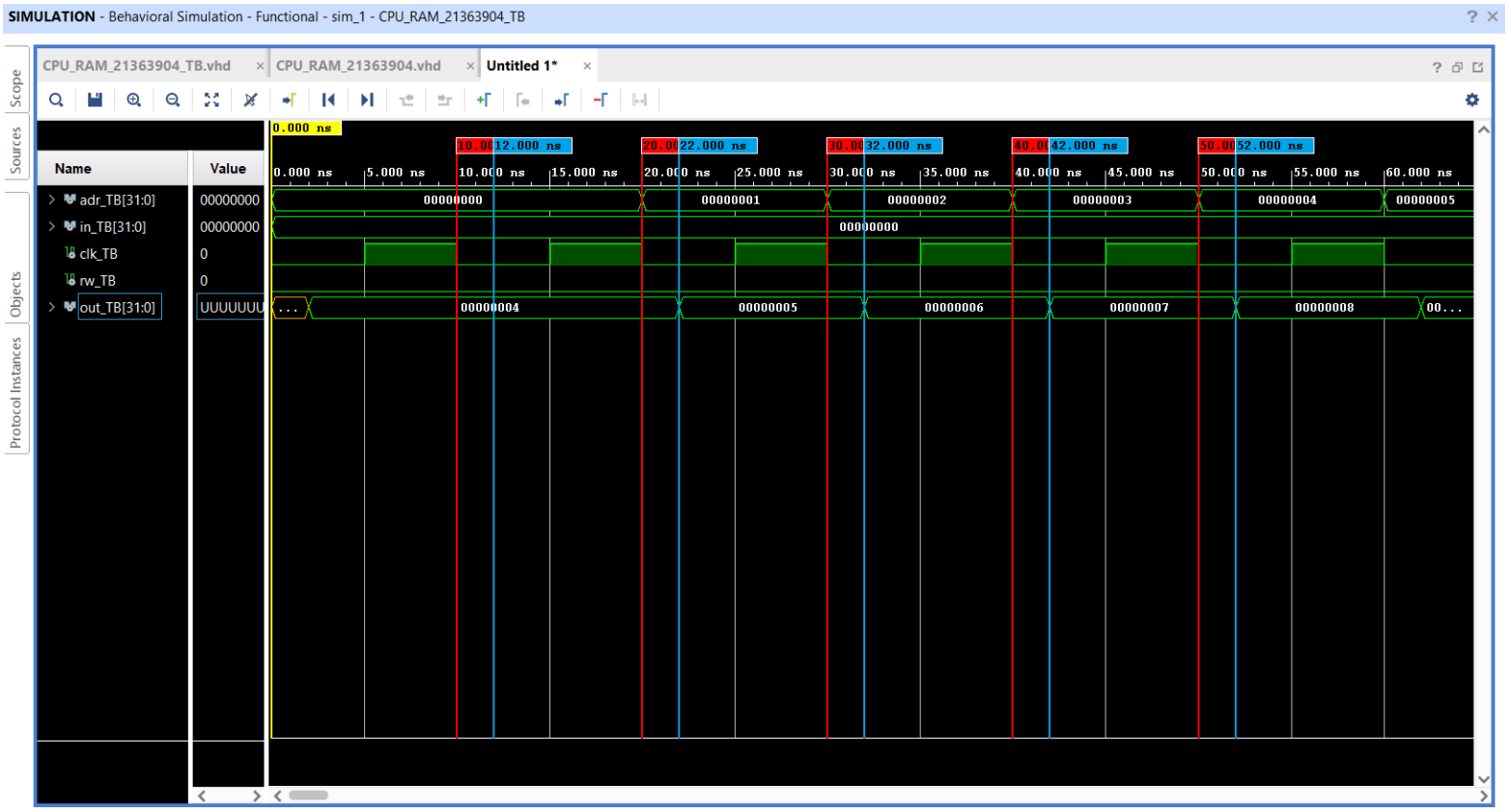
The timing diagrams for the Processor RAM are shown below. All numbers are in Hexadecimal notation. Inside the RAM design source the memory locations are initialized by default to the last 2 digits of my Student ID (04) incremented for every location.

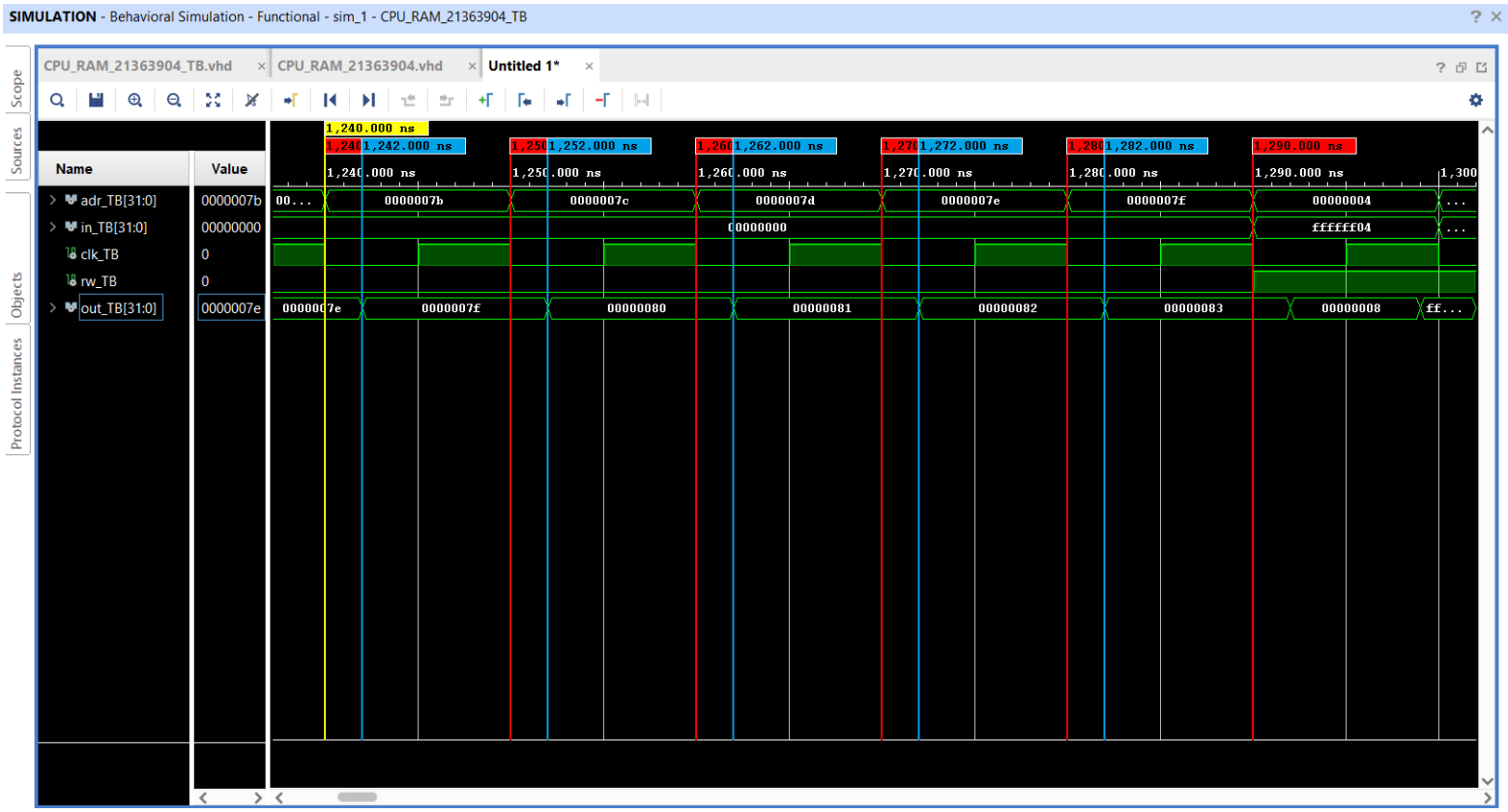
In the first two diagrams the memory addresses in the RAM are being read, starting with address 0x00000000 and ending with address 0x0000007F. The red lines show when the address data is loaded into the RAM 5ns after the rising edge of the clock (coinciding with the falling edge), and the blue lines show when the correct data corresponding to the chosen address appears at the output after a propagation delay of 2ns.

In the second two diagrams 32 memory locations (starting at address 0x00000004, the last digit of my ID) are overwritten with arbitrary incrementing values (0xFFFFFFxx, where xx is the last two digits of the current address). The red lines show when the address data is loaded into the RAM 5ns after the rising edge of the clock (coinciding with the falling edge), the pink lines show when the previous data corresponding to the address appears at the output after 2ns, and the blue lines show when the new data written to the location appears at the output during the next clock cycle, 9ns after it was inputted. This happens as writing to a location takes 4ns plus the standard 5ns every instruction takes to take effect after each rising clock edge.

At the right of the final diagram we can see an attempt to write the value 0xFFFFFFFF into memory location 0x00000000. The attempt is unsuccessful as the WriteEnable signal is not set, demonstrated by the fact that the output does not change from the value already stored in the address – 0x000000004.

CPU_RAM_21363904





CPU_RAM_21363904