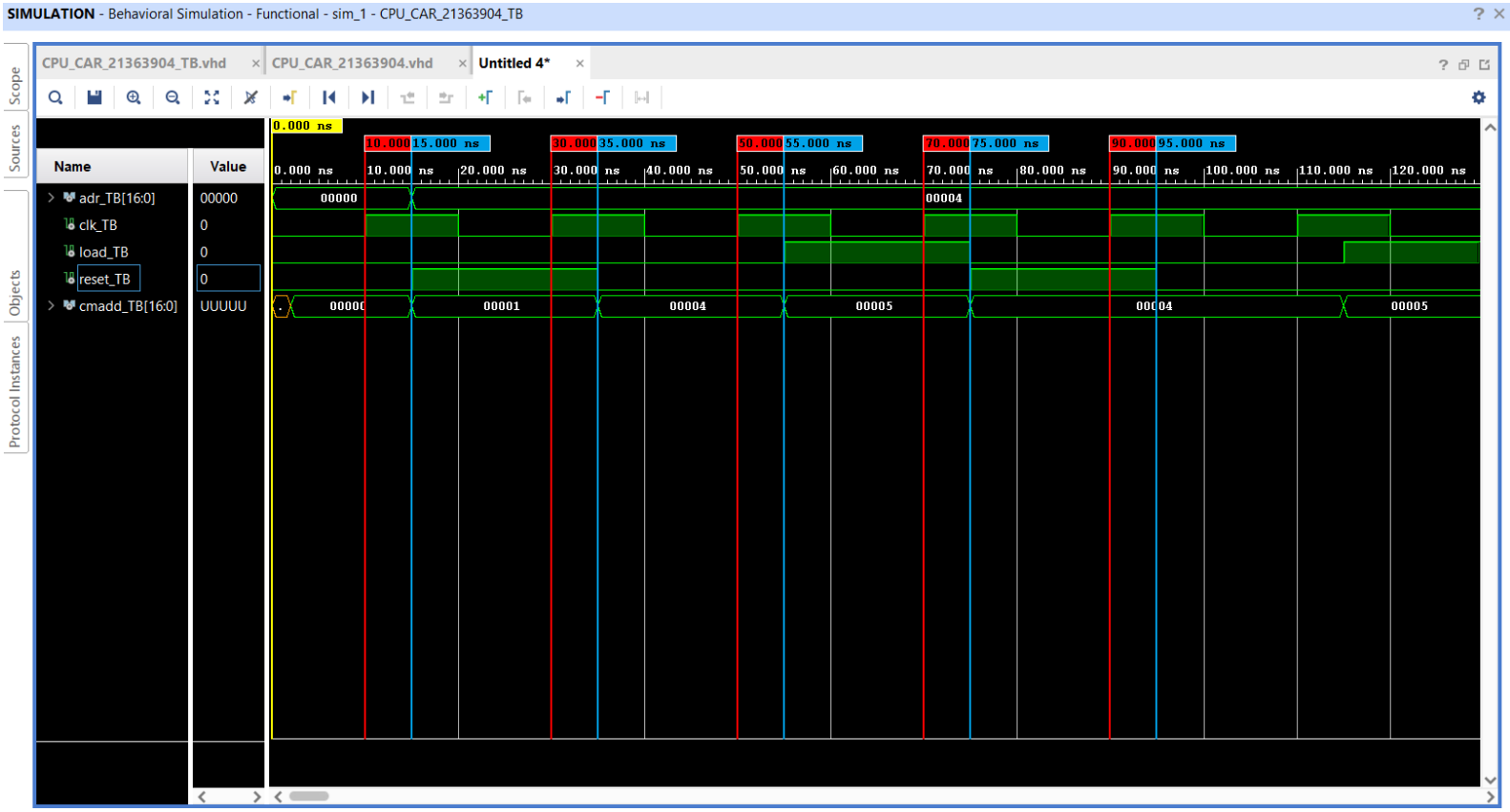
CPU_CAR_21363904



The timing diagram for the Control Access Register is shown above. All numbers are in Hexadecimal notation. Each Clock Cycle lasts 20ns.

The red lines denote the rising edges of the clock, and the blue lines mark both when the inputs change and when the result of the previous cycle's inputs are displayed. When the reset and load are both 0, the CAR increments, which is displayed during the first clock cycle before the reset is set, and during the third clock cycle after the CAR has been reset to the last digit of my ID (4) on the second cycle. On the fourth clock cycle the CAR is loaded with the last two digits of my ID (04, the same as the reset value) after the load signal is set during the third clock cycle.