CPU_SignExtend_21363904



The timing diagram for the Sign Extend is shown above. All numbers are in Binary notation.

The red lines denote when the input data changes, and the blue lines show when the corresponding output is shown after a 5ns propagation delay. The first input is a negative 2s complement number, while the second input is a positive 2s complement number. The leading 1 on the first input is extended to preserve the value across 32 bits, and the leading 0 on the second input is extended to preserve its value. This way the sign and number remain the same going from 10 to 32 bits.