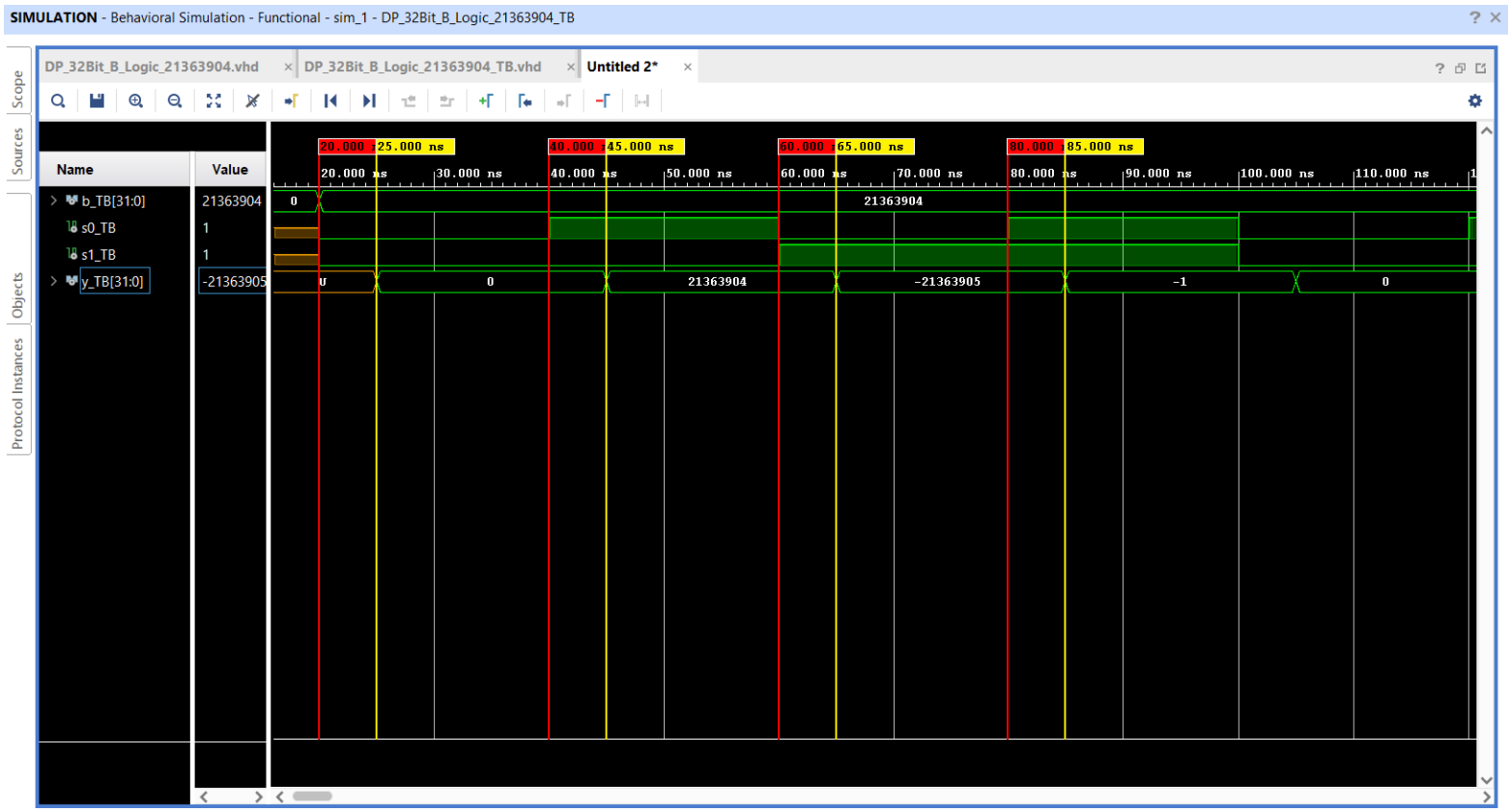
DP_32Bit_B_LogicCircuit_21363904



The timing diagram for the 32Bit B Logic Circuit is shown above. All numbers are in Signed Decimal notation. Input *B* is loaded with my Student ID (21363904). The red lines mark when the select inputs change and the yellow lines mark when the correct value appears at the output, after a propagation delay of 5ns. Looking at the diagram we can see that when both selects are set to 0, all 0s appear at the output. When *s*0 is set, the value at *B* (my Student ID) appears at the output, and the 1s Complement of *B* appears when *s*1 is set. When both selects are set, all 1s appear at the output (seen here as -1 in Signed Decimal).