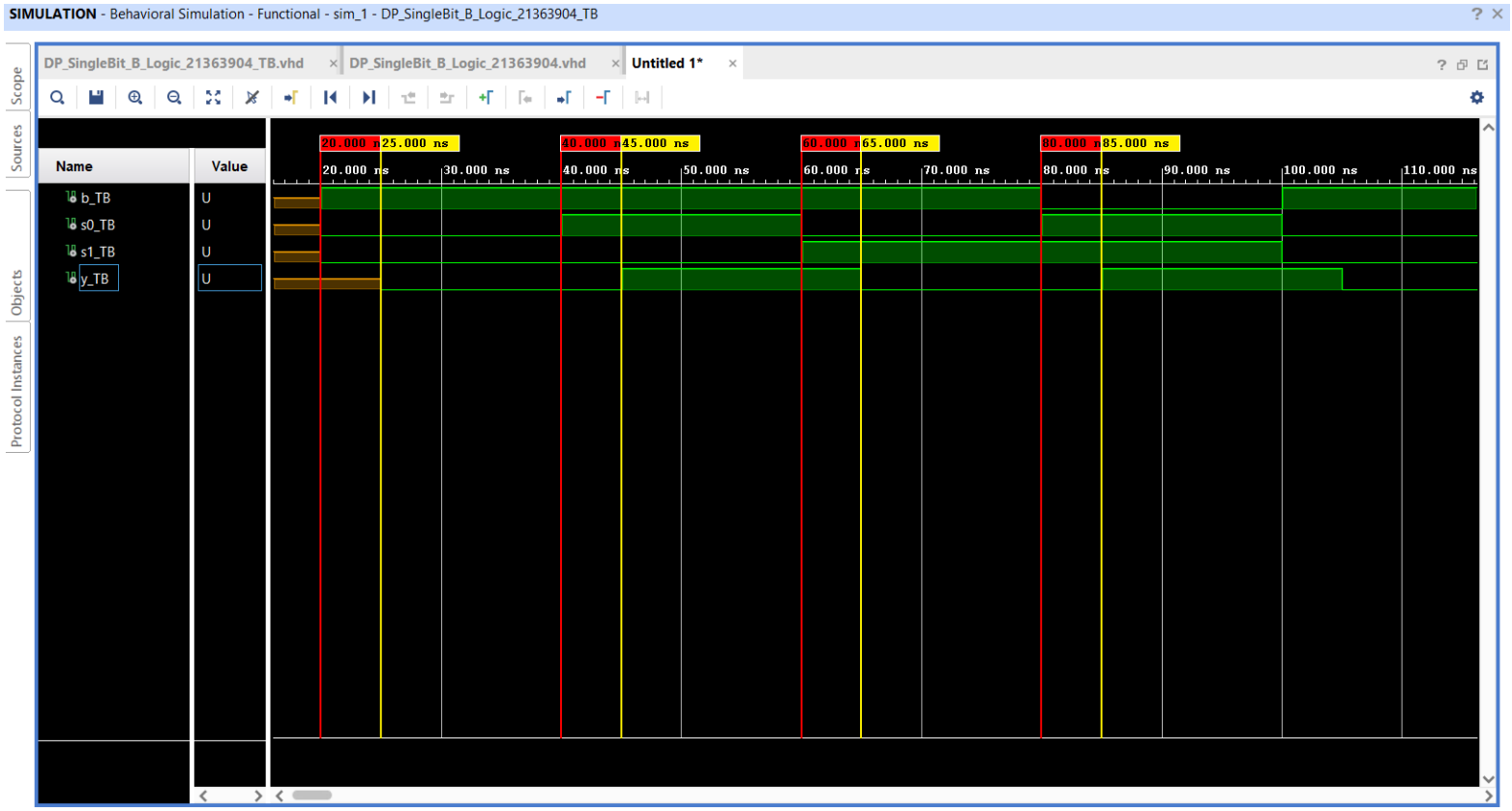
DP_SingleBit_B_Logic_21363904



The timing diagram for the Single Bit B Logic is shown above. The red lines mark when the select inputs change and the yellow lines mark when the correct value appears at the output, after a propagation delay of 5ns. Input *B* is set to 1 for demonstration purposes, except for the last test in which it is set to 0. When both selects are 0, the output is 0, regardless of input. When *s*0 is 1, the value at input *B* is displayed. When *s*1 is 1, the inverse (1s complement) of *B* is displayed, and when both selects are 1, the output is 1, regardless of input.