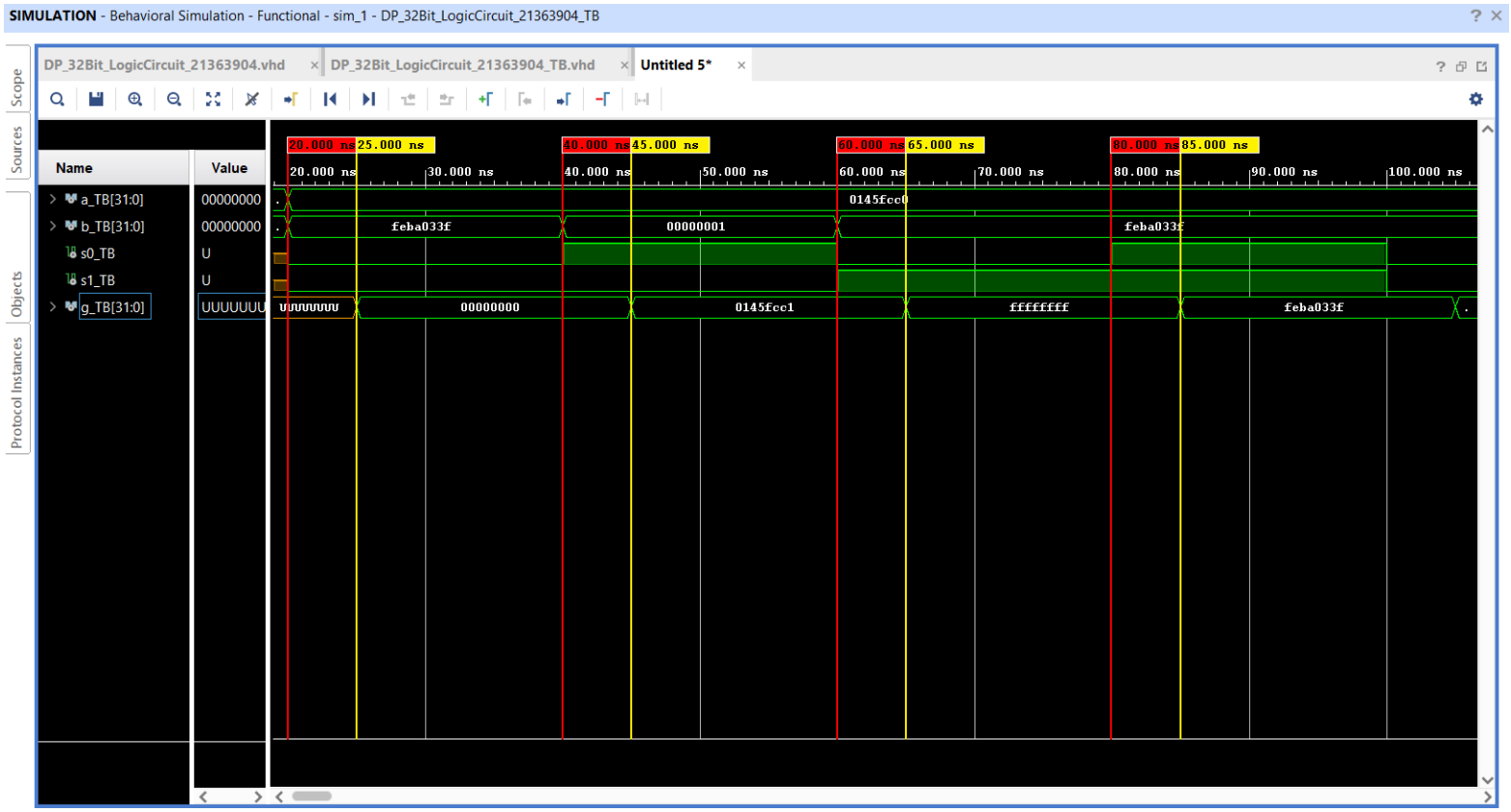
# DP_32Bit_LogicCircuit_21363904




The timing diagram for the 32Bit Logic Circuit is shown above. All numbers are in Hexadecimal notation. Input $A$ is loaded with my Student ID ($0145FCC0$) and Input $B$ is loaded with three different values to best demonstrate each operation. The red lines mark when the select inputs change and the yellow lines mark when the correct value appears at the output, after a propagation delay of 5ns. When both selects are set to 0, the result of $A\ AND\ B$ (with $B$ set to $FEBA033F$, the 1s Complement of my Student ID) appears at the output, which is 00000000, as the two numbers $AND$ed together cancel each other out. When $s0$ is set to 1, the result of $A\ OR\ B$ (with $B$ set to 00000001) appears at the output, which is $0145FCC1$, my Student ID + 1, as the last digit of the ID (0) $OR$ed with 1 will give 1, while all the other 1s in the output are from my Student ID. When $s1$ is set to 1, the result of $A\ XOR\ B$ (with $B$ set back to $FEBA033F$) appears at the output, which is $FFFFFFFF$ because $XOR$ing a number with its inverse will mean none of the bits are the same. When both selects are set to 1, the result of $NOT(A)$, the inverse of my Student ID, appears at the output, which is $FEBA033F$.