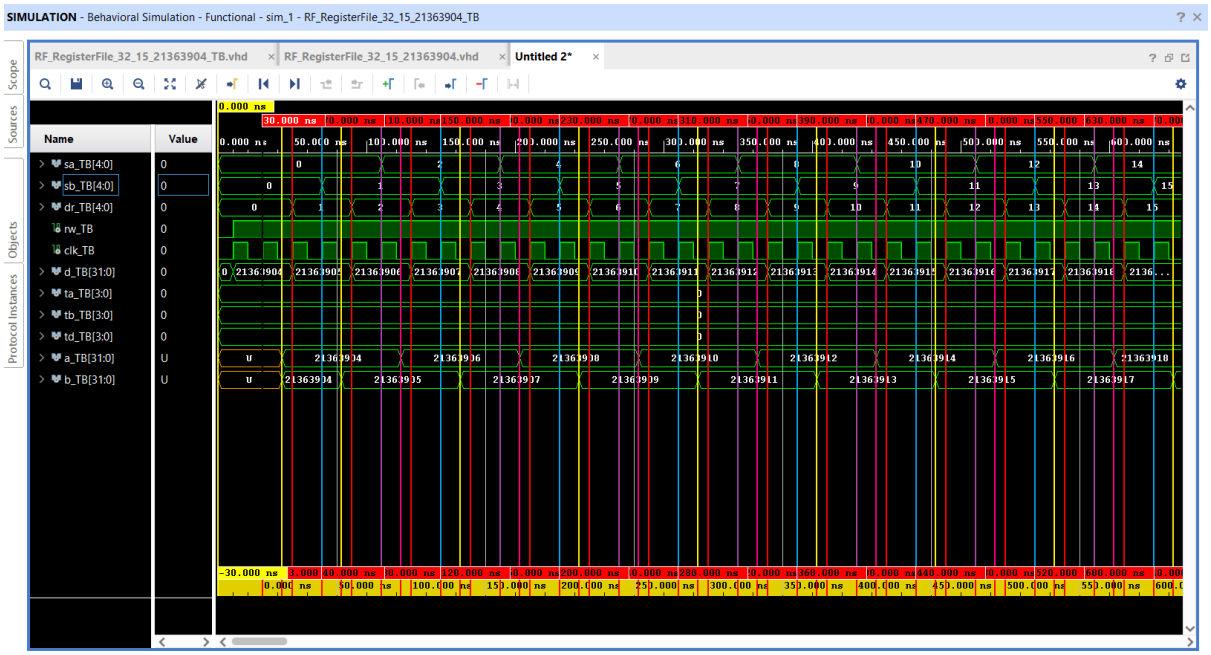
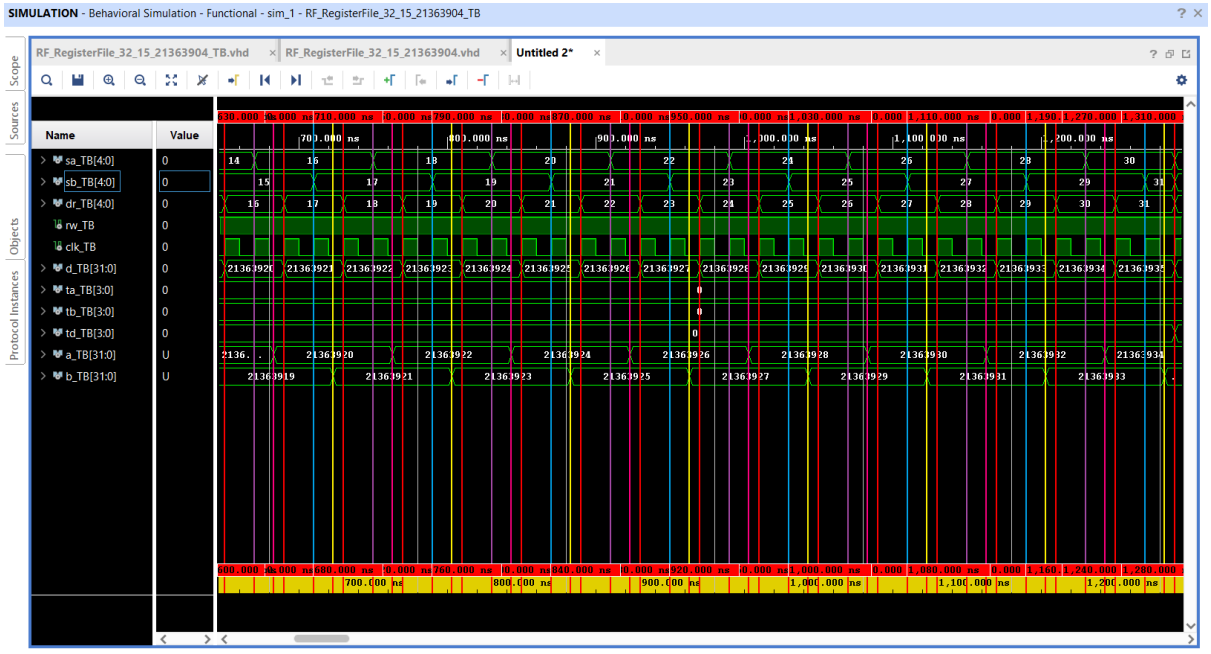
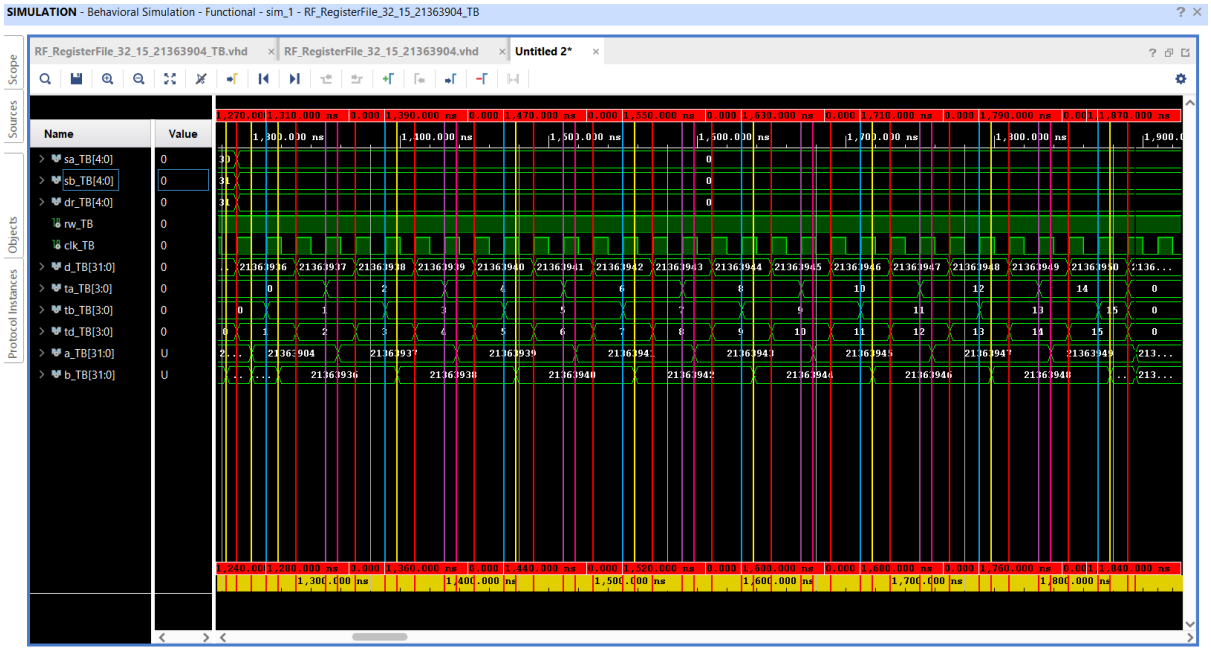
RF_RegisterFile_32_15_21363904





RF_RegisterFile_32_15_21363904



The timing diagrams for the Register File are shown above. The first diagram shows the input values being written into and read from the first 16 registers, the second image shows this for the other 16 registers, and the last shows it for all 15 temp registers.

In these diagrams, each register is first written to, then read from one of the ports to verify its contents (alternating between the A Port and B Port). This is done sequentially for all 32+15 registers.

The red lines indicate when the value at Data_In (the input value) changes to the next value (my student ID + *n*), and also the register that the data is to be written into (via DR or TD). The blue lines show when the register to read from is selected at SB or TB, and the purple lines show when the register to be read from is selected at SA or TA. The yellow lines show when the correct output value is read from the selected register at the B Port, while the pink lines show where the correct output value is read from the selected register at the A Port. The clock is used for the purpose of writing to (loading) registers.

The Read/Write signal RW is constantly enabled to decrease complexity for testing purposes. In the diagram for the Test_RegisterFile the RW signal is correctly enabled and disabled for the register transfer operations.