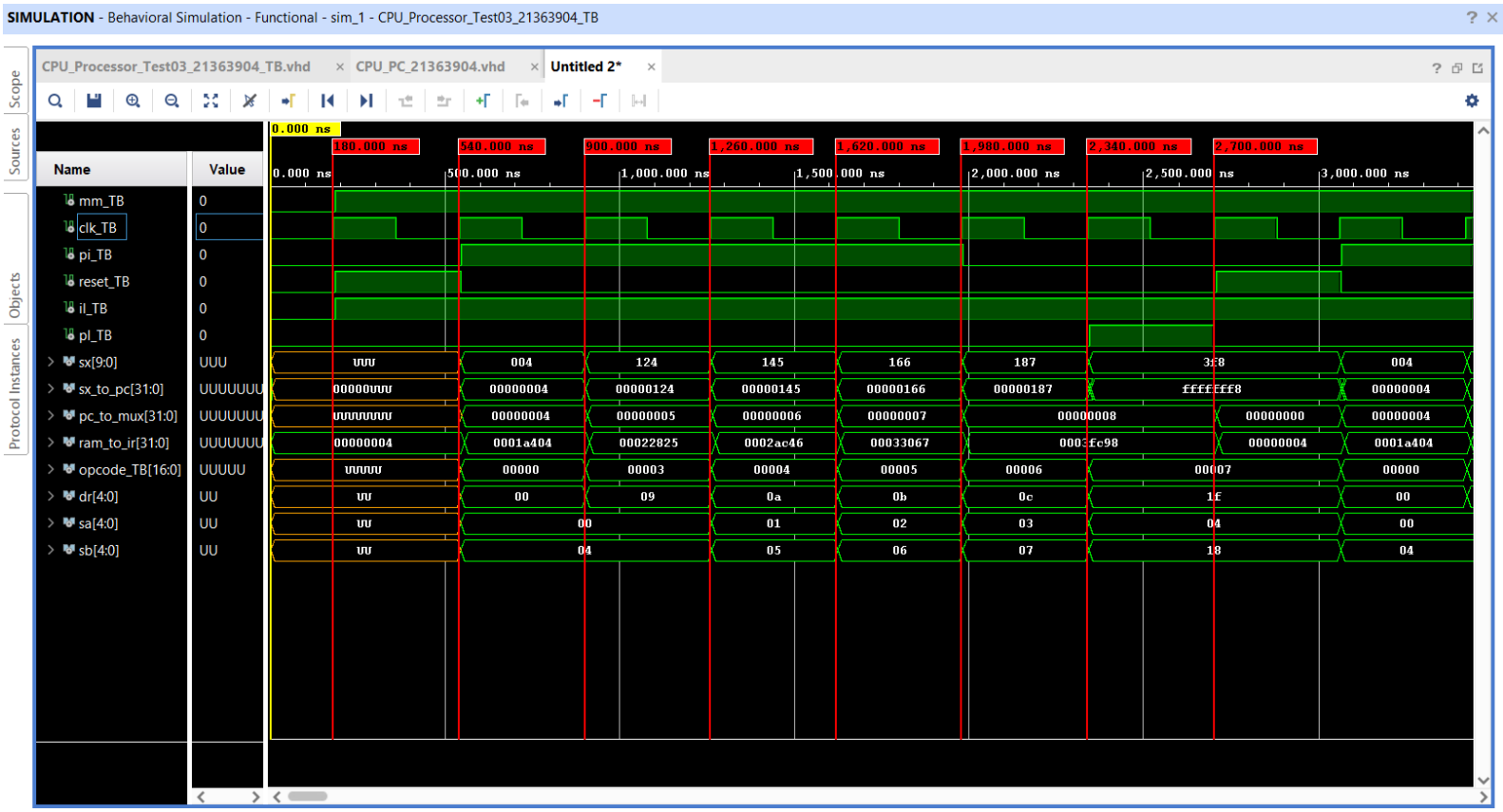
CPU_Processor_Test03_21363904



The timing diagram for the third Processor Test is shown above. I've removed any signals we are not interested in from the waveform. The RAM has been initialized with the requested instructions in memory addresses 0x04 – 0x08, with the final instruction containing a DR and SB value designed to displace the program counter back to the first address in memory (0x00). All numbers are in Hexadecimal notation. Each Clock Cycle lasts 360ns.

The red lines denote the rising edges of the clock. On the first clock cycle we reset the program counter to the Reset Value (0x04). We can see that by the second cycle the first instruction is loaded from this address in the RAM into the Instruction Register, which outputs the corresponding digits of my Student ID (3,9,0 and 4) as the Opcode, DR, SA and SB respectively on the next clock cycle. This is repeated for the other four instructions by incrementing the program counter, except when the last instruction is output from the Instruction Register, the Program Counter's load signal is set, allowing the counter to be displaced back to the first address in the RAM, which stored value 0x00000004 (coincidentally also the Reset Value of the PC).