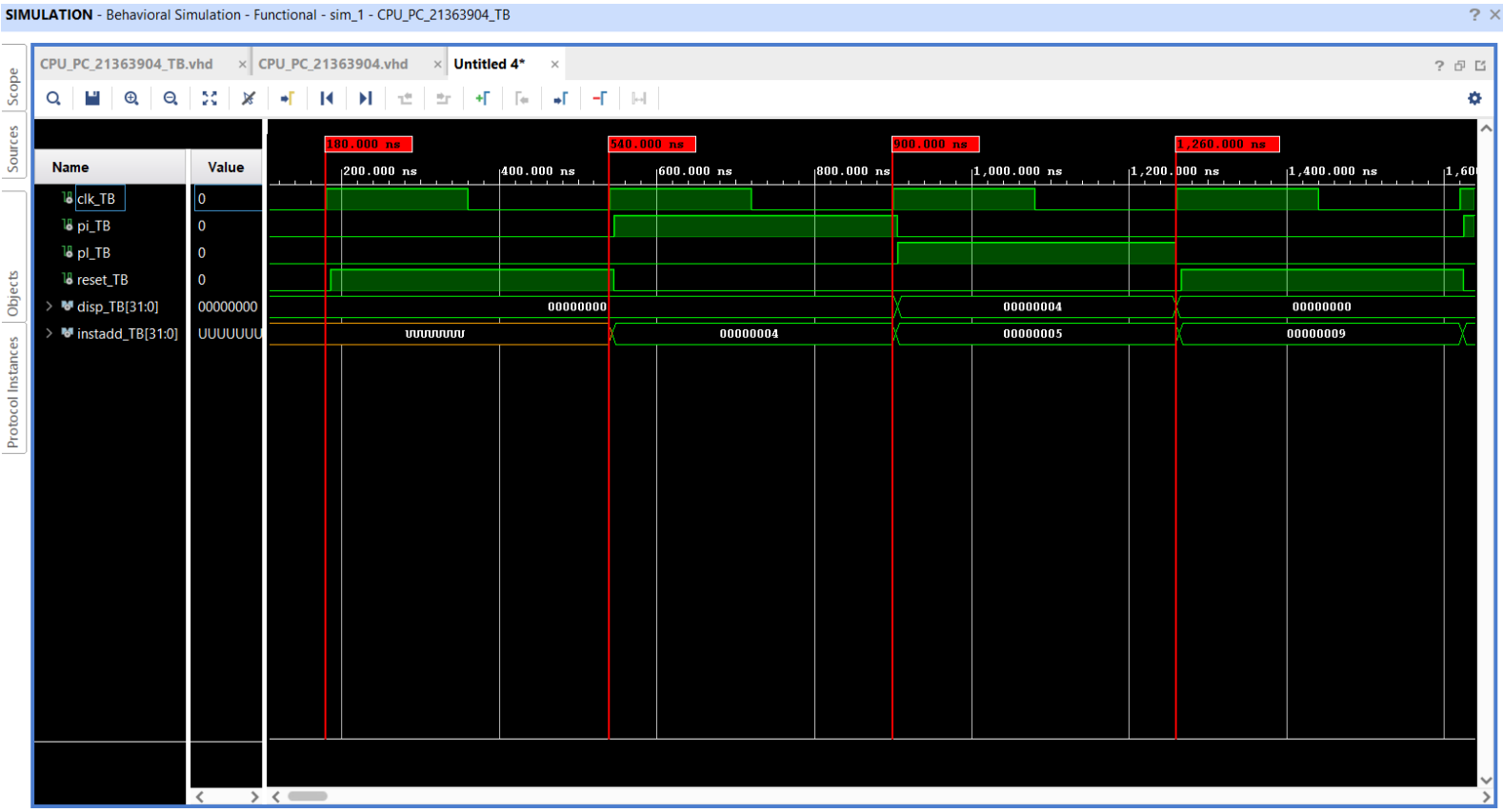
CPU_PC_21363904



The timing diagram for the Program Counter is shown above. All numbers are in Hexadecimal notation. Each clock cycle takes 360ns.

The red lines denote the rising edges of the clock. On the first clock cycle, the Reset signal is set after a 5ns delay, loading the Reset Value (4, the last digit of my ID) so that during the second cycle this data appears at the output after a 5ns propagation delay. On the third clock cycle the counter is incremented by 1 by setting PI, and on the fourth cycle the counter is displaced by the last 2 digits of my ID (04) by setting PL. The outputs are displayed one clock cycle later.