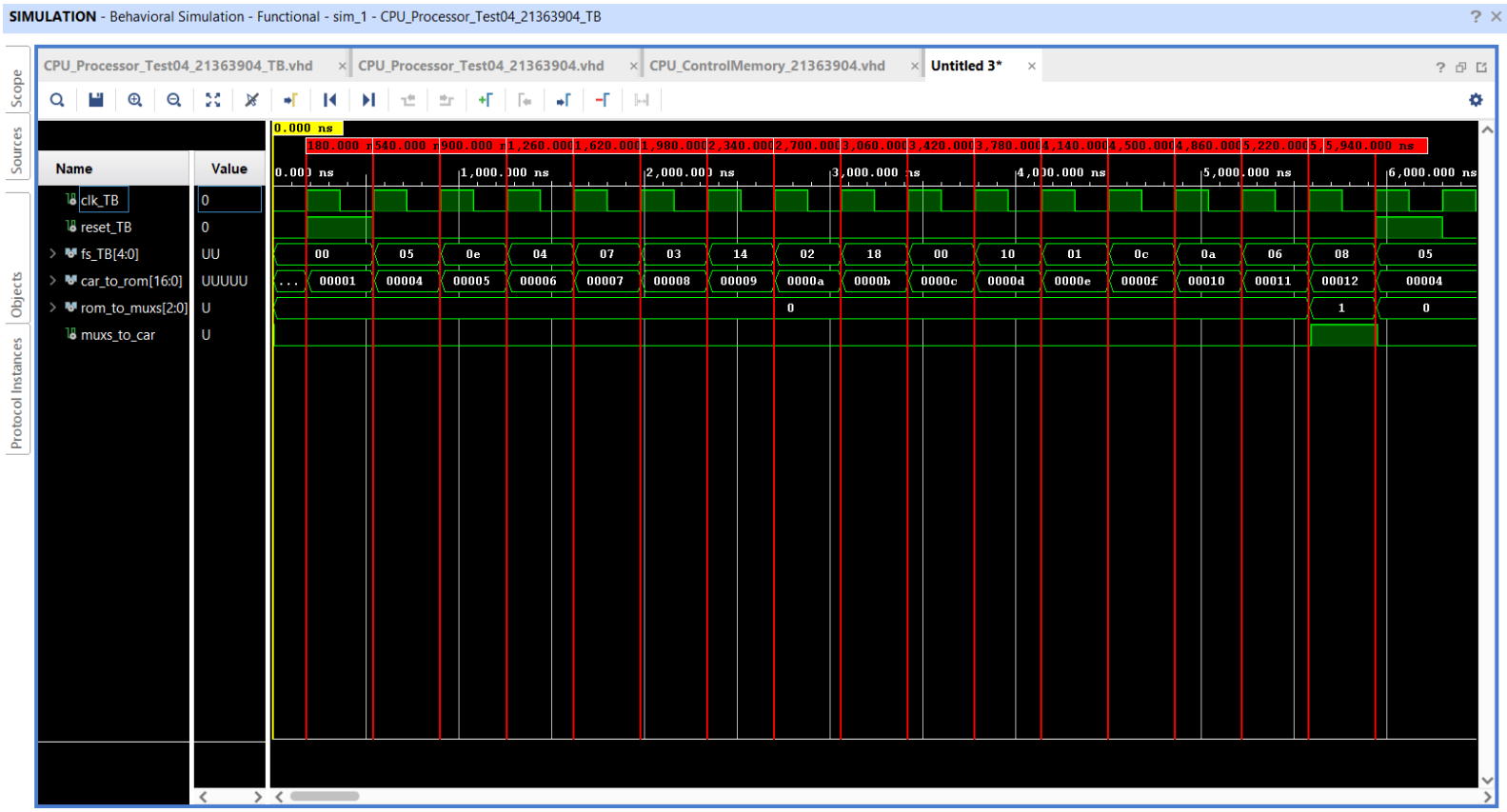
CPU_Processor_Test04_21363904



The timing diagram for the fourth Processor Test is shown above. All numbers are in Hexadecimal notation. Inside the ROM design source the FS values are loaded with the 15 microoperations in the order determined by the last digit of my Student ID as requested. The first of these operations is at the address determined by the last 2 digits of my ID (04). The Next Address field of the final microoperation points back to the address of the first (04), and the MS field is set to 001 so that the CAR loads this address instead of incrementing. Each Clock Cycle last 360 ns.

The red lines denote the rising edges of the clock. The first cycle resets the CAR to the address of the first microoperation (04), which is seen in the *car_to_rom* signal in the following clock cycle along with the correct FS value. In the second cycle the CAR increments to the next address, with the associated address and FS value shown in the next clock cycle. This pattern repeats right up until the address of the final microoperation is reached. At this point, the Next Address and MS are set to 04 and 001 respectively, in order to reset the CAR back to the address of the first microoperation by setting its load input and passing in said address. The CAR then returns to the address of the first microoperation and the cycle begins again.