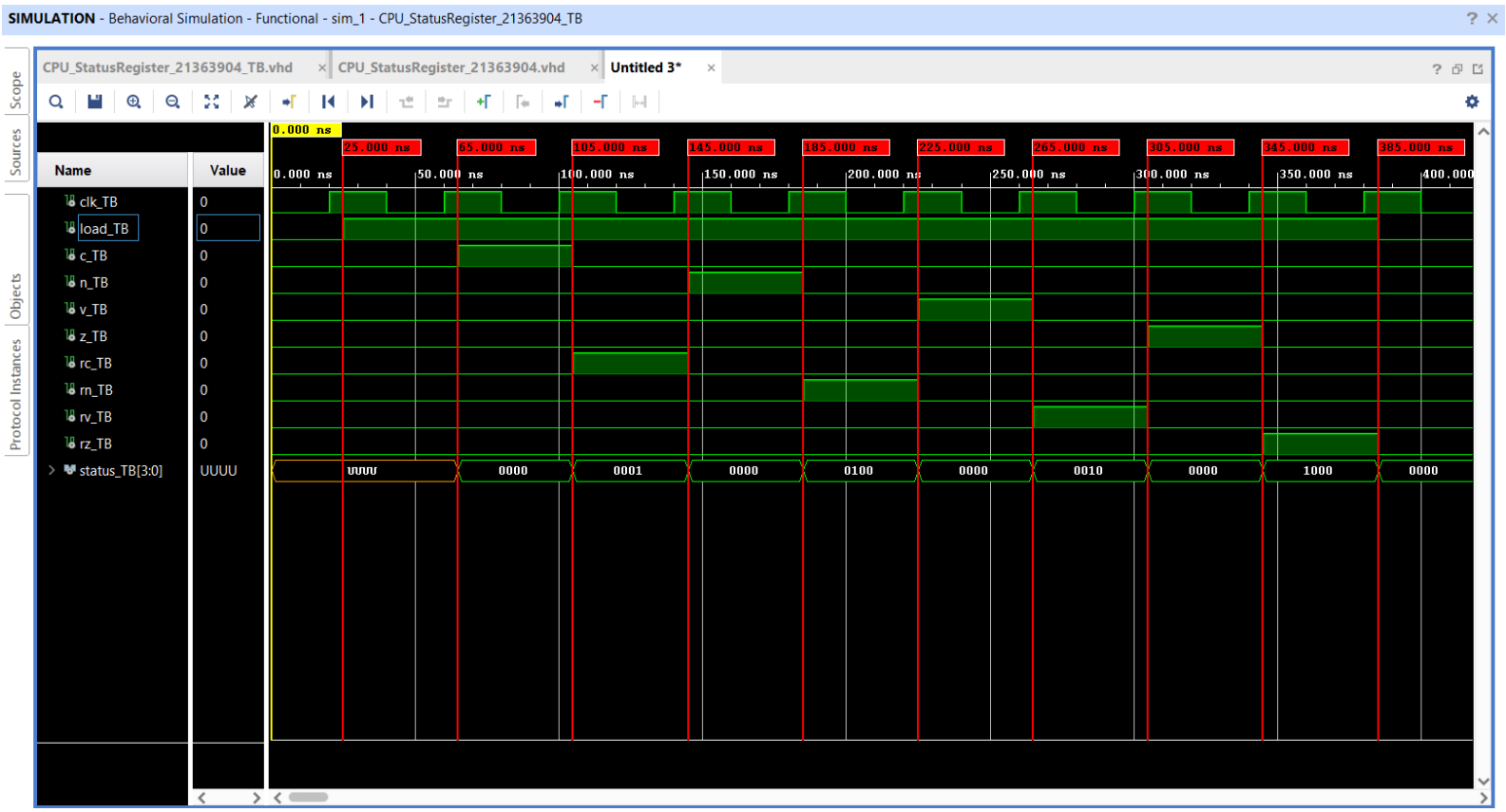
CPU_StatusRegister_21363904



The timing diagram for the Status Register is shown above. All numbers are in Binary notation. Each clock cycle lasts 40ns.

The red lines denote when the input data changes, 5ns after the rising edge of the clock. The corresponding output appears at the beginning of the next clock cycle. On the first clock cycle the load signal is set, allowing the flags to be loaded into the register. The C flag is loaded on the second clock cycle and reset on the third, which is reflected in the output by bit 0 being set at the third clock cycle and then unset at the fourth. This patterns follows for the N, V and Z flags, which are loaded into bits 2, 1 and 3 of the register respectively before being reset.