

CPU_DFlipFlop_21363904



The timing diagram for the D Flip Flop is shown above. Each clock cycle takes 20ns.

The **red lines** denote the rising edges of the clock, and the **blue lines** show when an input parameter is set 5ns later. On the first cycle, the data appears at the input, while on the second cycle, the enable signal is set, allowing the data to be loaded into the flip flop, appearing at the output during the next clock cycle, after a 5ns propagation delay. During this third clock cycle the enable is unset, so that during the fourth clock cycle the setting of the reset clears the output 5ns after the fifth rising clock edge.