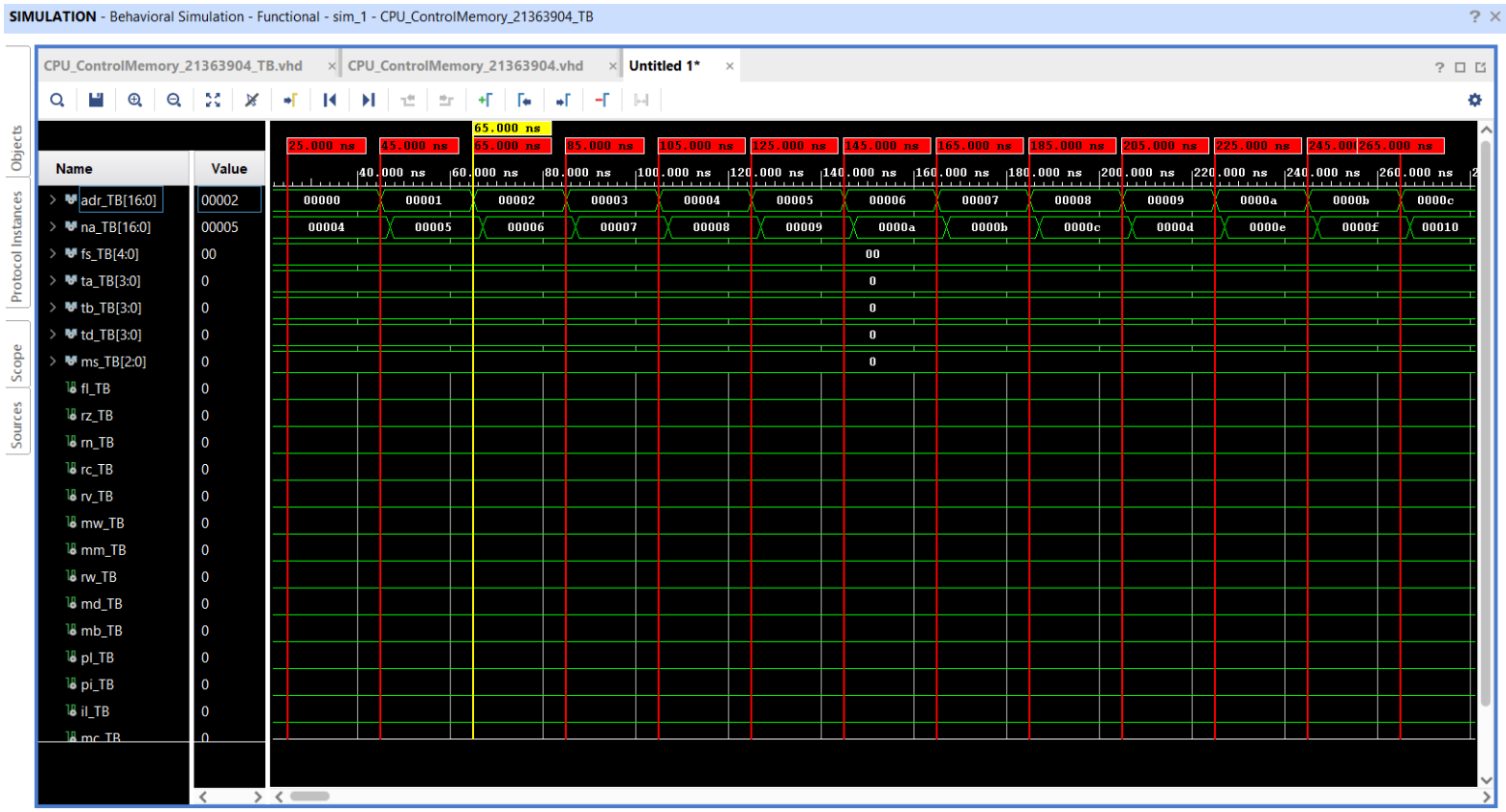
CPU_ControlMemory_21363904

The timing diagrams for the Control Memory are shown below. All numbers are in Hexadecimal notation. Inside the ROM design source the memory locations are initialized by default to the last 2 digits of my Student ID (04) incremented for every location.

The red lines show when the input address changes, and the corresponding output is shown 2ns later in the NA signal. Choosing the first address (0x00) gives the contents of the first address in the ROM, which is the last 2 digits of my ID (04). The second address (0x01) gives my ID + 1 (05), and so on all the way up to address 0x7C, which then gives the value 00 due to wrap around (incrementing 7F by 1 gives an 8Bit number, so the 8th bit does not appear, leaving us with just the rightmost 7 bits). Address 0x7F gives the value 03, so that returning to the first address brings us up to 04 again. The three diagrams below demonstrate this pattern.



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