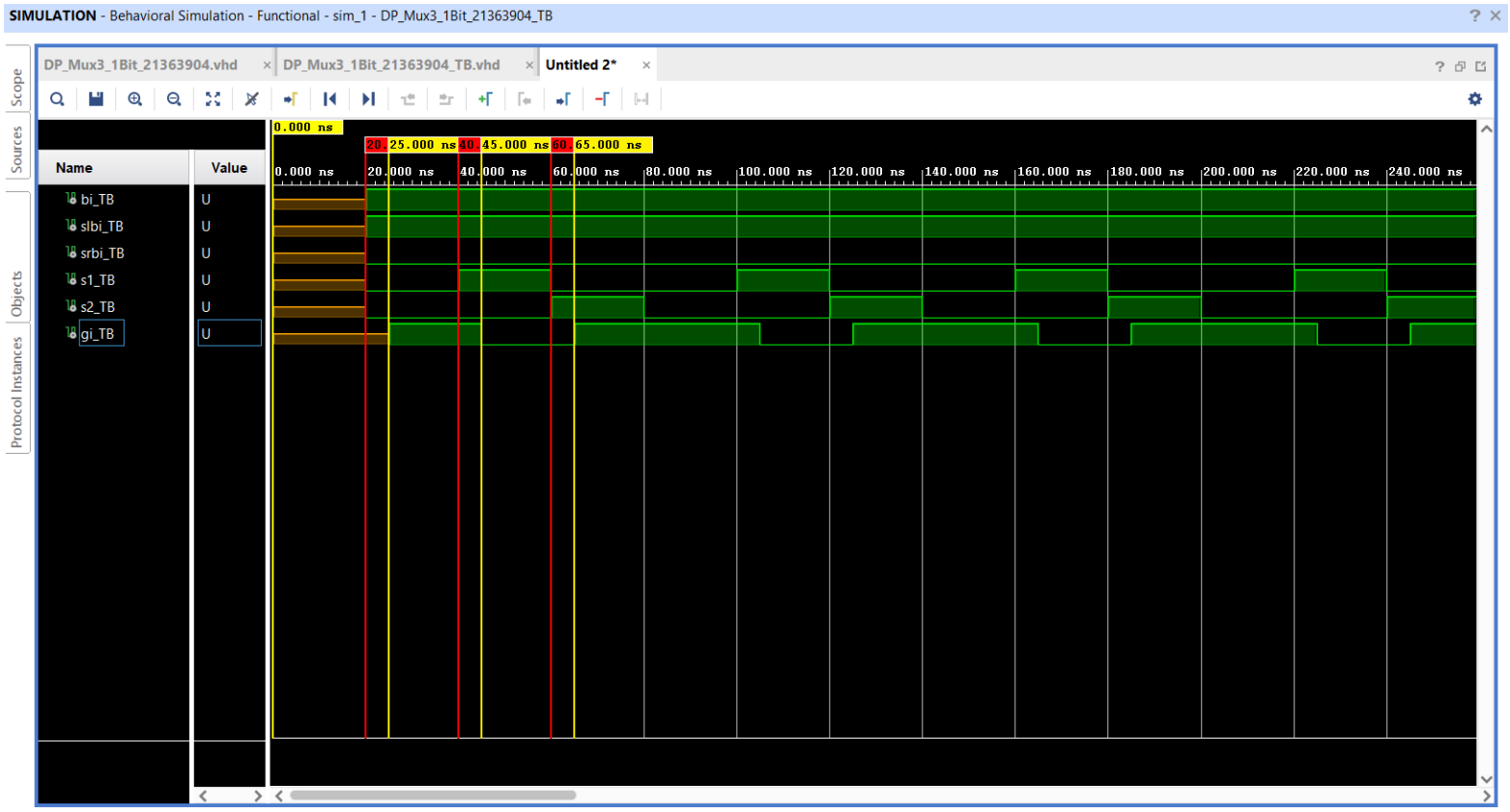
DP_Mux3_1Bit_21363904



The timing diagram for the 1Bit Multiplexer is shown above. The red lines mark when the select inputs change and the yellow lines mark when the correct value appears at the output, after a propagation delay of 5ns. B_i and slB_i are set to 1 and srB_i is set to 0 for the purposes of demonstration. When $s1$ is 1, srB_i (0) is displayed, and when $s2$ is 1, slB_i (1) is displayed. B_i (1) is shown in any other case.