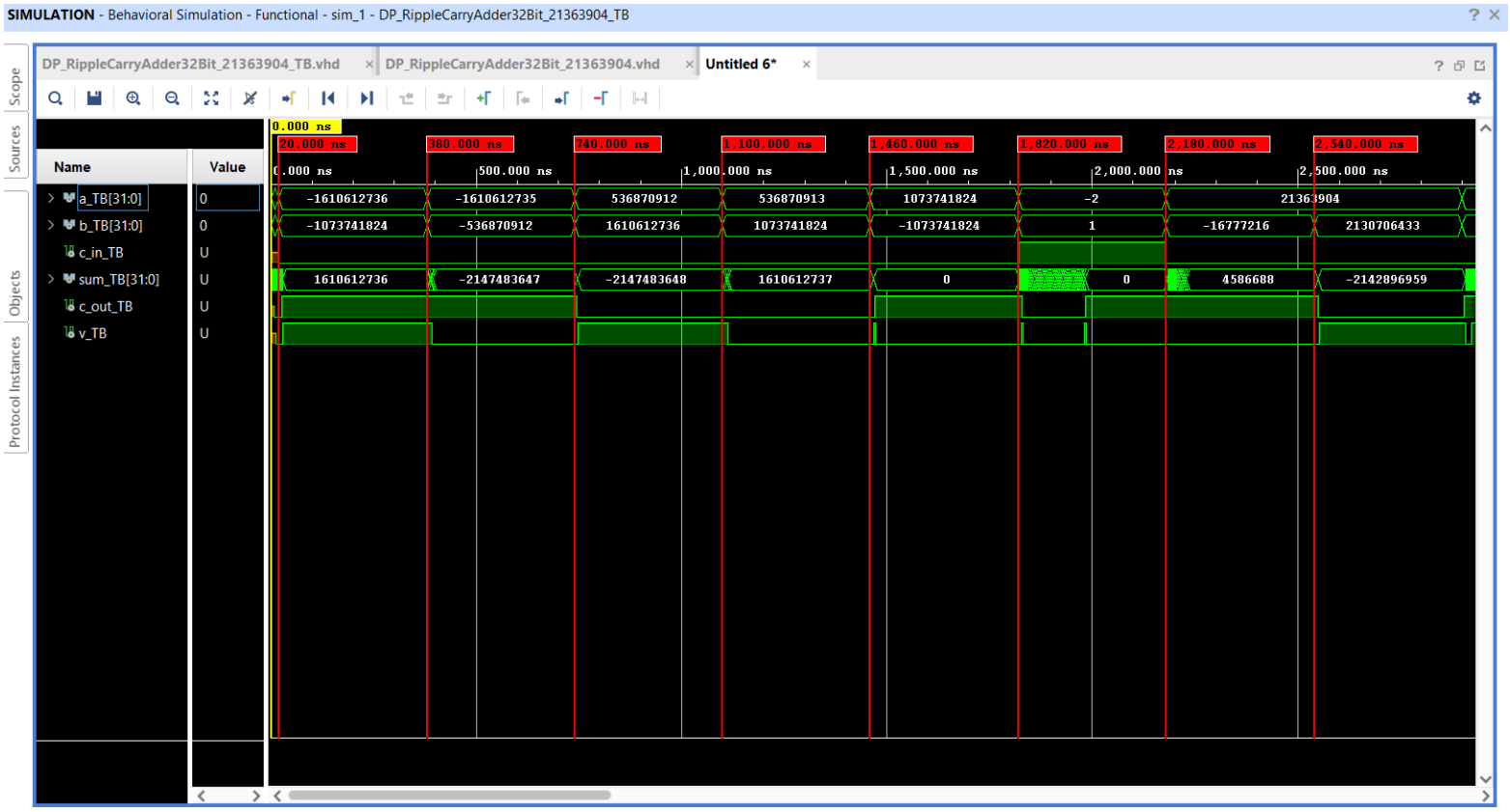
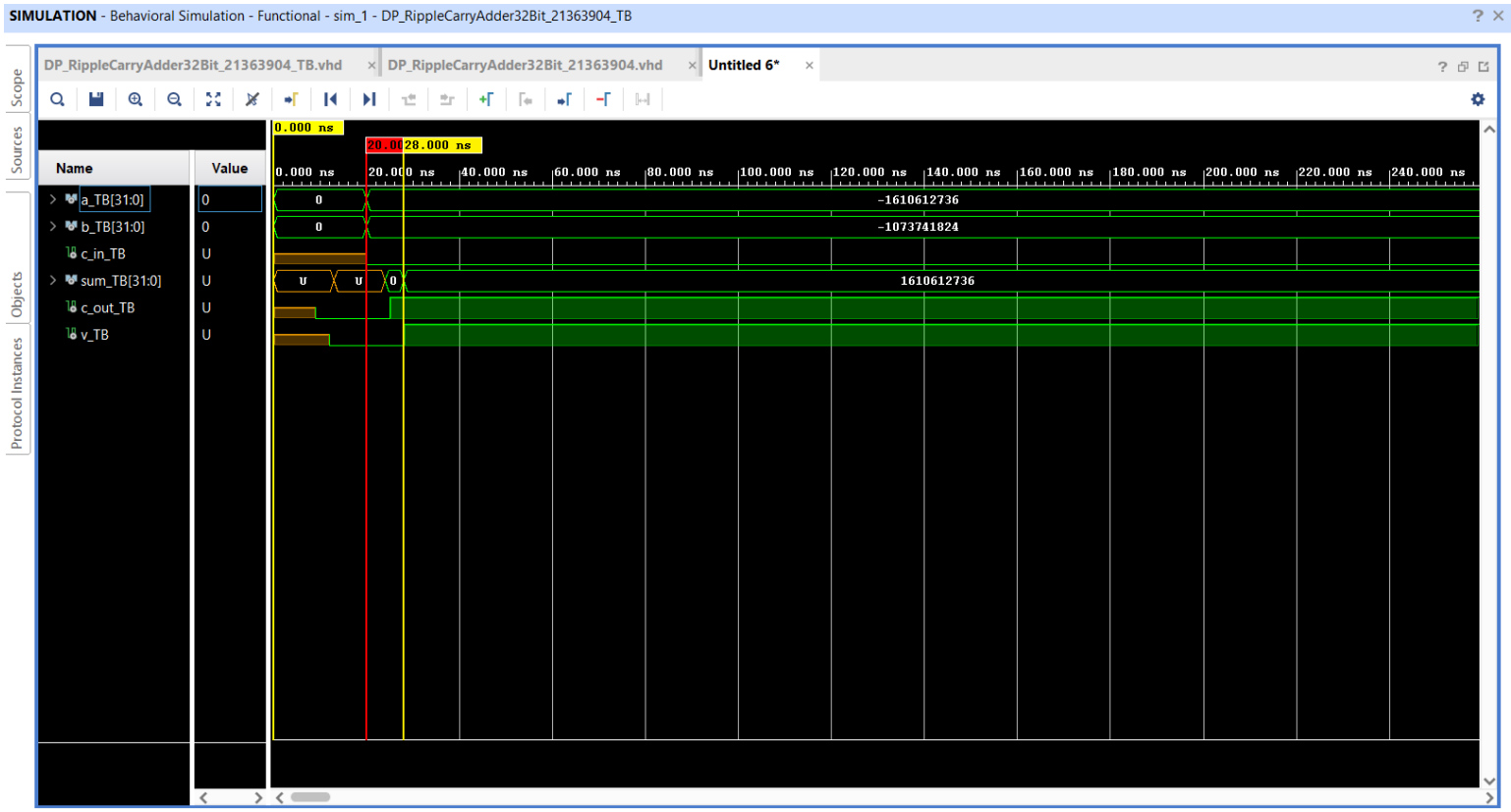
# DP_ArithmeticLogicUnit_21363904



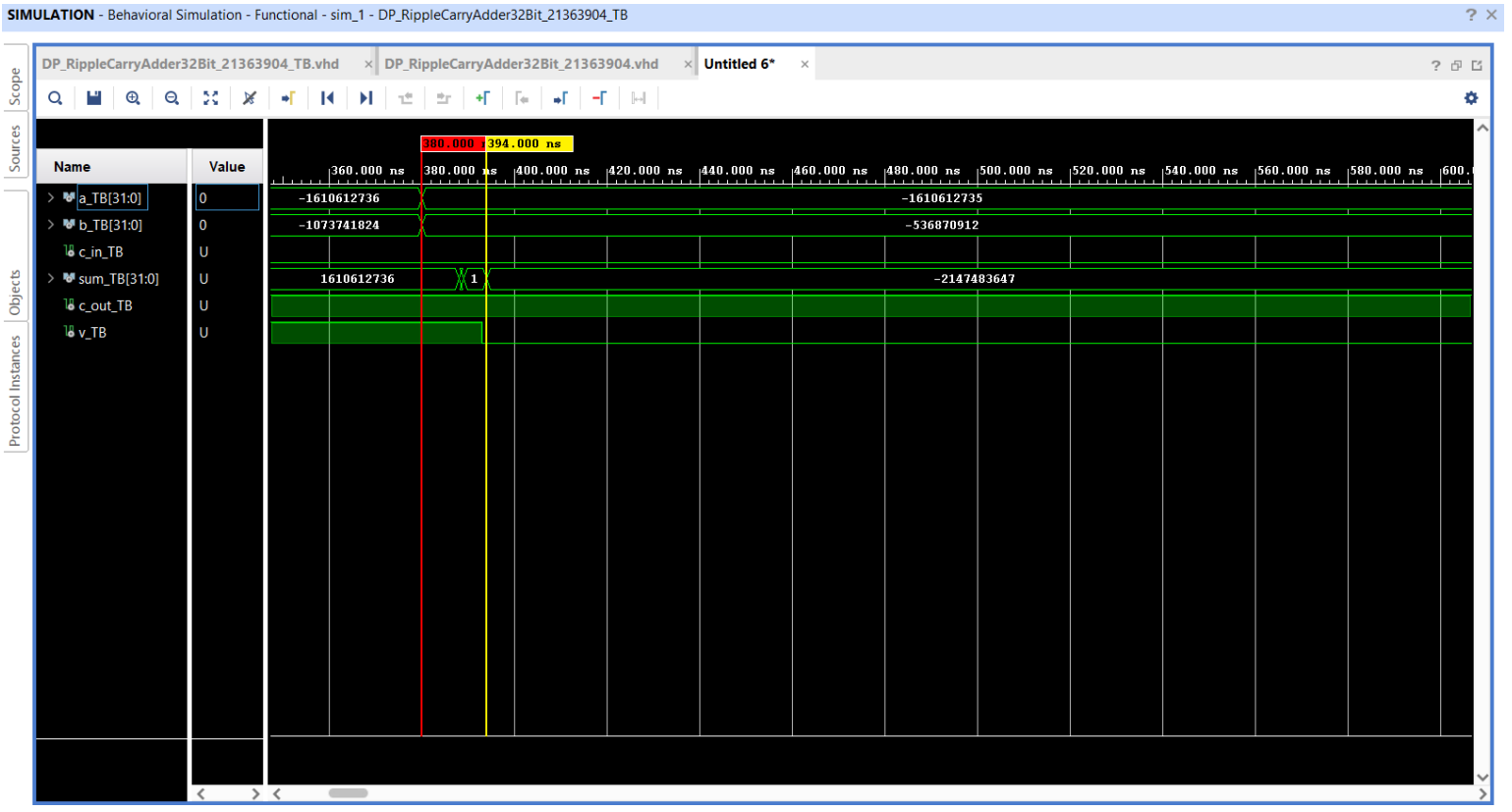

The timing diagram for the Ripple Carry Adder is shown above. On the following pages each of the eight cases are split up so we can see the propogation delay for each. All numbers are in Signed Decimal notatation. In the above waveform, the red lines mark when the inputs change and a new test case is performed. In the images below the yellow lines mark when the correct value appears at $SUM$, after the propogation delay. Case 6 shows the worst case propogation delay (163ns for the correct result at $SUM$, plus another 4ns for the correct $C_{OUT}$ and overflow). Cases 7 and 8 demonstrate adding numbers to my Student ID (21363904) to set the C Flag and V Flag respectively.

# DP_ArithmeticLogicUnit_21363904

## Case 1: Negative plus Negative with Overflow

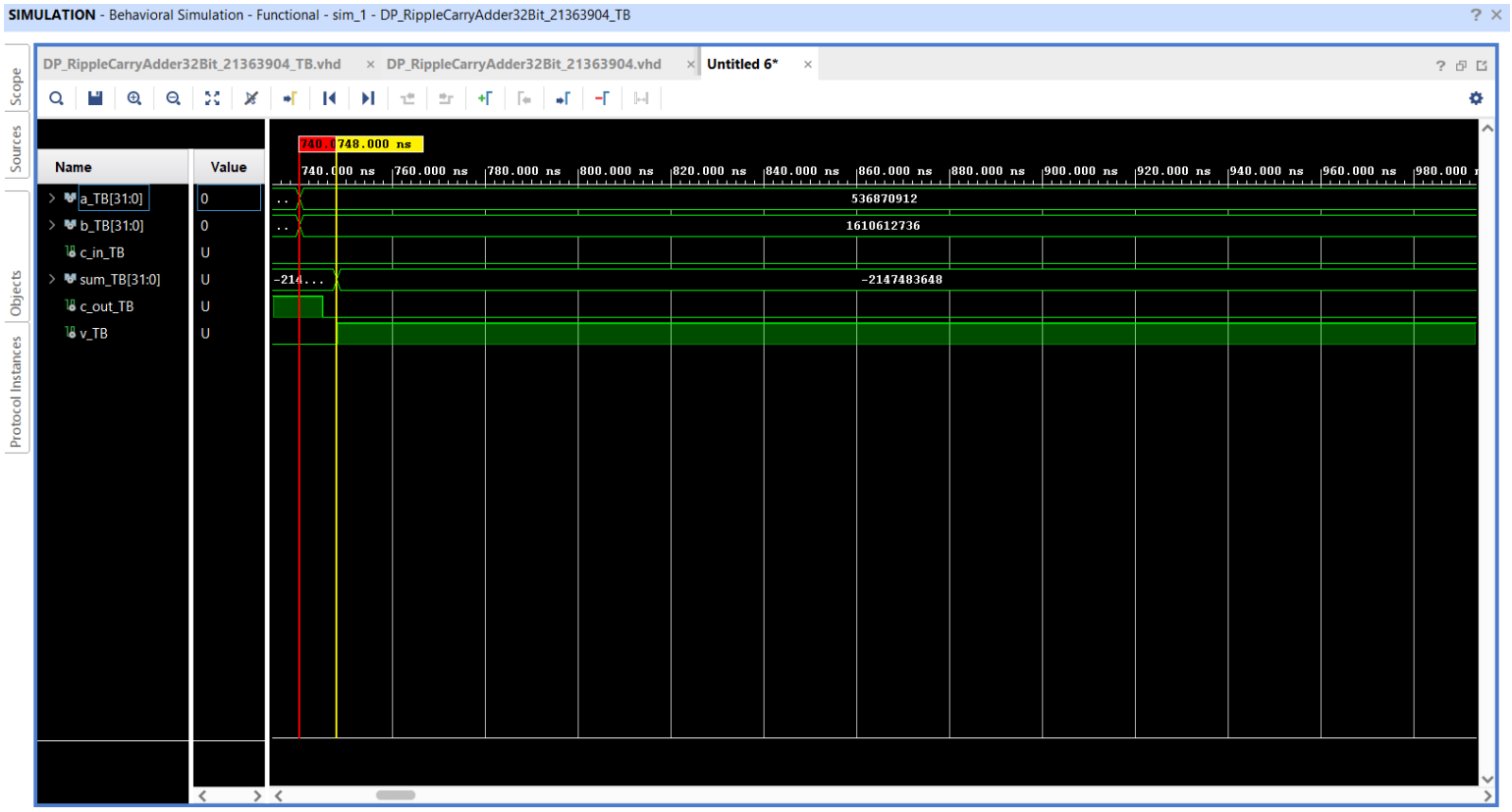



## Case 2: Negative plus Negative without Overflow

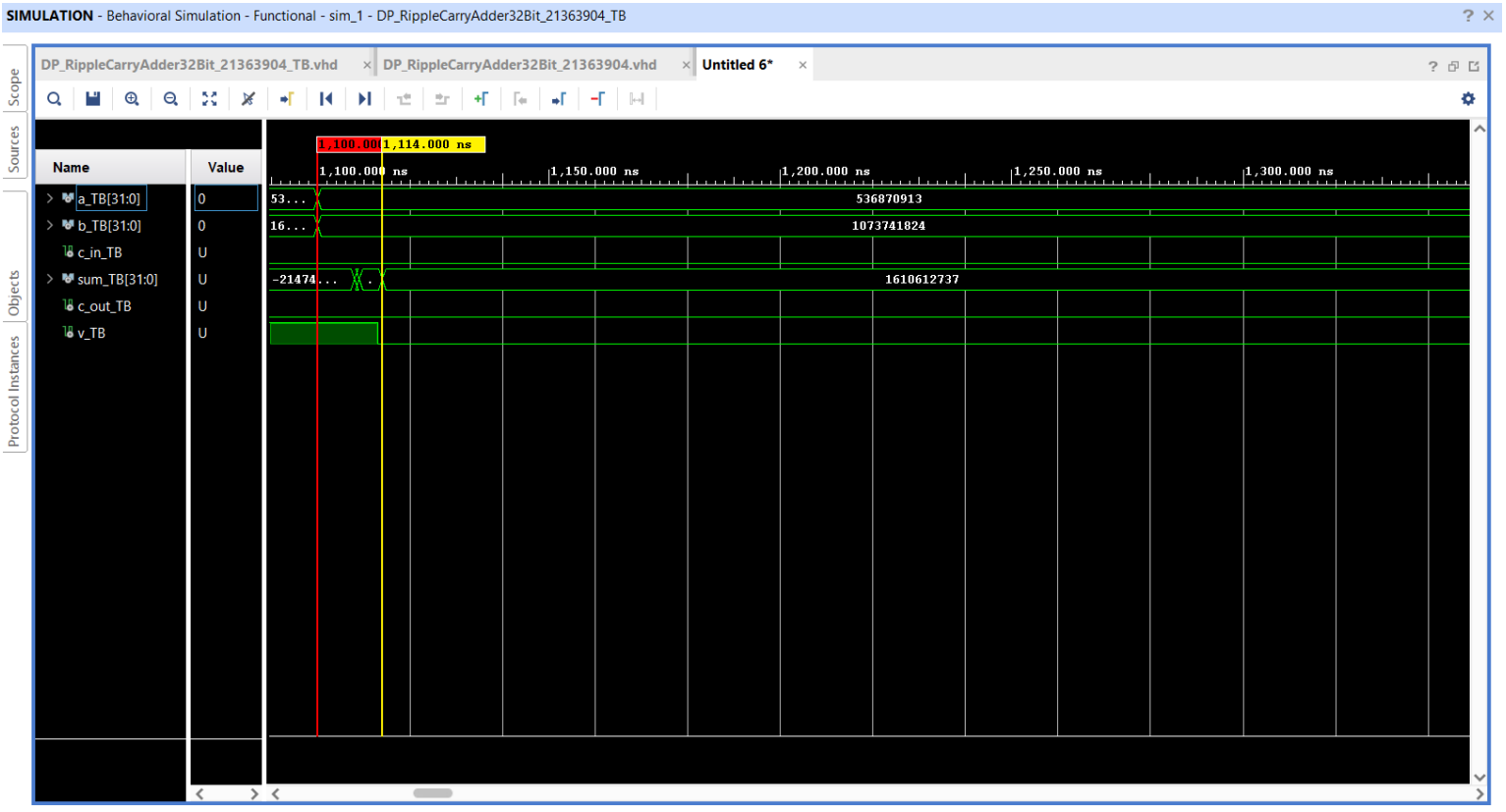


# DP_ArithmeticLogicUnit_21363904

## Case 3: Positive plus Positive with Overflow

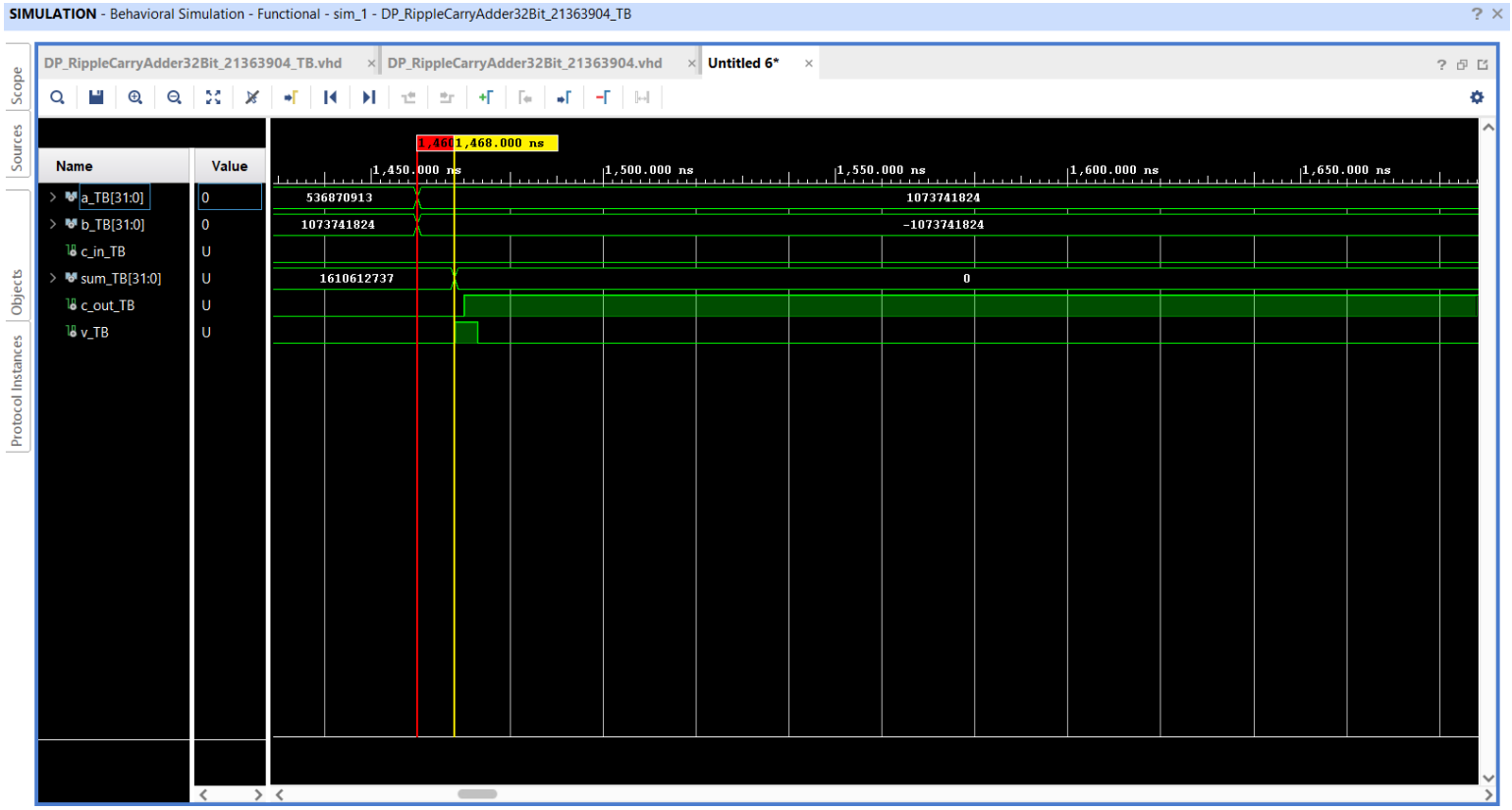



## Case 4: Positive plus Positive without Overflow

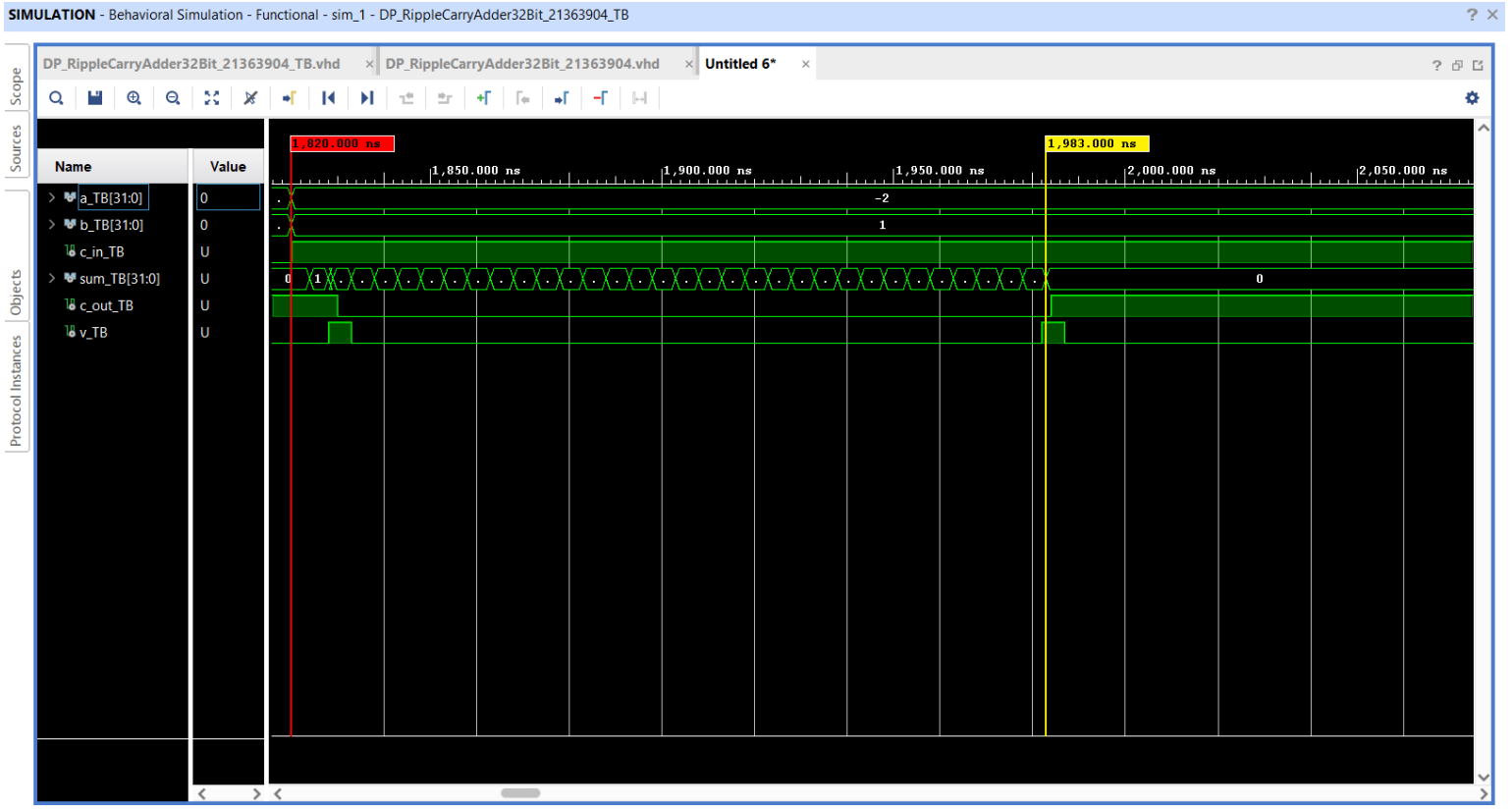


# DP_ArithmeticLogicUnit_21363904

## Case 5: Positive plus Negative without Overflow

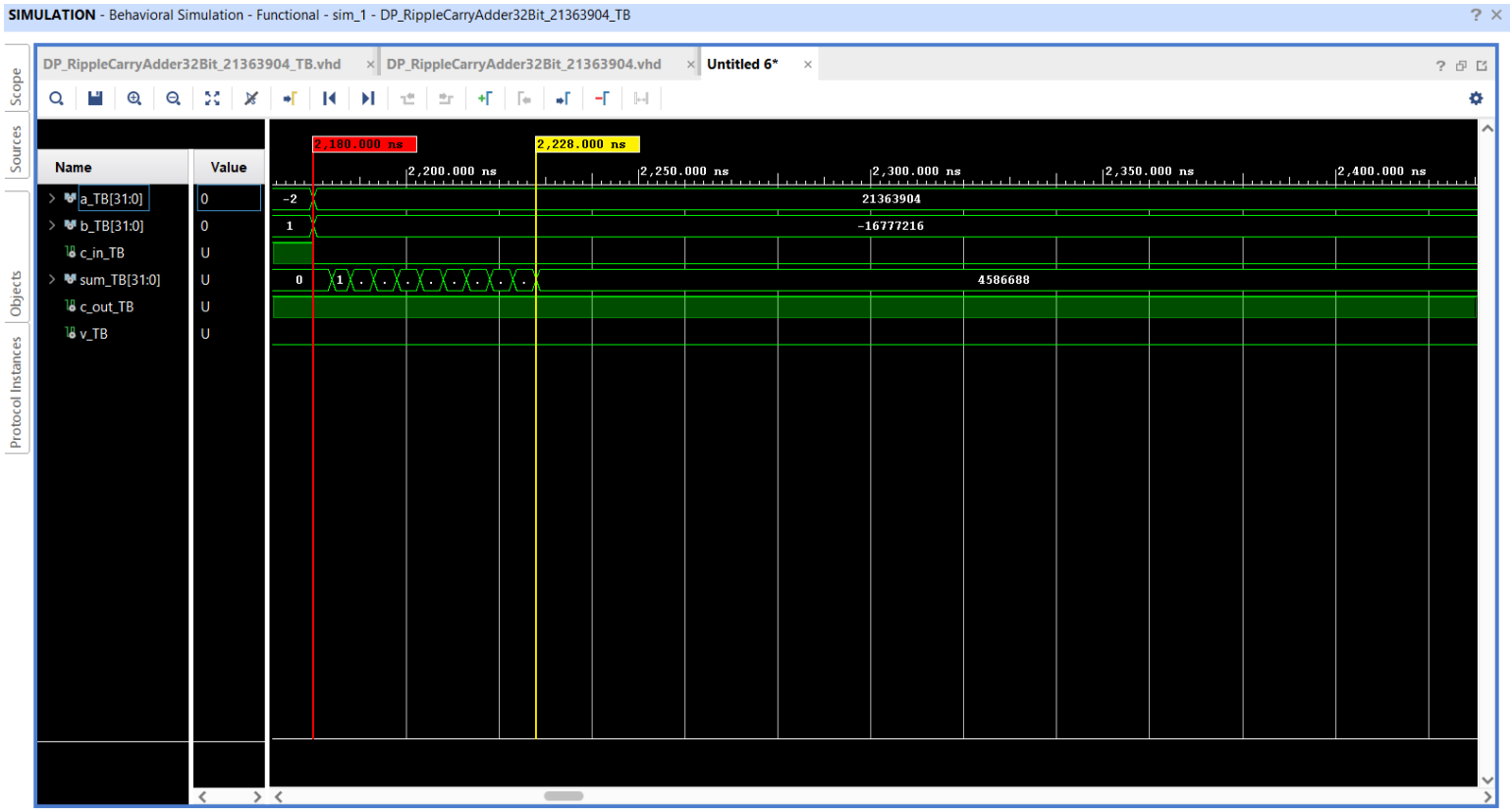



## Case 6: Negative plus Positive (worst-case Propogation Delay)



# DP_ArithmeticLogicUnit_21363904

## Case 7: Student ID – Set Carry Flag




## Case 8: Student ID – Set Overflow Flag