CPU_Processor_Test01_21363904

The timing diagrams for the first Processor Test are shown below. All numbers are in Hexadecimal notation. Inside the RAM design source the memory locations are initialized by default to the last 2 digits of my Student ID (04) incremented for every location. Each clock cycle takes 360ns.

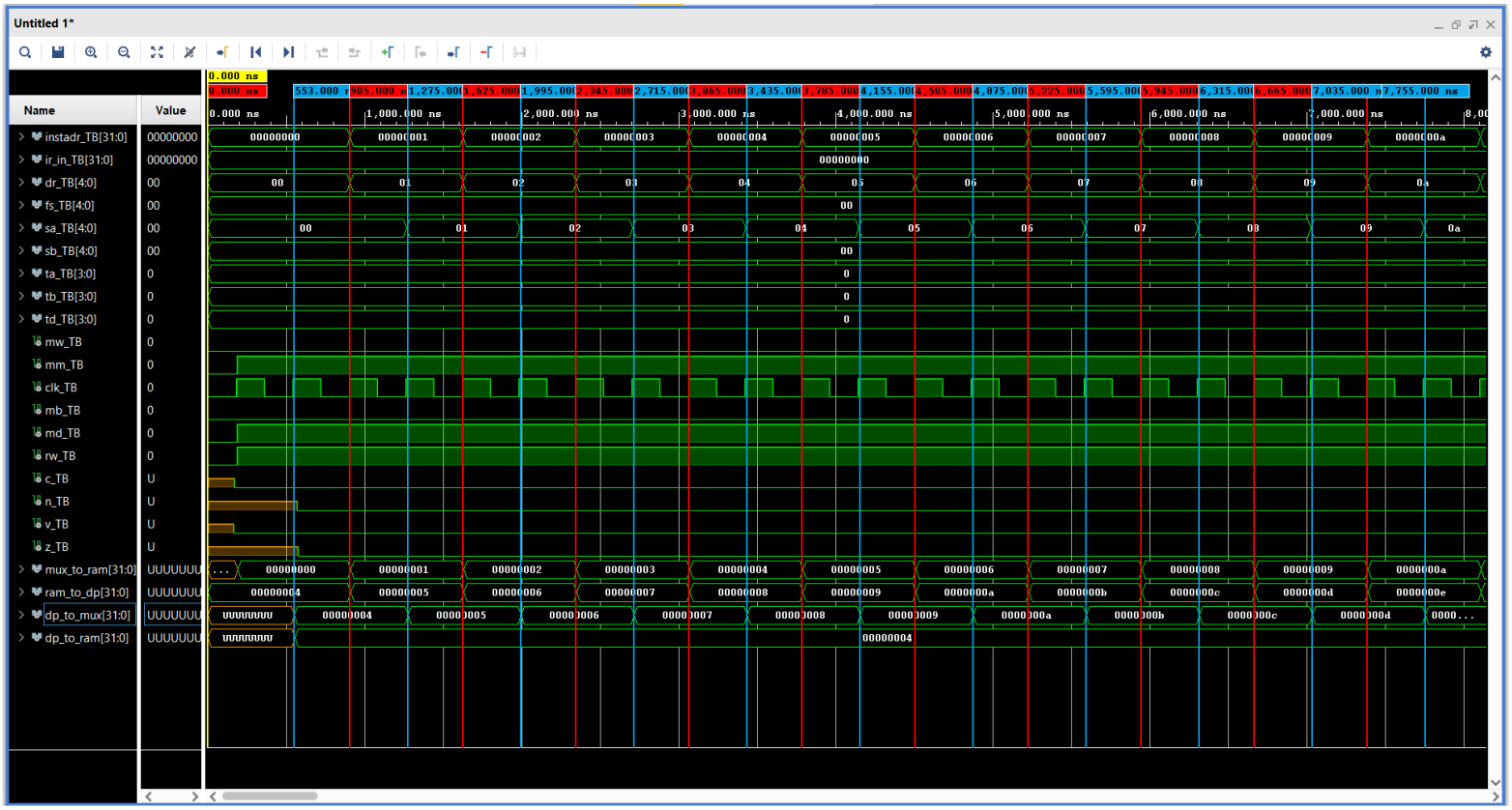
In the first two diagrams the memory addresses in the RAM are being written to the registers in the Register File, starting with the data at address 0x00000000 being loaded into Register 00 and ending with the data at address 0x0000007F being loaded into Temp Register 15. I also read the value of each register at Port A as I load them to verify their contents. The red lines show when the address data is loaded into the RAM 5ns after the rising edge of the clock, and the blue lines show when the correct register data is available at the output of the Datapath.

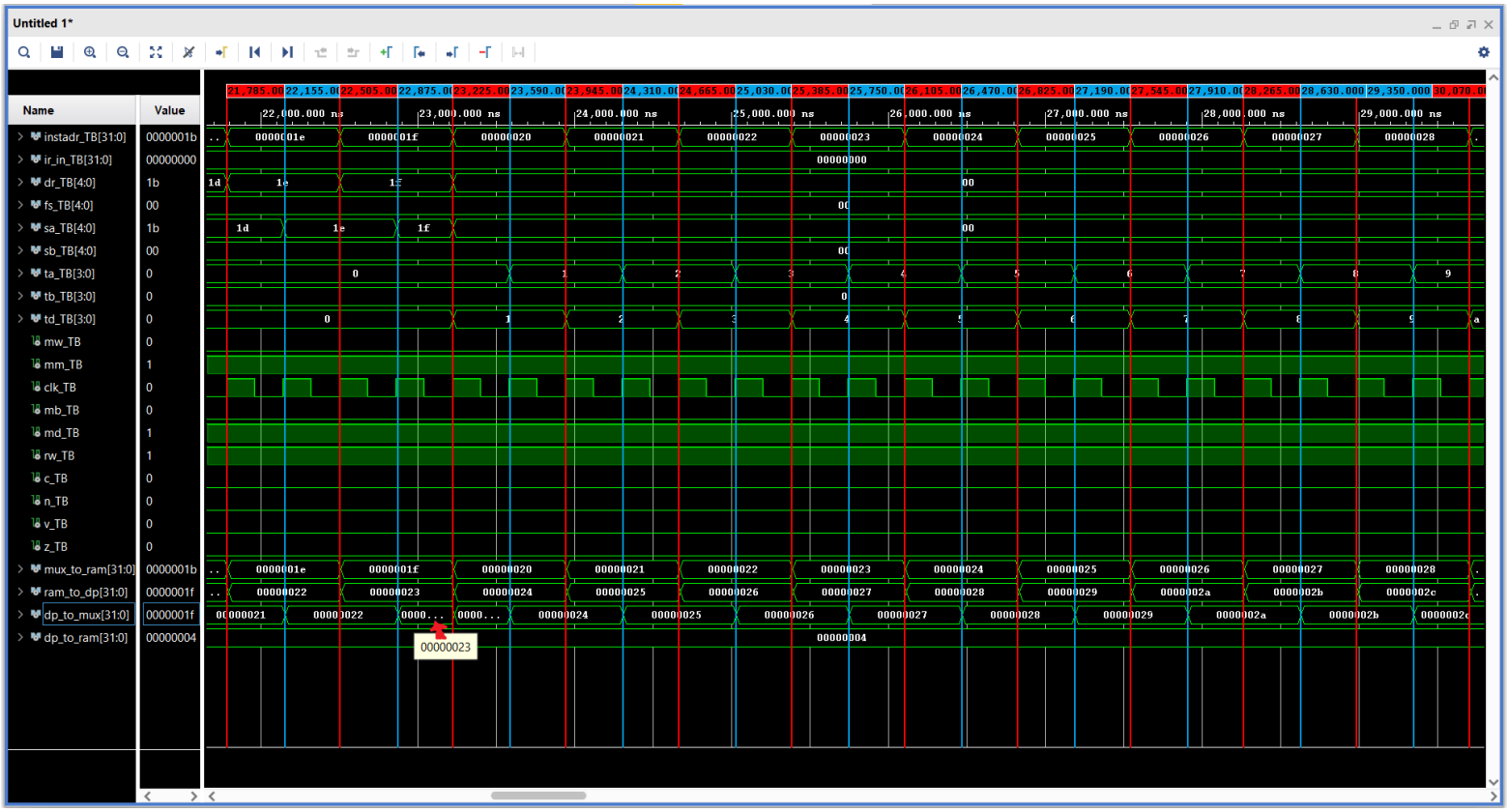
In the third diagram we can see source registers A and B being selected (Registers 4 and 5 respectively, 4 being the last digit of my ID), followed by the fifteen microoperations being performed in the specified order on these registers, with the results of each operation being stored in the fifteen registers starting with Register 6 (last digit of ID + 2). The correct results cannot be seen yet, so the red lines show when the next microoperation instruction is loaded 5ns after the rising clock edge.

In the fourth diagram we can see the correct results of the previous 15 microoperations being loaded from the registers they were stored in appearing at the Datapath output and being written into the RAM, starting with memory address 0x00000000. The last diagram will verify that the contents of the RAM have been written correctly. The red lines here show when each memory address and source register B are selected.

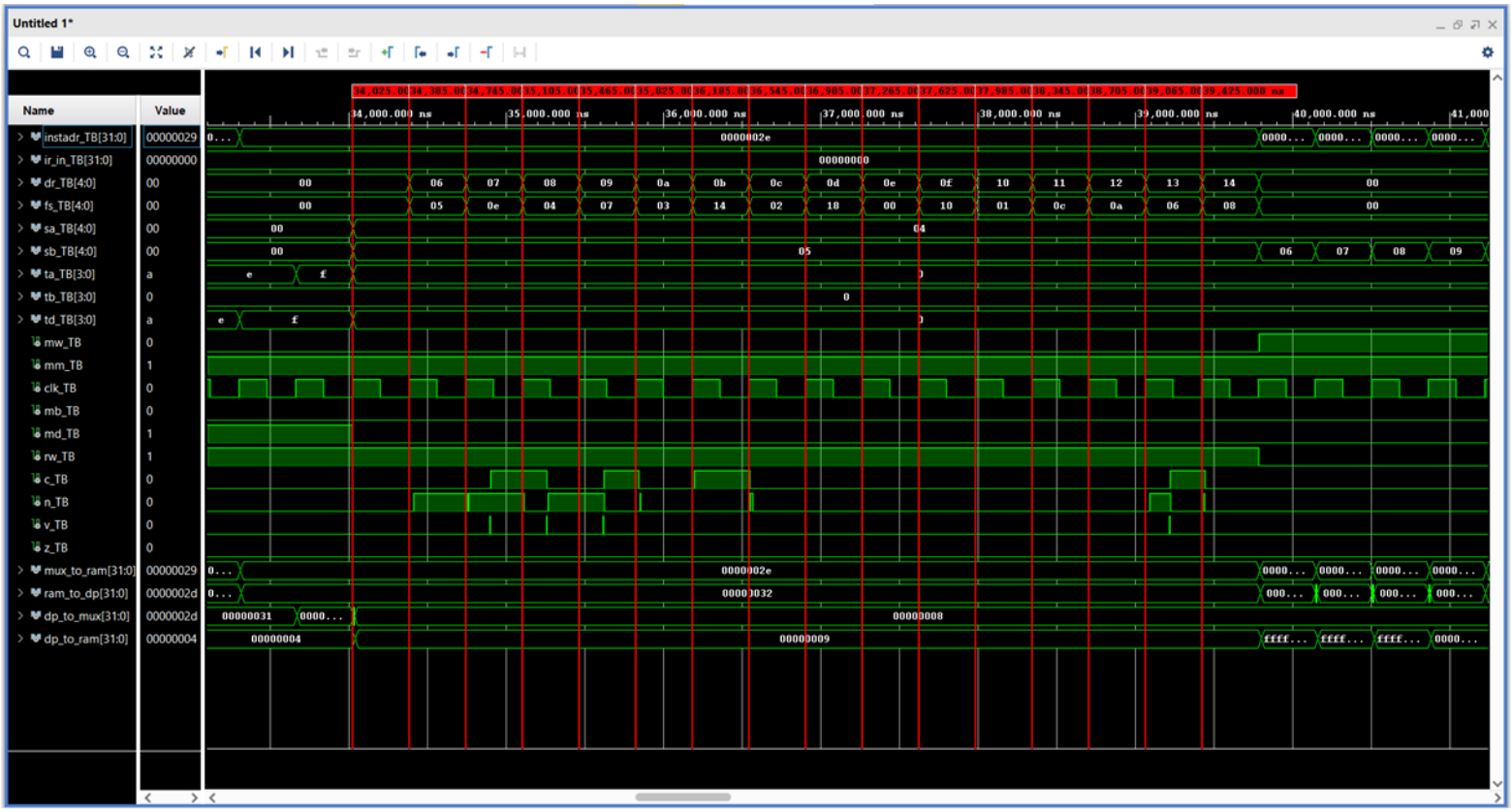
The final diagram shows that the contents of the RAM have indeed been written correctly, as we see them at the output of the RAM. These values are being overwritten into Register 1 sequentially, and I've set up Port A to read from Register 1 so we can verify the contents have been written correctly. The red lines show when the correct data appears at the output of the Datapath exactly one clock cycle after it was input, verifying that everything is as it should be.

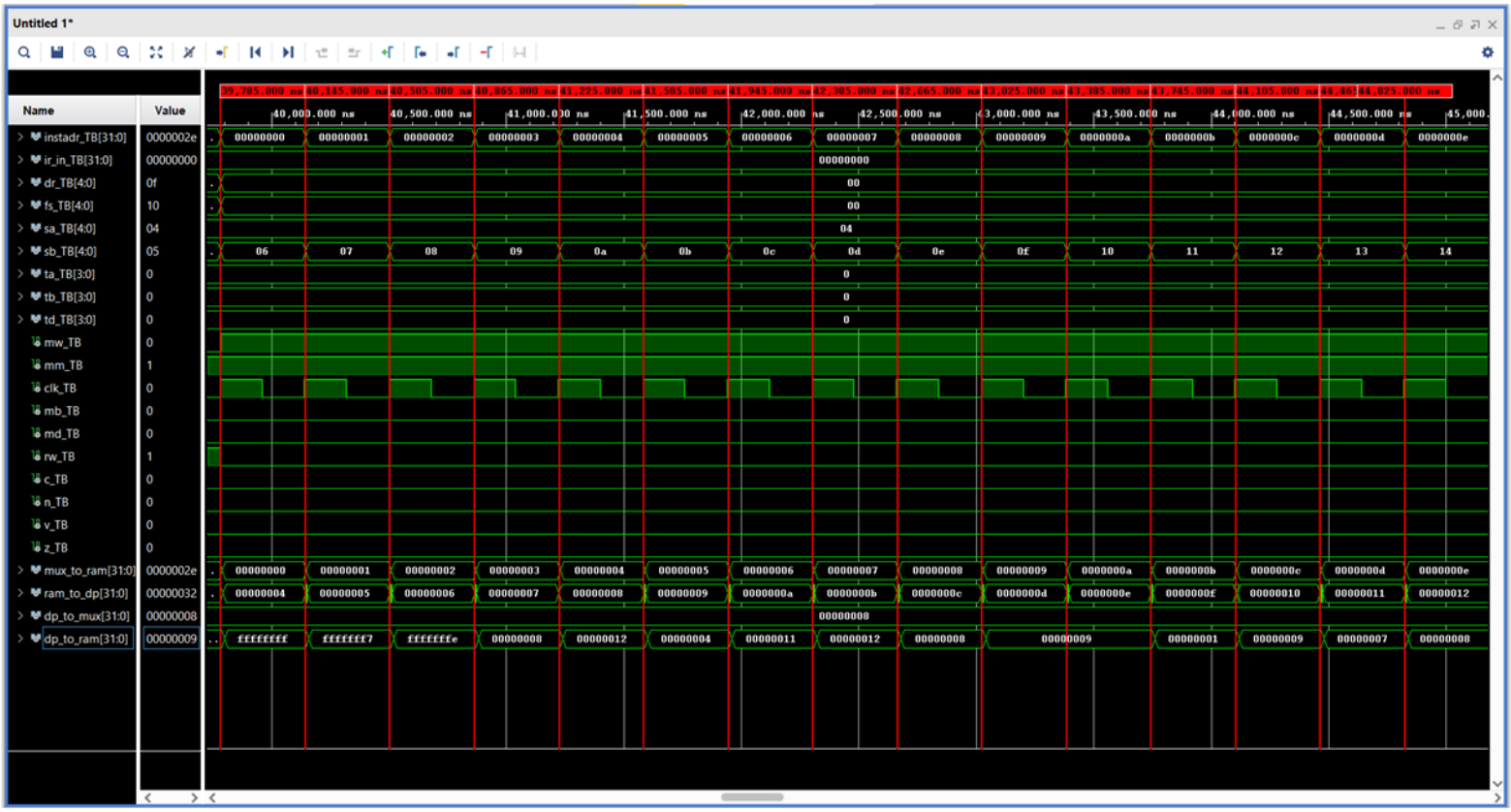
CPU_Processor_Test01_21363904





CPU_Processor_Test01_21363904





CPU_Processor_Test01_21363904