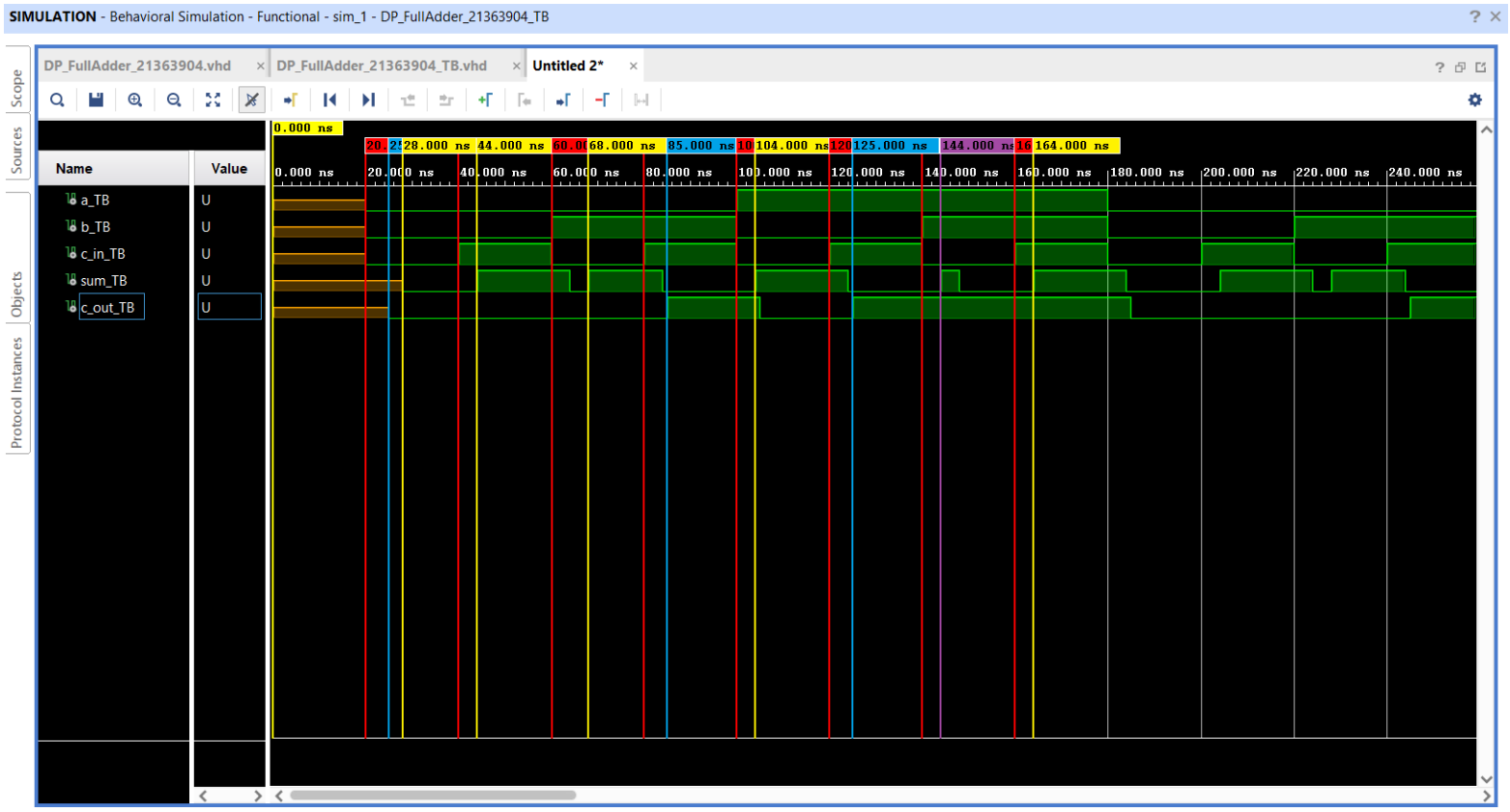
DP_FullAdder_21363904



The timing diagram for the Full Adder is shown above. The red lines mark when the input changes, the yellow lines mark when the correct value appears at the output, and the blue lines mark when the correct value appears at the carry out (the lines only mark when the output in either case is 1). This waveform displays the full truth table for a full adder, shown below. The propogation delay for the adder varies depending on the number of gates passed through. For instance, when only C_{IN} is set, the propogation delay is 4ns, whereas when only B is set, the propogation delay is 8ns. The purple line shows when an incorrect result appears at SUM due to propogation delay.

A	B	C_IN	SUM	C_OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1