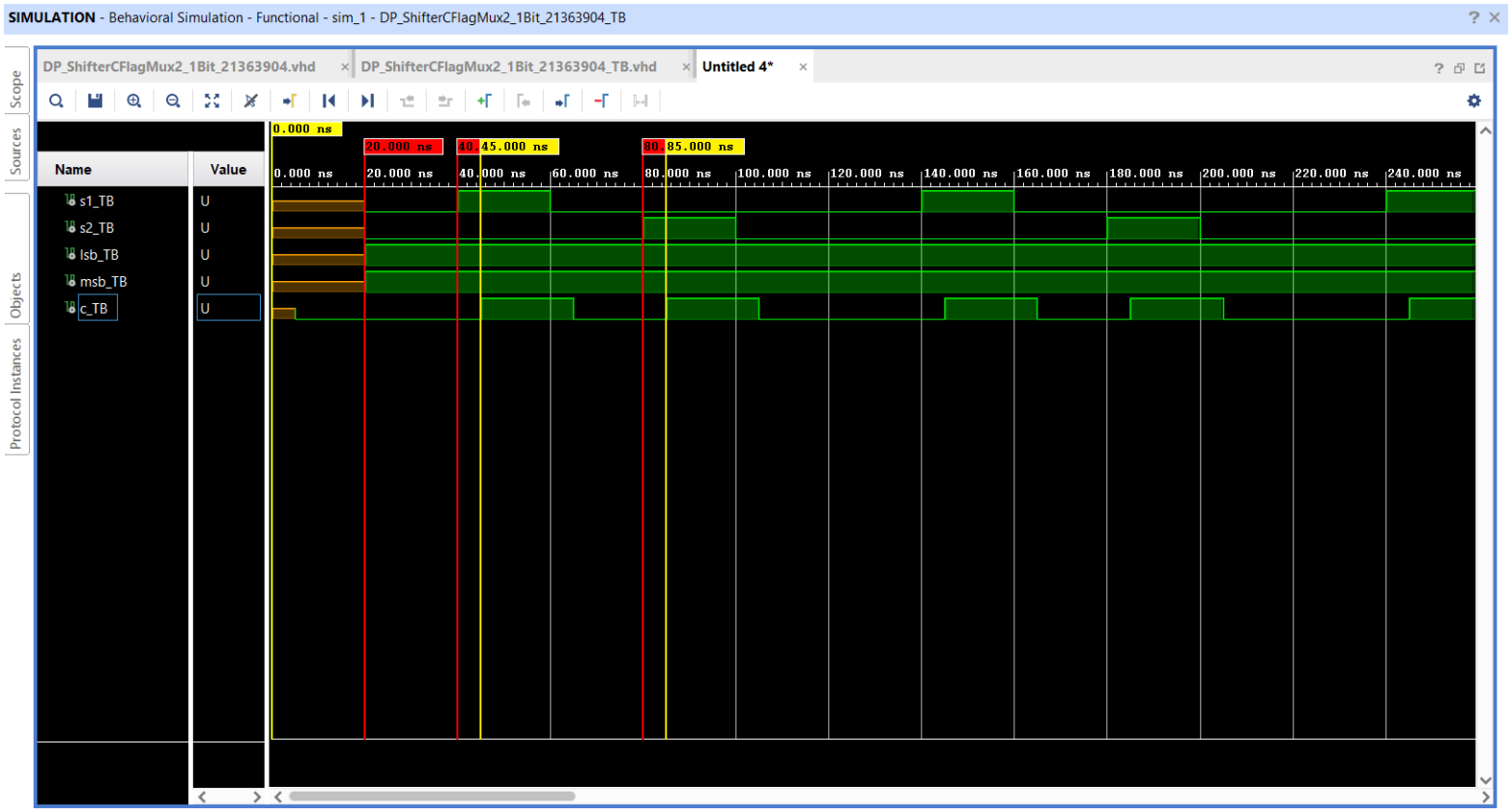
DP_ShifterCFlagMux2_1Bit_21363904



The timing diagram for the Shifter C Flag Multiplexer is shown above. The red lines mark when the select inputs change and the yellow lines mark when the correct value appears at the output, after a propagation delay of 5ns. *LSB* and *MSB* are both set to for the purposes of demonstration. When $s1$ is 1, the value of *LSB* (1) is displayed, and when $s2$ is 1, the value of *MSB* (1) is displayed. In any other case the output is 0.