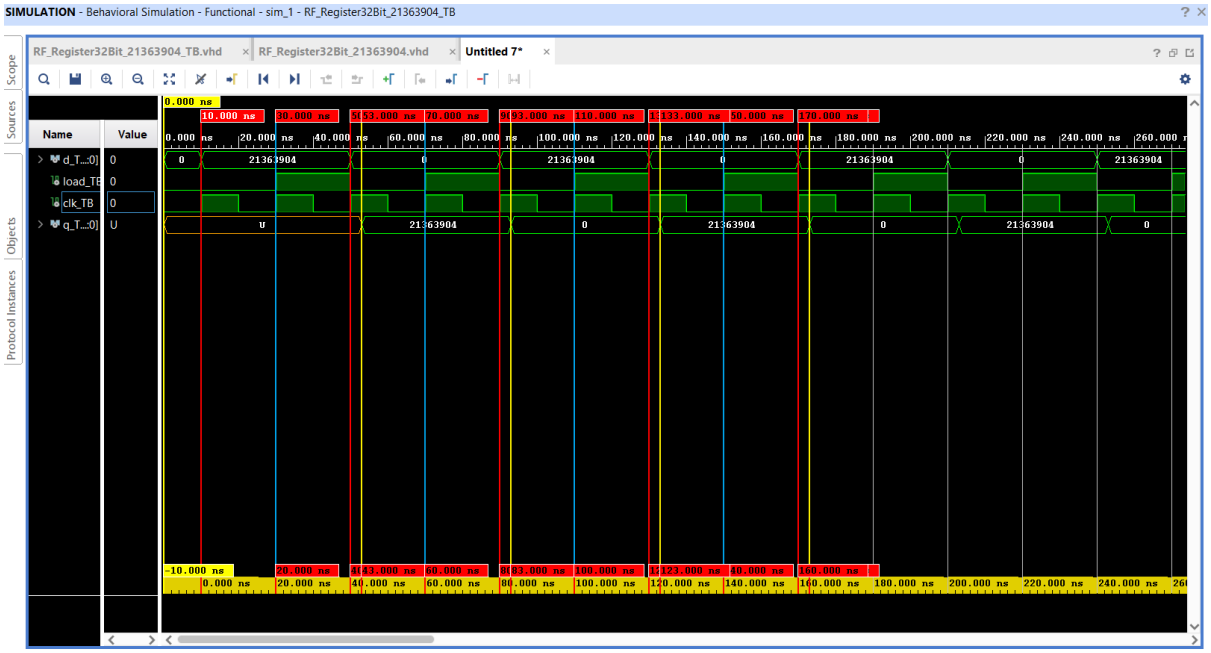
RF_Register32Bit_21363904



The timing diagram for the 32Bit Register is shown above. The red lines mark where the input value changes, the blue lines show when the load signal is enabled, allowing the input value to be written into the register, and the yellow lines show when the value loaded into the register appears at the output. The register is clocked, so the first rising edge is when the input value is set, the second rising edge is when the load signal is enabled, and the third rising edge is when the value is set at the output (due to propagation delay this takes 3ns after the rising edge of the clock).