# Study Questions (Part 8)
# Sunday April 7, 2019

## Covering:

- Performance evaluation

1. Question 6.4 at page 395: A data transmission system transmits data in the form of a master frame containing 16 sub-frames. Each sub-frame includes a 1,024-bit data word and a 12-bit error-correcting code. The master frame itself contains a 32-bit error correcting code. What is the *efficiency* of this system?

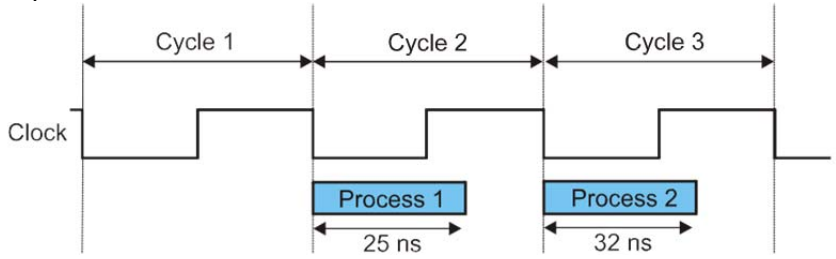
2. Question 6.5 at page 395: The time taken by machines A, B, and C to execute a given task is

   | | |
   |---|---|
   | A | 16m 9s |
   | B | 14m 12s |
   | C | 12m 47s |

   What is the performance of each of these machines relative to machine A?

3. Question 6.6 at page 395: Why is clock rate a poor metric of computer performance? What are the relative strengths and weaknesses of clock speed as a performance metric?

4. Question 6.7 at page 395: The figure below illustrates a system in which operations occur as three consecutive clock cycles. Actions taking place in clock cycle 1 are scalable; that is, if the clock cycle time changes, the actions can be speeded up or slowed down correspondingly. In cycle 2, the action process 1 requires 25 ns and in clock cycle 3 the action process 2 requires 32 ns. If the clock cycle is less than the time required for process 1 or process 2, then one or more wait cycles have to be inserted for the process to complete.




   What is the time to complete an operation if the clock cycle time is
   a. 50 ns
   b. 40 ns
   c. 30 ns
   d. 20 ns
   e. 10 ns

5. Question 6.8 at page 395: What are the relative strengths and weaknesses of the MIPS as a metric of computer performance?

6. Question 6.10 at page 395: How is it possible for one computer with a low MIPS rating to have a better performance in practice than a computer with a high MIPS rating?

7. Question 6.11 at page 395: Overclocking a computer means operating it at a higher clock rate than that specified by its manufacturer; for example, a 2 GHz chip might be clocked at 2.1 GHz to squeeze more performance out of it. Does overclocking disprove the famous aphorism, "There's no such thing as a free lunch", or is there a hidden cost? If so, what is the *cost* of overclocking?

8. Question 6.12 at page 395: The following figures define the typical operating parameters of a processor.

| **Operation** | **Frequency** | **Cycles** |
|---|---|---|
| Arithmetic/logical instructions | 45% | 1 |
| Register load operations | 20% | 3 |
| Register store operations | 10% | 2 |
| All branch instructions | 25% | 2 |

If the clock rate could be reduced by 15%, it would require only 2 cycles to perform a register load. Would that be a good idea?

9. Question 6.13 at page 395: A computer has the following parameters.

| **Operation** | **Frequency** | **Cycles** |
|---|---|---|
| Arithmetic/logical instructions | 65% | 1 |
| Register load operations | 10% | 5 |
| Register store operations | 5% | 2 |
| Conditional branch instructions | 20% | 8 |

If the average performance of the computer (in terms of its CPI) is to be improved by 20%, i.e., its CPI to be only 80% of the current CPI, while executing the same instruction mix, what target must be achieved for the cycles per conditional branch instruction?

10. Question 6.14 at page 396: A program is run on a computer with the following parameters

| | |
|---|---|
| clock cycle time | 10 ns |
| instructions with 1 cycle | 70% |
| instructions with 2 cycles | 20% |
| instructions with 3 cycles | 10% |

What is the MIPS rating of this computer?

11. Question 6.15 at page 396: For the following data, what is the average number of cycles per instruction?

| **Operation** | **Frequency** | **Cycles** |
|---|---|---|
| Arithmetic/logical instructions | 45% | 1 |
| Register load operations | 18% | 5 |
| Register store operations | 10% | 2 |
| Unconditional branch instructions | 7% | 1 |
| Conditional branch instructions | 20% | 6 |

12. Question 6.16 at page 396: In a particular system, a CPU is used for 78% of the time and a disk drive for 22% of the time. A designer has two options:
    a. improve the disc performance by 40% and the CPU performance by 20%
    or
    b. improve the disc performance by 10% and the CPU performance by 80%
    Which is the better option, and why?

13. Question 6.19 at page 396: A computer employed in arithmetic processing uses a software division routine. A program runs for two minutes on this machine, with division taking 60% of the total time. If we wish to add a dedicated division unit in order to increase the performance of the computer by a factor of two, how much faster do we have to make the hardware division unit than the existing division mechanism?

14. Question 6.21 at page 396: A program is executed in 200 ms, during which 250 million instructions are executed. What is the average MIPS rating for this program?

15. Question 6.27 at page 397: You are redesigning a system. You can replace the existing single processor by two P processors or by four Q processors. However, the P processors are able to run 80% of the code in parallel, whereas the Q processors are able to run 50% of the code in parallel. Which is the better option?

16. Question 6.33 at page 397: Two computers and a reference machine produce the following results.

| **Machine** | **Benchmark 1** | **Benchmark 2** | **Benchmark 3** |
|---|---|---|---|
| Reference | 150 s | 65 s | 95 s |
| A | 120 s | 40 s | 65 s |
| B | 70 s | 35 s | 80 s |

Present the results in a normalized form and provide benchmarks for machines A and B.

17. A computer executes 2.5 x $10^{10}$ instructions in 12 seconds. All instructions except loads take 1 cycle, and register loads take 4 cycles. The clock rate is 3,000 MHz. What fraction of the instruction workload consists of register loads?

18. Consider the following loop:

```
int sum = 0, int x[64]

for (j = 0; j < max, j++
{   sum+= x[j] * max;
}
```

This can be encoded in an ARM- language as:

```
     ADR   r0,x       ; r0 points to array X
     MOV   r1,#max    ; r1 contains max
     MOV   r2,#0      ; r2 is loop variable j initialized to 0
     MOV   r3,#0      ; r3 is sum  initialized to 0
Next LDR   r4,[r0]    ; get x[j]
     MUL   r5,r4,r1   ; calculate r4 * max
     ADD   r3,r3,r5   ; add new element to running total
     ADD   r0,r0,#4   ; point to next element in X
     ADD   r2,r2,#1   ; increment loop variable j
     CMP   r2,r1      ; test for end of loop
     BLT   Next       ; repeat until all done
```

Note that the integers of array X are expressed as 32-bit values.

These instructions have the following characteristics

```
   ADR                    2 CPI
   LDR                    4 CPI
   MOV, ADD,CMP, BLT      1 CPI
   MUL, B                 8 CPI
```

a. What is the average CPI for this code if the value of max is 1?
b. How many instructions does this code execute in total if the value of max is 50?
c. What is the average CPI for this code if the value of max is 50?
d. If the clock frequency is 1 GHz, what is the execution time if the value of max is 50?

19. Consider three different processors P1, P2, and P3 executing the same instruction set.
    P1 has a 3.0 GHz clock rate and a CPI of 1.5.
    P2 has a 2.5 GHz clock rate and a CPI of 1.0.
    P3 has a 4.0 GHz clock rate and a CPI of 2.2.
    a. Which processor has the highest performance expressed in MIPS?
    b. If the processors each execute a program in 10 seconds. Find the number of cycles required.
    c. If the processors each execute a program in 10 seconds. Find the number of executed instructions.

20. Consider two different implementations of the same instruction set architectures. The instructions can be divided into four classes according to their CPI (class A, B, C, and D).
    P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3.
    P2 with a clock rate of 3.0 GHz and CPIs of 2, 2, 2, and 2.
    Given a program with 1 million instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D.
    a. Which implementation is faster?
    b. What is the global CPI for each implementation?
    c. Find the clock cycles required in both cases?