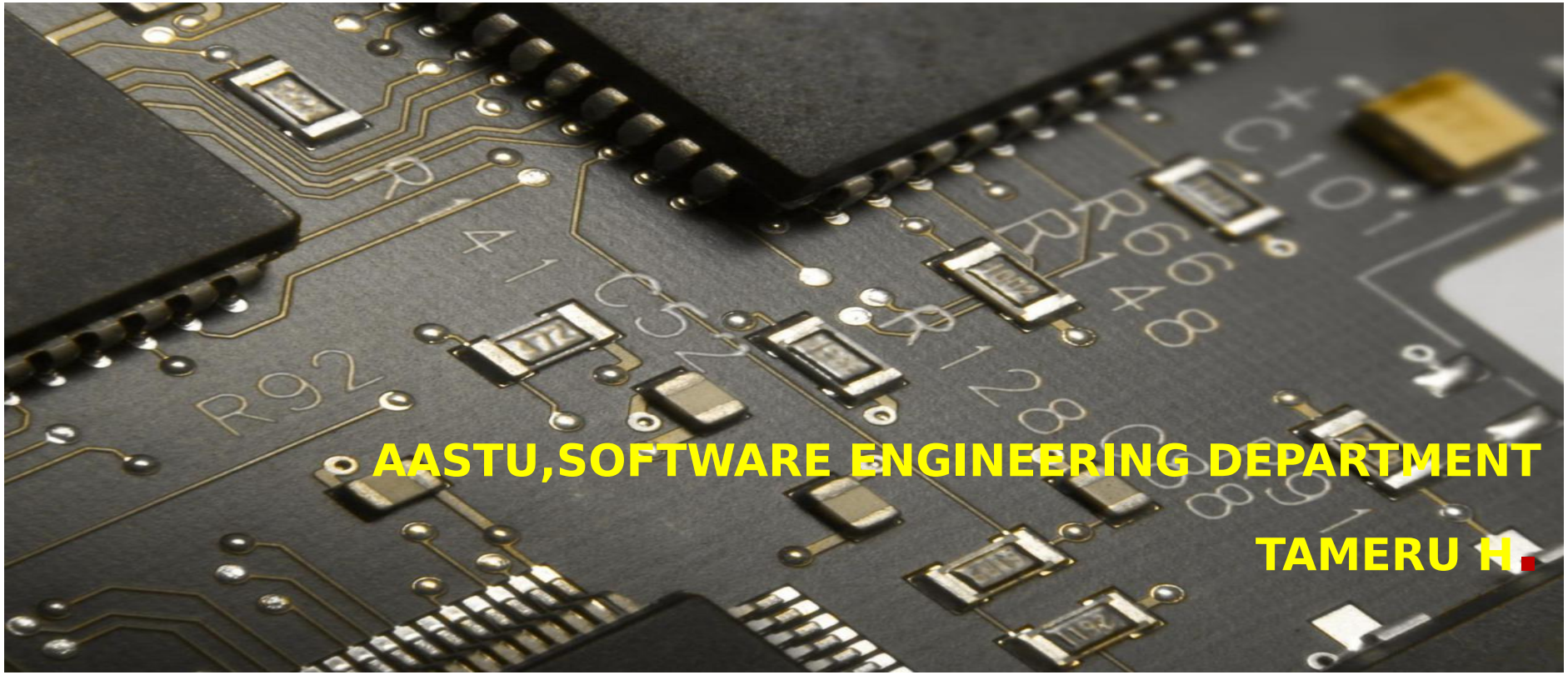
Chapter 5

Internal Memory

Part One



AASTU,SOFTWARE ENGINEERING DEPARTMENT

TAMERU H.

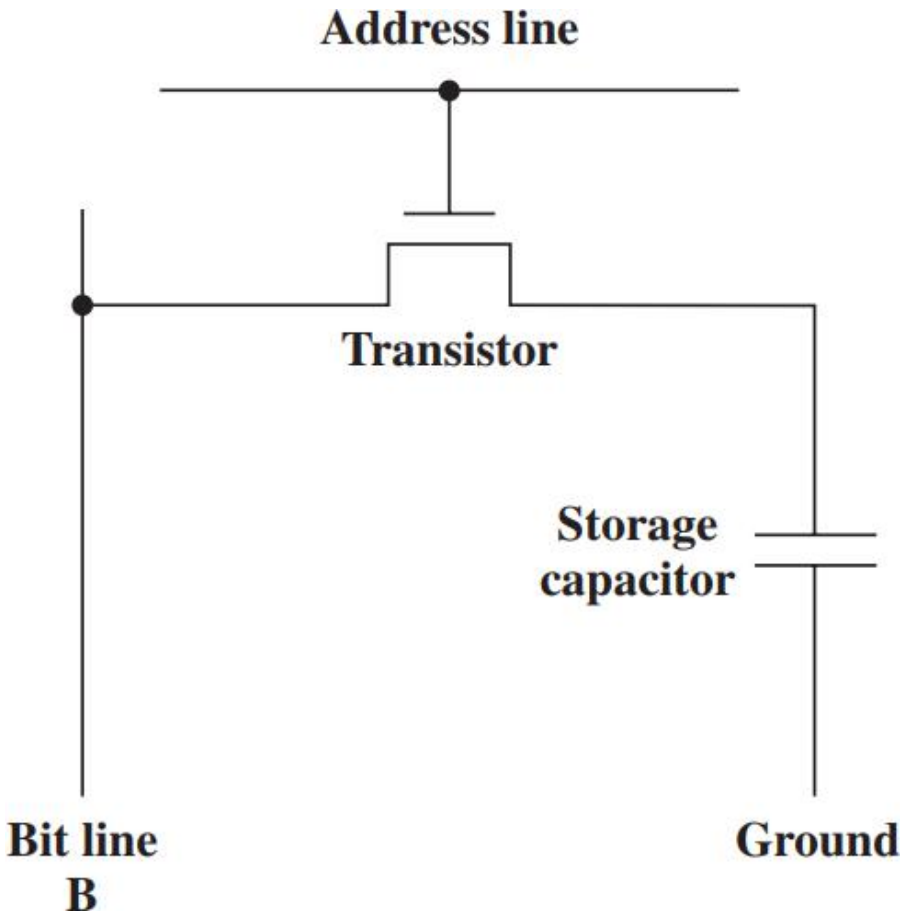
Semiconductor Memory

- RAM (Random Access Memory)
  - Misnamed as all semiconductor mem. are random access
  - Read/Write
  - Volatile
  - Temporary storage
  - Static or dynamic
- ROM (Read only memory)
  - Permanent storage
  - Read only

Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory (static RAM would be too expensive)

Dynamic RAM


Address line
Transistor
Storage
capacitor
Bit line
B
Ground

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache (here the faster the better)

Read Only Memory (ROM)

- Permanent storage
- Microprogramming (see later)
- Library subroutines
- Systems programs (BIOS)
- Function tables

Types of ROM

- Written during manufacture
  - Very expensive for small runs
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Read "mostly"
  - Erasable Programmable (EPROM)
    - Erased by UV (it can take up to 20 minuts)
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read
    - a single byte can be erased
  - Flash memory
    - Erase memory electrically "block-at-a-time"

Physical Characteristics

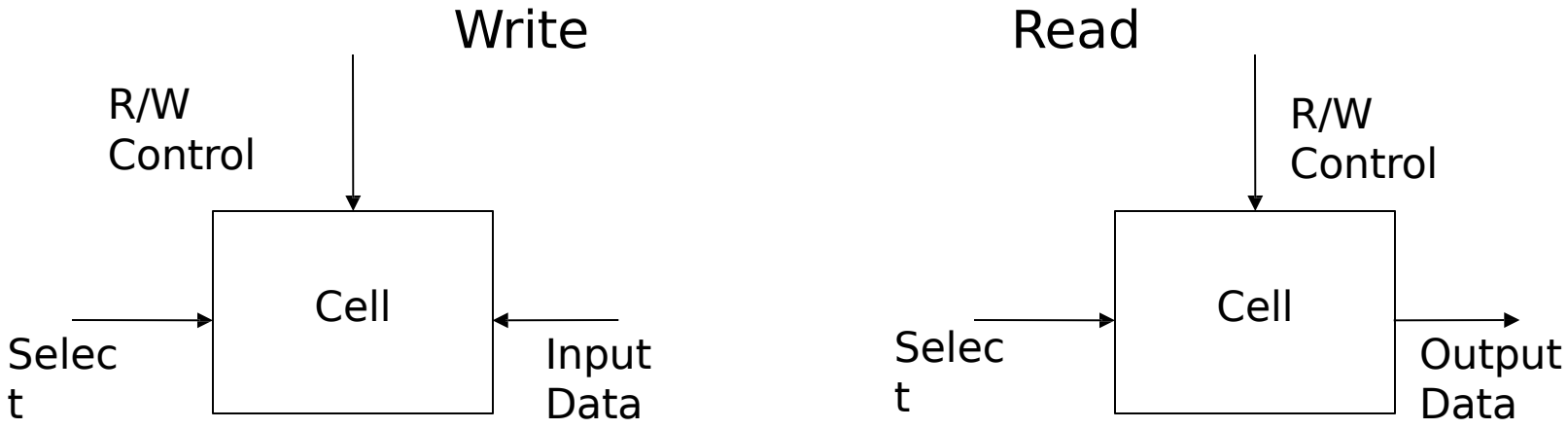
- Decay (refresh time)
- Volatility (needs power source)
- Erasable
- Power consumption

Organisation

- Physical arrangement of bits into words
- Not always obvious
  - e.g. interleaved

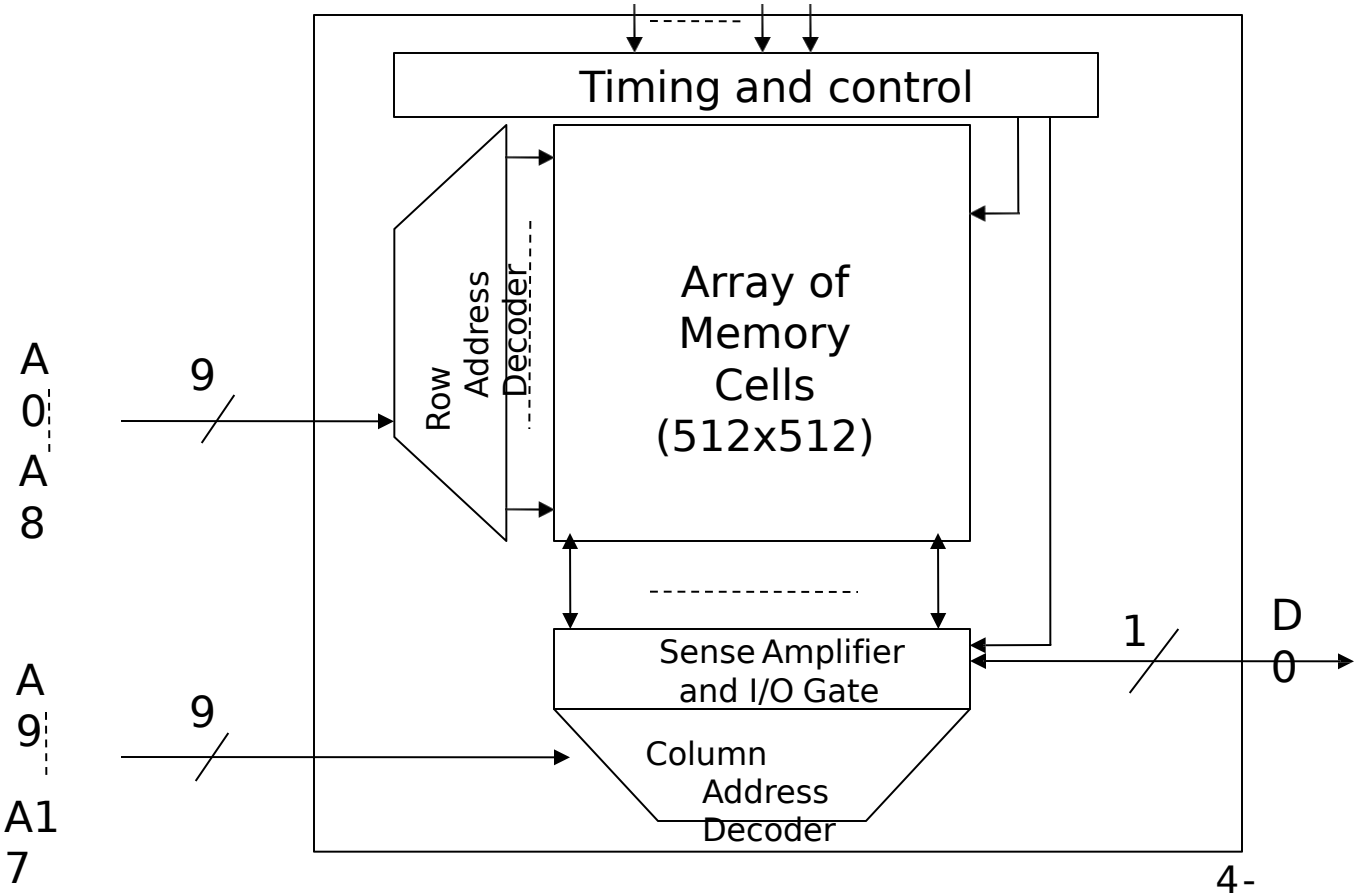
Basic Organization (1)

- Basic element: memory cell
  - has 2 stable states: one represent 0, the other 1
  - can be written at least once
  - can be read



Basic Organization (2)

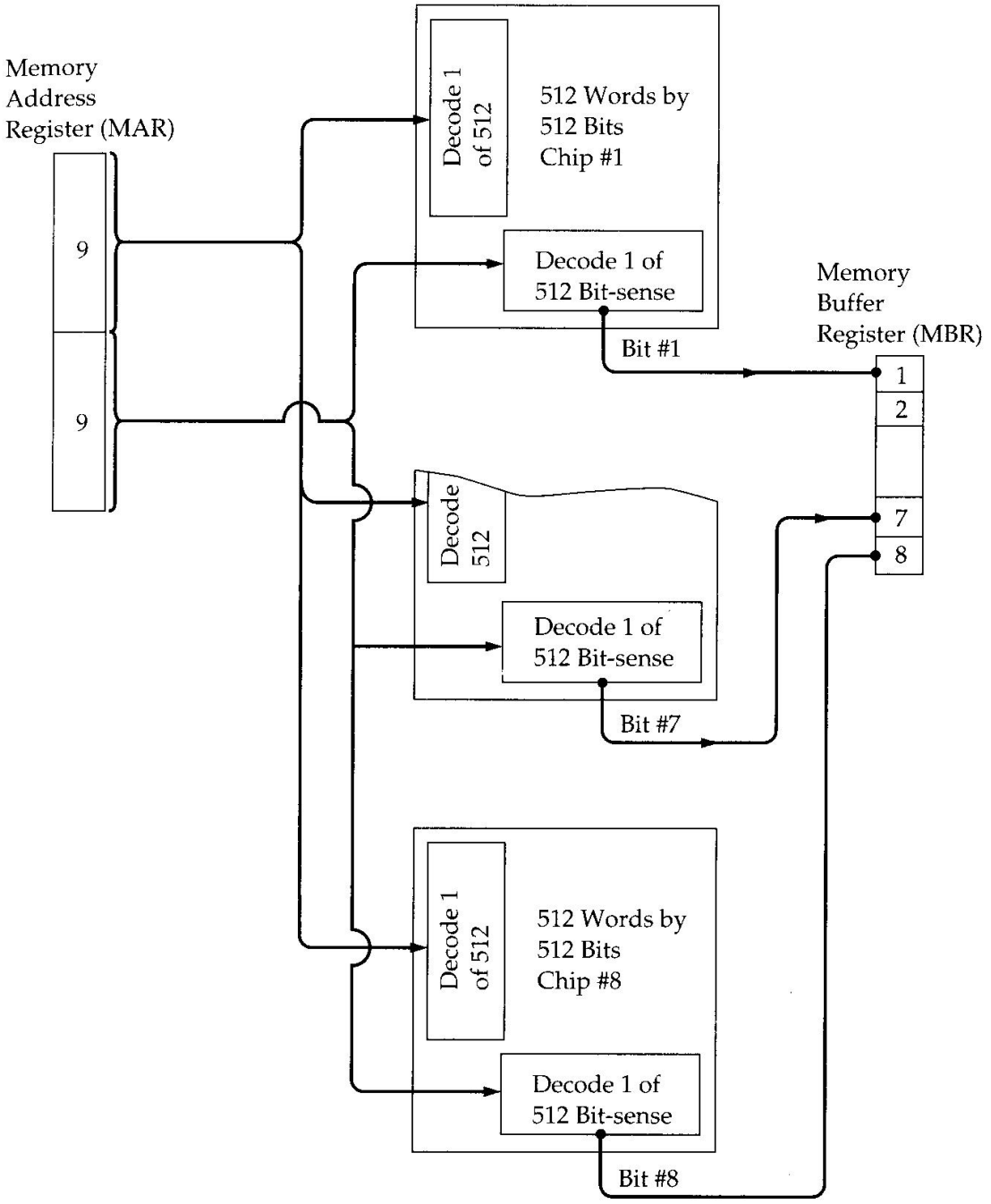
- Basic organization of a 512x512 bits chip



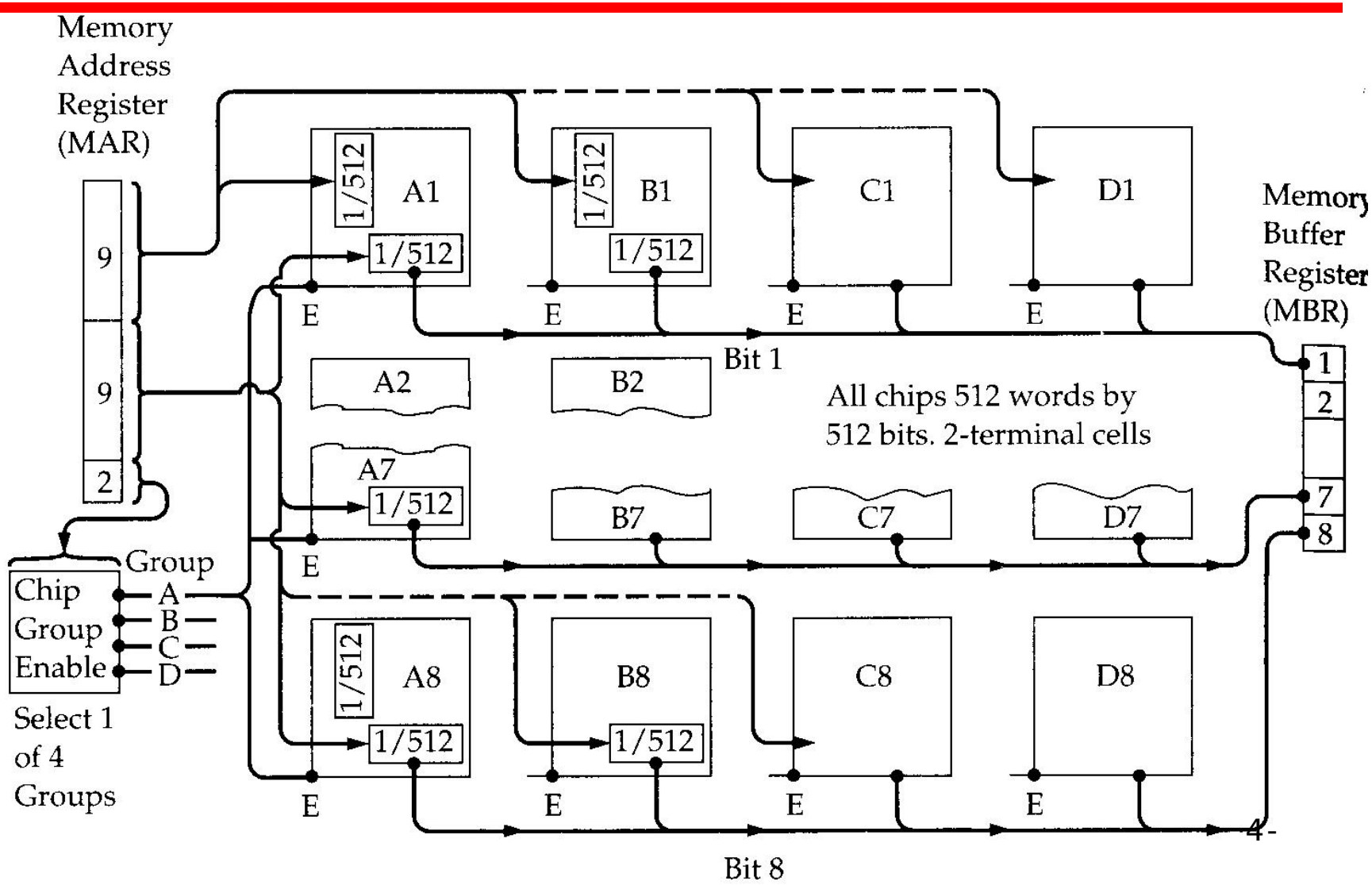
Module Organisation

- Basic organization of a 256KB chip
- 8 times a 512x512 bits chip

- ...For a 1 MB chip replicate 4 times this organization...



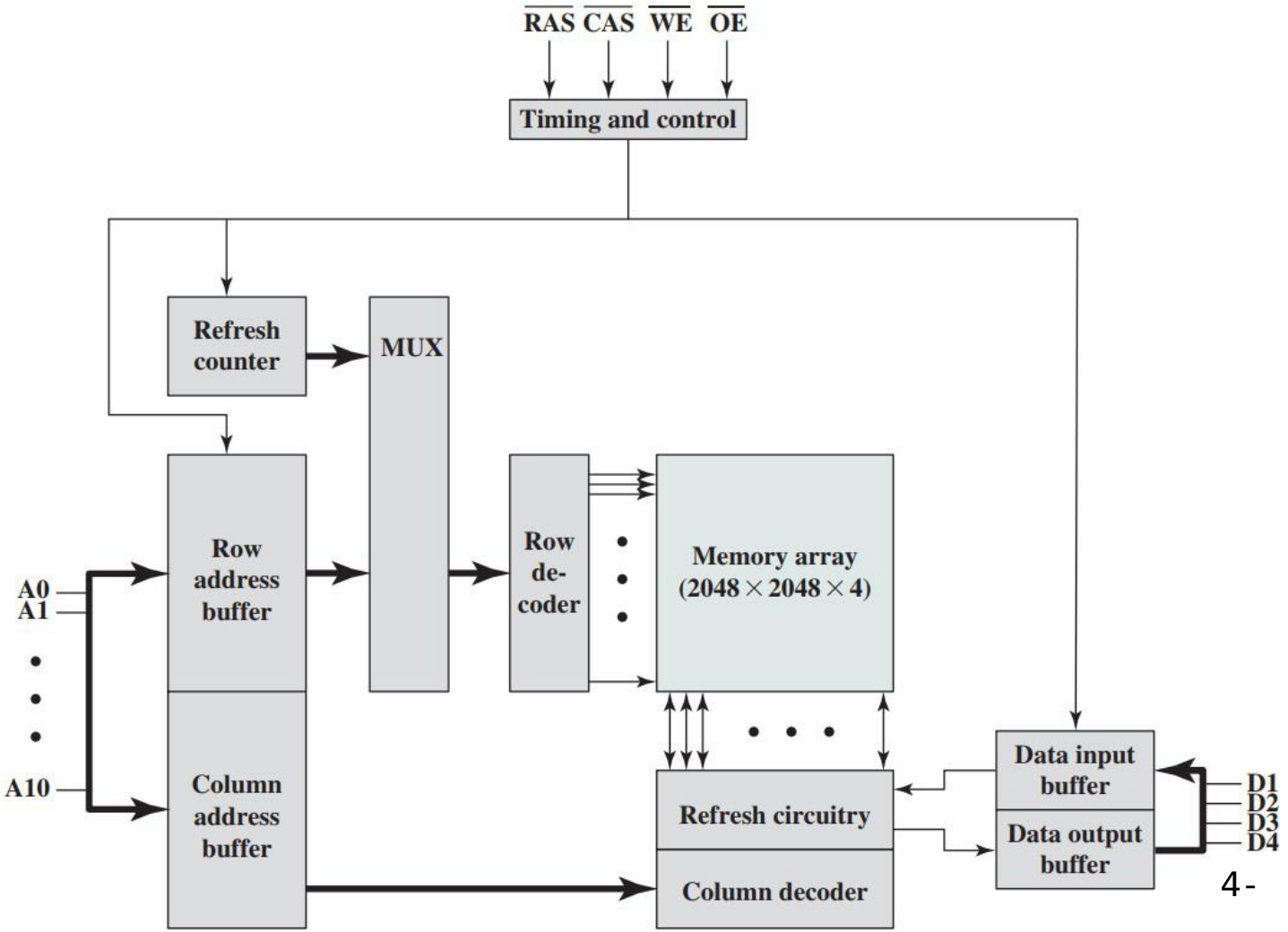
Module Organisation (1 MByte)



Organisation for larger sizes

- The larger the size the higher the number of address pins
- For 2^k words, k pins are needed
- A solution to reduce the number of address pins
  - Multiplex row address and column address
  - k/2 pins to address 2^k Bytes
  - Adding one more pin doubles range of values so x4 capacity

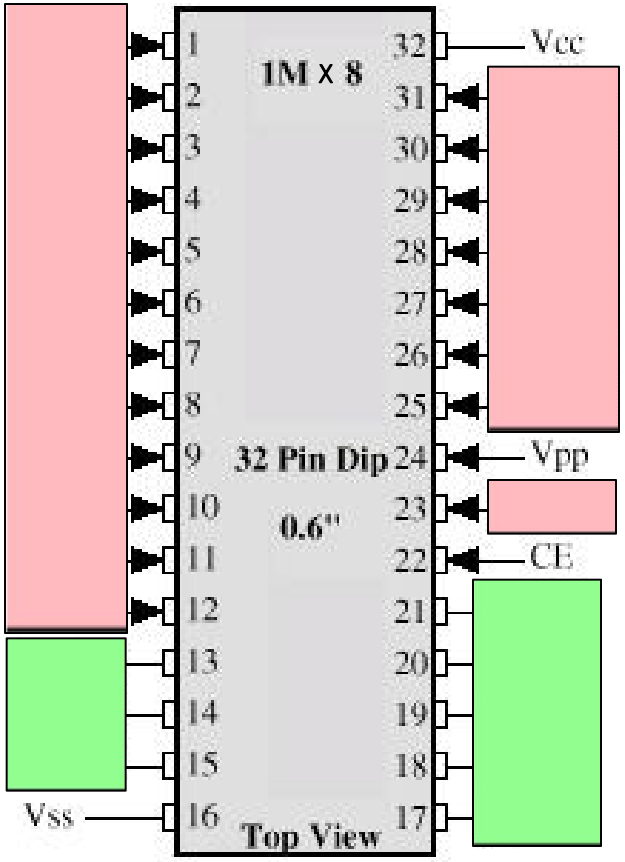
Typical 16 Mb DRAM (4M x 4)



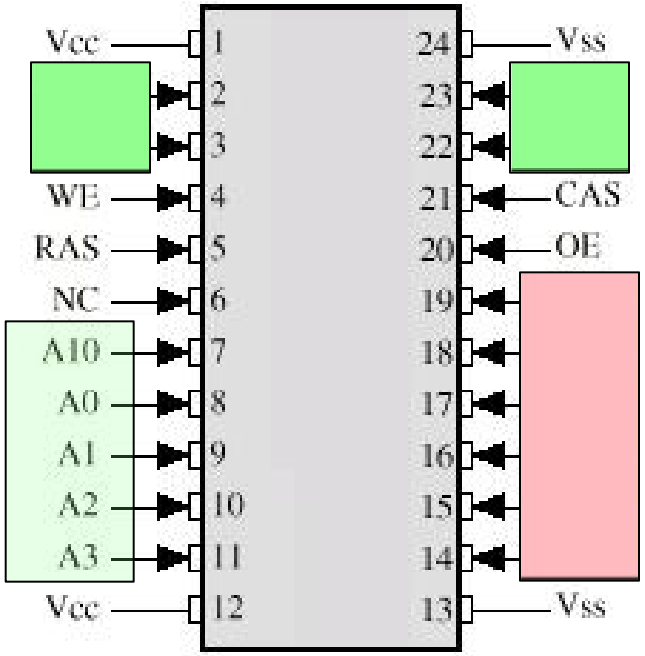
Refreshing (Dynamic RAM)

- Refresh circuit included on chip
- Disable chip
- Count through rows
- Read & Write back
- Takes time
- Slows down apparent performance

Packaging



(a) 8 Mbit EPROM

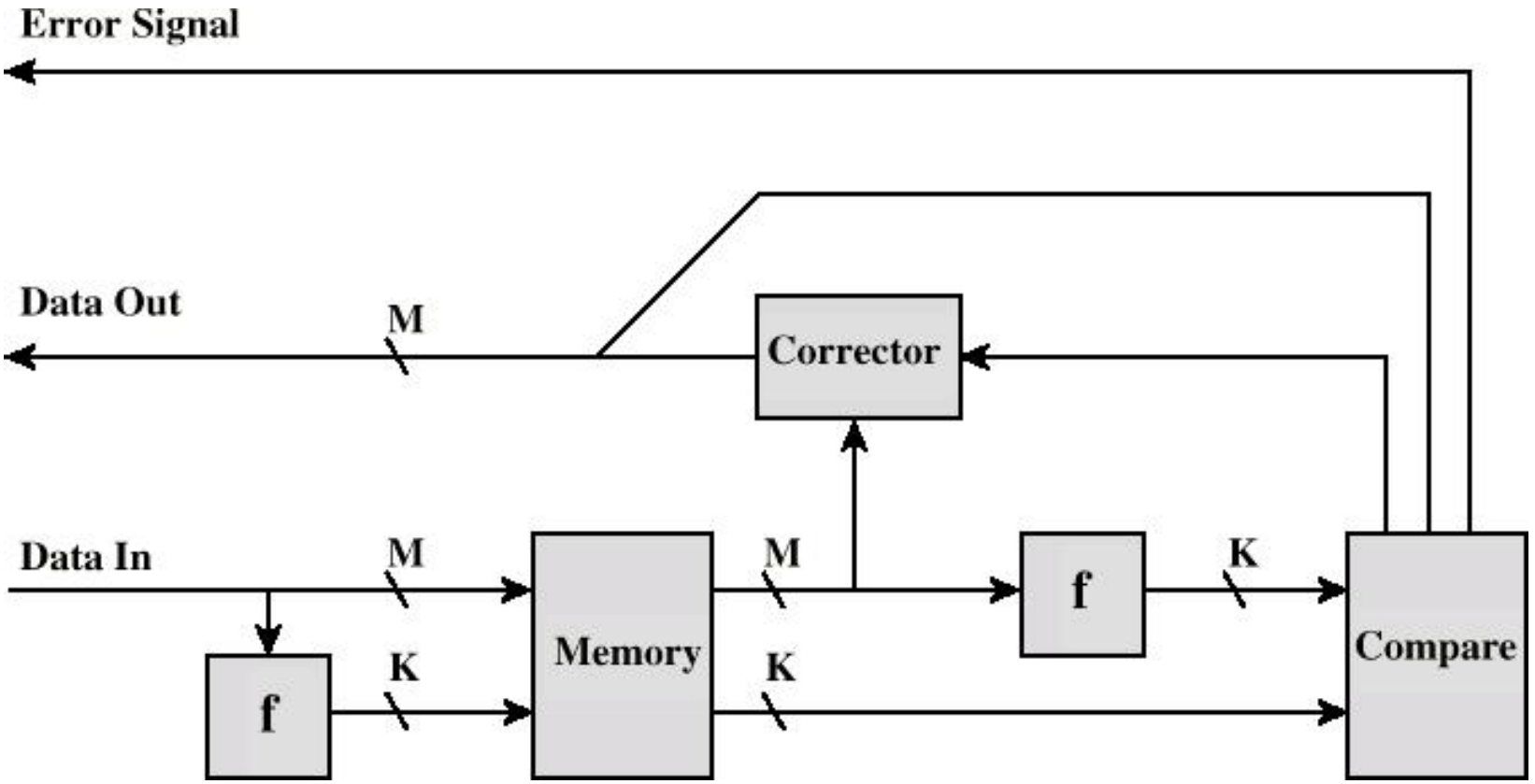


(b) 16 Mbit DRAM

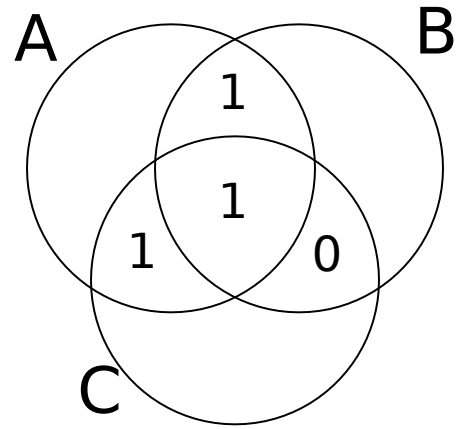
Error Correction

- Hard Failure
  - Permanent defect
- Soft Error
  - Random, non-destructive
  - No permanent damage to memory
- Detected using Hamming error correcting code
  - it is able to detect and correct 1-bit errors

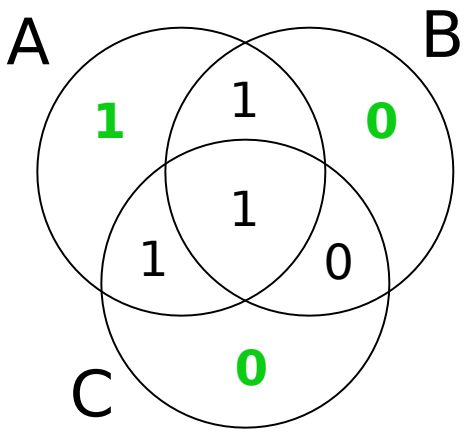
Error Correcting Code Function



A simple example of correction (1)

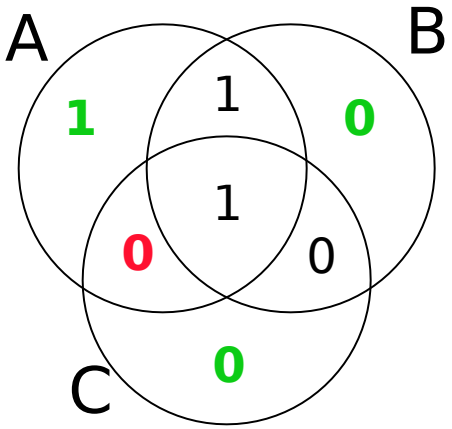


- Correcting errors in 4 bits words
- 3 control groups

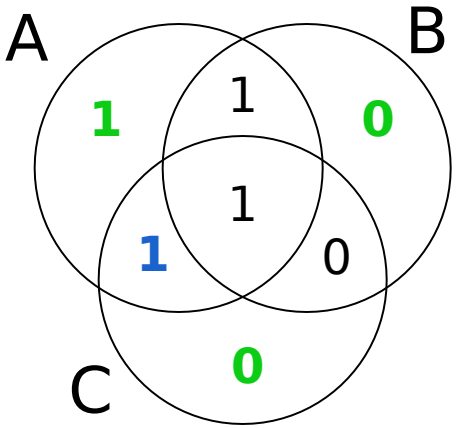


- In each control group add 1 parity bit

A simple example of correction (2)



- One of the bits change value



- Using control bit the right value is restored

Compare Circuit

- it takes two K-length binary strings X, Y as input
  - $X=X_K \cdots X_1$
  - $Y=Y_K \cdots Y_1$
- it returns a K-length binary string Z (syndrome)
  - $Z=Z_K \cdots Z_1$
  - $Z_i=X_i \oplus Y_i$ for each $i=1,\cdots,K$
- $Z=0 \cdots 0$ means no error

Relation between M and K

- Z may assume 2^K values
- the value Z=0...0 means no error
- the error may be in any bit among the M+K bits
- it must be

$$2^K - 1 \geq M + K$$

Data bits (M)	Control Bits (K)	Additional Memory (%)
4	3	75
8	4	50
16	5	31,25
32	6	18,75
64	7	10,94
128	8	6,25
256	9	3,52

How to arrange the M+K bits

- the M+K bits are arranged so that
  - if Z contains a single bit equal to 1
    - error occured in the corresponding control bit
  - if Z contains more than one bit equal to 1
    - error occured in the i-th bit where i is the value (in binary) of Z

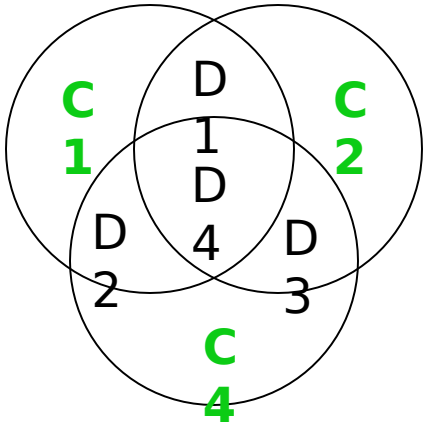
The case M=4

bit position	7	6	5	4	3	2	1
position number	111	110	101	100	011	010	001
data bits	D4	D3	D2		D1		
control bits				C4		C2	C1

$C1 = D1 \oplus D2 \oplus D4$

$C2 = D1 \oplus D3 \oplus D4$

$C4 = D2 \oplus D3 \oplus D4$



Exercise

- Design a Hamming error correcting code for 8-bit words
- See the textbook for the solution